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A 3-CHANNEL 14-BIT OPTIMUM SNS WIDEBAND DIGITAL ANTENNA: ANALYSIS OF THE ELECTRO-OPTIC SAMPLING FRONT END

by

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ABSTRACT ***(maximum 200 words)*** Space considerations onboard naval surface ships frequently preclude adequate separation between high frequency (HF) transmit antennas and HF receive only antennas. As a result, high power shipboard emanations (for example Link-11), interfere with low power signals of interest operating within the same frequency band. Symmetrical-Number-System (SNS) digital antennas provide high-resolution direct digitization of wideband signals with excellent in-band signal-rejection characteristics, which makes them ideal for operating within high RF environments. This thesis describes the design, construction, testing and analysis of the optical electronics at the front end of a prototype optimum SNS digital antenna with a desired accuracy of 14 bits and a bandwidth of 2.5 MHz. The digital antenna utilizes pulsed laser sampling in conjunction with a parallel configuration of Mach-Zehnder interferometers which provide superior bandwidth and isolation performance over electronic sampling mechanisms. The interferometer folded output signal is in accordance with the optimum Symmetrical Number System (SNS) which yields the maximum amount of information from a folding waveform. The theory and experimental performance of the optical subsystem and the analog electronics subsystem is presented, and the total system performance is evaluated. A summary of results and a conclusion with recommendations for improvements to follow-on systems is also discussed.

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A 3-CHANNEL 14-BIT OPTIMUM SNS WIDEBAND DIGITAL ANTENNA: ANALYSIS OF THE ELECTRO-OPTIC SAMPLING FRONT END

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ABSTRACT

Space considerations onboard naval surface ships frequently preclude adequate separation between high frequency (HF) transmit antennas and HF receive only antennas. As a result, high power shipboard emanations (for example Link-11), interfere with low power signals of interest operating within the same frequency band. Symmetrical-Number-System (SNS) digital antennas provide high-resolution direct digitization of wideband signals with excellent in-band signal-rejection characteristics, which makes them ideal for operating within high RF environments. This thesis describes the design, construction, testing and analysis of the optical electronics at the front end of a prototype optimum SNS digital antenna with a desired accuracy of 14 bits and a bandwidth of 2.5 MHz. The digital antenna utilizes pulsed laser sampling in conjunction with a parallel configuration of Mach-Zehnder interferometers which provide superior bandwidth and isolation performance over electronic sampling mechanisms. The interferometer folded output signal is in accordance with the optimum Symmetrical Number System (SNS) which yields the maximum amount of information from a folding waveform. The theory and experimental performance of the optical subsystem and the analog electronics subsystem is presented, and the total system performance is evaluated. A summary of results and a conclusion with recommendations for improvements to follow-on systems is also discussed.

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I. INTRODUCTION

A. SYMMETRICAL NUMBER SYSTEM DIGITAL ANTENNAS

Symmetrical number system (SNS) digital antennas provide high-resolution direct digitization of wideband signals with excellent in-band signal rejection characteristics, making them ideal for operating within high RF environments. Figure (1) shows a prototype optimum SNS wideband digital antenna that uses 3 reflective interferometers that provide a folded output signal in accordance with the Optimum Symmetrical Number System [Ref. 1], 253 comparators, and a Field Programmable Gate Array (FPGA) device to achieve 14-bit accuracy.

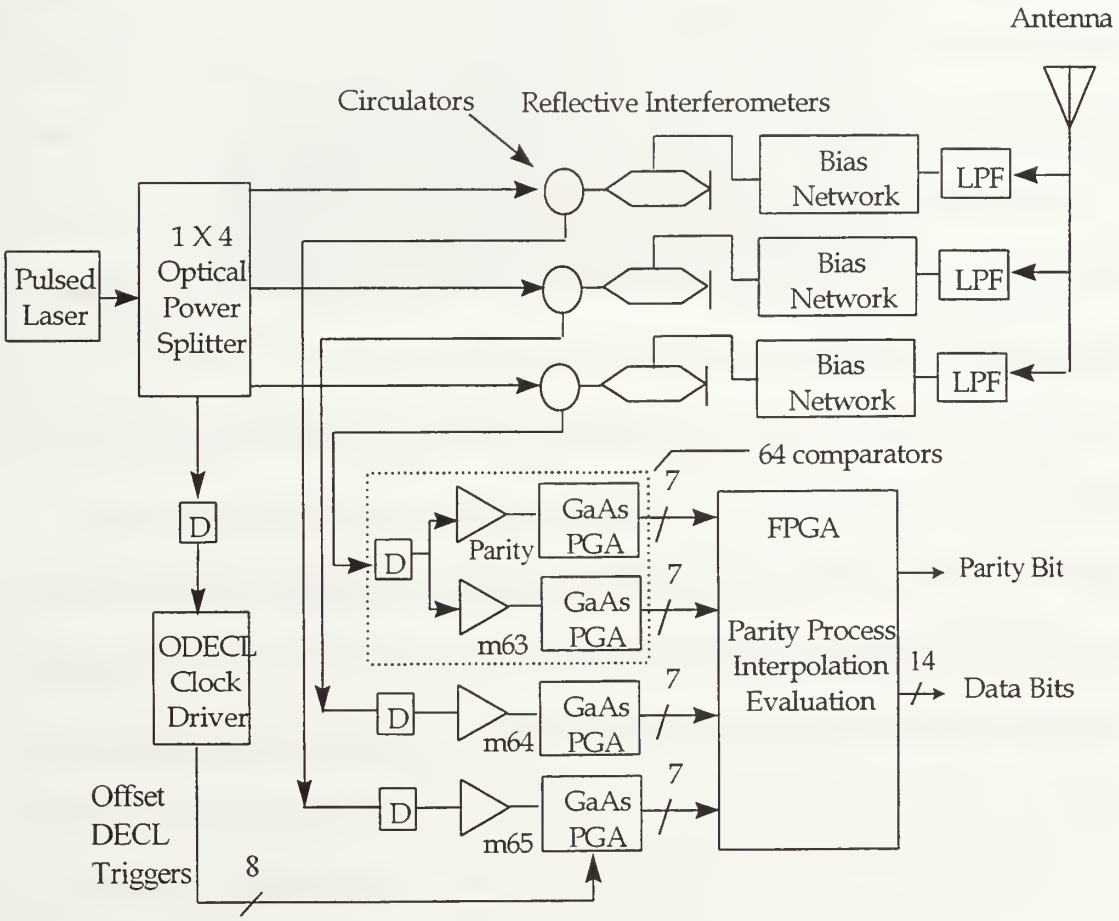

Figure (1): SNS digital antenna block diagram

For each channel, the received RF energy (picked up by the antenna shown in the upper right hand corner of the figure) is passed through an anti-aliasing Low-Pass Filter (LPF) and then fed through an impedance matched DC bias/attenuation circuit and applied to three reflective Mach-Zehnder interferometers (MZIs). The optical input to the three interferometers is provided by a pulsed laser (6-ns pulsewidth at a pulse repetition interval of 200 ns) and is used to sample the RF signal. The optical pulse train is sent through a 1 x 4 optical power splitter, through three optical circulators and on to the respective interferometers. The RF input signal applied to the interferometer modulates the amplitude of the laser pulse as a function of the interferometer's V_{π}. The laser pulse is then detected and applied to a DC restoration amplifier circuit and then amplitude analyzed by *m-1* comparators where *m* is the channel modulus in accordance with the optimum symmetrical number system. This design utilizes three parallel optimum SNS moduli of $m_1 = 63$, $m_2 = 64$, and $m_3 = 65$. The binary representation of the resulting thermometer code generated by the GaAs comparators within a Pin Grid Array (PGA) for each channel is sent to a logic map (for example, a Field Programmable Gate Array (FPGA) circuit) for conversion to a 14-bit digital representation of the input analog signal. The timing of the digital encoding is controlled by an Offset Differential Emitter-Coupled-Logic (ODECL) adjustable-delay trigger circuit. The m=63 channel requires an additional 63 comparators that assist in correcting encoding errors that might occur [Ref. 1].

B. PRINCIPAL CONTRIBUTIONS

In this thesis, a prototype wideband optimum SNS digital antenna was designed, constructed and tested. Particular contributions to this project entail the complete system integration of the optics and analog electronics packages, as well as the detailing of the various sub-system architectures used in this experiment. The complete laboratory set-up for the project is shown in Figure (2).

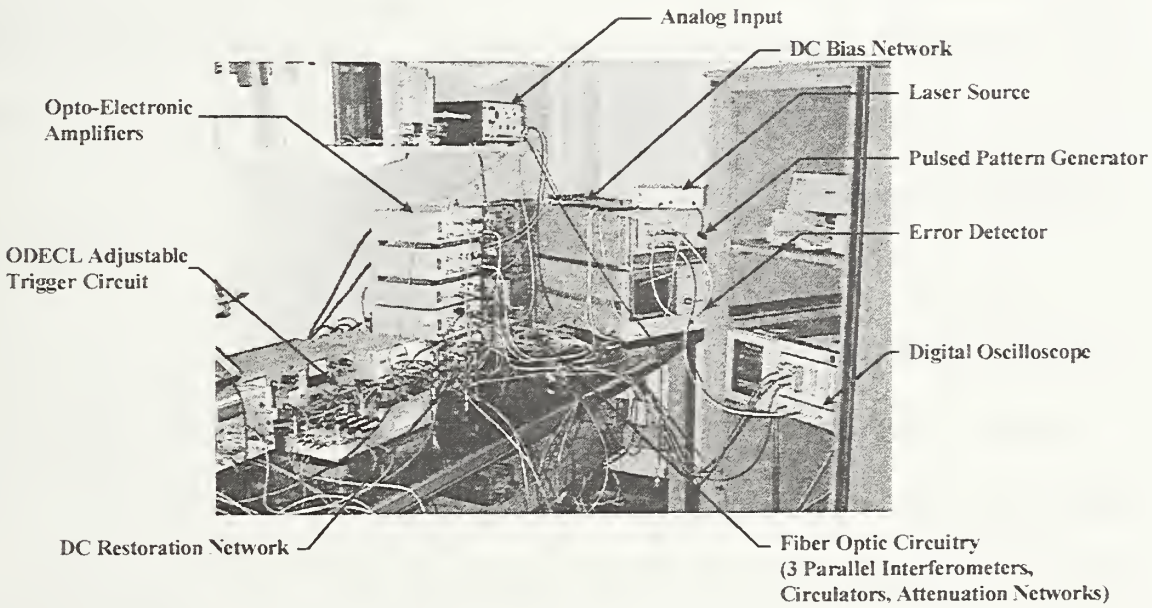

Figure (2): Laboratory set-up of electro-optical front end

For the optics subsystem, the principal contributions include: a) the interfacing of the laser transmitter, optical splitter, and the three circulator/interferometer combinations. b) the precise polarization alignment of the fiber optics in order to maximize the output intensity, c) the application of index matching gel to all connectors in order to minimize loss and maintain optical signal integrity, and d) providing pulsed laser sampling by

applying the pulsed digital output of the pattern generator to the digital input of the laser transmitter.

The analog electronics subsystem work includes: a) the integration and testing of the amplifier outputs, DC restoration network, and the ODECL adjustable trigger delay circuit; b) the phasing of each individual modulus using the DC bias circuitry to yield the correct interferometer folding periods; c) the cascading of the converter/amplifiers in order to yield the correct opto-electronic converter gains; d) the troubleshooting and repair of the ODECL adjustable delay trigger circuitry; e) the attenuation adjustments of the passive termination networks in order to achieve the proper moduli ratios; and f) the complete system performance measurements.

C. THESIS OUTLINE

Chapter II of this thesis presents background material on the design and implementation of the subsystem architectures. Section A focuses on the optical subsystem: the Mach-Zehnder interferometers, the pulsed laser transmitter, the opto-electronic converter/amplifier, the optical circulators, and the optical power splitter. Section B concentrates on the analog electronic subsystem: the DC bias network, the passive attenuation network, the DC restoration circuit, and the adjustable delay trigger circuit. Chapter III details the intermediate results of the individual subsystems. Chapter IV illustrates the total system performance results and analysis. Chapter V presents a summary and conclusion and looks forward to the needed improvements for follow-on systems.

II. OVERVIEW OF SUBSYSTEM ARCHITECTURES

This chapter details the individual subsystems that are an integral part of the digital antenna project. It is broken down into two basic segments, the optical subsystem and the analog electronics subsystem.

A. OPTICAL SUBSYSTEM

The overall subsystem architecture is illustrated in Figure (3), with the components particular to the optical subsystem shown in shaded blocks.

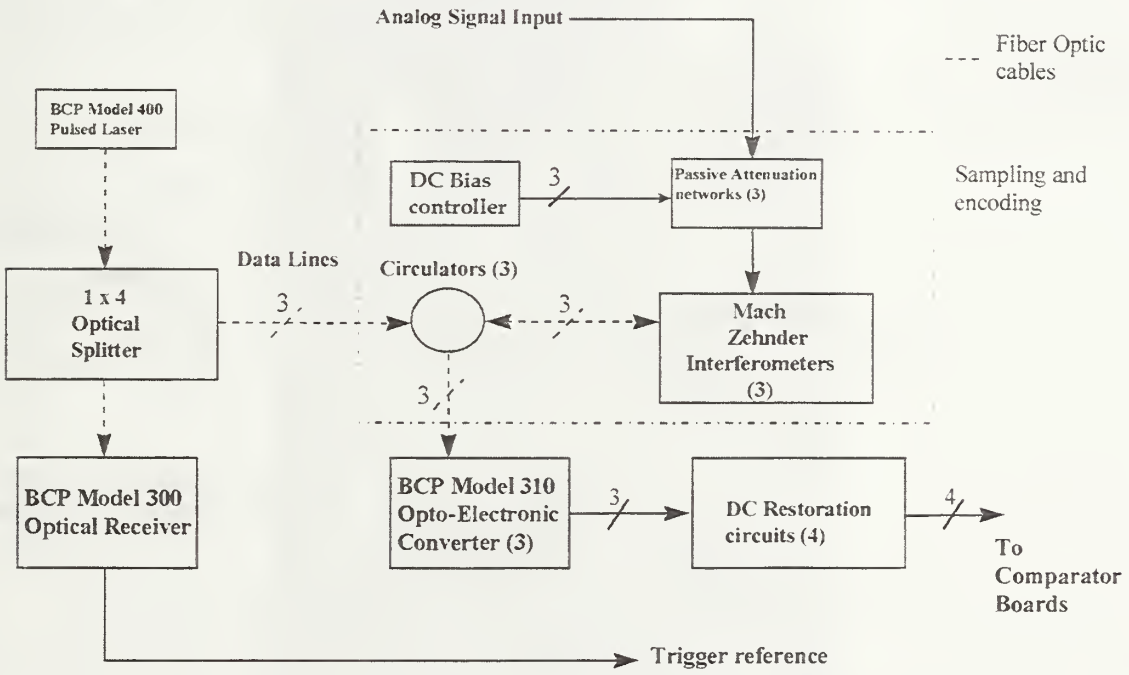

Figure (3): Optical subsystem block diagram

Note that there are three channels being processed simultaneously and that the blue box indicates the parallel sampling and encoding configuration. Also note that fiber optic cable is delineated with a dashed line. This figure illustrates the analog input being preprocessed by the passive attenuation network and the DC bias controller circuitry prior

to entering the interferometers. The optical laser pulse trains are routed through the circulators and into the interferometers, where they sample the analog RF input, and reflect back through the port through which it entered. The circulators then route the reflected, modulated output pulses to the opto-electronic converters/amplifiers for processing. Figure (4) illustrates the laboratory construction of the three parallel networks of Mach-Zehnder interferometers, optical circulators, and attenuation circuits.

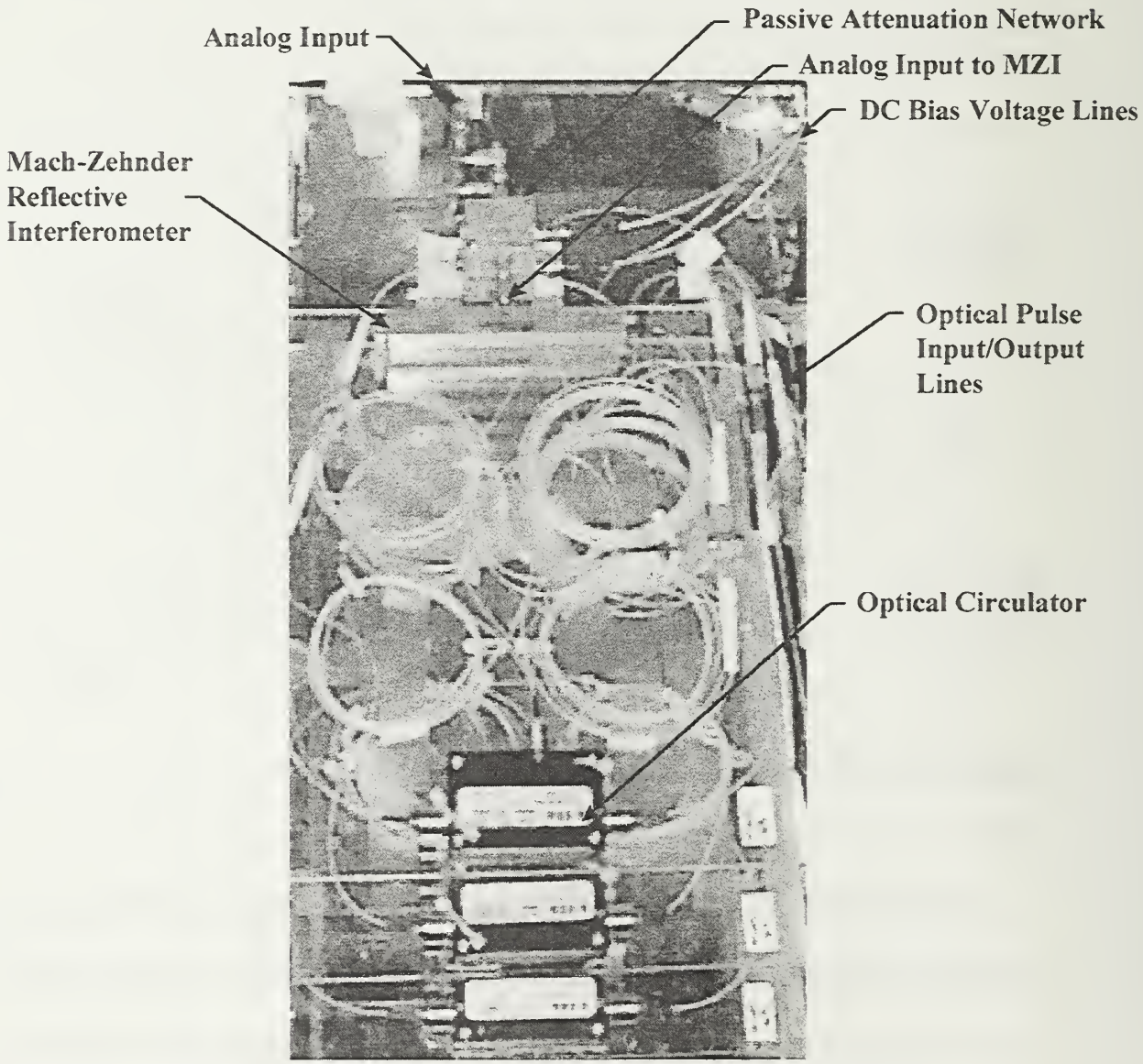

Figure (4): Laboratory construction of parallel electro-optical network

1. Overview of the Optimum Symmetrical Number System

The optimum SNS scheme is composed of a number of pairwise relatively prime moduli m_i. The integers within each SNS modulus are representative of a symmetrically folded waveform with the period of the waveform equal to twice the modulus ($2m_i$). For a given modulus m, the integer values for one period of the folded waveform are given by [Ref. 1]

$$\bar{x}_m = [0,1,\cdots,m-1,m-1,\cdots,1,0]. \quad (1)$$

Figure (5) illustrates an example of the optimum SNS folding waveforms and SNS output codes for both $m_1 = 4$ and $m_2 = 5$.

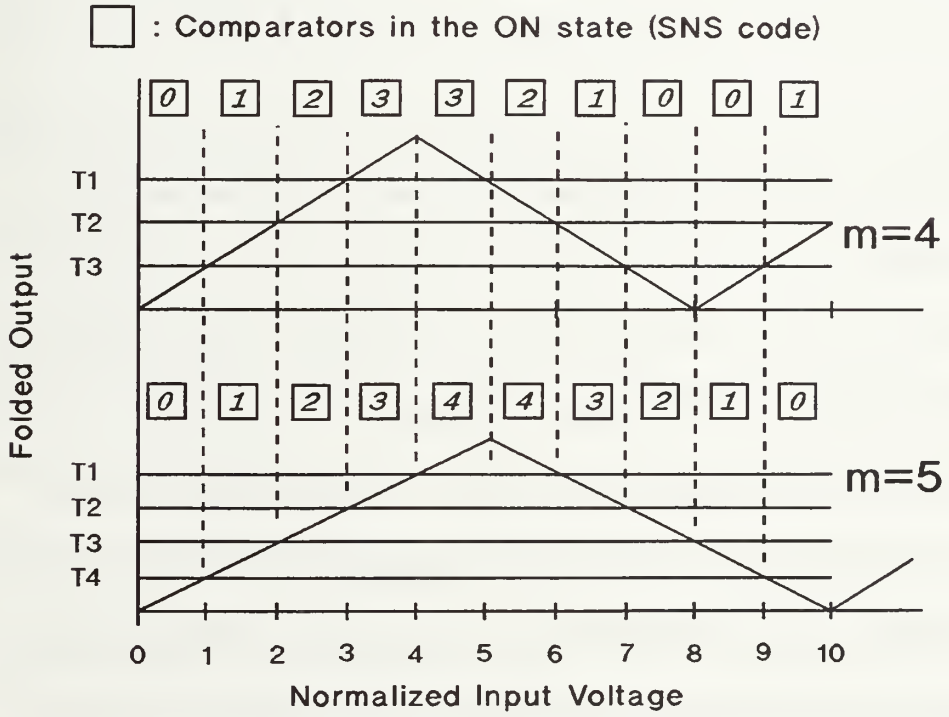

Figure (5): OSNS folding waveforms and output codes for $m_1 = 4$ and $m_2 = 5$.

The horizontal axis represents the normalized input voltage. The "T" values along the vertical axis represent predetermined voltage levels which are used as reference levels

for a bank of comparator circuits. The numbers in squares at the top of the figure represents the number of comparators that are turned on for the given input voltage. For the $m = 4$ channel, we observe from the figure that as the normalized input voltage increases from 0 to 4 volts, the folded output swings from its minimum to its maximum value, or half of a complete fold. The period of one complete fold is equal to twice the modulus, or 8 volts. The output of the $m = 5$ channel obeys the same relationship. From equation (1) we can observe that the required number of comparators for each channel is $m_i - 1$. The dynamic range DR of the system is given by [Ref. 1]

$$DR = \prod_{i=1}^{N} m_i \tag{2}$$

where N is equal to the number of PRP moduli.

This thesis is an extension of the simple example given in figure (5). Three parallel Mach-Zehnder interferometers (MZIs) are used as the folding circuits that will produce a desired 14-bit dynamic range $DR = 2^{14}$ or 16,382. The moduli chosen to produce this dynamic range are $m_1 = 63$, $m_2 = 64$ and $m_3 = 65$. From equation (2) these moduli yield a dynamic range of 262,080, which is more than ample range for 14 bit precision. An input signal is applied to the three different moduli in parallel. The folded outputs from each optimum SNS preprocessor are then quantized by the comparator boards. The output of the comparator boards represents the input signal in an OSNS format. Digital processing of the comparator board outputs for this project is carried out in a follow-on thesis [Ref. 2].

2. Mach-Zehnder Interferometers

The three parallel, reflective Mach-Zehnder Interferometers (MZI) perform pulse amplitude modulation and Optimum Symmetrical Number System (OSNS) encoding. Figure (6) illustrates the schematic of the Mach-Zehnder interferometer.

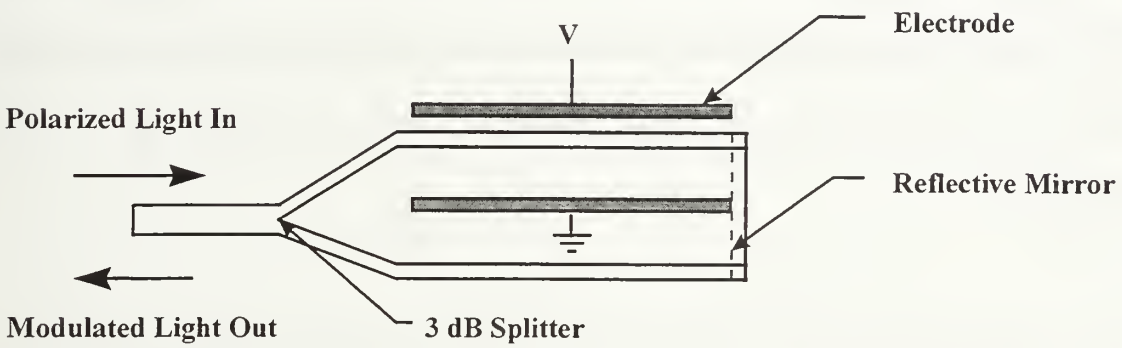

Figure (6): Mach-Zehnder interferometer

An optical pulse is split into two parallel pulses, one pulse being modulated by the analog input as it passes the electrode. The pulses reflect off the mirror and, after recombining, exit the interferometer as a modulated output. The feature that makes the MZI so attractive for high speed analog-digital conversion is its periodic dependence of output optical intensity as a function of the applied voltage on the electrode. A voltage applied to the modulator electrodes produces a relative phase retardation for the two arms of the interferometer, which results in amplitude modulation of the output pulse, in accordance with the linear Pockel's effect [Ref. 3]. The transfer function, *I*, of the MZI is given by

$$I(v,m) = \tfrac{1}{2} + \tfrac{1}{2}\cos\left(\Delta\phi + \pi\right) \qquad (3)$$

where $\Delta\phi$ is the voltage-dependent phase shift and is represented by [Ref.4]

$$\Delta\phi = \frac{2\pi n_e^3 r \Gamma L v}{G\lambda} = \frac{\pi v}{m} \tag{4}$$

where v is the applied analog voltage to the interferometer, m is the modulus, n_e is the effective index of the optical guide, r is the pertinent electro-optical coefficient, G is inter-electrode gap, Γ is the electrical-optical overlap parameter, L is the length of the electrode, and λ is the free space optical wavelength. In terms of electro-optic parameters,

$$\Delta\phi = KL\,v \tag{5}$$

[Ref. 4] where K is a proportionality constant that relates the index of refraction, the electro-optic coefficient, the interelectrode gap, the electrical-optical overlap parameter, and the optical wavelength. The DC portion of the phase of the MZI folded waveform is a function of the DC voltage level on the electrode. An adjustable DC bias is applied to the electrodes of each interferometer through the DC bias controller in order to provide a means to align a minimum output intensity (or "trough") to a particular input RF voltage (The RF voltage is AC coupled to the MZI). To fold the signal properly the electrode lengths should vary as

$$L = \frac{\pi}{Km} \tag{6}$$

[Ref. 4] where it is evident that the electrode length is inversely proportional to the modulus m. Since the moduli are spaced so close together ($m_1 = 63$, $m_2 = 64$, $m_3 = 65$), the electrodes of the interferometers and the electro-optic transfer curves are essentially identical. The passive attenuation network of Figure (3) is incorporated into the design in

order to provide a means of adjusting the folding periods of the MZI transfer function in accordance with the desired moduli ratios between MZI sections. This preprocessing technique is detailed in Section B, as a part of the analog electronics subsystems.

One important performance specification for an integrated optical interferometer is the amount of electrode voltage needed to transition the normalized output from a minimum, $\Delta\phi = 0$, to a maximum, $\Delta\phi = \pi$. This performance specification, V_π, is [Ref. 4]

$$V_\pi = \frac{G\lambda}{2L\, n_e^3 r\Gamma} \tag{7}$$

where G is the interelectrode gap, λ is the free space optical wavelength, L is the interferometer electrode length, n_e is the effective index of the optical guide, r is the pertinent electro-optic coefficient, and Γ is the electrical-optical overlap parameter. The three interferometers used in this project were fabricated with a nominal V_π of 0.32 volts. By combining equations (7) with (4) we determine a relationship between V_π and the modulus m, for the normalized output of equation (3),

$$\Delta\phi = \frac{\pi v}{m} = \frac{\pi v}{V_\pi}. \tag{8}$$

In practical (unnormalized) implementation, V_π and m are directly related by a scaling factor, which is the least significant bit, *LSB*:

$$LSB = \frac{V_\pi}{m} \tag{9}$$

Figure (7) shows the MZI transfer functions for all three interferometers given a linear input voltage, v.

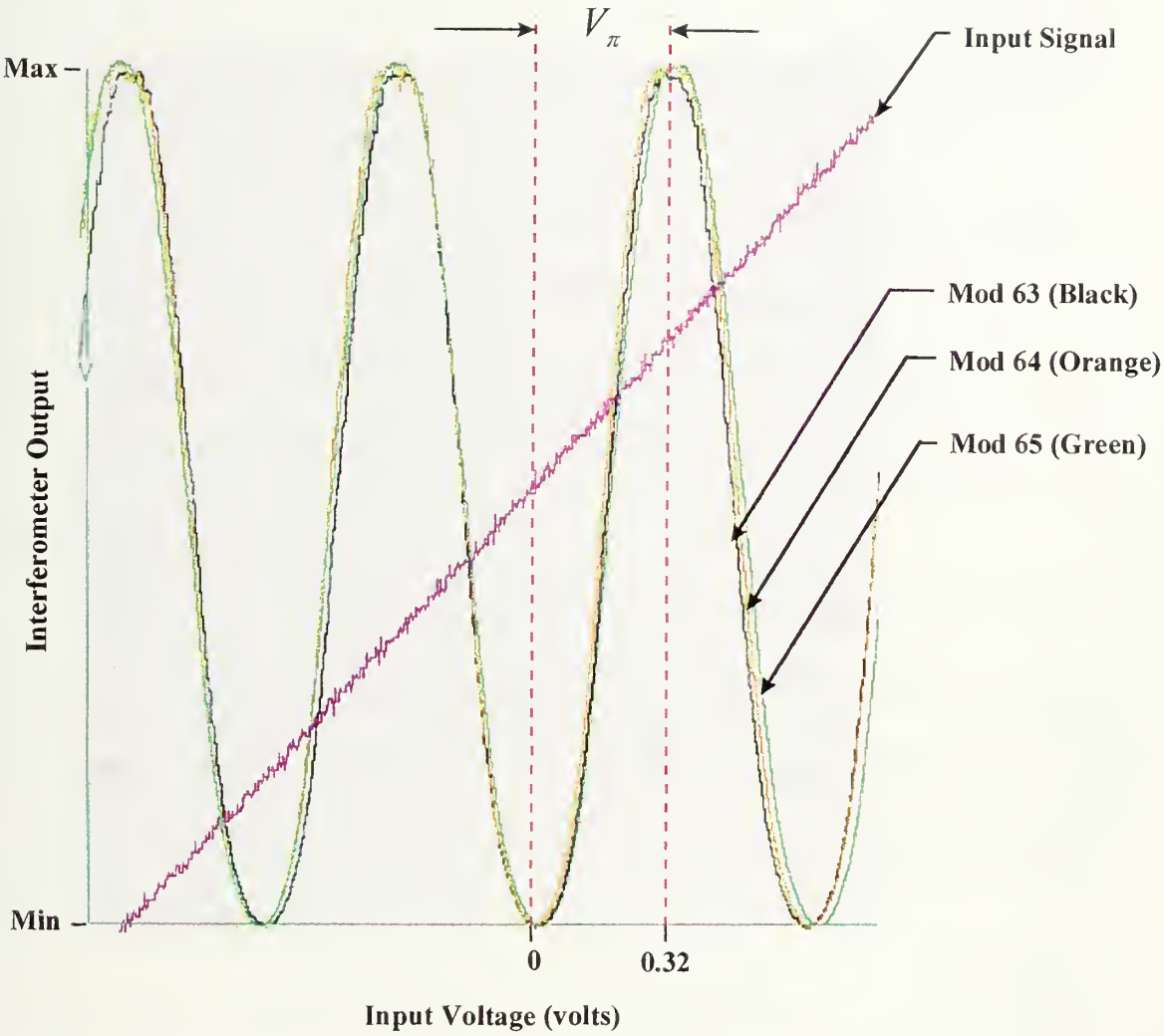

Figure (7): Interferometer outputs for a given input voltage

We observe that given a linear input voltage, v, the interferometer output is sinusoidal in accordance with equation (3). The Mod 63 MZI output swings from its minimum, at $v = 0$, to its maximum, at $v = V_\pi$, which is equal to 0.32 volts. Observe that folding periods of the Mod 64, and Mod 65 outputs, are greater than the Mod 63 output. These two channels have a passive attenuation network applied to the input voltage in

order to yield the proper moduli ratios for the optimum SNS. The passive attenuation network is developed in Section B.

The dynamic range of the three channel optimum SNS is given by $DR = m_1 m_2 m_3$, so the larger the moduli, the larger the dynamic range of the system. In order to obtain more folds from the MZI, the size of V_π was reduced. The interferometer was designed to be completely reflective, giving the signal a second pass over the electrode, thus doubling the virtual electrode length and reducing V_π by one-half. Complete specifications for the Mach-Zehnder interferometers fabricated for this project are contained in the Appendix.

Another important design consideration is the maximum voltage, V_{max}, that may be applied to the electrodes. Applying a higher potential than this maximum voltage can cause a spark across the electrode gap and seriously damage the interferometer. The value of V_{max} for this thesis were ± 42 volts. The maximum number of folds available from a device is [Ref. 4]

$$F = \frac{2V_{\max}}{2V_\pi} \tag{10}$$

where a complete fold is defined by $2V_\pi$. For this project, with a V_π of 0.32 volts and a nominal $V_{\max}$ of 42 volts, the maximum number of folds available from the interferometers is 131. The largest number of folds required from an interferometer in a n-bit optimum SNS ADC is [Ref. 4]

$$F_{req} = \frac{2^n - 1}{2m_{\min}} < \frac{2V_{\max}}{2V_\pi} \tag{11}$$

where $m_{\min}$ is the smallest modulus in the optimum SNS system. For a 14-bit system with a minimum modulus of 63, the required number of folds from the interferometer is 130, which is within the limitation of 131 that was just computed.

3. Laser Transmitter

High speed digital pulsing is accomplished using a semiconductor laser transmitter triggered by an HP70841B Pattern Generator. The BCP 400 laser transmitter is a low power (0.75 mW peak coupled power) device with a wavelength of 1300 nm and a spectral width of 4 nm. It is driven by the digital pattern generator programmed to trigger a 6 ns optical pulse at a repetition interval of 200 ns, yielding a 5 MHz sampling waveform. This pulsed laser configuration is the key to the high speed, low distortion, precision sampling required for this project. After splitting into four channels the pulsed laser signals are routed through the interferometers and then reflected back through a circulator and on to a detector/amplifier circuit for processing and decoding. Through an analysis of the error in the sampled input voltage due to the total electro-optical interaction time, a maximum pulse width, ΔT, for a specified maximum modulation frequency can be determined. The pulse width must satisfy [Ref. 4]

$$\Delta T < \frac{\sqrt{\frac{3}{2^{N-1}}}}{\pi f_{\max}} \tag{12}$$

where N is the equivalent number of bits required for each channel and f_{max} is the maximum frequency of interest. Due to the SNS architecture each channel has m-1 comparators. The comparator threshold values, however, are non-uniformly spaced (the threshold levels are closer together at the top and bottom of the folded output). The

maximum precision required is dictated by the largest modulus (m=65). For the modulator normalized output given by equation (3), the normalized threshold values for the comparators within a modulus, m, are

$$T_i = \cos^2\left(\frac{\pi}{2mv_i} + \frac{\pi}{2}\right) \tag{13}$$

where the quantized voltage, v_i, is [Ref. 4]

$$v_i \in \left\{1, \frac{1}{2}, \frac{1}{3}, \ldots, \frac{1}{m-1}\right\}. \tag{14}$$

The worst-case value will be for the Mod 65 because it has more quantization levels per fold than the other two channels. The maximum normalized threshold value for m = 65 is:

$$T_{\max} = \cos^2\left(\frac{\pi}{2\left(\frac{65}{64}\right)} + \frac{\pi}{2}\right) = 0.999416,$$

where $v_{65} = \frac{1}{m-1} = \frac{1}{64}$. The next lowest threshold value ($v_{64} = \frac{1}{63}$) is similarly determined to be $T_{max\text{-}1} = 0.997665$. The difference, $\Delta T = 0.0017501$. Therefore the precision of the channel (equivalent number of bits for the SNS) is

$\frac{1}{\Delta T} = \frac{1}{0.0017501} = 571.4$ levels, which means that a resolution of $N_{equiv} = 10$ bits is required (a 9-bit resolution would produce only 512 levels).

For this project, to digitize a maximum frequency of 2.5 MHz with an equivalent bit resolution of 10, the maximum pulse width allowed is 9.747 ns. The actual pulse

width established by the bit error encoder is 6.0 ns, which is within the maximum pulse width calculation.

The maximum fluctuation in the sampling interval, or sample jitter is given by [Ref. 3]

$$\delta t_{\max} = \frac{1}{2^{N+1}\pi f_{\max}}. \tag{15}$$

For this project, with a bandwidth of 2.5 MHz and an equivalent number of bits equal to 10, the pulse jitter must be less than 62.17 ps.

4. Optical Power Splitter

The laser pulse train is split off into four parallel signals, using the 1 x 4 optical power splitter. Three of the pulse trains are used to sample the RF signal at the interferometers and the fourth is used as a reference pulse train for the ODECL adjustable-delay trigger circuit that latches the output of the comparator array.

5. Optical Circulators

In order to accommodate the returning signal from the reflective MZI, a polarization insensitive fiber optic circulator was used to direct the source pulse train down into the interferometer and to route the modulated return pulse train from the MZI to the detector and amplification circuitry. A block diagram of the routing for a typical channel is shown in Figure (8).

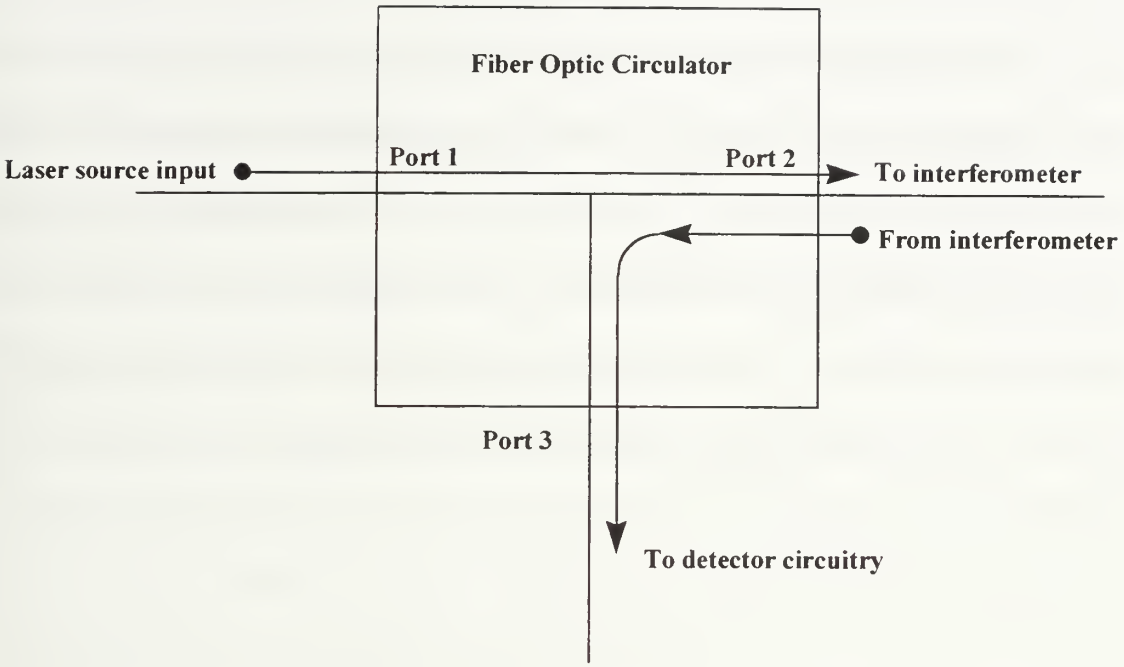

Figure (8): Fiber optic circulator port specifications

The fiber optic circulator is a passive optical device that transmits an incoming signal from port one to port two, with little crosstalk to port three. Similarly, a separate incoming signal is sent from port two to port three, with little signal appearing at port one. The device performs this operation with a high degree of isolation, providing greater than 50 dB peak isolation between the other adjacent ports.

6. Opto-Electronic Converter/Amplifier

For each channel. the optical optimum SNS encoded signal is detected by germanium photodiodes and amplified with variable-gain wideband amplifiers. The optical pulse-amplitude-modulated signal is hence converted into a corresponding electrical pulse-amplitude-modulated signal. The AC coupling of the amplifiers dictates the need for a DC restoration circuit in order to add a correct DC level for the detected pulse going to the comparator arrays. Figure (9) demonstrates the evolutionary process of the pulse recovery.

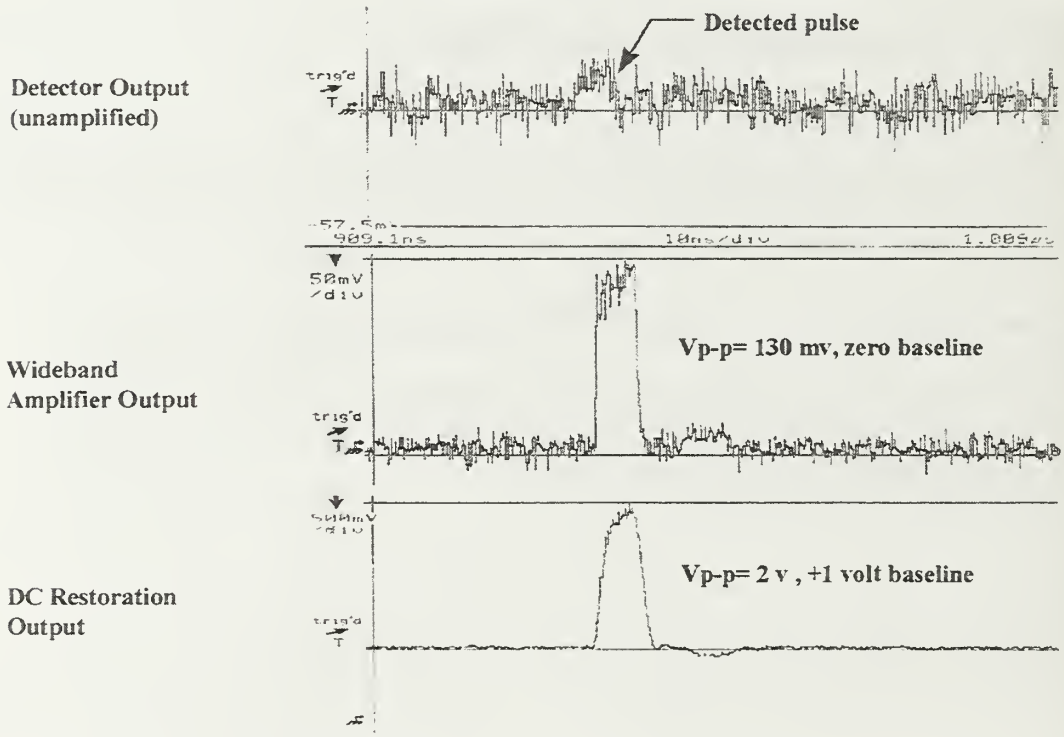

Figure (9): Evolution of pulse recovery process

The waveform at the top of the figure shows the output of the detector diode, converting the optical pulse to an electronic representation. This electronic pulse is then

fed through an amplifier to pull the signal out of the noise floor, as shown in the middle of the figure. At the bottom of the figure, a DC reference level has been added to the pulse train, which ensures that the signal is now located between +1 and +3 volts and is ready for the next stage of processing.

Figure (10) illustrates the laboratory configuration of the opto-electronic converter/amplifier bank. Scanning from right to left in the figure, the recovery process is illustrated. The yellow optical fiber from the interferometers is connected to the converter/amplifiers and the electrical outputs from these components are connected to the DC restoration network on the left. The outputs of the DC restoration network are then connected to the comparator boards for processing.

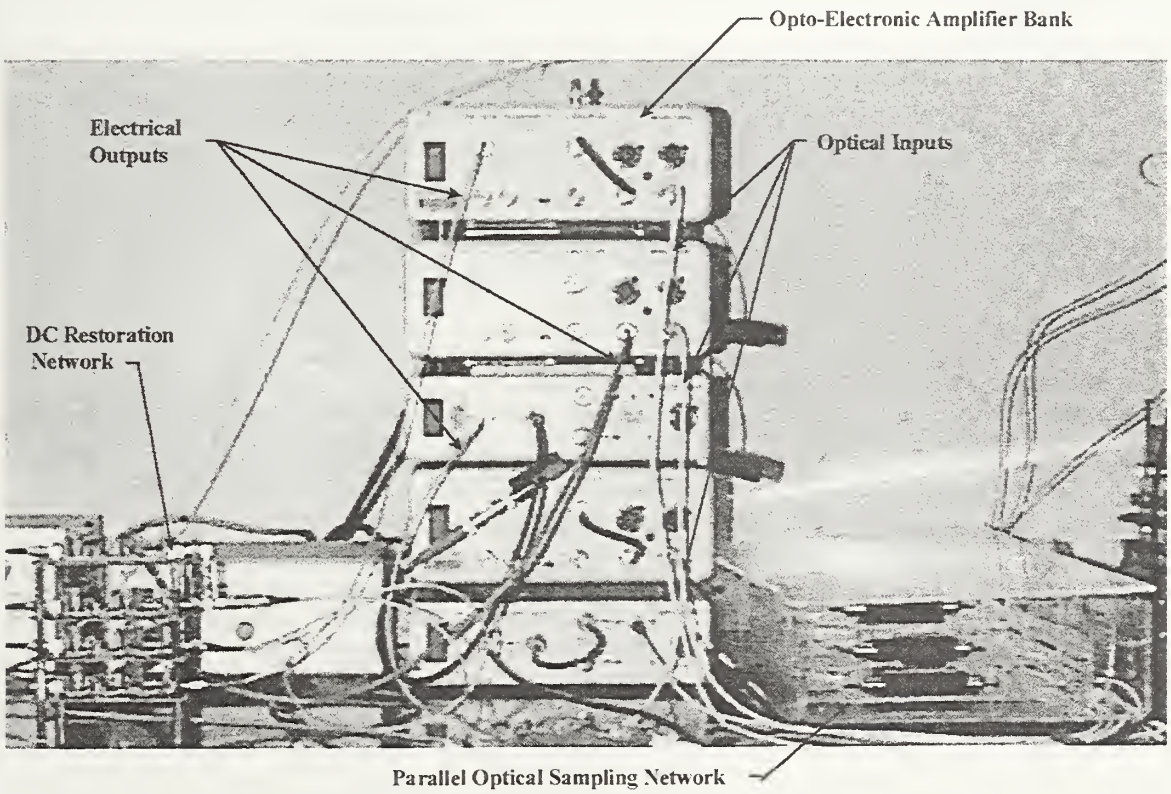

Figure (10): Laboratory configuration of opto-electronic converter/amplifier bank

With the optical subsystems detailed sufficiently, the analog electronics subsystem is developed in Section B.

B. ANALOG ELECTRONIC SUBSYSTEM

The overall subsystem architecture block diagram is shown in Figure (11), with the components particular to the analog electronics subsystem shaded gray. The components within the blue box indicate the parallel three-channel configuration. Also note that fiber optic cables are indicated with dotted lines.

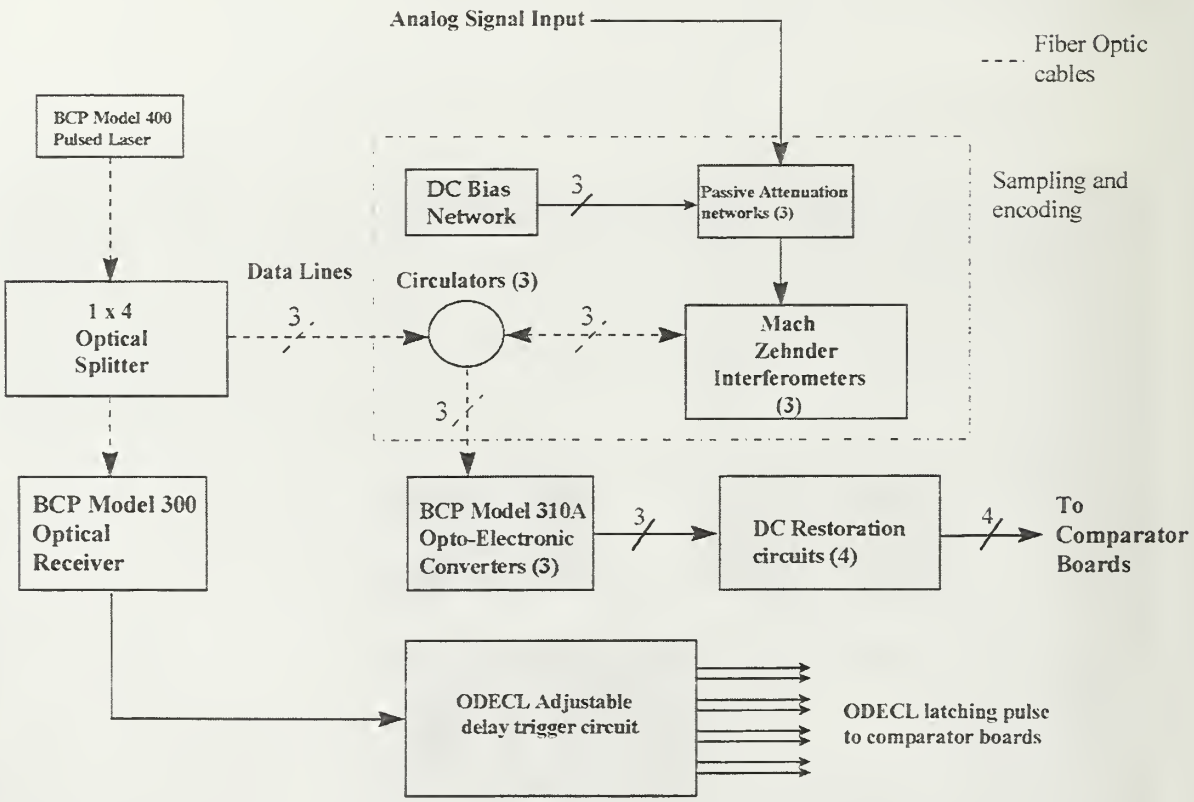

Figure (11): Analog electronic subsystem block diagram

1. DC Bias Network

As was discussed earlier, the phase of the MZI folded waveform is a function of the DC voltage level on each electrode. Thus, a DC bias applied to each electrode of the MZIs provide a means of aligning a trough of each transfer function of the parallel outputs to a desired value of input voltage, in accordance with the optimum SNS [Ref. 1]. The normalized output of the MZI is given, again, by equation (3).

A DC bias circuit was designed and fabricated [Ref. 5] in order to provide a method of supplying the desired DC voltage for adjusting the relative phase of the transfer function of each channel of the MZI network. A schematic of the biasing circuitry is shown in Figure (12).

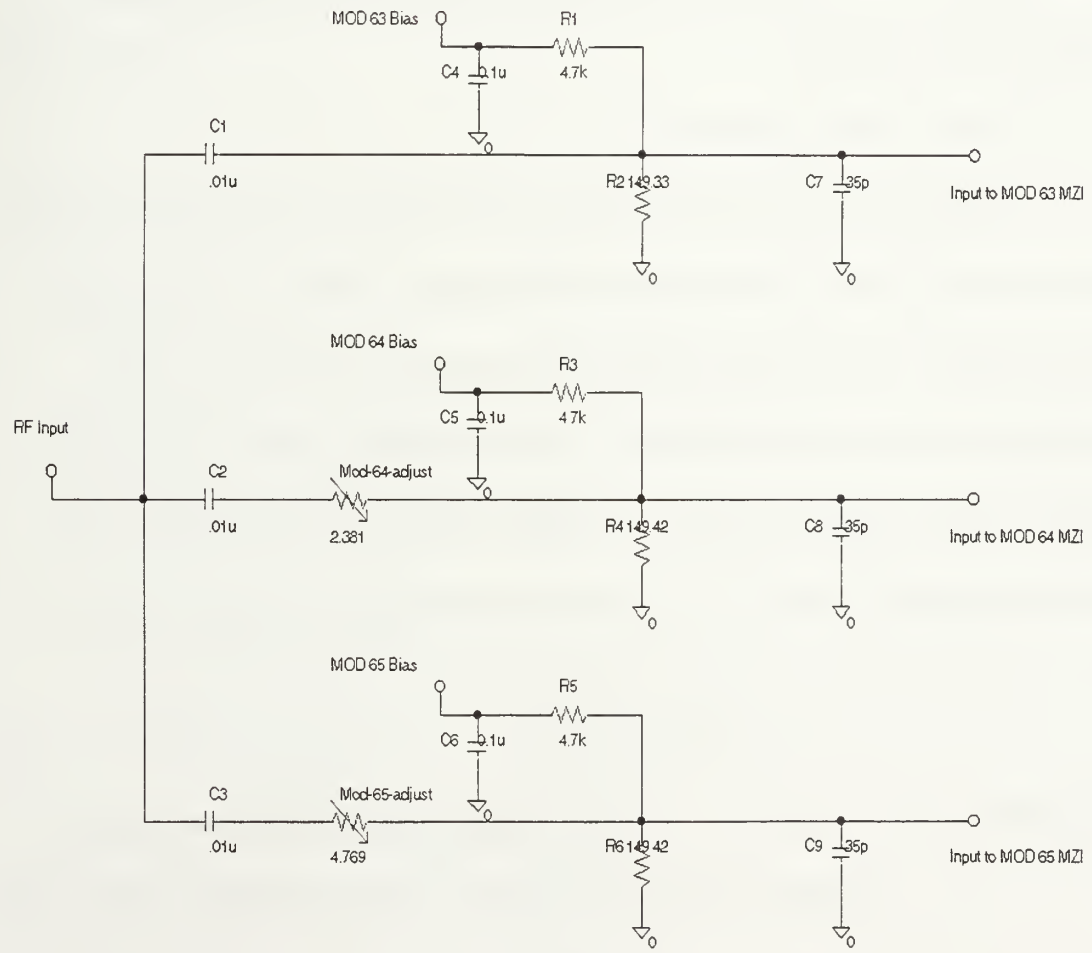

Figure (12): DC bias network schematic

The total impedance for the Mod 63 network is the parallel combination of the 4.7 kΩ and 149.33 Ω resistors or 144.73 Ω. The total impedance for the Mod 64 network is 2.3810 Ω plus the parallel combination of the 4.7 kΩ and the 149.42 Ω resistors, or

147.2 Ω. The total impedance for the Mod 65 network is 4.769 Ω plus the parallel combination of 4.7 kΩ and the 149.42 Ω resistors, or 149.6 Ω. The total impedance of the input network is the parallel combination of the three equivalent impedances or 49.1 Ω. This input impedance is well within acceptable limits for a 50 Ω impedance match from the antenna. Note that *C1, C2,* and *C3* for the circuit shown in Figure (10) are used as DC blocking capacitors on the input side, and *C4* through *C9* are used as high frequency bypass capacitors.

2. Passive Attenuation Network

For a given input signal, the MZI output will undergo a specified number of folds depending on the modulus of the individual interferometer. The electro-optic transfer curves of the MZI's are basically identical within manufacturers tolerances, so an attenuation network was designed [Ref. 5] in order to provide a means to adjust for the desired V_π, which is directly related to the channel modulus of the optimum SNS. By combining equations (3) and (8), we can rewrite the interferometer transfer function as,

$$I = \frac{1}{2} + \frac{1}{2}\cos\left(\frac{v}{V_\pi} + \pi\right). \qquad (16)$$

By applying a passive attenuation to the input voltage, the transfer function becomes,

$$I = \frac{1}{2} + \frac{1}{2}\cos\left(\frac{av}{V_\pi} + \pi\right) \tag{17}$$

where a is the attenuation applied to the input voltage. In order to establish the proper V_π for each channel (which in turn will establish the proper modulus for the optimum SNS), the desired attenuations are:

$$a_{63} = 1, \tag{18}$$

$$a_{64} = \frac{63}{64}, \tag{19}$$

$$a_{65} = \frac{63}{65}. \tag{20}$$

A simplified schematic of the attenuation network used to form the moduli ratios is shown in Figure (13) where Z is the input impedance of the individual MZI, which is equal to 150 Ω.

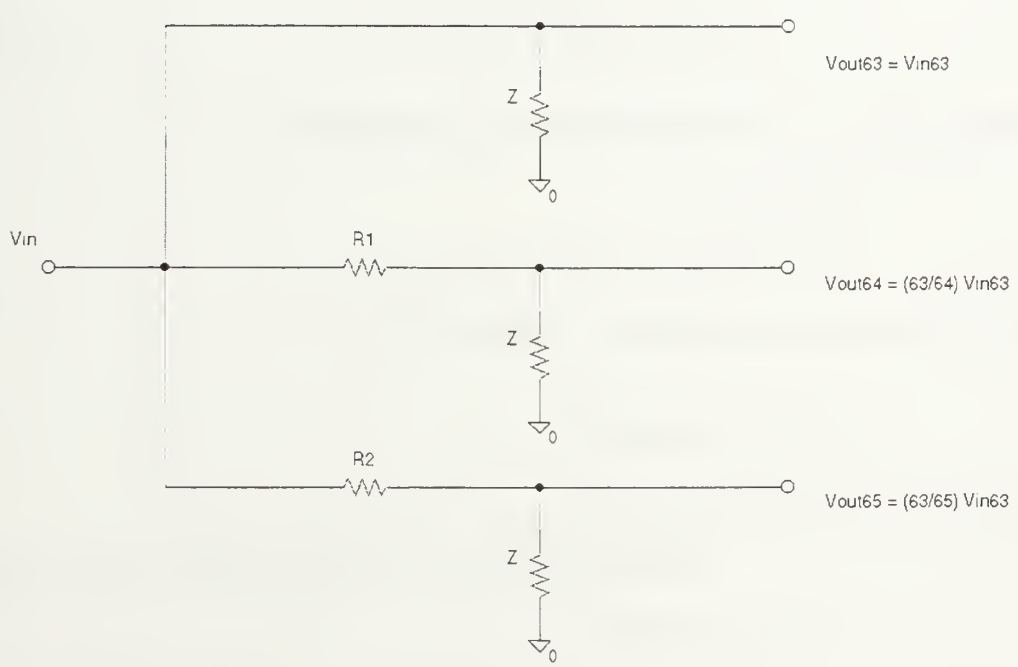

Figure (13): Simplified schematic of passive attenuation network

The equivalent low frequency input circuit for each parallel Mach-Zehnder interferometer is represented in Figure (14):

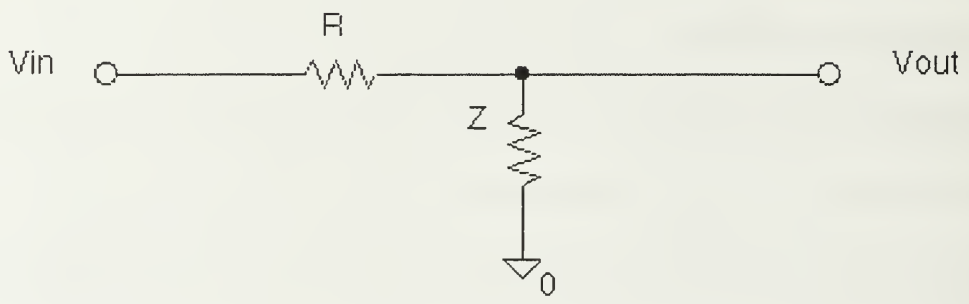

Figure (14): Mach-Zehnder interferometer low frequency equivalent circuit

The output for each channel is given by:

$$V_{out} = \left(\frac{z}{z+r}\right)V_{in} \Rightarrow \frac{V_{out}}{V_{in}} = \frac{z}{z+r}. \tag{21}$$

The nominal value for r_1 of the Mod 64 network is determined by:

$$\frac{63}{64} = \frac{z}{z+r_1}. \tag{22}$$

Recalling that the MZI input impedance, z, is equal to 150 Ω:

$$r_1 = \frac{1}{63}z = 2.3810\ \Omega.$$

The nominal value for r_2 of the Mod 65 network is similarly determined by:

$$r_2 = \frac{2}{63}z = 4.769\ \Omega.$$

In order to compensate for component tolerances, temperature coefficients, power handling capabilities, power derating versus temperature, and taking into account the precise values desired, a parallel resistor-potentiometer circuit was designed. Using a high-power, fixed, low-value resistor in parallel with a potentiometer that is at least 10 times the value of this fixed resistor, the desired qualities of sensitivity and high power are achieved. The Mod 64 resistance is equal to 2.38 Ω with a desired adjustment range of 2.33 Ω to 2.43 Ω. Similarly, this circuit is used for the Mod 65 resistance, which is equal to 4.77 Ω with a desired adjustment range of 4.72 Ω to 4.82 Ω. The complete configuration is shown in Figure (15).

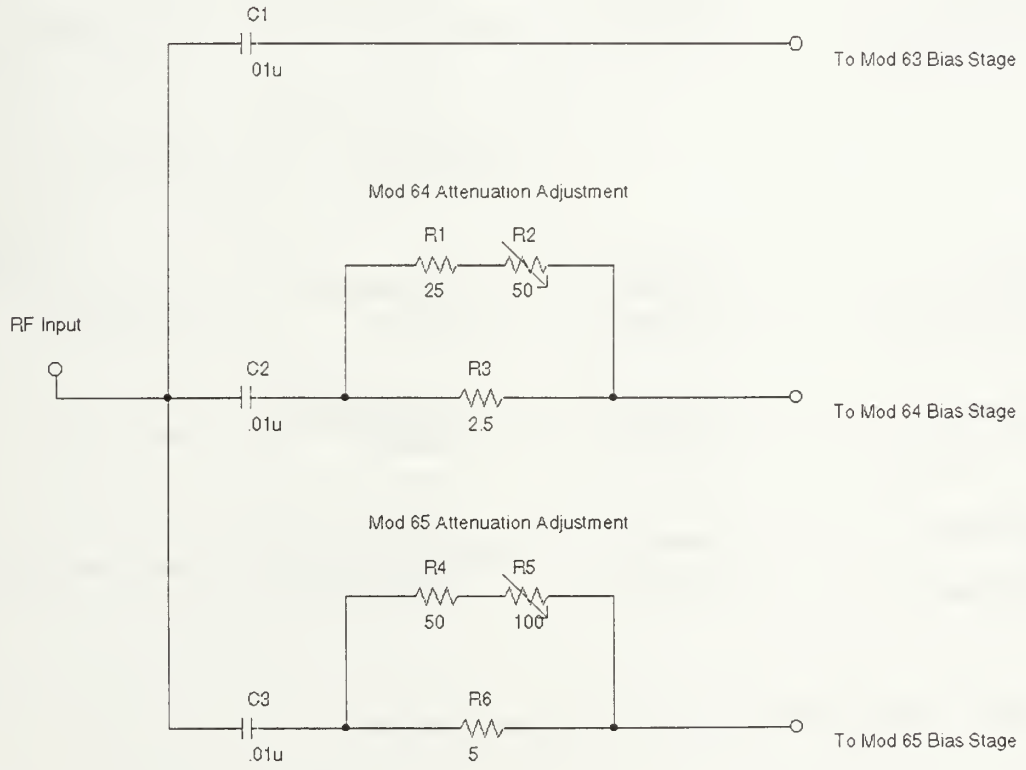

Figure (15): Attenuation network schematic diagram

The blocking capacitors C1, C2, and C3 are to prevent any DC voltage leaking into the network, which of course would affect the phasing of the folded output of the interferometer. Note that this low-frequency blocking prevents any low frequency testing for this project.

3. Opto-Electronic Conversion/Amplification, DC Restoration

Figure (16) illustrates the signal conversion process. For each channel, the high speed, optimum-SNS-encoded optical pulse train returning from the interferometer is detected using germanium avalanche detectors and converted to an electrical pulse.

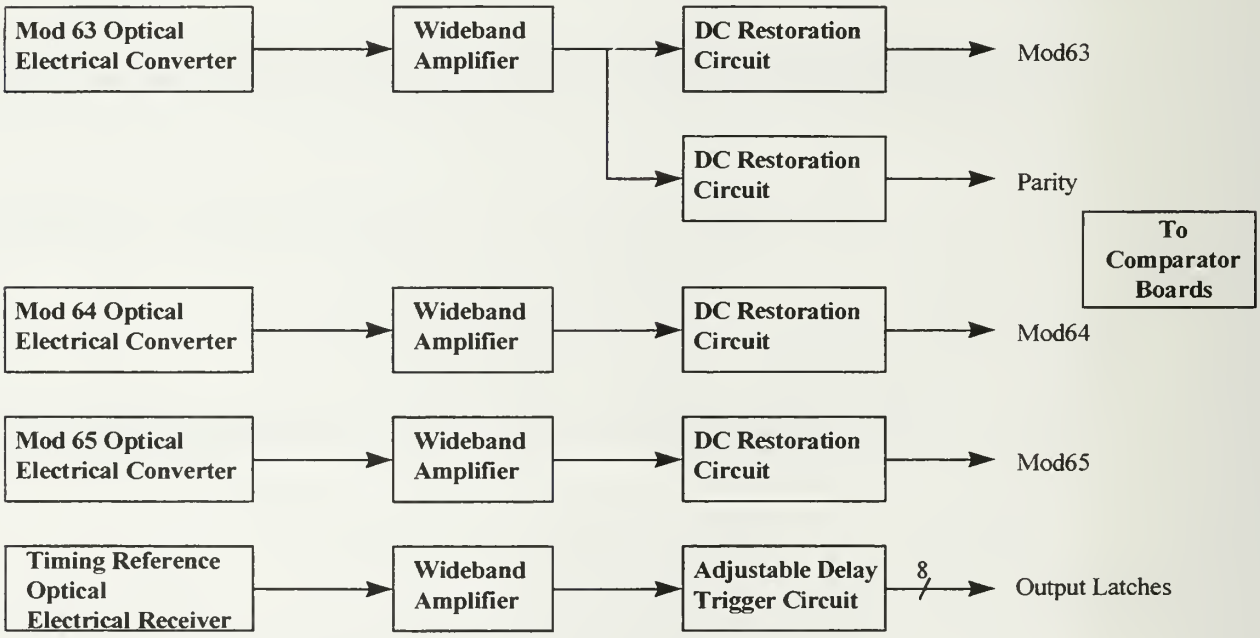

Figure (16): Analog electronic subsystem block diagram

The detector outputs are then applied to a variable-gain wideband amplifier which aids in the pulse recovery process. The wideband amplifier is AC coupled, which dictates the need for a DC restoration circuit in order to establish a reference level prior to the

comparator board stage. This circuit ensures that the pulsed signal is now operating between +1 and +3 volts DC, and away from the voltage rails of the comparator boards. Navy Research and Development, San Diego, CA conducted the design and implementation of the DC restoration circuit, as shown in Figure (17).

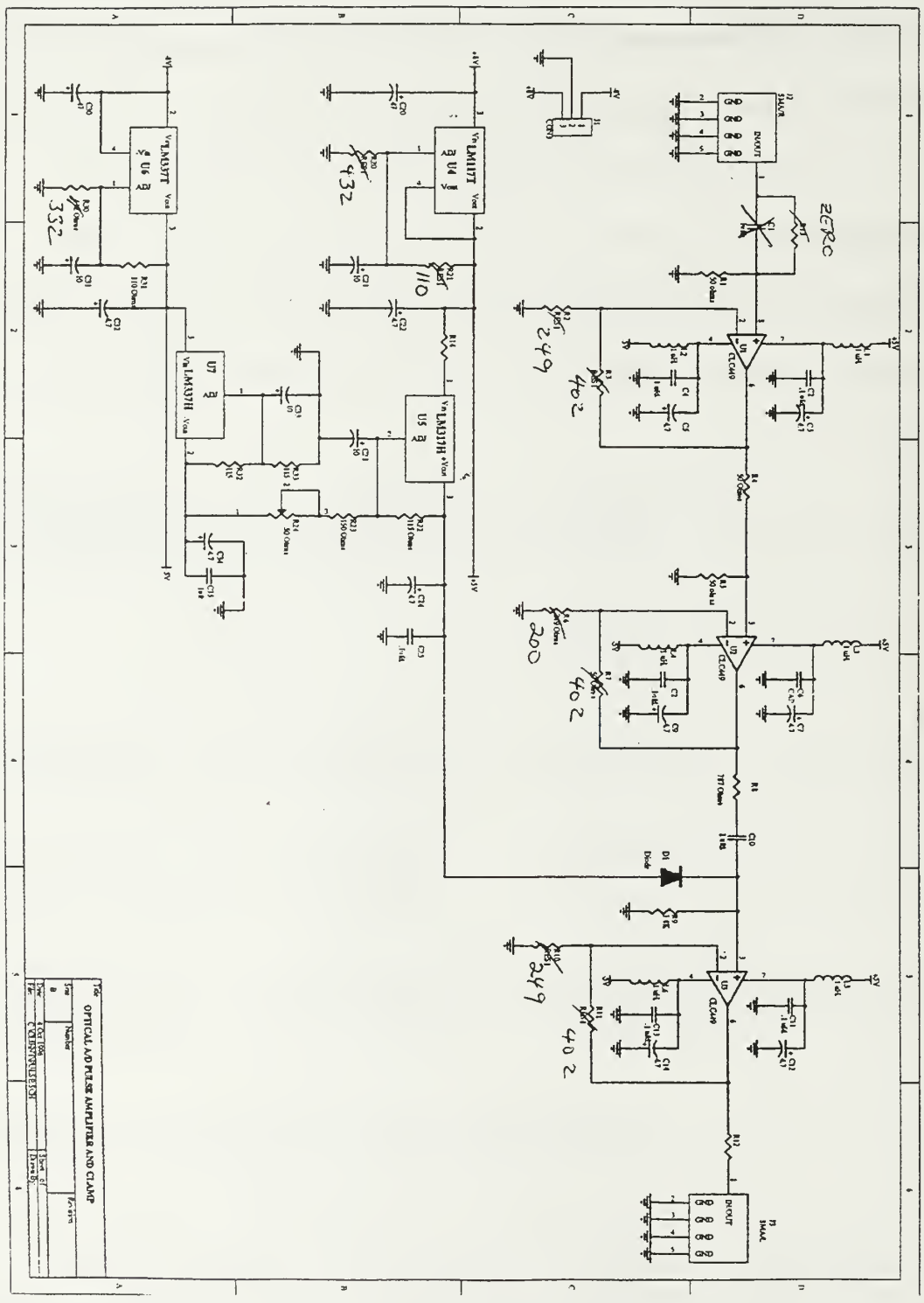

Figure (17): DC restoration circuit schematic

4. Adjustable Delay Trigger Circuit

Because of the different delays inherent in the three channels, an offset differential emitter coupled logic (ODECL) adjustable delay trigger circuit was designed and fabricated [Ref. 6] to ensure that the comparator latches are triggered synchronously with the arrival of the analog data. A block diagram of the adjustable delay trigger circuit is shown in Figure (18).

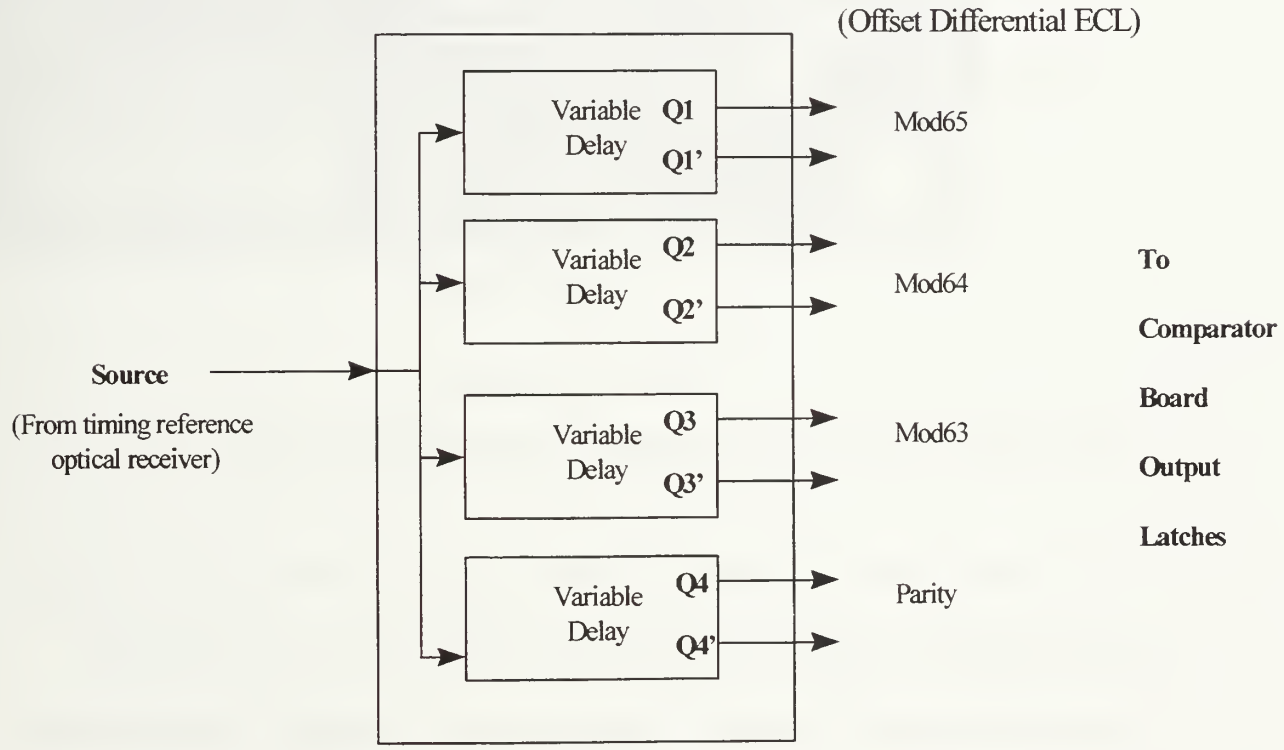

Figure (18): Adjustable delay trigger circuit block diagram

The ODECL adjustable delay trigger circuit reads the source pulse and triggers an adjustably delayed pulse that latches the comparator outputs for the four parallel channels when the data is valid.

Figure (19) illustrates the actual wire wrap construction of the circuit.

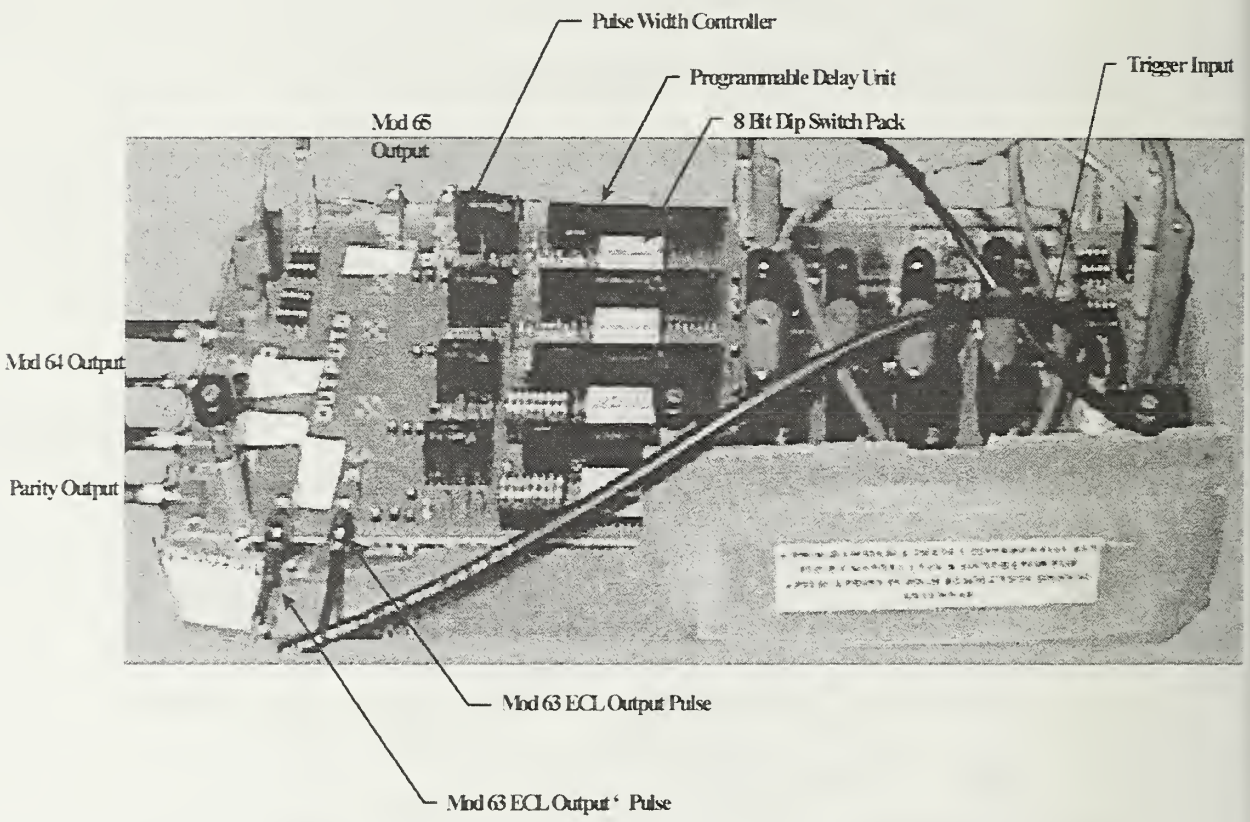

Figure (19): Laboratory construction of adjustable delay trigger circuit

The logic circuits use differential emitter coupled logic. The incoming 6-ns pulse is fed into stage one, a triple-line receiver, and then on to stage two, a mono-stable multivibrator ("one-shot"), in order to lengthen the pulse to the drive requirements of the programmable delay units. Stage three introduces the timing delay. This timing alignment is accomplished using 8-pin dip packs in conjunction with 2.5 kΩ resistor blocks which provide variable resistance to the programmable delay units. This stage introduces independent, variable delays for each channel in order to stagger the latching pulses so that they are in timing alignment with the data pulses arriving at the comparator boards. The

final stage is a pulse-width controller circuit which reduces the 100 ns pulse from stage three to a 30 ns pulse for the comparator boards. The overall circuit ensures that the comparator boards are latching at the precise moment of data arrival for all four channels.

Typical delays experienced are between 70 ns and 85 ns for the four individual channels. Figure (20) illustrates the time difference between the reference pulse train (lower waveform) and the Mod 65 data pulse (upper waveform) showing the non-zero delay them. The adjustable delay trigger circuit compensates for this delay. Chapter III illustrates the proper alignment of the data pulse train with the comparator latching pulse train.

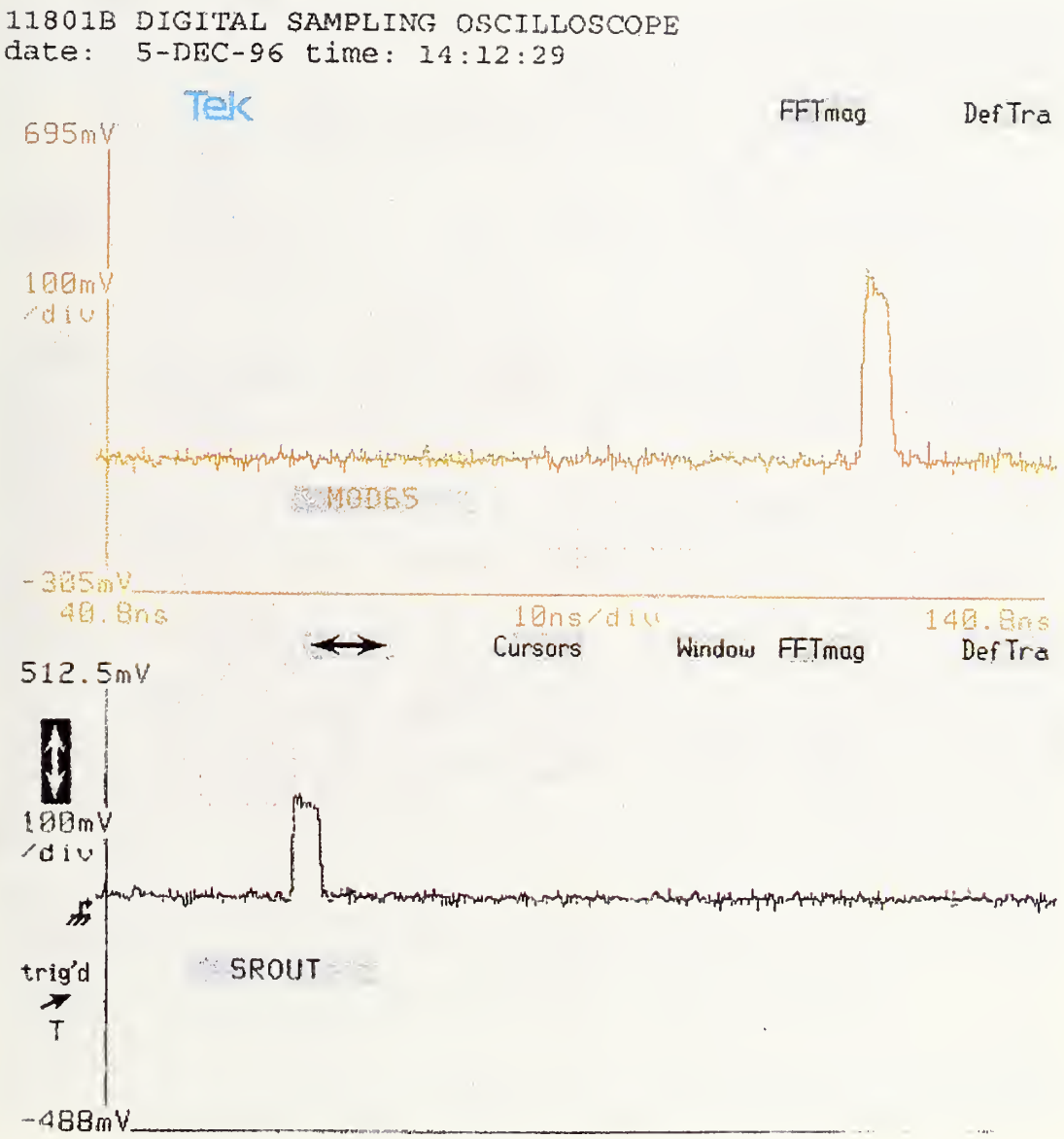

Figure (20): Delay between Mod 65 data pulse and reference pulse

Figure (21) illustrates a typical ODECL latching pulse from one of the parallel channels.

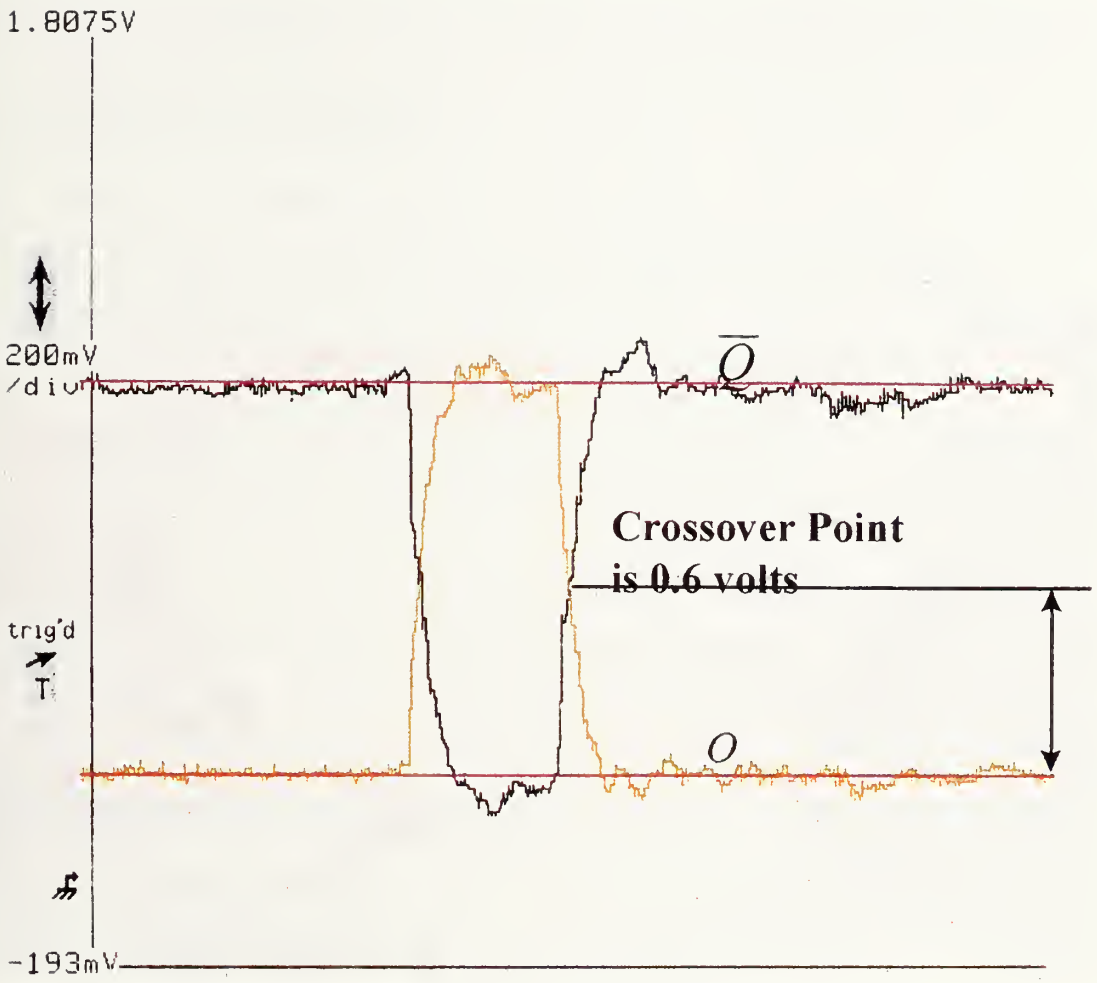

Figure (21): Offset differential emitter coupled logic latching pulse

The figure shows the two ODECL pulse outputs (Q and $\overline{Q}$) superimposed upon each other. For each channel, the two pulses are connected to the comparator boards where the crossover of Q and $\overline{Q}$, which occurs at 0.6 volts, is used to latch the comparators.

After a comprehensive review of the theory, modeling and laboratory set-up of the optical and analog electronics packages, described in this chapter, Chapter III introduces the actual experimental results of the individual subsystems.

III. INTERMEDIATE RESULTS

A. SUBSYSTEM OUTPUTS

This chapter details the experimental results of the individual subsystems, and also covers the phase alignment process, measured Signal to Noise Ratio (SNR) and calculation of the effective number of bits based on these measurements.

1. Mod 63, Mod 64, Mod 65 Signal-To-Noise Ratio

Figure (22) illustrates the channel outputs of the Mod 63, Mod 64, Mod 65, and the laser reference pulse versus time. In this figure, there is no analog input applied to the interferometers. Observe the significant levels of noise that have been impressed upon the pulse as it passes through the circulator, into the interferometer, and back through the circulator to the converter. The reason for this noise is still unclear, as there are no instruments within the laboratory to isolate the noise, given the circuit's unique one port configuration. One probable cause is constructive/destructive interference within the interferometer. As the pulse reflects off of the mirror, travels for a second pass over the electrode, and exits through port 1, it may experience interference with the subsequent incoming pulse. A second possibility is constructive/destructive interference between the entering and exiting pulses within the circulator.

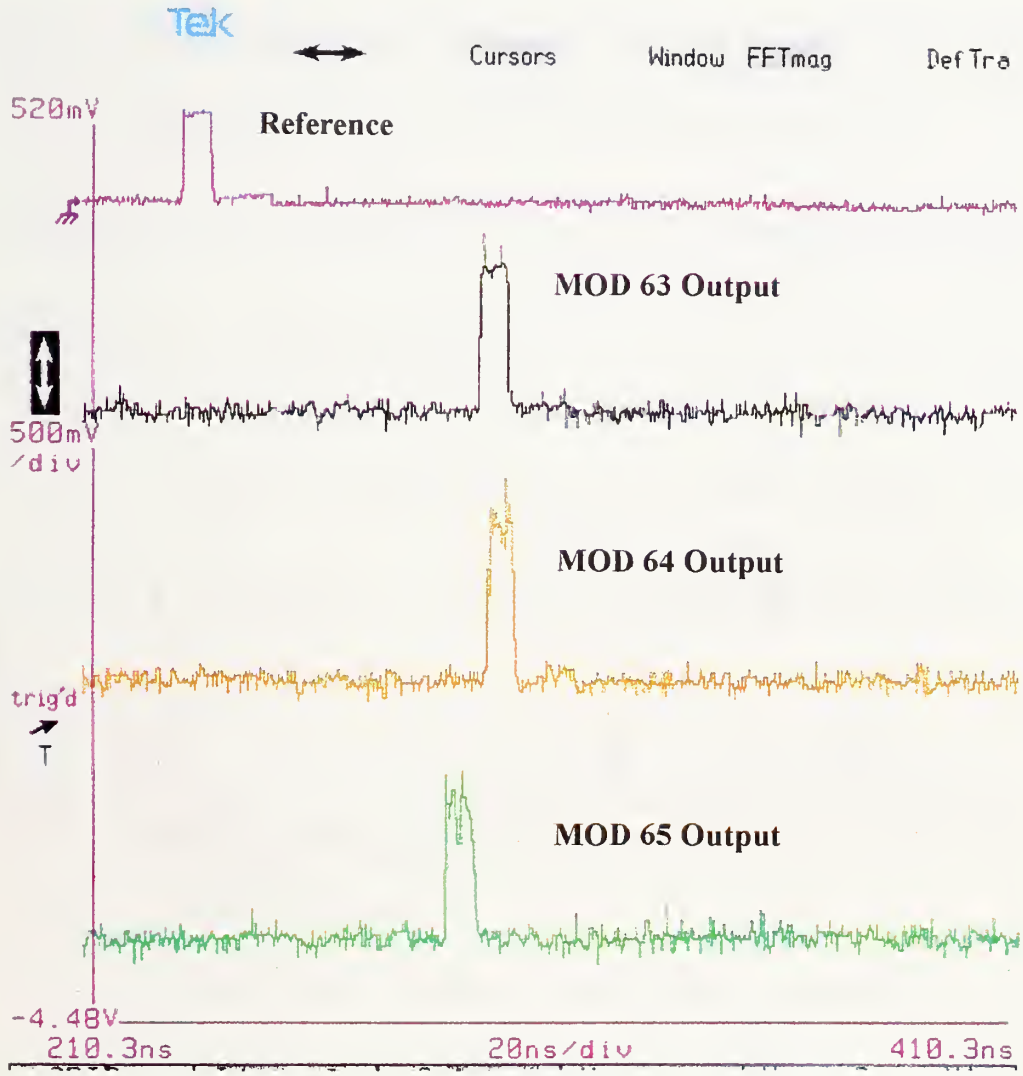

Figure (22): Comparison of interferometer outputs with the reference pulse

a. Mod 63 Signal-to-Noise Ratio, Effective Number of Bits

The measured signal-to-noise ratio is determined by:

$$\frac{S}{N} = \frac{V_{rms}}{V_{noise(rms)}} = \frac{300\,\text{mv}}{20\,\text{mv}} = 15.0\,,\ \text{or } 23.52\ \text{dB}.$$

The effective number of bits can now be calculated using [Ref. 7]:

$$\frac{S}{N}_{dB} = 6.02 n_{eff} + 1.76 \qquad (23)$$

For the Mod 63: n_{eff} = 3.62 bits, or approximately 3 bits.

b. Mod 64 Signal-to-Noise Ratio, Effective Number of Bits

Similarly, the signal-to-noise ratio for the Mod 64 channel is determined to be: $\frac{S}{N}_{dB} = 20\log\left(\frac{290\,\text{mv}}{20\,\text{mv}}\right) = 23.23\ \text{dB}$, and the effective number of bits, n_{eff} = 3.57 bits, or approximately 3 bits.

c. Mod 65 Signal-to-Noise Ratio, Effective Number of Bits

The signal-to-noise ratio for the Mod 65 channel is determined to be: $\frac{S}{N}_{dB} = 20\log\left(\frac{180\,\text{mv}}{40\ \text{mv}}\right) = 13.064\ \text{dB}$, and using equation (23) the effective number of bits, n_{eff} = 1.88 bits, or 1 bit.

2. DC Restoration Circuit Outputs

a. *Mod 63 Channel*

Figure (23) illustrates the output of the DC restoration circuit for the Mod 63 channel. The interferometer was modulated by a 5 kHz triangle wave analog input. Observe that the output signal is now folding between +1 and +3 volts and is ready for input to the comparator boards.

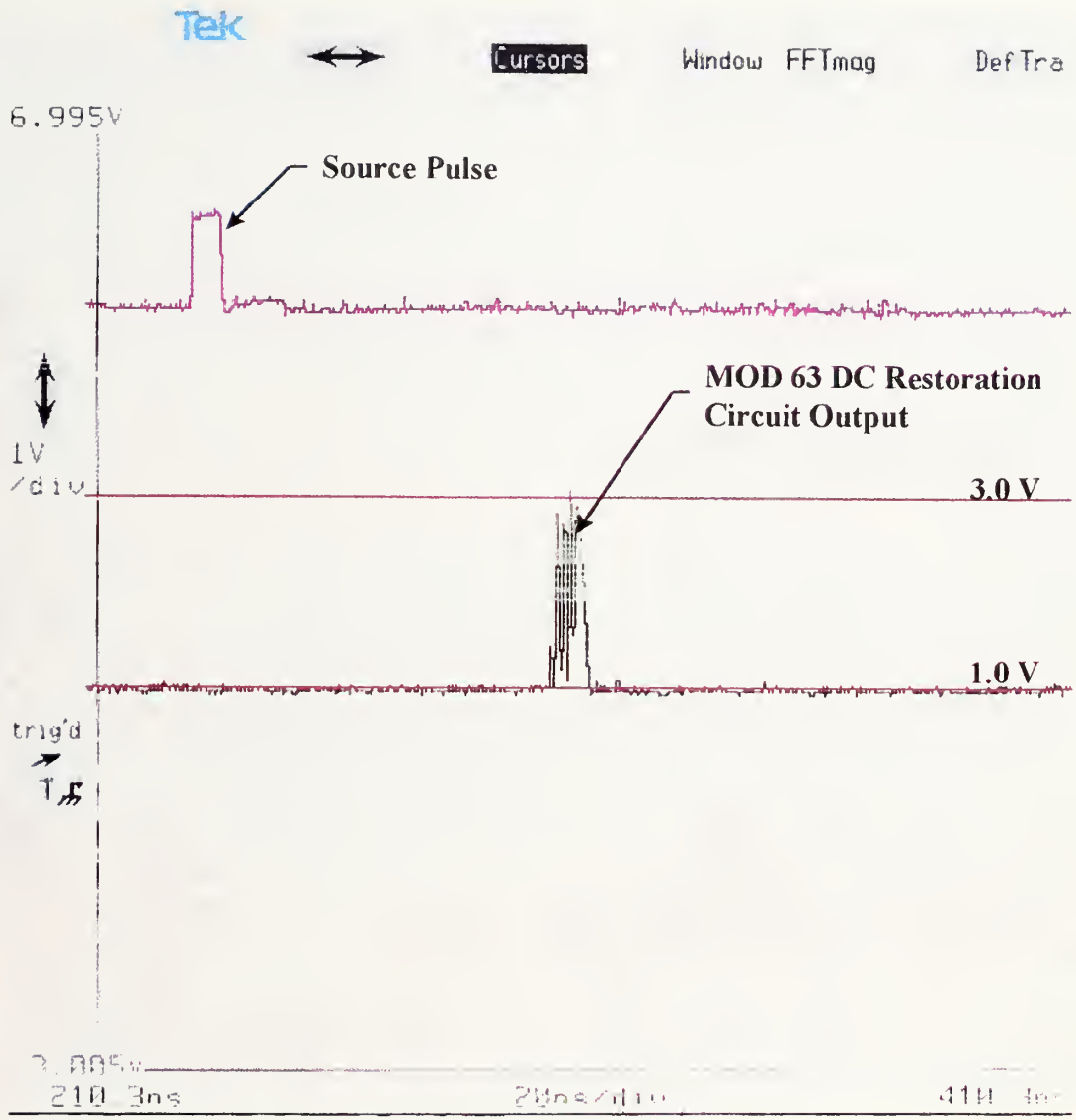

Figure (23): Mod 63 DC restoration circuit output

b. *Mod 64 Channel*

Figure (24) illustrates the output of the DC restoration circuit for the Mod 64 channel. The interferometer had the same 5 kHz triangle wave analog input. Again, observe that the output signal is now folding between +1 and +3 volts and is ready for input to the comparator boards.

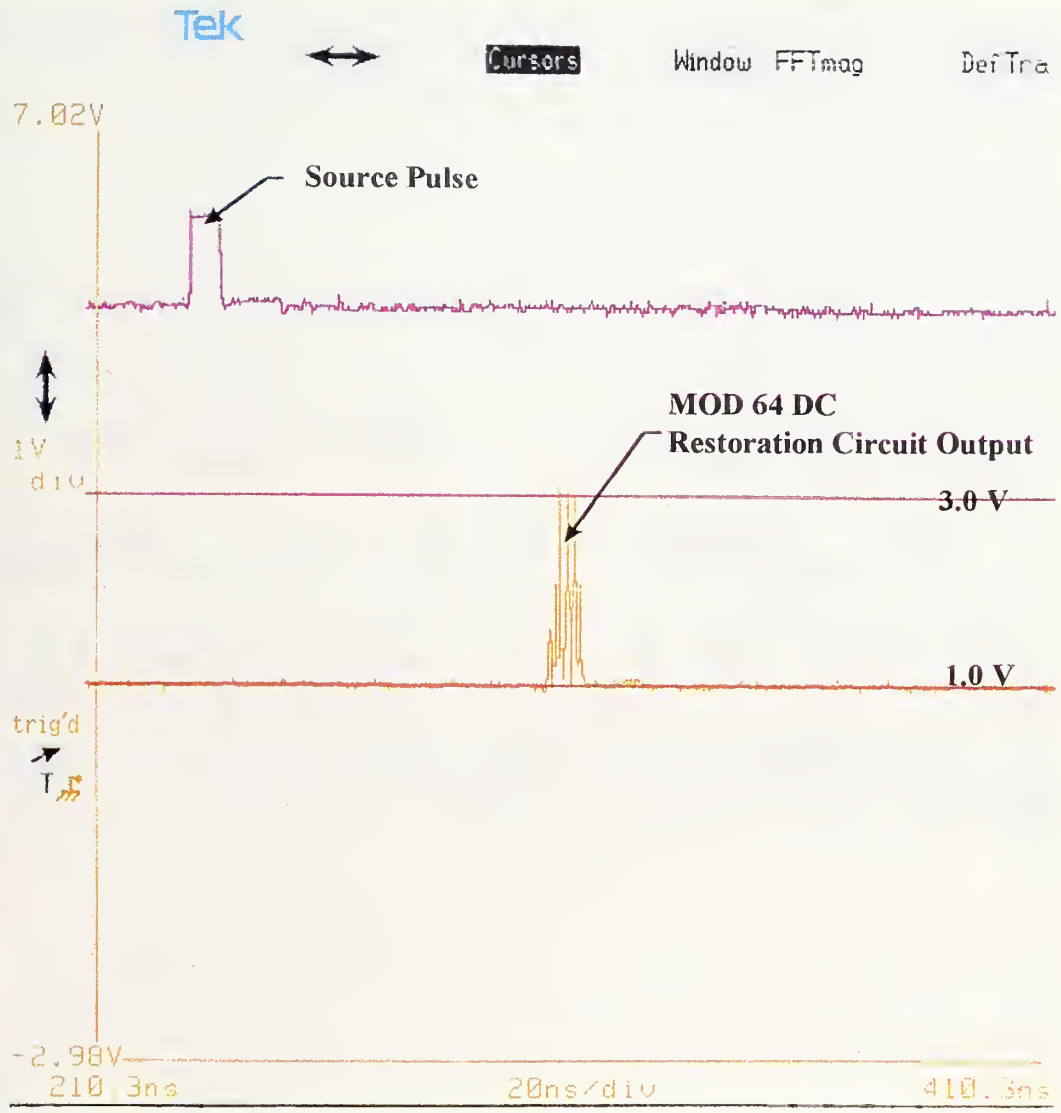

Figure (24): Mod 64 DC restoration circuit output

c. ***Mod 65 Channel***

Figure (25) illustrates the output of the DC restoration circuit for the Mod 65 channel. The figure verifies that the output optimum SNS waveform is folding between +1 and +3 volts. As before, a 5 kHz triangle wave test signal is applied to the electrodes of the MZI.

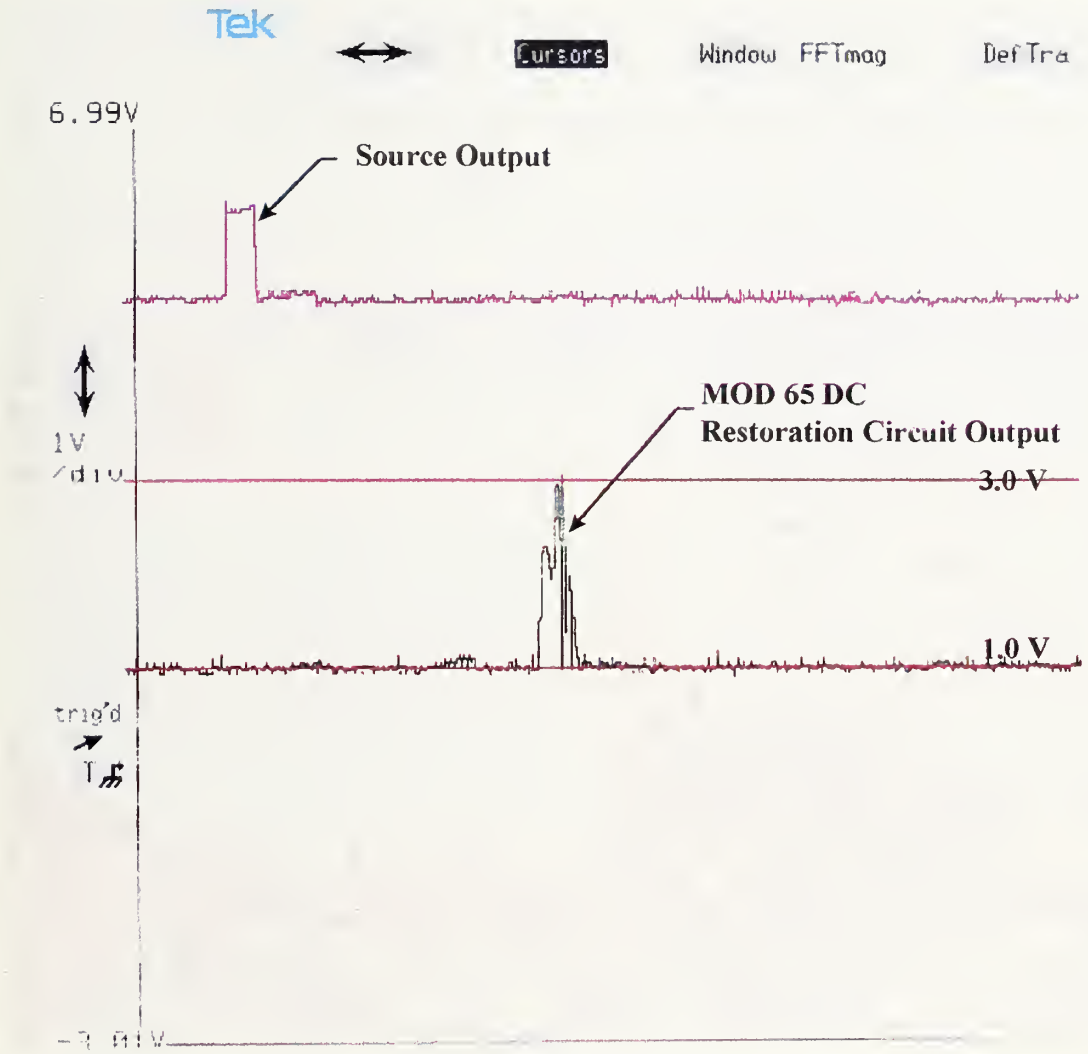

Figure (25): Mod 65 DC restoration circuit output

3. Adjustable Delay Trigger Circuit

a. *Parity Channel: Comparison of Latching Pulse with Data Pulse*

Figure (26) shows the offset differential emitter coupled logic pulse from the parity channel of the adjustable delay trigger circuit versus the data pulse.

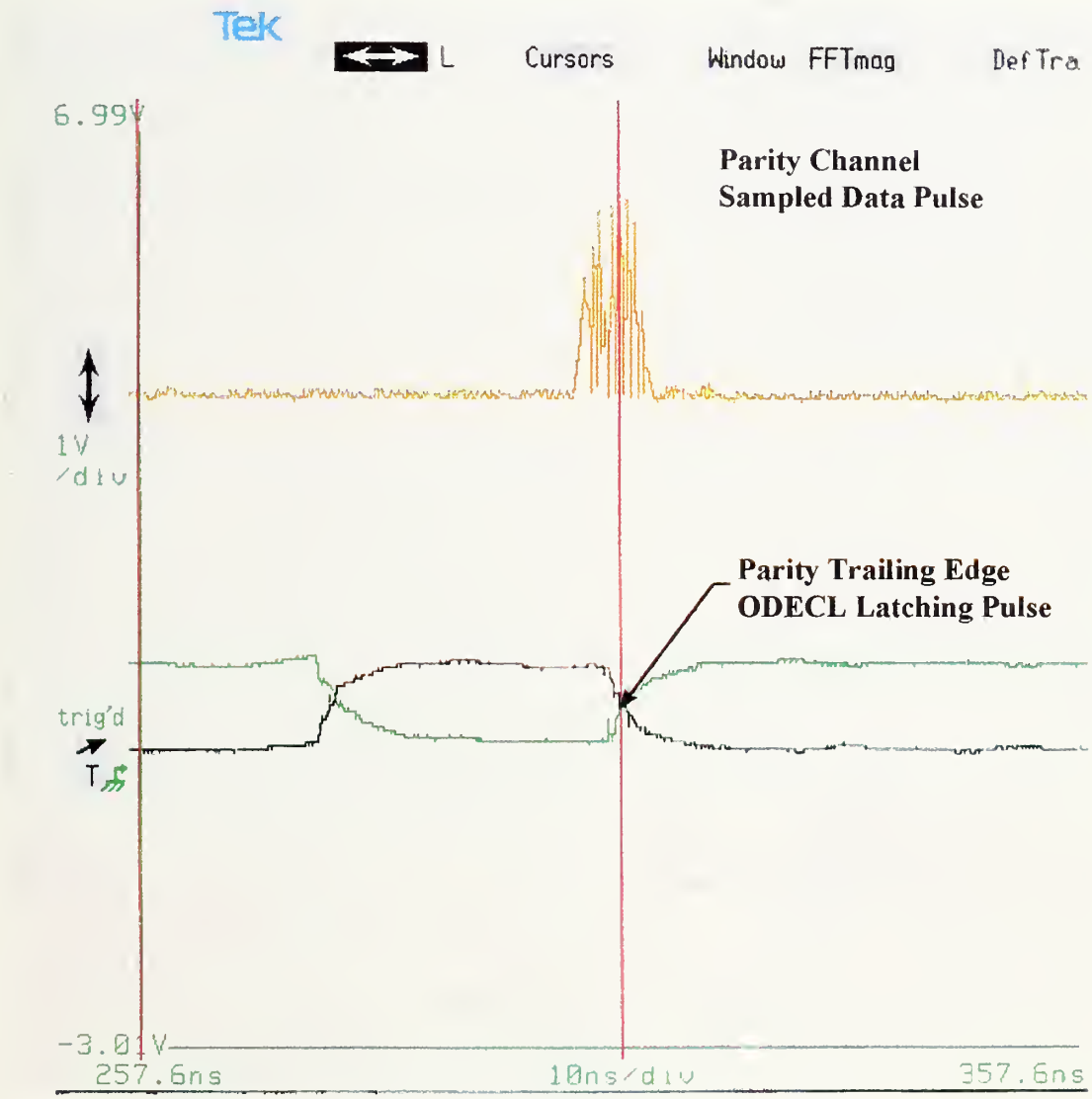

Figure (26): ODECL trigger circuit alignment with data pulse

The data pulse is modulated by a 5 kHz triangle wave test signal. Observe how the trailing edge of the logic pulse was adjusted via the dip switches so that it is in

timing alignment with the approximate center of the data pulse. Thus, the comparators are latched time coincidental with data arrival.

b. ***Mod 63 Channel: Comparison of Latching Pulse with Data Pulse***

Figure (27) shows the offset differential emitter coupled logic pulse from the Mod 63 channel of the adjustable delay trigger circuit versus the data pulse. Again, the data pulse is modulated by a 5 kHz triangle test signal. The trailing edge of the logic pulse is in timing alignment with the approximate center of the data pulse, ensuring that the comparators are latching at the same time as data arrival.

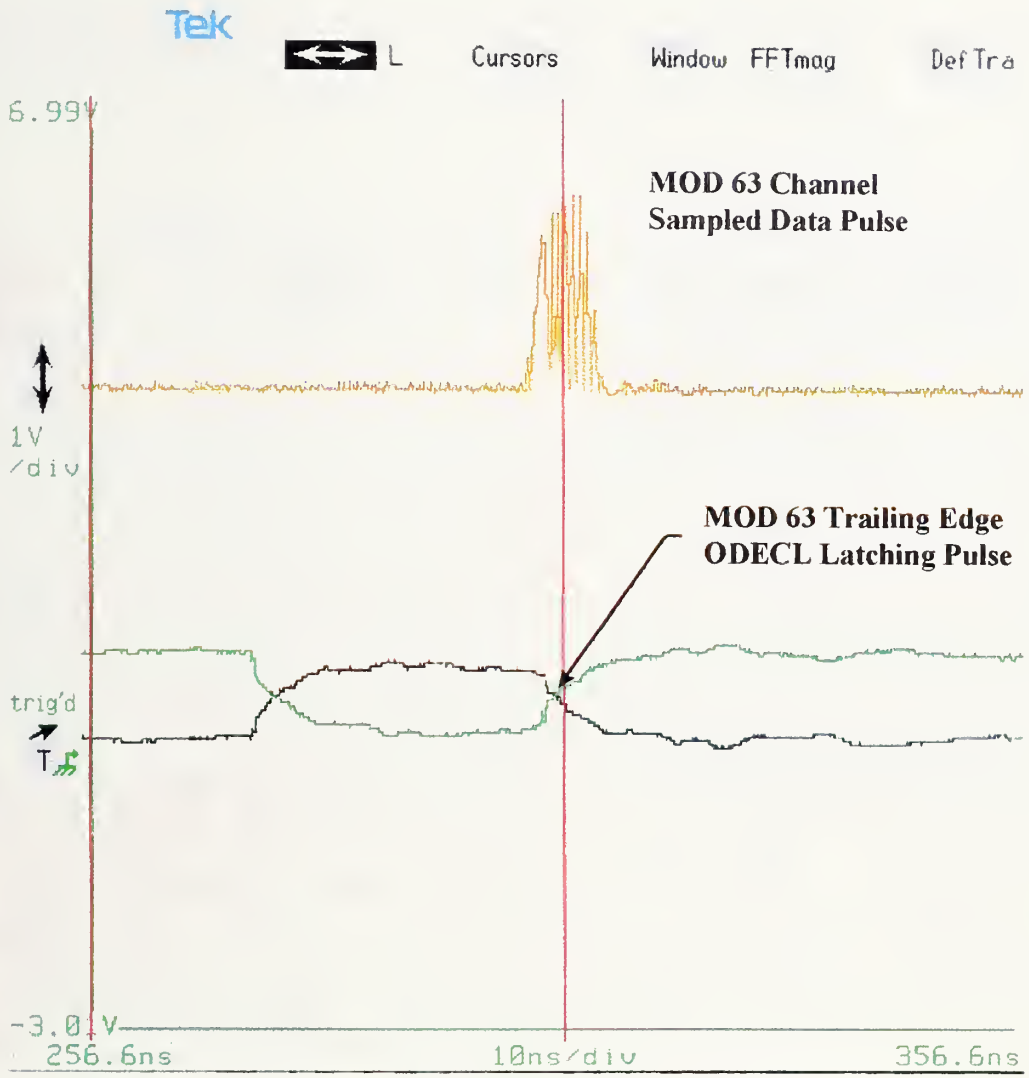

Figure (27): Mod 63 ODECL trigger alignment with data pulse

c. ***Mod 64 Channel: Comparison of Latching Pulse with Data Pulse***

Figure (28) shows the offset differential emitter coupled logic pulse for the Mod 64 channel of the adjustable delay trigger circuit versus the data pulse. The data pulse is modulated by a 5 kHz triangle wave test signal. The trailing edge of the logic pulse is adjusted via the dip switches so that it is in timing alignment with the

approximate center of the data pulse thus ensuring the comparators are latched time coincidental with data arrival.

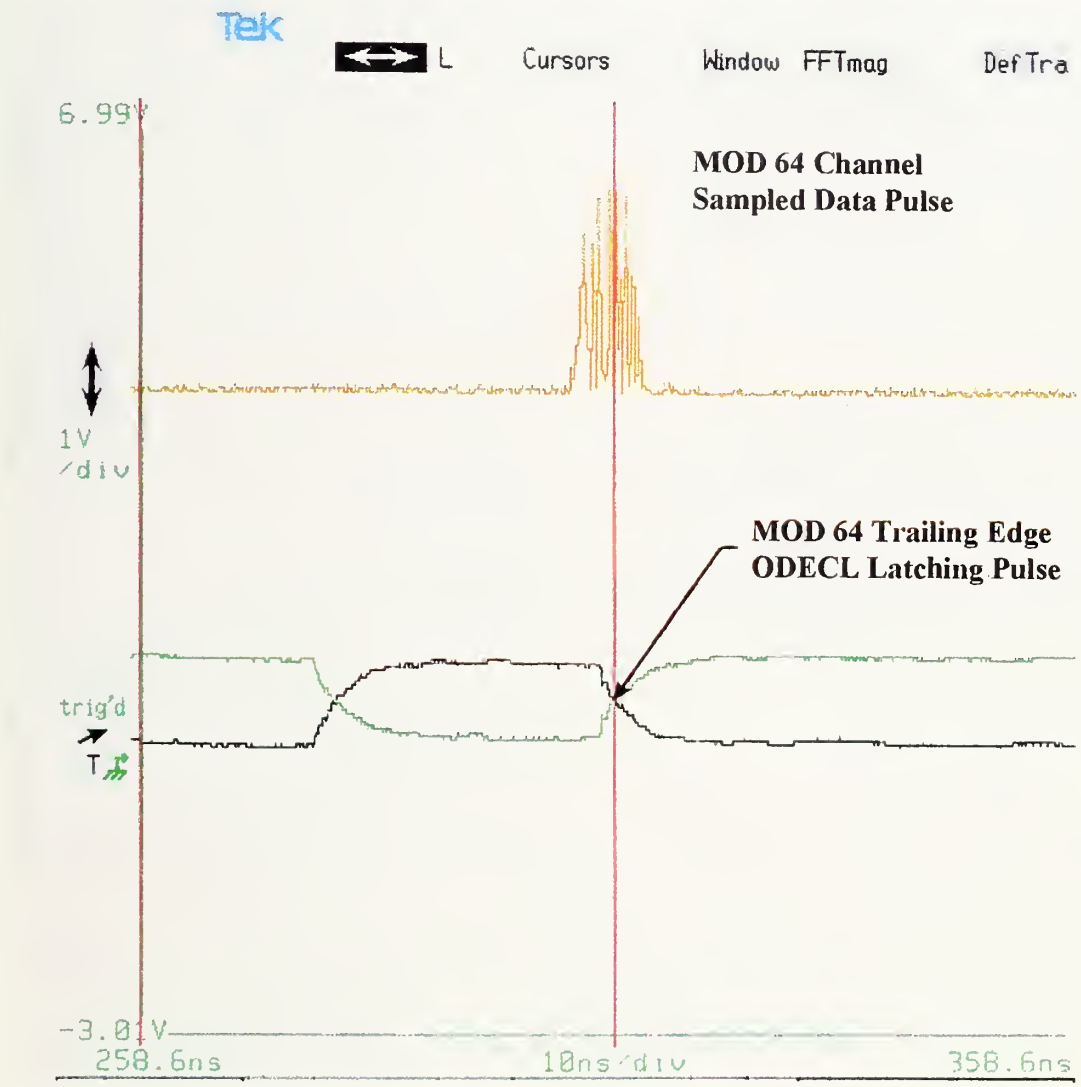

Figure (28): Mod 64 ODECL trigger alignment with data pulse

d. ***Mod 65 Channel: Comparison of Latching Pulse with Data Pulse***

Figure (29) shows the offset differential emitter coupled logic pulse from the Mod 65 channel of the adjustable delay trigger circuit versus the data pulse.

Again, the figure demonstrates proper timing of the latching pulse to the comparator boards and the data pulse of the particular channel.

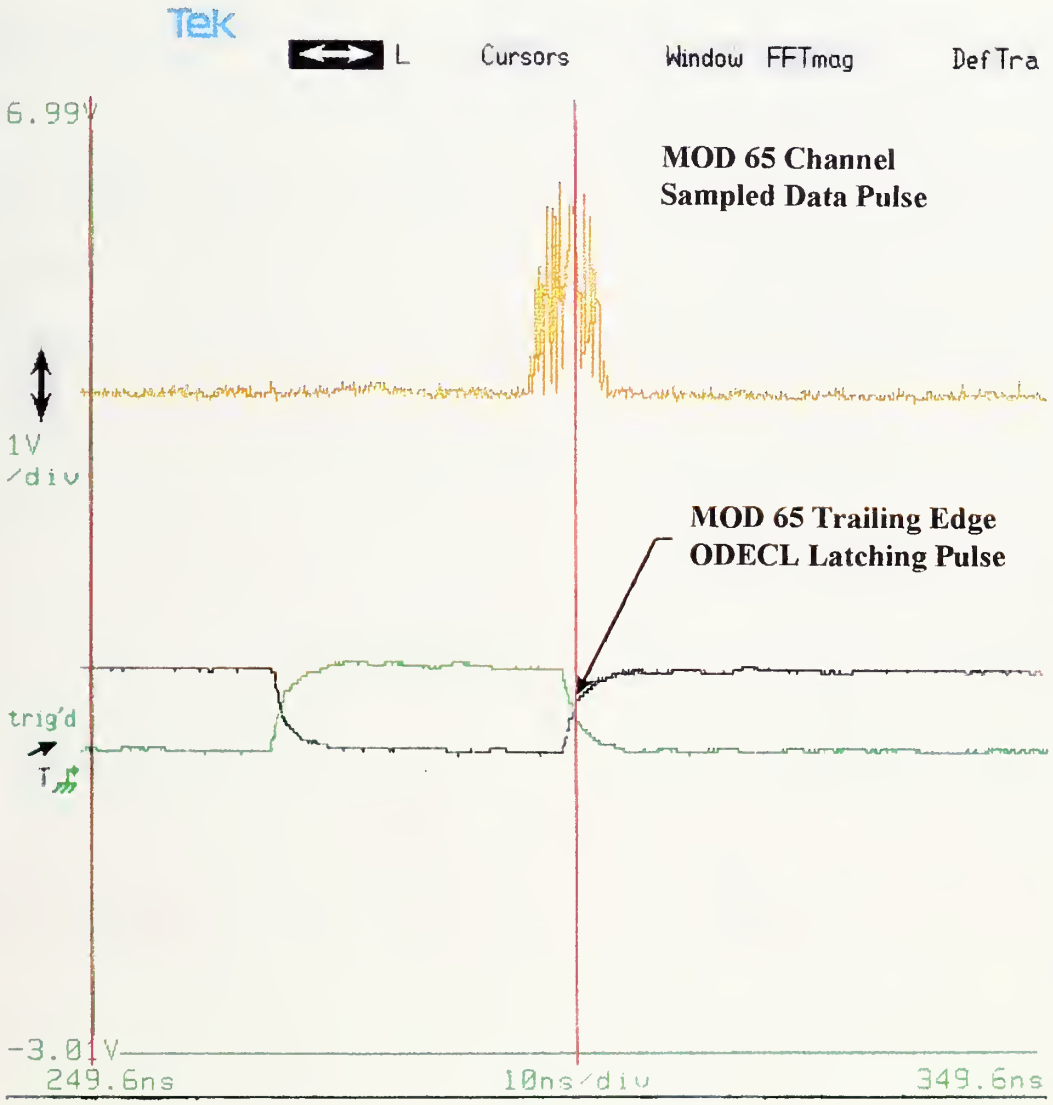

Figure (29): Mod 65 ODECL trigger alignment with data pulse

4. Phasing Of Folded Output Waveforms

a. *Parity Channel*

Figure (30) illustrates the precise phasing of the output waveform using the DC bias circuitry for the parity circuit. A 5 kHz triangle wave was applied to the

analog input of the interferometer. At the measured zero crossover point of the triangle wave (the triangle wave and the analog input are measured on two different amplitude scales), the interferometer output will be at a minimum, which for this particular case is +1 volts (measured from the DC restoration circuit output). By applying a DC bias to the input, the phasing of the interferometer output can be adjusted to yield its minimum value at the desired zero crossover point of the analog input signal. A time delay of 83.0 ns was observed, which is attributed to differing path lengths at the measurement points. In the follow-on stage, the adjustable delay trigger circuit delays the latching of the comparators in order to compensate for the delayed data arrival.

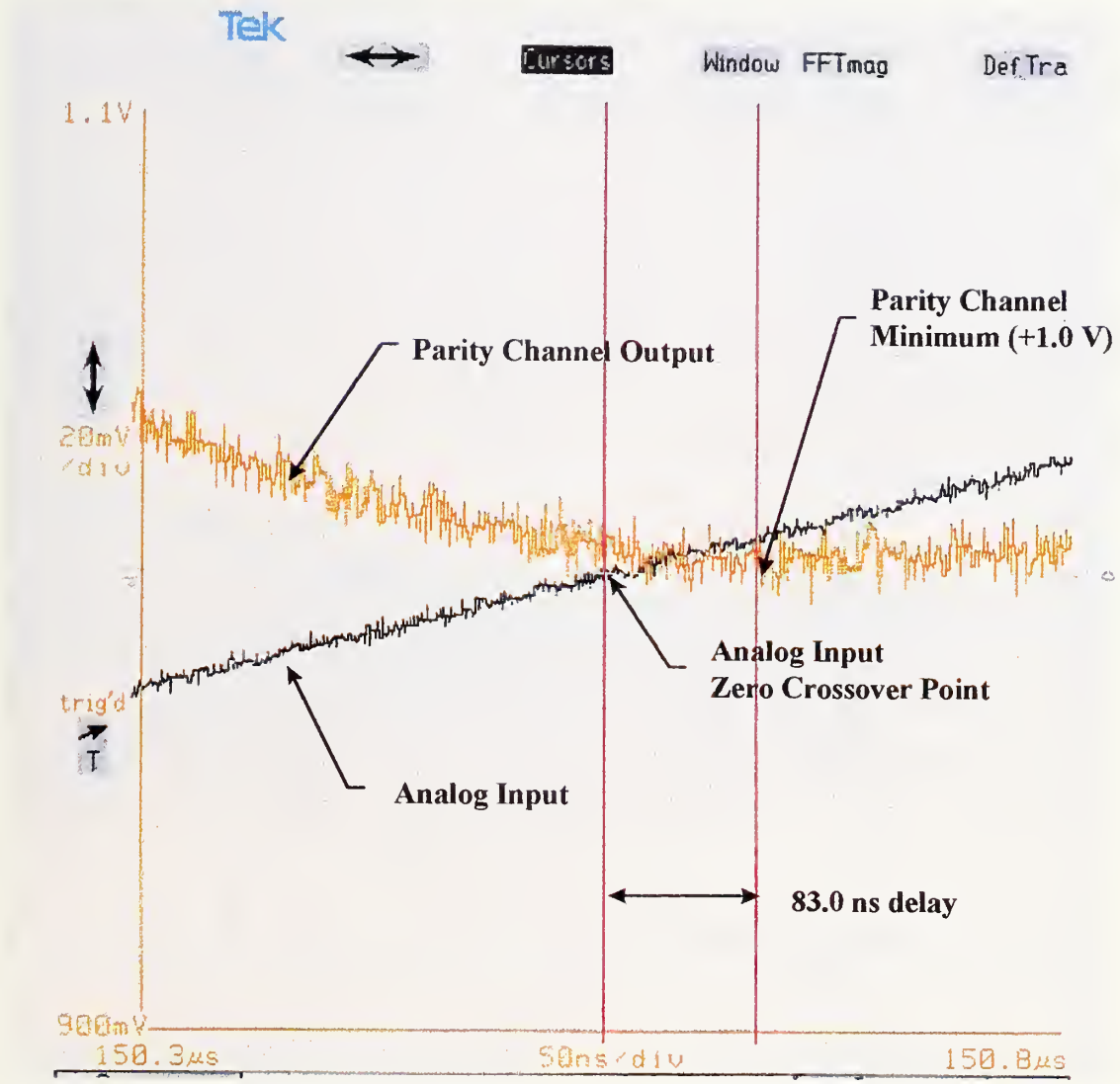

Figure (30): Phasing of Parity channel minimum and zero crossover point

b. *MOD 63 Channel*

Figure (31) illustrates the precise phasing of the Mod 63 output waveform using the DC bias circuitry. The figure shows that at the zero crossover point of the analog input, the optimum SNS output voltage is at its established minimum of +1 volt. The timing delay between the two measurement points is 82.9 ns.

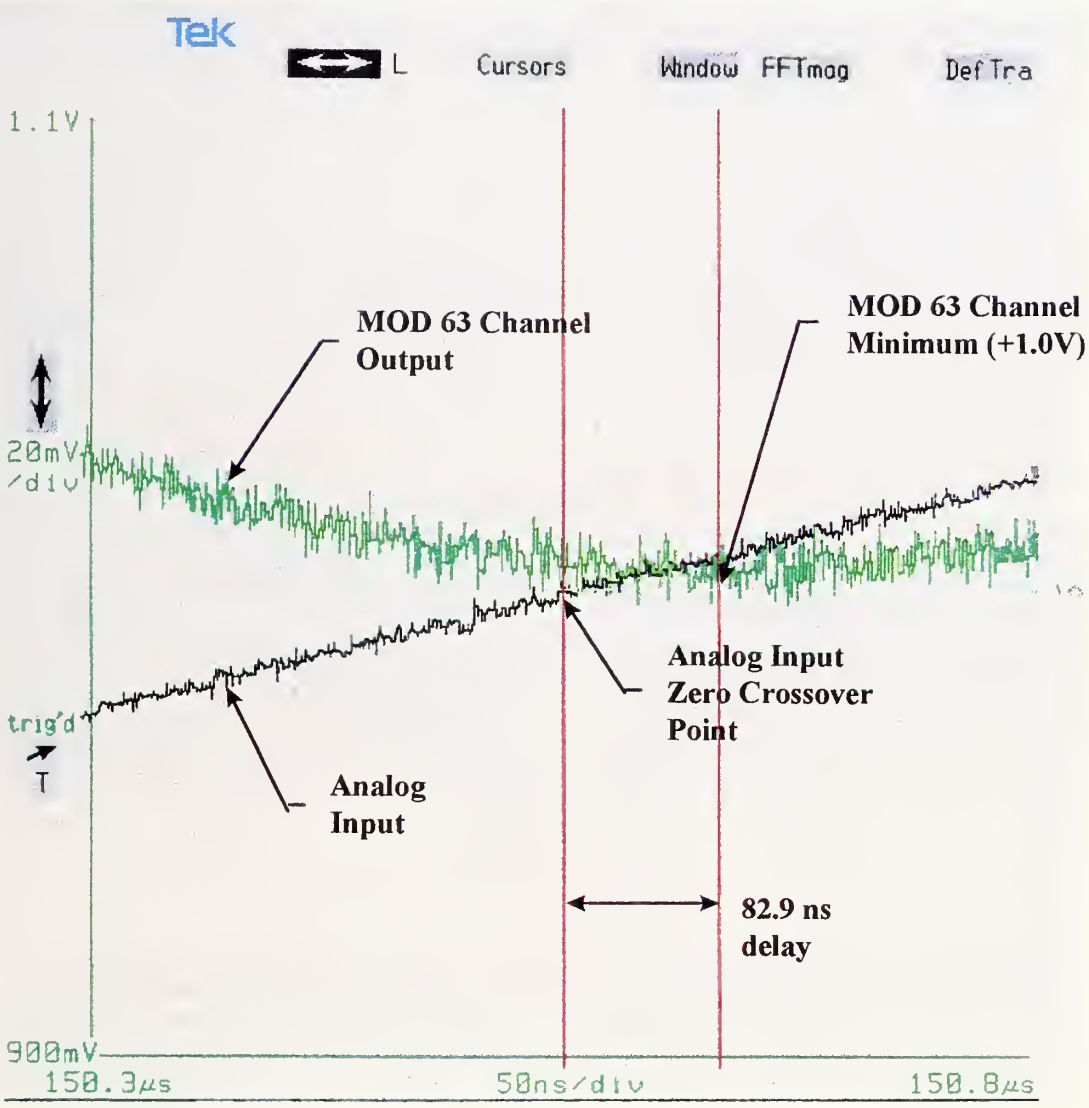

Figure (31): Phasing of Mod 63 minimum and zero crossover point

c. *Mod 64 Channel*

Figure (32) illustrates the detailed phasing of the Mod 64 output waveform using the DC bias circuitry. This channel has a delay of 82.4 ns.

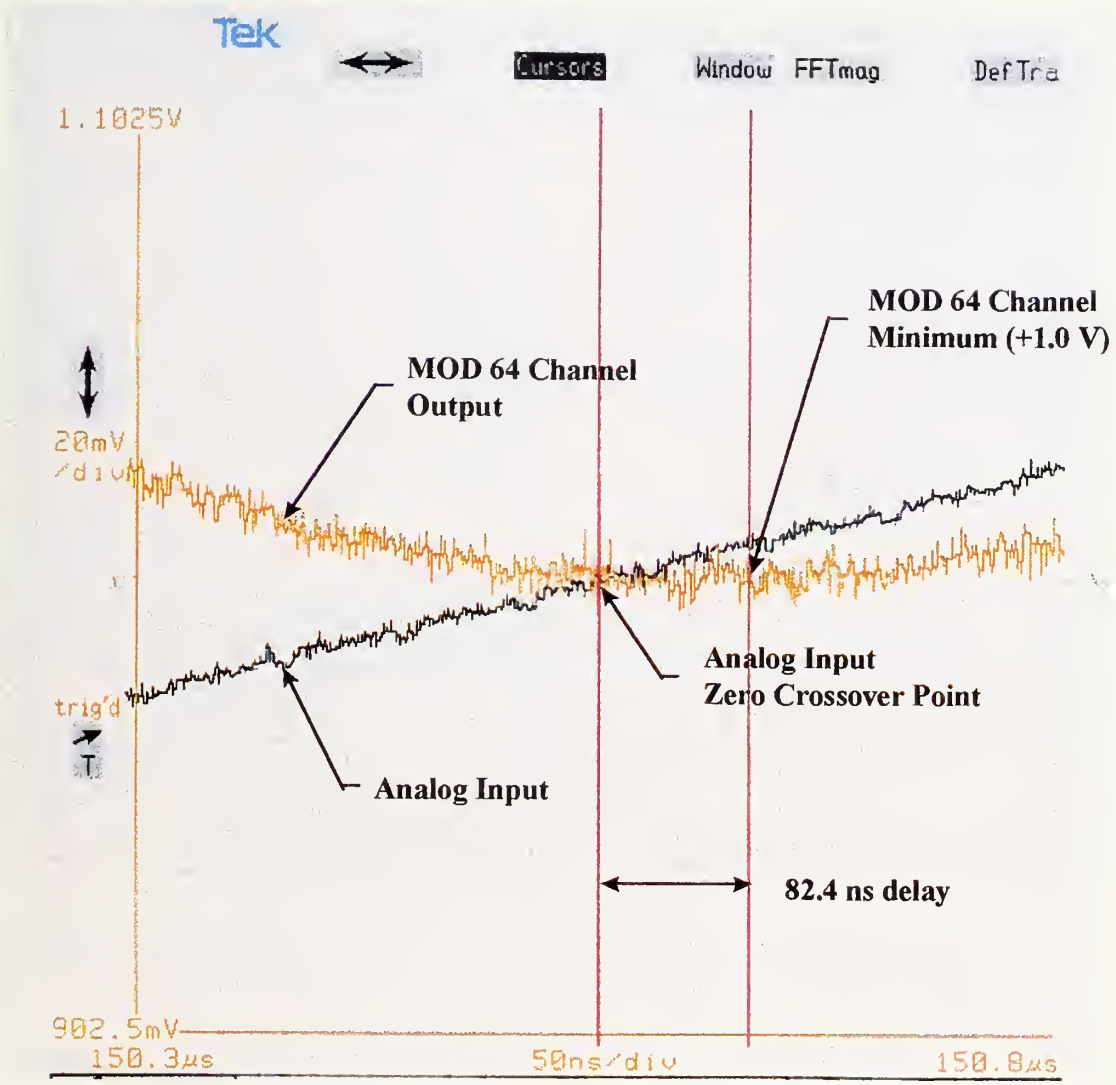

Figure (32): Phasing of the Mod 64 minimum and the zero crossover point

d. ***Mod 65 Channel***

Figure (33) illustrates the detailed phasing of the Mod 65 output waveform using the DC bias circuitry. The figure illustrates the interferometer output to be at its minimum of +1 volt, when the 5 kHz triangle wave is at its zero crossover point. The delay due to differing propagation times is 70.0 ns.

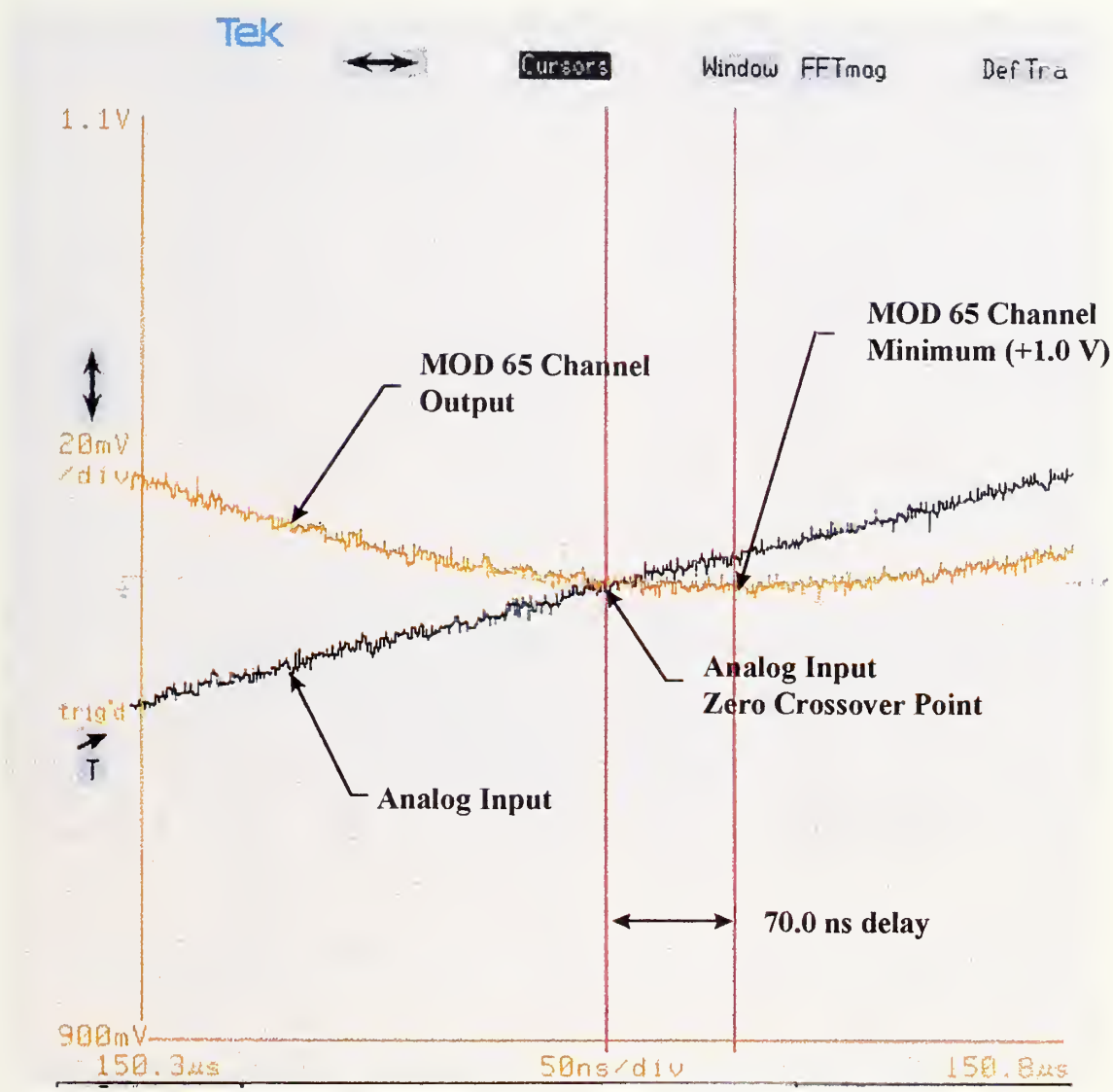

Figure (33): Phasing of Mod 65 output minimum and zero crossover point

e. *Combined, Phase Adjusted Channel Outputs*

Figure (34) illustrates the combined 4 channel output of the precise phase adjusted waveforms versus a 5 kHz triangle wave analog input. Observe that the signals are phased properly and folding between +1 and +3 volts.

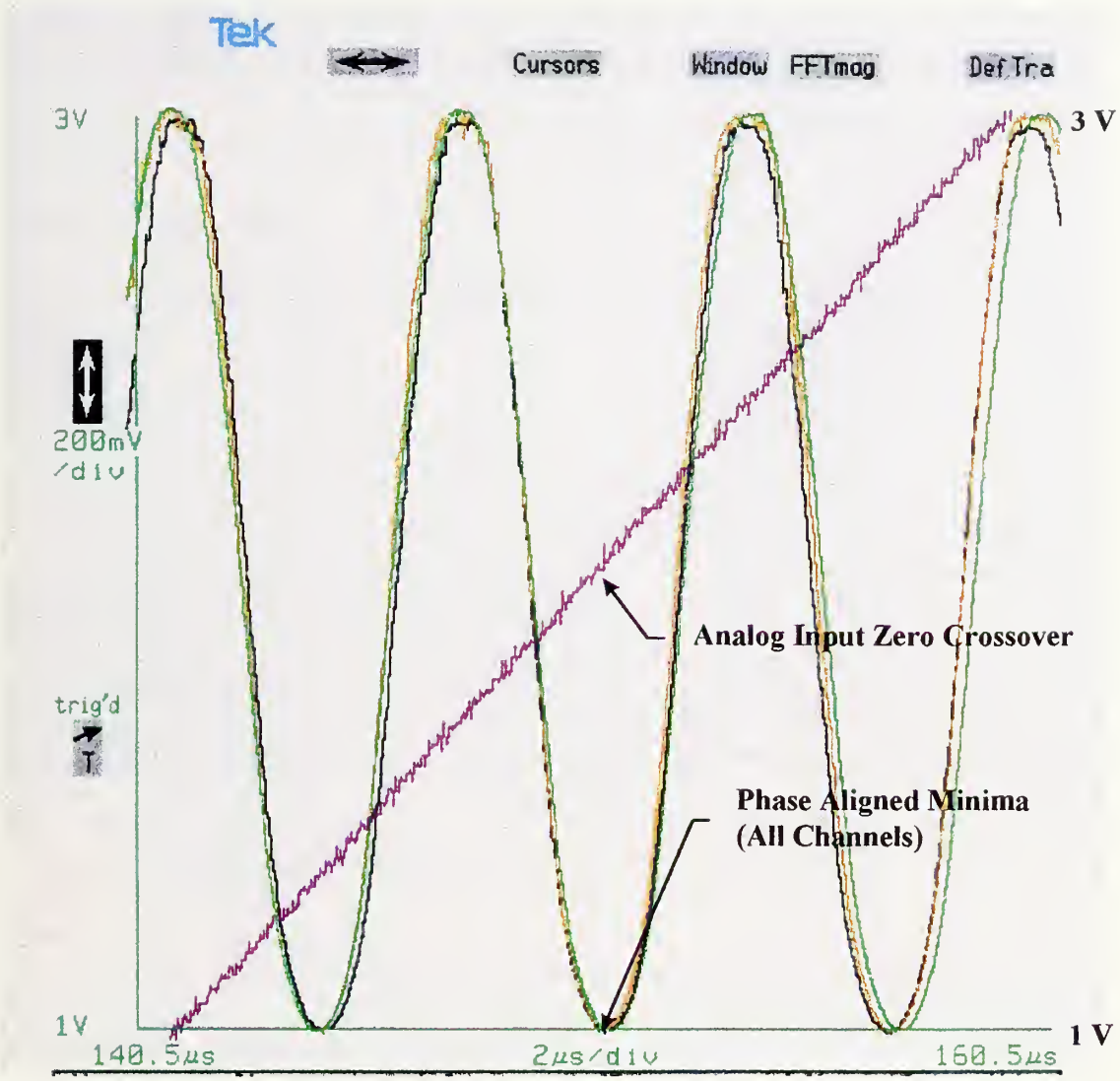

Figure (34): Combined, phase adjusted outputs versus analog input

5. Measurement And Analysis Of V_π

a. *Mod 63 Interferometer*

With a 10 volt peak-to-peak, 5-kHz triangle wave applied to the analog input and the laser sampling in continuous mode, the output frequency of the interferometer was measured and compared to the input frequency to determine V_π. The measured output frequency was: $f_{measured}$ = 153.9 kHz. The number of folds per

10 volts is determined by: N = 153.9 kHz / 5 kHz = 30.78 folds. Therefore the measured V_π is: $V_{\pi\,(measured)}$ = 10.0 volts / 30.78 folds = 0.3249 volts. This value corresponds directly to the theoretical value of V_π which is: $V_{\pi\,(theoretical)}$ = 0.32 volts, determined from equation (7). From this, $N_{(theoretical)}$ = 31.25 folds. The percent deviation from the measured value and the calculated value of V_π is determined to be 1.5 %.

b. ***Mod 64 interferometer***

Using the same technique as before, V_π for the Mod 64 interferometer was determined. The measured output frequency was: $f_{measured}$ = 147.4 kHz. The number of folds per 10 volts is: N = 147.4 kHz / 5 kHz = 29.48 folds. Therefore the measured V_π is: $V_{\pi\,(measured)}$ = 10.0 volts / 29.48 folds = 0.3392 volts. The theoretical value of V_π is determined by: $N_{(theoretical)} = \left(\frac{63}{64}\right)31.25 = 30.76$ folds, hence, $V_{\pi\,(theoretical)}$ = 10 volts / 30.76 folds = 0.3251 volts. The percent deviation between the theoretical and the measured values of V_π is 4.15 %.

c. ***Mod 65 Interferometer***

The measured output frequency was: $f_{measured}$ = 146.2 kHz. The number of folds per 10 volts is: N = 146.2 kHz / 5 kHz = 29.24 folds. Therefore the measured V_π is: $V_{\pi\,(measured)}$ = 10.0 volts / 29.24 folds = 0.3420 volts. The theoretical value of V_π is determined by: $N_{(theoretical)} = \left(\frac{63}{65}\right)31.25 = 30.29$ folds, therefore,

$V_{\pi\,(\text{theoretical})}$ = 10 volts / 30.29 folds = 0.3302 volts. The percent deviation between the theoretical and measured values of V_{π} is 3.45 %.

The error between the theoretical and measured values is most likely attributed to the amount of constructive/destructive interference within the optical circuitry. This interference directly affects the measurement of the output frequency from the interferometer by introducing nonlinearities to the folded output waveform. This chapter provided pertinent outputs of some key components within the optical and analog electronics subsections. Chapter IV will detail the digital output code of the comparator boards for linear and non-linear test signals.

IV. SYSTEM PERFORMANCE

This chapter illustrates the digital output code of the comparator banks for a variety of test signals used as the antenna input. A Field Programmable Gate Array (FPGA) processed the thermometer code output from the comparator banks and translated it into a digital representation [Ref. 2]. A logic analyzer measured the digital value of the number of comparators in the *on* state and recorded them over time.

A. PARITY CIRCUIT

Figure (35) illustrates the digital output for a 5 kHz triangle wave. In the logic analyzer display shown in the figure, the Y axis indicates the number of comparators turned on, and the X axis indicates time. The figure shows qualitatively a sinusoidal output in accordance with the transfer function of the interferometer referenced in equation (3). The phase of the folded output changes in proportion to the linear ramped input voltage level. Some distortion is evident due to the amount of noise introduced within the optical circuitry.

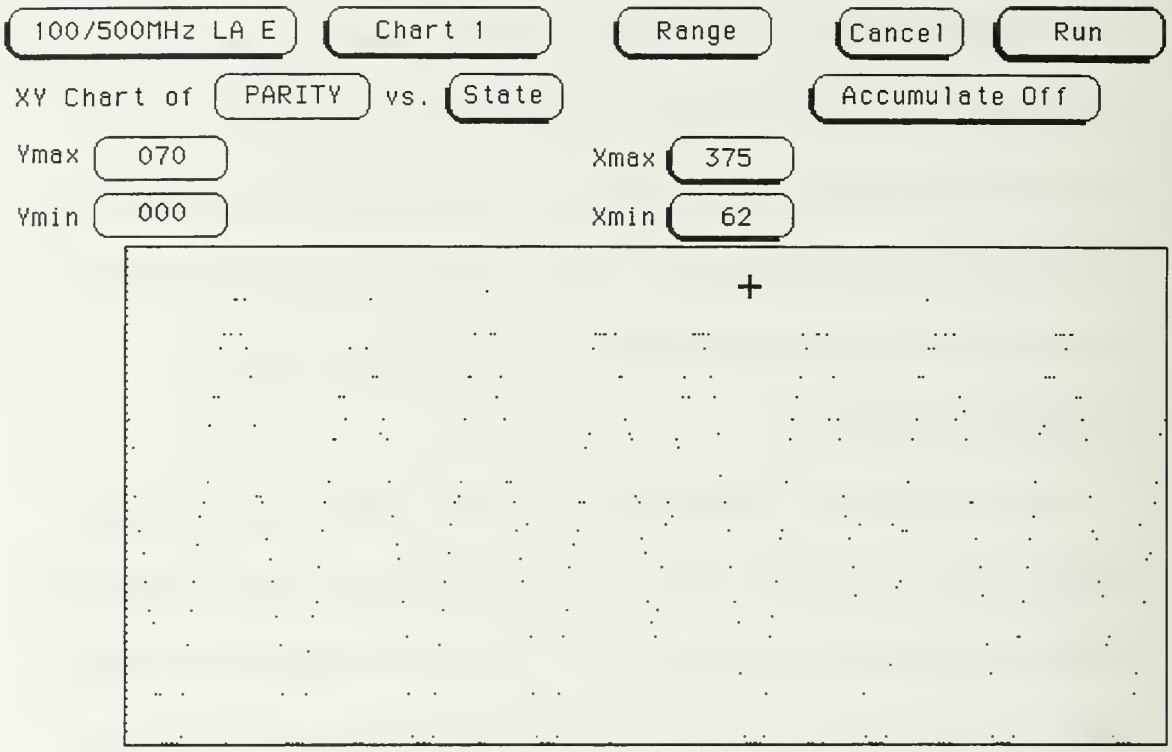

Figure (35): Digital output of Parity channel for a triangle wave antenna input

Figure (36) illustrates the digital output code of the Parity channel comparator bank for a 5 kHz analog sinusoidal antenna input. This figure shows a non-linear output in accordance with equation (3). Two phase crossovers are observed on the left and right sides of the figure.

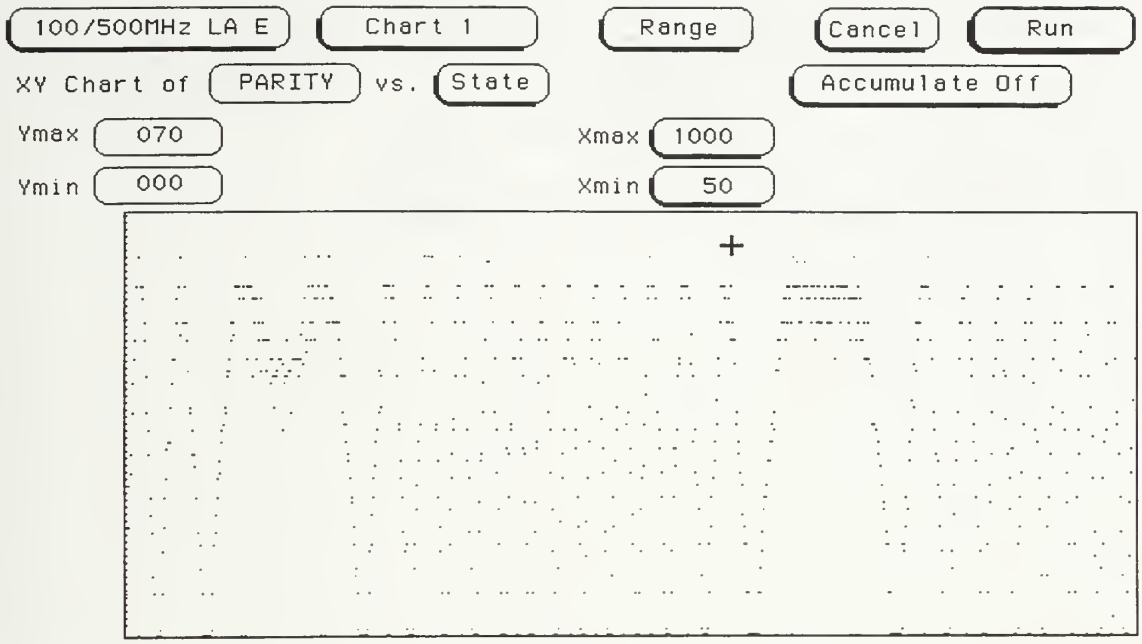

Figure (36): Digital output of parity channel for a sinusoidal antenna input

B. MOD 63 CHANNEL

Figure (37) illustrates the digital output of the Mod 63 comparator bank for an linear ramped triangle wave antenna input. The figure shows a sinusoidal output in accordance with the transfer function of the interferometer referenced in equation (3). Some distortion is evident due to the amount of noise introduced within the optical circuitry.

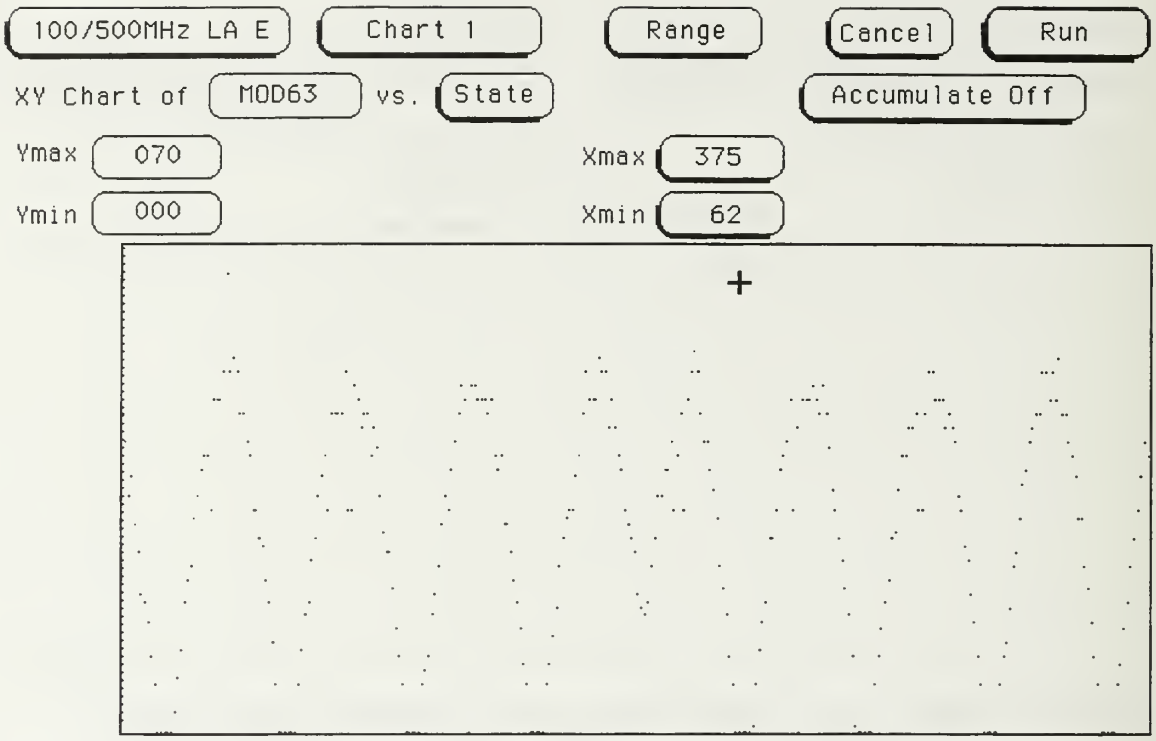

Figure (37): Digital output of Mod 63 channel for triangle wave antenna input

Figure (38) illustrates the digital output code of the Mod 63 channel comparator bank for a 5 kHz analog sinusoidal antenna input. This figure shows a non-linear output in accordance with equation (3). Phase crossovers are apparent on the left and right side of the figure.

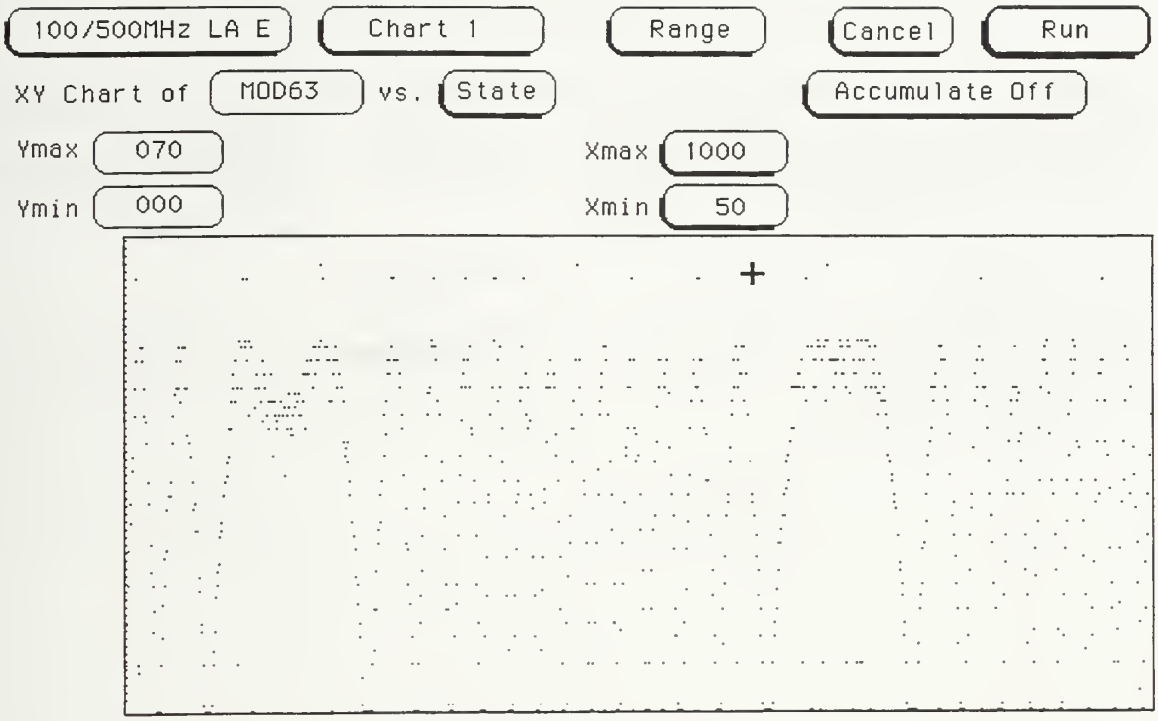

Figure (38): Digital code output of Mod 63 channel for sinusoidal antenna input

C. MOD 64 CHANNEL

Figure (39) illustrates the digital output for a 5 kHz triangle wave antenna input. A sinusoidal output in accordance with the transfer function of the interferometer for a linear input voltage is observed.

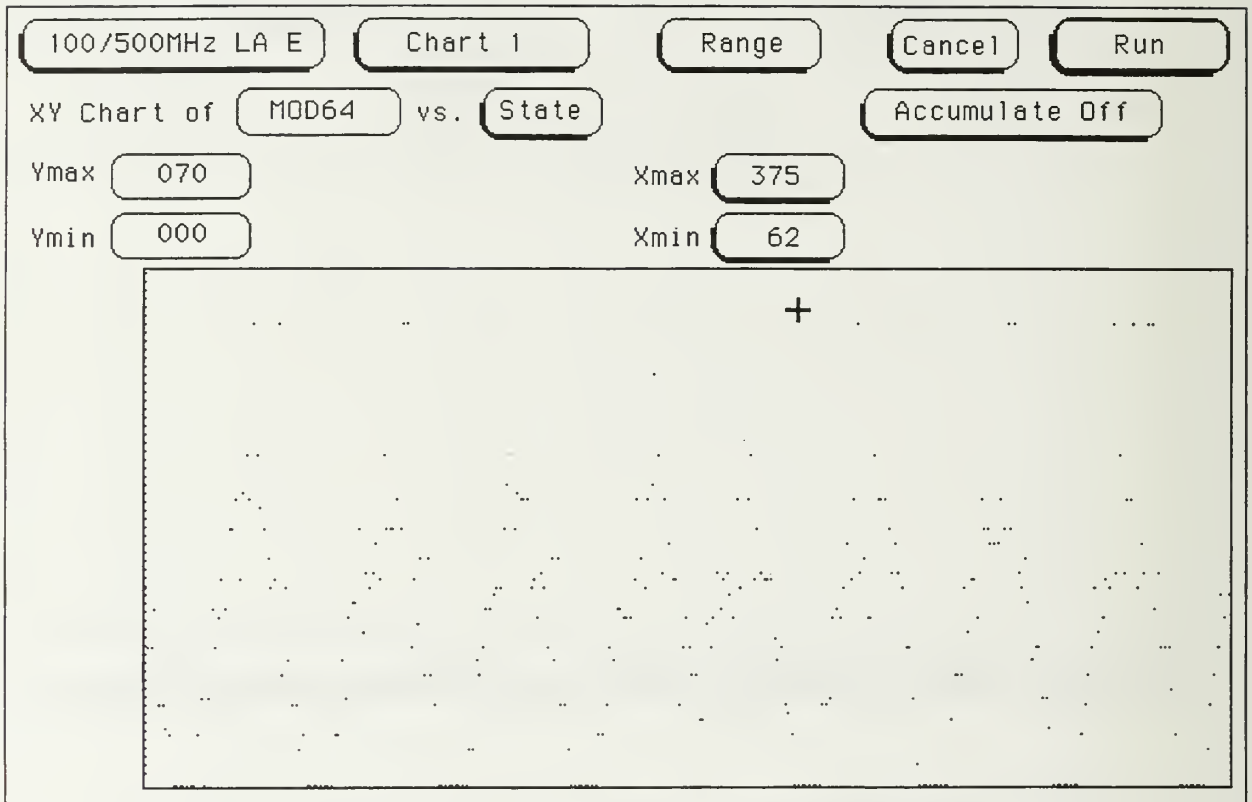

Figure (39): Digital output of Mod 64 channel for a triangle wave antenna input

Figure (40) illustrates the digital output code of the Mod 64 comparator bank for a 5 kHz analog sinusoidal antenna input. The figure shows a non-linear output in accordance with the transfer function of the interferometer given in equation (3).

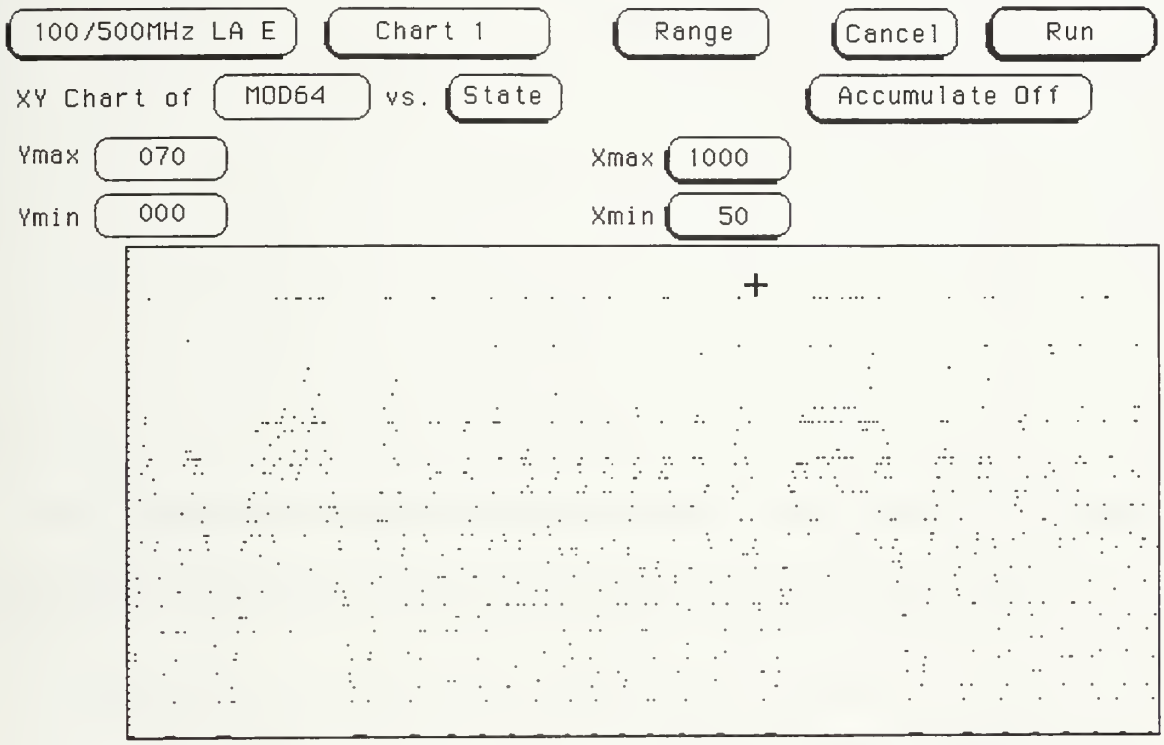

Figure (40): Digital output of Mod 64 channel for sinusoidal antenna input

D. MOD 65 CHANNEL

Figure (41) illustrates the output of the Mod 65 comparator bank for a linear ramped antenna input voltage. Again, a sinusoidal output is observed in accordance with equation (3).

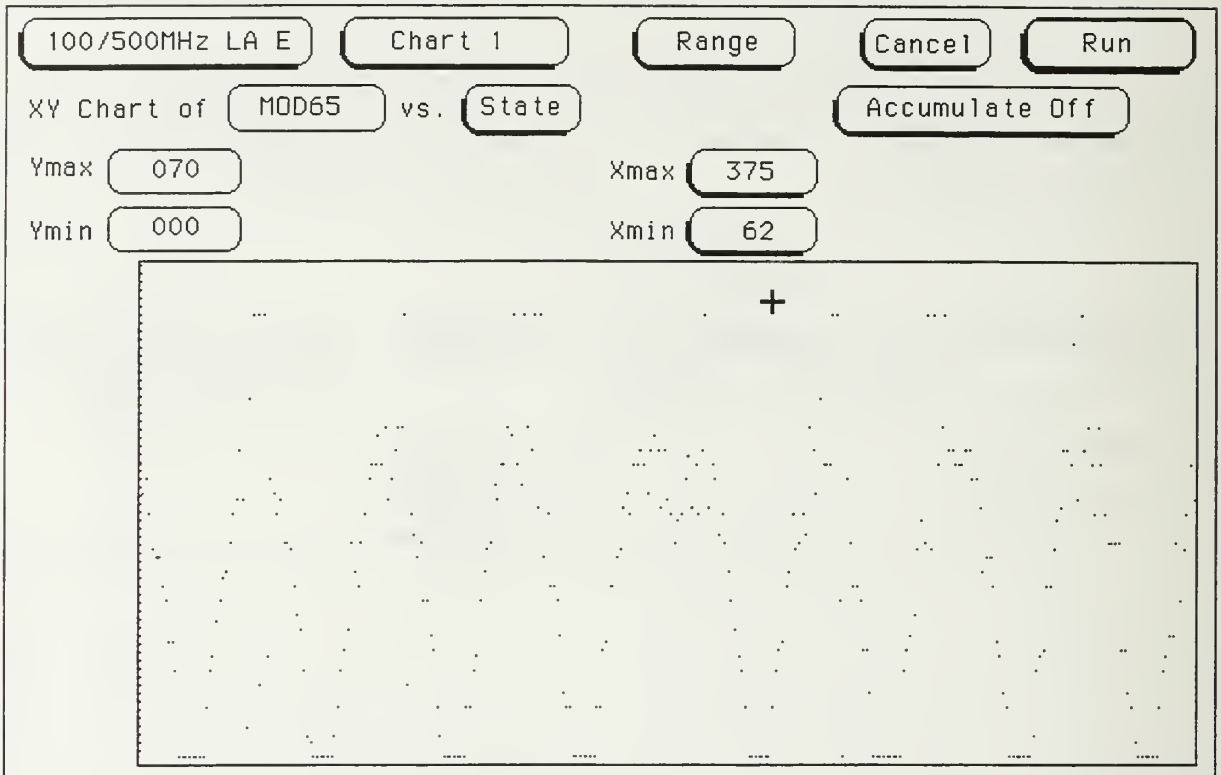

Figure (41): Digital output of Mod 65 channel for a triangle wave antenna input

Figure (42) illustrates the digital output code for a 5 kHz sinusoidal antenna input. A non-linear output is observed.

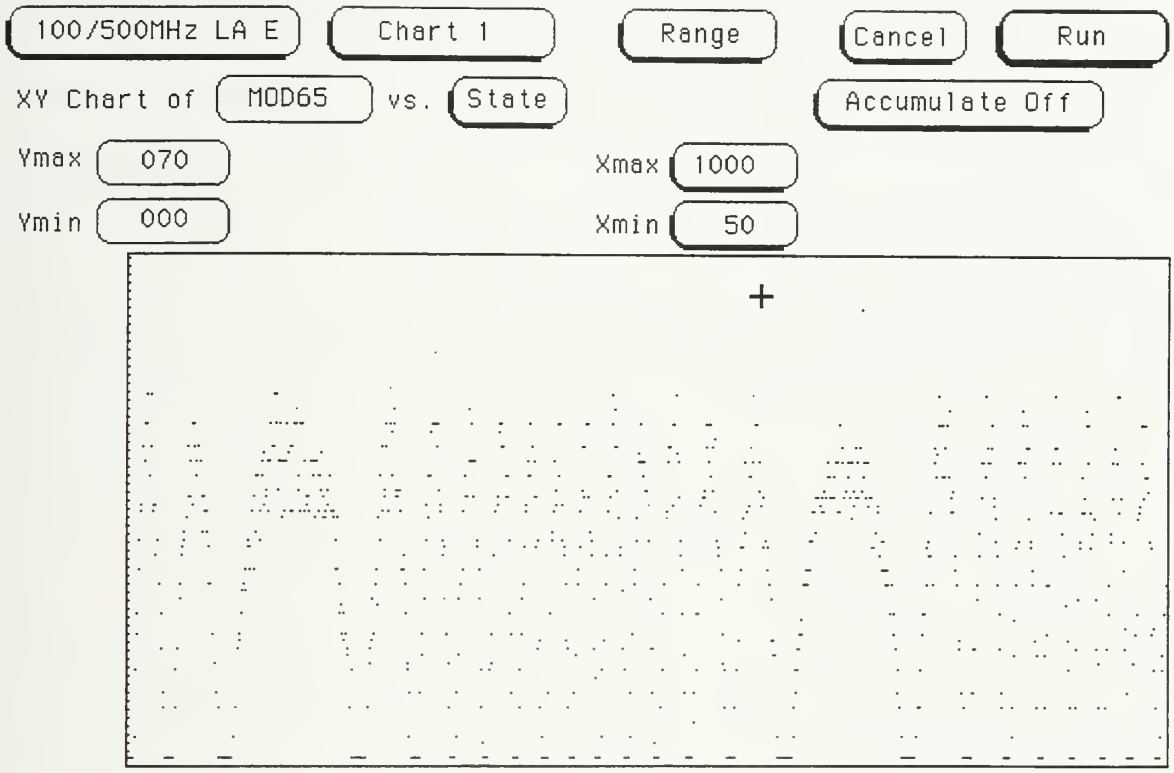

Figure (42): Digital output of Mod 65 channel for a sinusoidal antenna input

This chapter illustrated the digital output code of the comparator banks for all four channels. Further digital signal processing is carried out in a follow-on thesis [Ref. 2]. The next chapter summarizes the results and looks forward to needed improvements for follow-on work.

V. CONCLUSIONS

The test results clearly demonstrate the proof of concept for the parallel opto-electronic sampling front end. Signal integrity was maintained throughout the circuit.

A. OPTICS PACKAGE

With a 5 kHz test signal applied, the output of the parallel interferometers were within 4.5 % of the theoretical values. The signal was distorted somewhat due to probable constructive/destructive interference introduced within the interferometer and/or circulators within the optical circuit. This noise proved to be significant and had a clear, negative impact on the bit accuracy of the analog-to-digital conversion process. This amount of noise is even more acute, given the inherent non-linearity of the optimum Symmetrical Number System. For example, if the sampled result is displaced one least significant bit (which for this case is 5.07 mV) due to noise, the SNS output will *not* be displaced one integer away from its target value. In fact, the SNS output could fall anywhere between zero and 2^{14} (16,384) different integers, depending on the values of the other two moduli. To improve the performance of the optical circuitry the following is recommended:

1. Use a mode-locked laser. A mode-locked laser will produce a pulse train to ensure that the laser sampling is precise and stable. In order to achieve 14-bit accuracy, precise sampling with low jitter will keep output bit errors to a minimum.

2. Use polarization preserving fiber and components between the laser and the MZIs. Considerable signal loss can be realized due to phase mismatch within the fiber and connectors. Although expensive, this will maintain optical signal integrity

throughout the circuit and spare the tedious process of having to polarization align the fiber and connectors by hand twisting until the maximum output is observed, and then securing the components to the terminal board.

3. Eliminate the interference. This can be accomplished by using a two-port interferometer, which will also eliminate the need for the optical circulators, which are another possible source of interference. In a two-port interferometer, the sampling pulse enters the interferometer, passes over the electrode one time, and then exits the interferometer for decoding. This configuration minimizes interference because there will be no interaction between consecutive sampling pulses within the interferometer or circulator. Optical signal flow will be straightforward and simple. Also, in the present reflective configuration, the effect on signal integrity of having to pass the pulse twice over the electrode have yet to be determined.

4. Use an encoding scheme that can accommodate noise and irregularities. The optimum Symmetrical Number System encoding scheme is ingenious in theory, but is intolerant of bit errors. A new encoding scheme should be applied with qualities similar to a Gray code, where one bit error will not render the data point unusable.

B. ANALOG ELECTRONICS PACKAGE

The analog electronics circuitry detected and amplified the output optical pulses from the interferometer and properly preprocessed the signal so that the output waveforms are folding between +1 and +3 volts. The DC bias network properly adjusted the phasing of the analog inputs in accordance with the SNS. The passive attenuation network correctly gave the proper moduli ratios for each channel. The

ODECL adjustable trigger circuit delay circuit proved to be a challenge, however. The construction of this prototype circuit had many cold solder joints which caused floating ground problems, and led to many hours of troubleshooting and repair in order to get the circuit to function properly. Also, the lack of a voltage regulator for the board made the circuit very sensitive to minor voltage changes from the bench top power supplies, which are required to produce an impressive 2.8 amperes of current to power the circuit. It is recommended that a printed circuit board version of the circuit be fabricated in order to eliminate the floating grounds and the sensitivity to voltage fluctuations which cause false triggering of the outputs.

LIST OF REFERENCES

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2. Ringer W.P., "Design, construction, and analysis of the digital processor on a 3-channel, 14-bit optimum SNS wideband antenna for shipboard DF applications," Master's Thesis, Naval Postgraduate School, Monterey CA, September 1997.

3. Taylor, H.F., "An optical analog to digital converter - design and analysis," *IEEE Journal of Quantum Electronics*, vol. QE-15, no. 4, pp. 210-216, April 1979.

4. Pace, P.E., Styer D., "High resolution encoding process for an integrated optical analog-to-digital converter," *Optical Engineering,* vol.33, no.8, pp. 2638-2645, August 1994.

5. Patterson, R.H., "Input termination network for a high resolution integrated optical analog to digital converter," NRaD Engineering report, San Diego CA, October 1995.

6. Pietruszewski, A.P., "A programmable offset differential ECL four channel clock generator for applications in high resolution digital antennas," Master's Thesis, Naval Postgraduate School, Monterey CA, September 1996.

7. Van de Plassche, R., "Integrated analog-to-digital and digital-to-analog converters," Philips Research Laboratories, The Netherlands, 1994.

APPENDIX

The following pages include manufacturer specification data sheets for the following subsystems:

1. United Technologies Photonics Mach-Zehnder Interferometers

United Technologies Photonics

Final Test Data Sheet

Customer Name:	Naval Postgraduate School
Purchase Order Number:	N62271-95-M-0605 P94-067-4
Item Number:	1
Count:	1 of 3
Catalog Number:	Low-Vpi 1320-nm Interferometer
Description:	1.3-nm Interferometer
Job Number	733
Serial Number:	1144
Date Code:	9503
Sliver ID Number:	1916-1-C
Input Fiber Type:	Fujikura SM-13-P-7/125-UV/UV-400

Optical Performance Parameters

Insertion Loss:	8.83 dB
On/Off Extinction:	22.9 dB
RF Electrode Half-wave Voltage:	.32 V
Test Wavelength:	1319-nm
Source Type:	1-line YAG

United Technologies Photonics

Final Test Data Sheet

Customer Name:	Naval Postgraduate School
Purchase Order Number:	N62271-95-M-0605 P94-067-4
Item Number:	1
Count:	2 of 3
Catalog Number:	Low-Vpi 1320-nm Interferometer
Description:	1.3-nm Interferometer
Job Number	733
Serial Number:	1142
Date Code:	9503
Sliver ID Number:	1916-1-E
Input Fiber Type:	Fujikura SM-13-P-7/125-UV/UV-400

Optical Performance Parameters

Insertion Loss:	9.57 dB
On/Off Extinction:	26.1 dB
RF Electrode Half-wave Voltage:	.32 V
Test Wavelength:	1319-nm
Source Type:	1-line YAG

3. BCP Model 300 Series Optical Waveform Receiver, Electro-optical converter/amplifier

1.0 INTRODUCTION

1.1 General Description

The Model 300 Optical Waveform Receiver is designed for detection and analysis of high speed optical waveforms. DC-coupled avalanche detectors are used for optical-to-electrical conversion, covering all of the wavelengths in common use for optical communications (500 to 1550 nm).

Detector gains are adjustable via a front panel precision locking potentiometer, which controls an internal high voltage regulated power supply. Most standard fiber optic connectors are available as interface options. A removable sub-panel is used for mounting one or two detector/connector units, enabling easy substitution of different detection devices or different connector interfaces without the expense of several separate instruments.

The Model 300 also includes a 26 dB AC-coupled amplifier, with both input and output ports accessible from the front panel. Detector outputs may be routed through the amplifier for detection sensitivity enhancement, or the amplifier may be used independently as a general purpose gain block. An internal AC power supply provides the necessary operating voltages.

3.1 Block Diagram Description

The block diagram of the Model 300 is drawn in figure 3.1. Two AC/DC power supplies are required. The low voltage (+15V) supply powers all internal circuitry, while the high voltage supply (400V) generates the voltage required for avalanche photodetector (APD) biasing. The high voltage is processed by a precision HV regulator, which is controlled by the front panel vernier gain adjust potentiometer. The maximum output from this regulator is determined by limit set #1, which sets the maximum voltage supplied to the first photodetector. This is usually the short wavelength APD. This regulated voltage is further scaled down by limit set #2, which supplies the bias voltage to detector #2 (usually the long wavelength APD). These two limit adjustments are set such that at maximum gain (front panel vernier fully clockwise), each APD is just on the verge of breakdown, and thus exhibits the maximum possible ionization current gain. The HV regulator is also thermally compensated to approximate the voltage shift with temperature required for fixed short wavelength detector gain.

The photodetectors are source terminated into 50 ohm loads for increased waveform fidelity. Thus the resistive load seen by both detectors when the user also supplies a 50 ohm termination is 25 ohms. Both photodetector outputs are DC-coupled to the front panel.

3.2 Short Wavelength Photodetector

The short wavelength APD is a silicon device, typically receptacle-mounted at the front panel with no internal fiber pigtail. Figure 3.2.a illustrates the APD-only sensitivity vs. wavelength characteristic when biased for a current gain near the maximum.

Figure 3.2.b illustrates the minimum guaranteed, front-panel delivered, volts-per-watt short wavelength detector sensitivity curve vs. incident optical power. The sensitivity obviously declines with increasing optical power, which is an intentional design feature. If the detector sensitivity was maintained at 2500 V/W for very high input optical power levels the APD would be damaged. For instance, with 100 microwatts of average input optical power, the APD photocurrent would be on the order of 10 mA. At 200V typical bias, the APD would dissipate 2 watts and self-destruct. Thus, the user must be aware that the detector output signal amplitude is not linearly proportional to the <u>average</u> input, optical power, but is indeed highly linear and accurately reproduces individual pulses or high frequency modulation. The detector gain should be

Digital Input-Electrical

Bit Rate	0 to 1.0 Gb/s (min.)	Typically 1.3 Gb/s or higher
Pulse Pattern	No constraint	All zeroes, all ones, or any combination
Logic Levels	Any standard ECL	10K, 10KH, 100K, Si or GaAs ASIC
Logic Threshold	-1.3, ±.2V	Front panel adjustable
Termination	50 ohms to -2V	Single-ended input

Digital Output-Optical (Note 1)

Pulse Rise/Fall Times	0.5 nsec (max.)			10-90%, typ. 0.3 nsec
Maximum Pulse Width	No Limit			DC Coupled
Minimum Pulse Width	0.75 ns			FWHM, max
Extinction Ratio	10:1 (min.)			Back-panel adjustable (UNCAL mode)
	Options 01-05	Options 11-15	Options 21-25	
Pulse Overshoot	30%	30%	30%	Maximum (Note 3)
Peak Coupled Pwr. (fiber)	1.0 mw (50/125)	1.0 mw (50/125)	0.75 mw (8/125)	Minimum
Wavelength	780 nm (±15 nm)	850 nm (±50nm)	1300 nm (±30nm)	Typical (actual is supplied with each unit) Contact factory for 1550 nm
Spectral Width	2 nm	1 nm	4 nm	FWHM, typ

Analog Input—Electrical

	Options 01-05	Options 11-15	Options 21-25	
Frequency	0.1-500 MHz	0.1-700 MHz	0.1-1000 MHz	Minimum
Input Level	1.0 vpp	1.0 vpp	1.0 vpp	Typ for 0.8 peak mod. index
	2.0 vpp	2.0 vpp	2.0 vpp	Max safe input
Input Impedance	50 ohms, AC coupled			

Analog Output—Optical (Note 1)

	Options 01-05	Options 11-15	Options 21-25	
Average Optical Pwr. (fiber)	0.5 mw	0.5 mw	0.4 mw	May be adjusted ± 10% via rear panel control (UNCAL mode)
Spectral Width	2 nm	1 nm	3 nm	FWHM typ
Frequency Response	0.1-500 MHz	0.1-700 MHz	0.1-1000 MHz	Min -3dB
Polarity	Inverting	Inverting	Inverting	

General

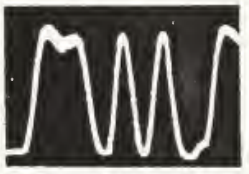
22 SN: 196

Options:

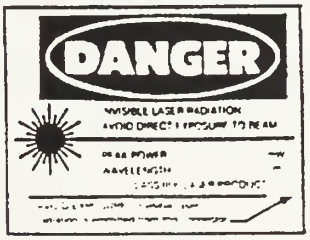
Model 400-XX

Wavelength	Optical Connector
0 - 780 nm	1 - SMA
1 - 850 nm	2 - ST
2 - 1300 nm	3 - FC
3 - 1550 nm	4 - Biconic
4 - 670 nm	5 - Special
5 - Special	

AC Power Control	Keyswitch
Analog/Digital Input Connectors	BNC Female
Power Requirements	120/240 VAC, 50-60 Hz
Temperature Range	
Operating	0° to 50° C
Storage	-30° to 70° C
Dimensions	9.25"W, 10.5"D, 2.75"H
Weight	3.8 pounds



Digital Optical Output at 1.2 Gb/s NRZ (Note 2)



Notes

1. Calibrated laser bias mode selected, 25° C
2. 1.2 Gb/s NRZ Laser output as viewed through a 750 MHz linear channel filter, 1 nsec/div.
3. When viewed through a 1.0 GHz low pass filter.

Specifications subject to change without notice

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