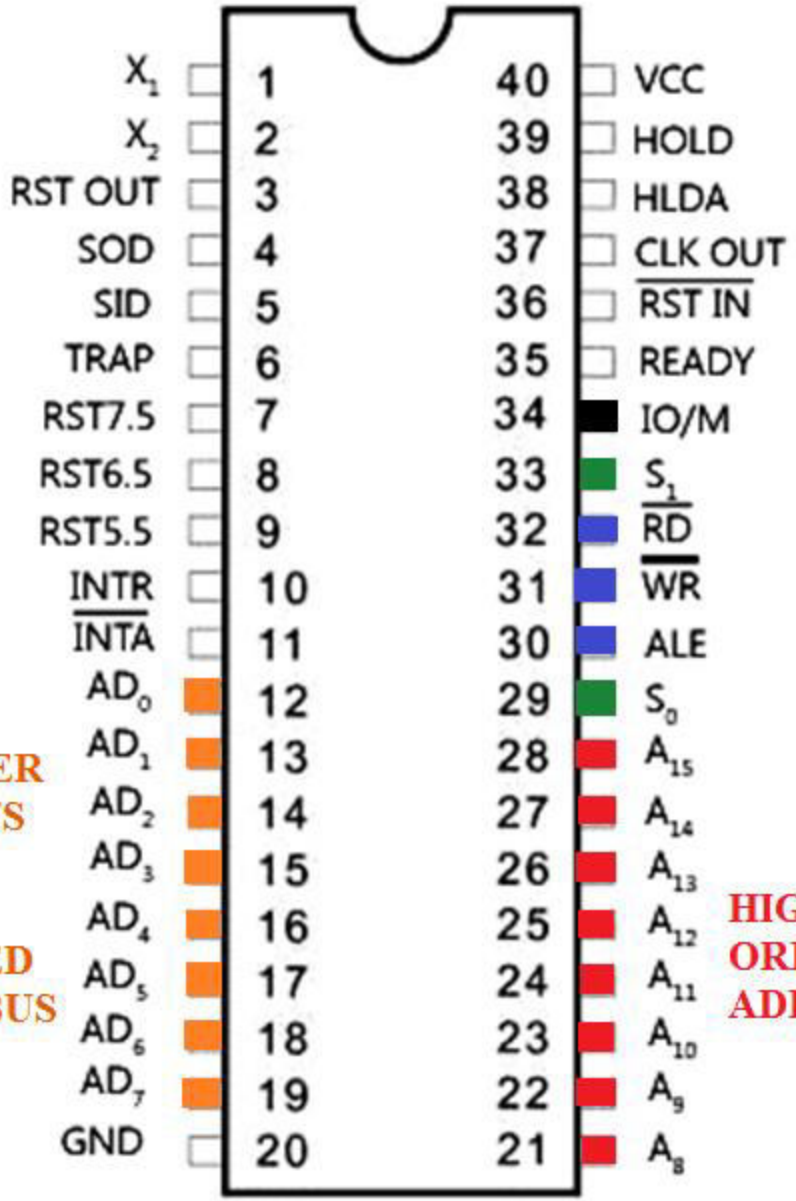
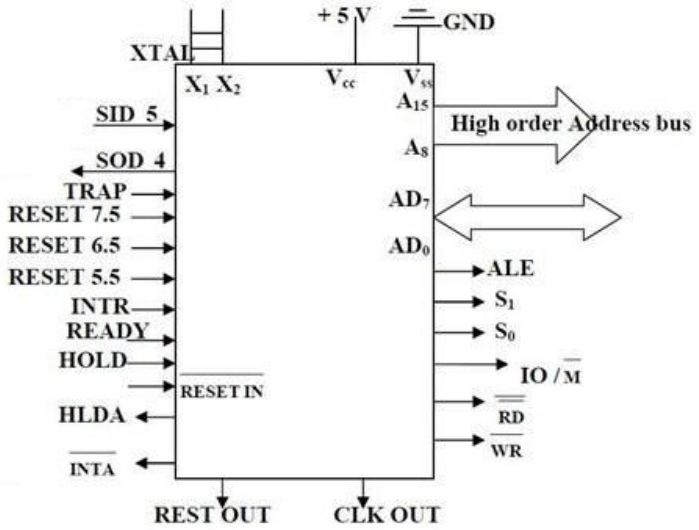
80856 PIN DIAGRAM



LOWER ORDER ADDRESS BITS

TIME MULTIPLEXED WITH DATA BUS

HIGHER ORDER ADDRESS BITS

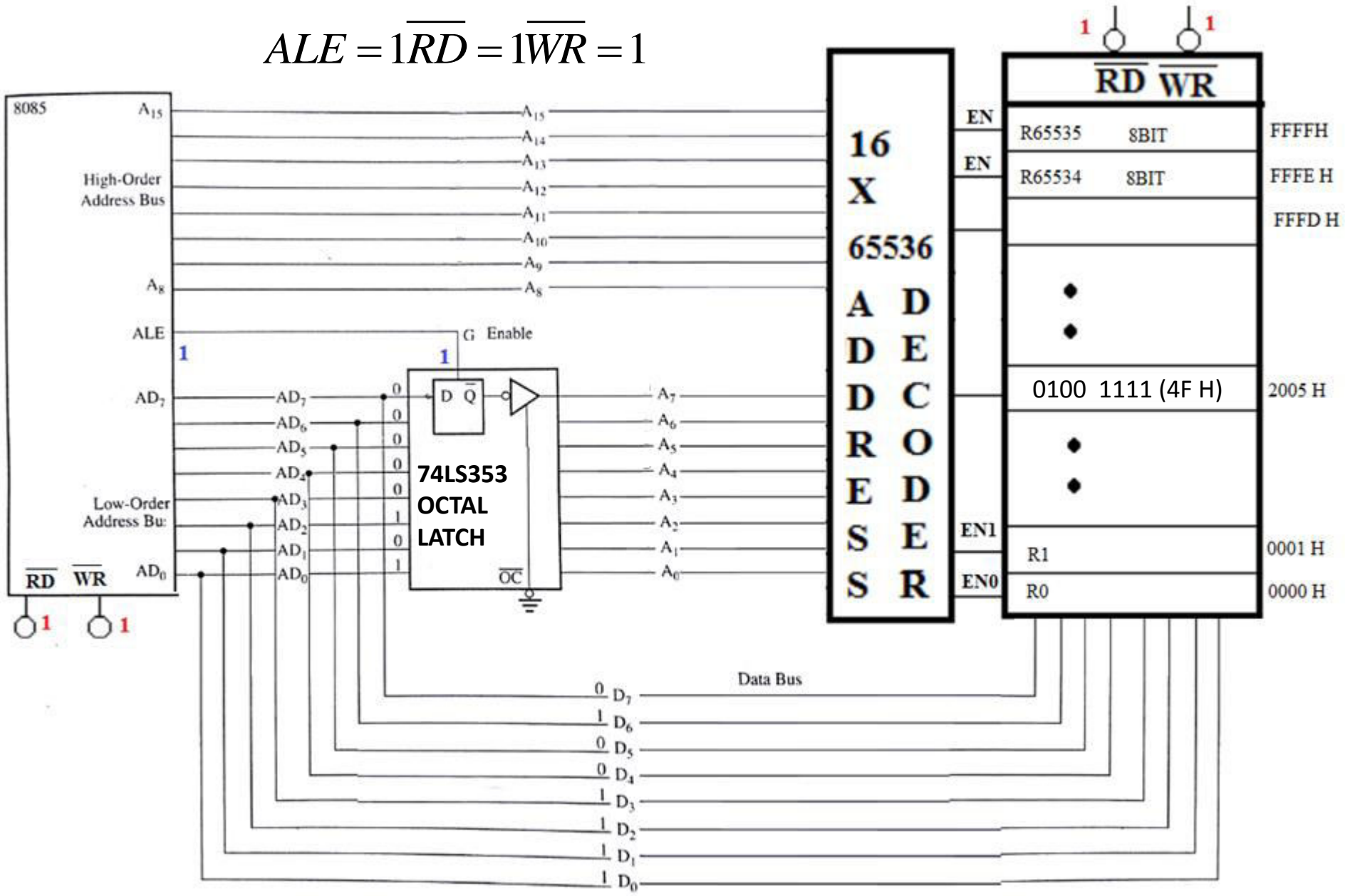


DEMULTIPLEXING THE BUS AD7- AD0

AD7 - AD0 to be used as ADDRESS BUS ALONG WITH A15-A8

Ignoring Chip Select signal

$$ALE = 1 \quad \overline{RD} = 1 \quad \overline{WR} = 1$$

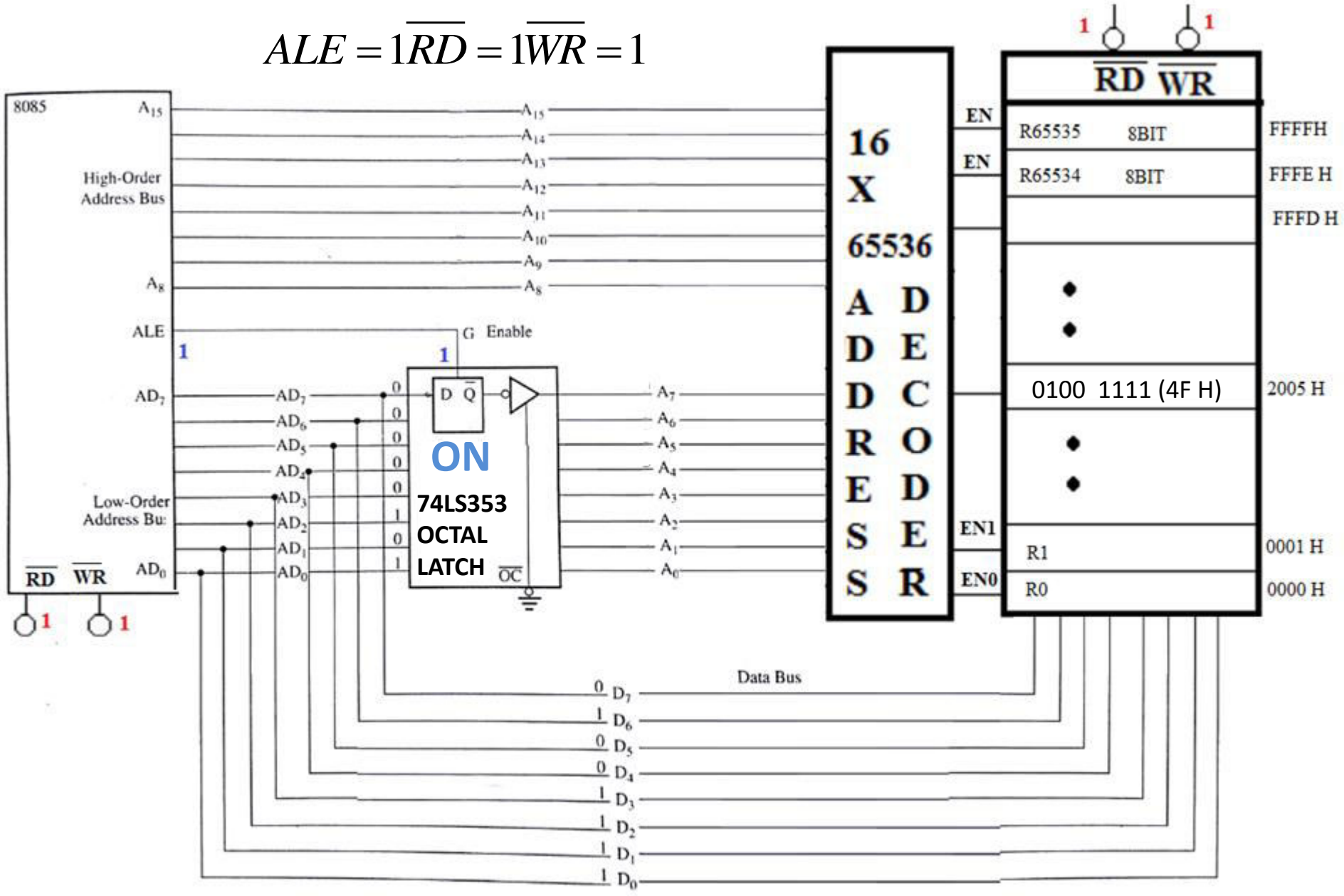


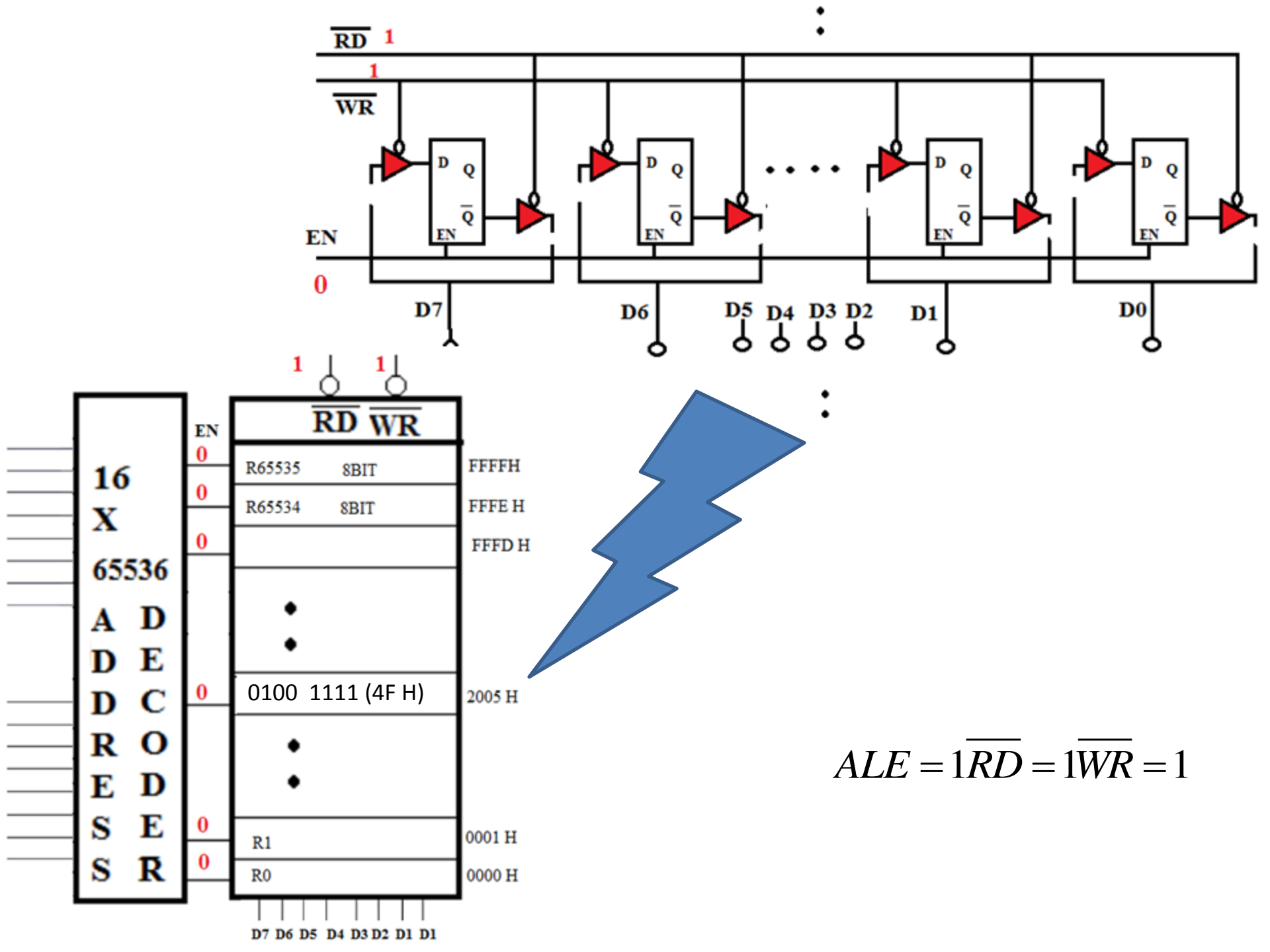
DEMULTIPLEXING THE BUS AD7- AD0

AD7 - AD0 to be used as ADDRESS BUS ALONG WITH A15-A8

Ignoring Chip Select signal

$$ALE = 1 \quad \overline{RD} = 1 \quad \overline{WR} = 1$$





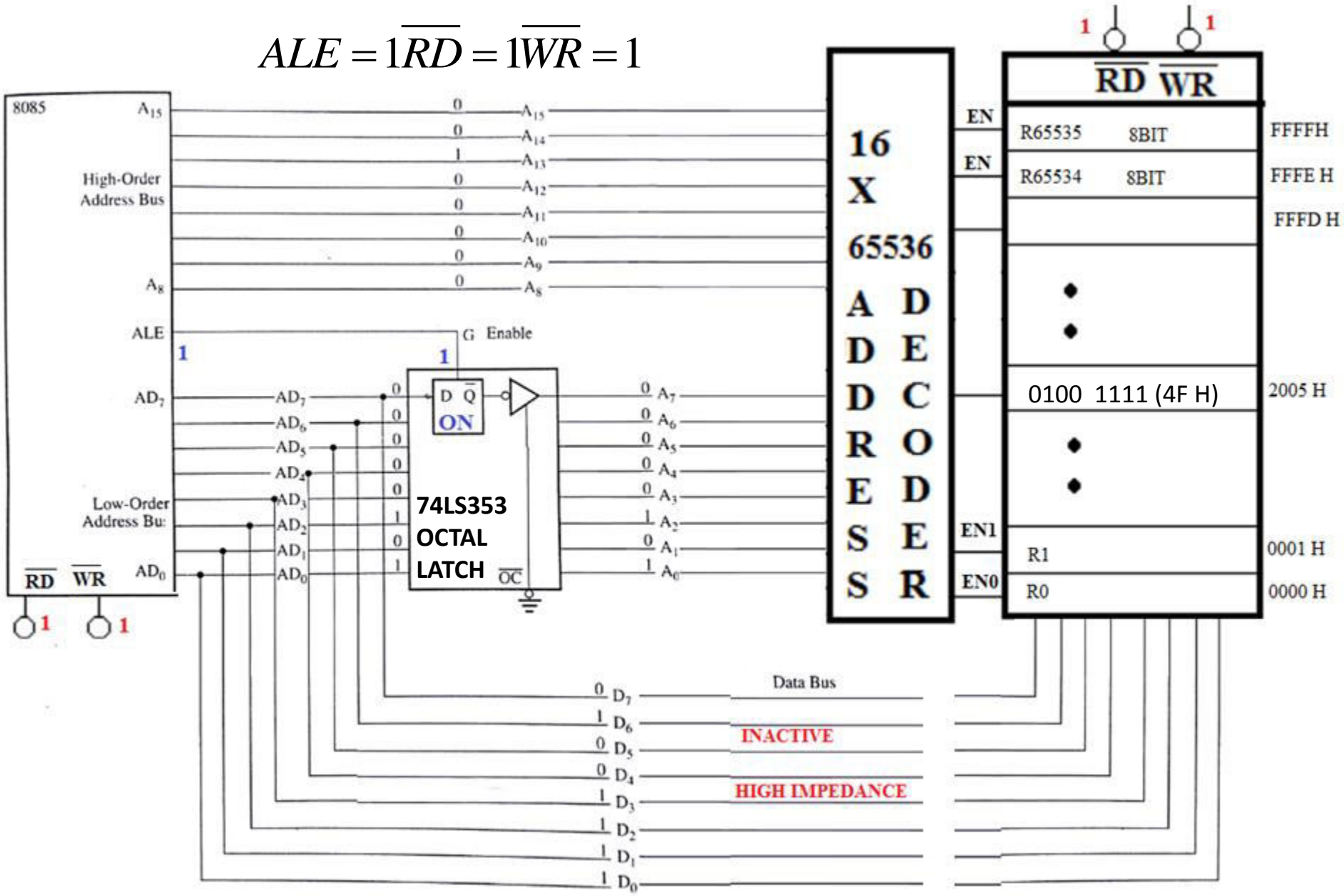
$$ALE = 1 \overline{RD} = 1 \overline{WR} = 1$$

DEMULTIPLEXING THE BUS AD7- AD0

AD7 - AD0 to be used as ADDRESS BUS ALONG WITH A15-A8

Ignoring Chip Select signal

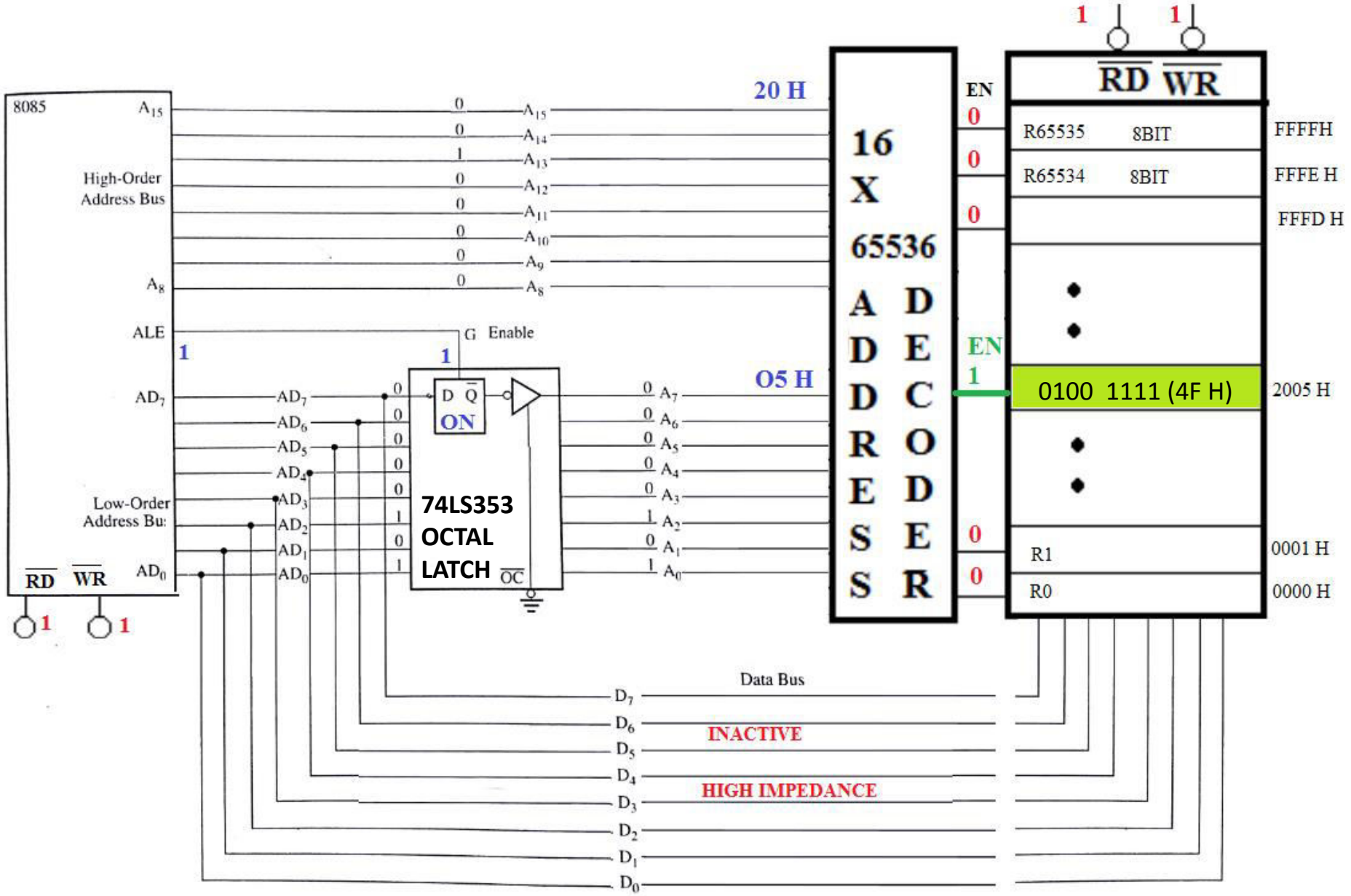
$$ALE = 1 \quad \overline{RD} = 1 \quad \overline{WR} = 1$$



DEMULTIPLEXING THE BUS AD7- AD0

µP Puts 2005 H address on Address BUS (A15-A0)

Ignoring Chip Select signal

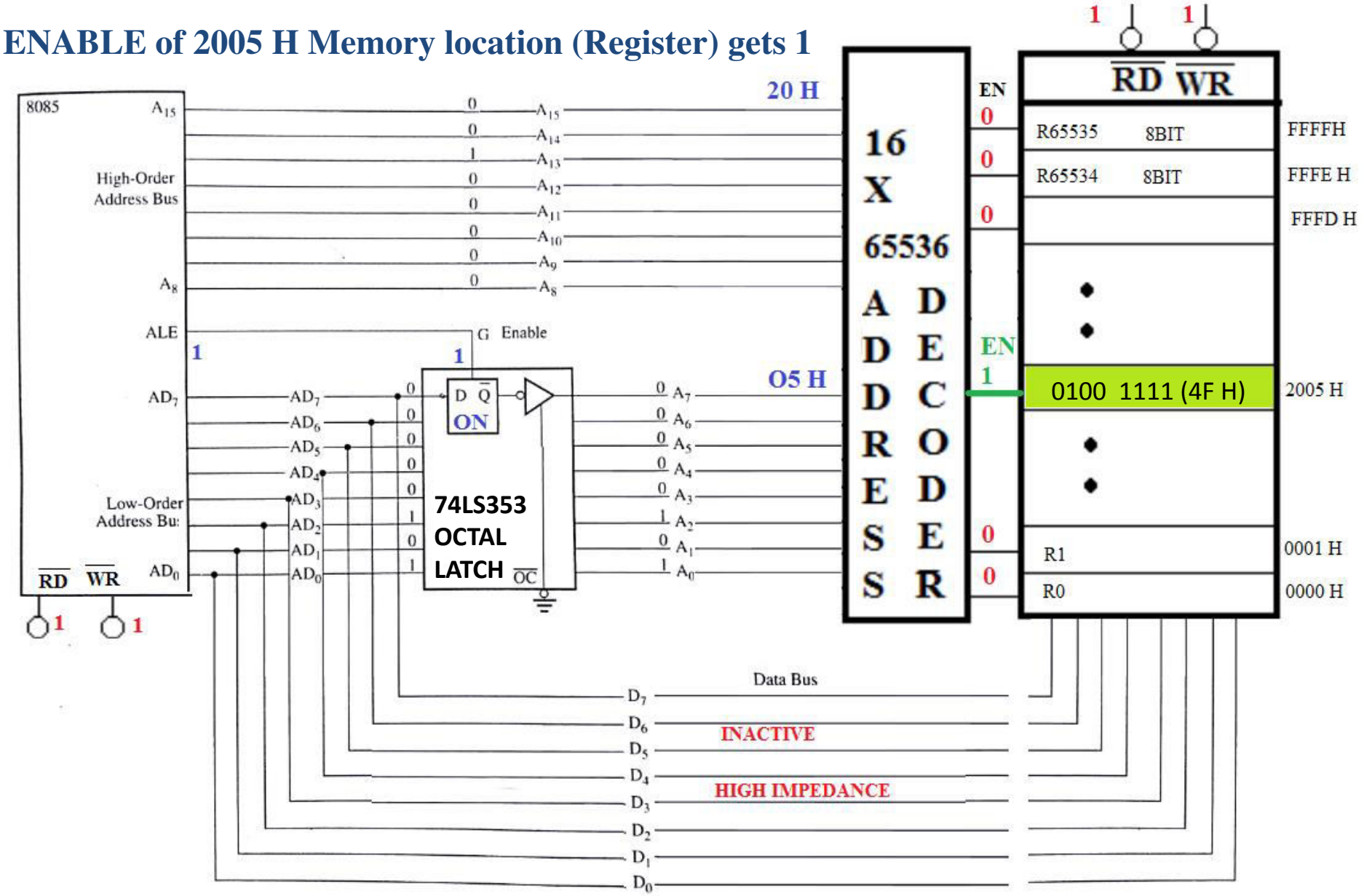


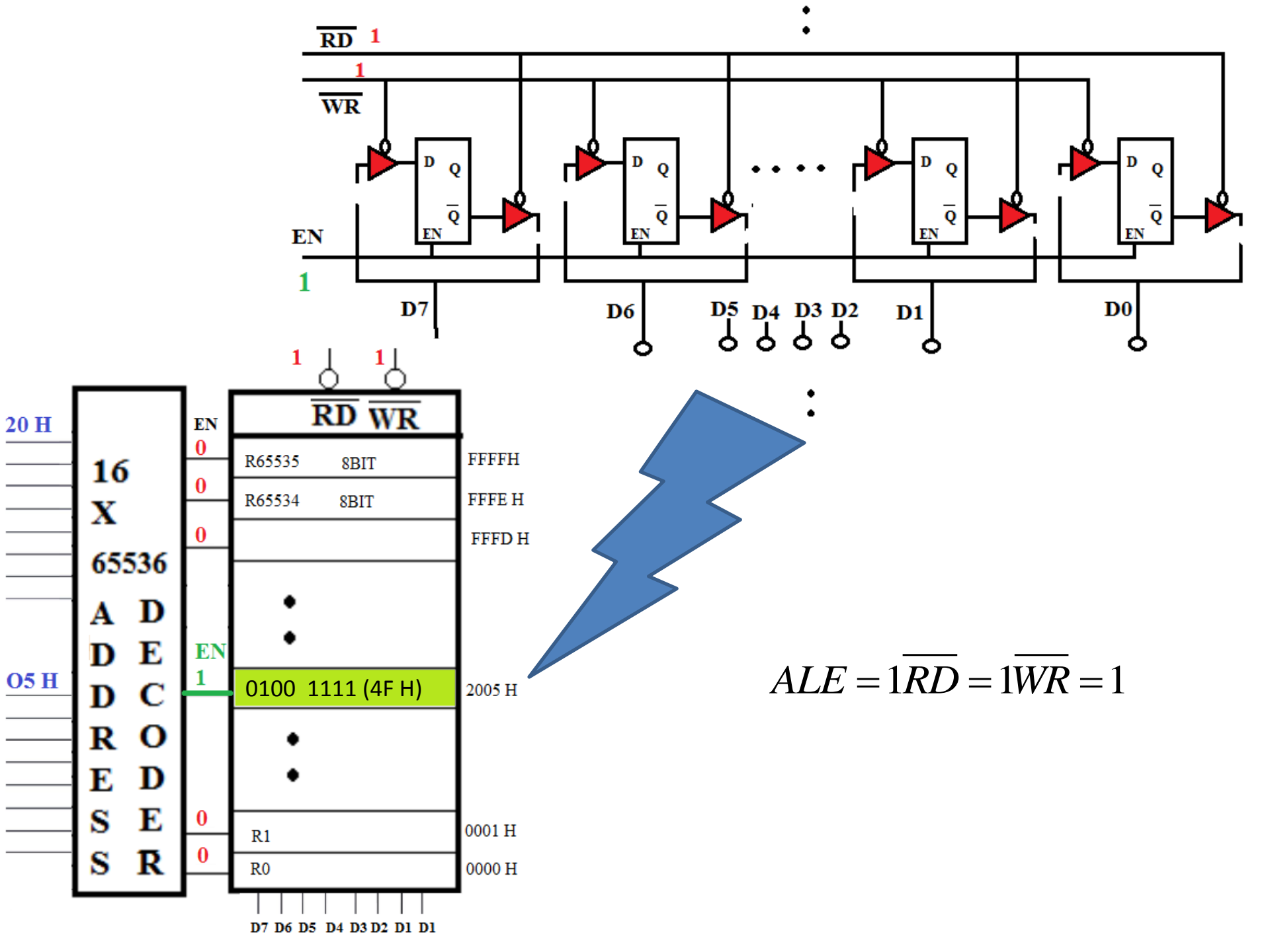
DEMULTIPLEXING THE BUS AD7- AD0

µP Puts 2005 H address on Address BUS (A15-A0)

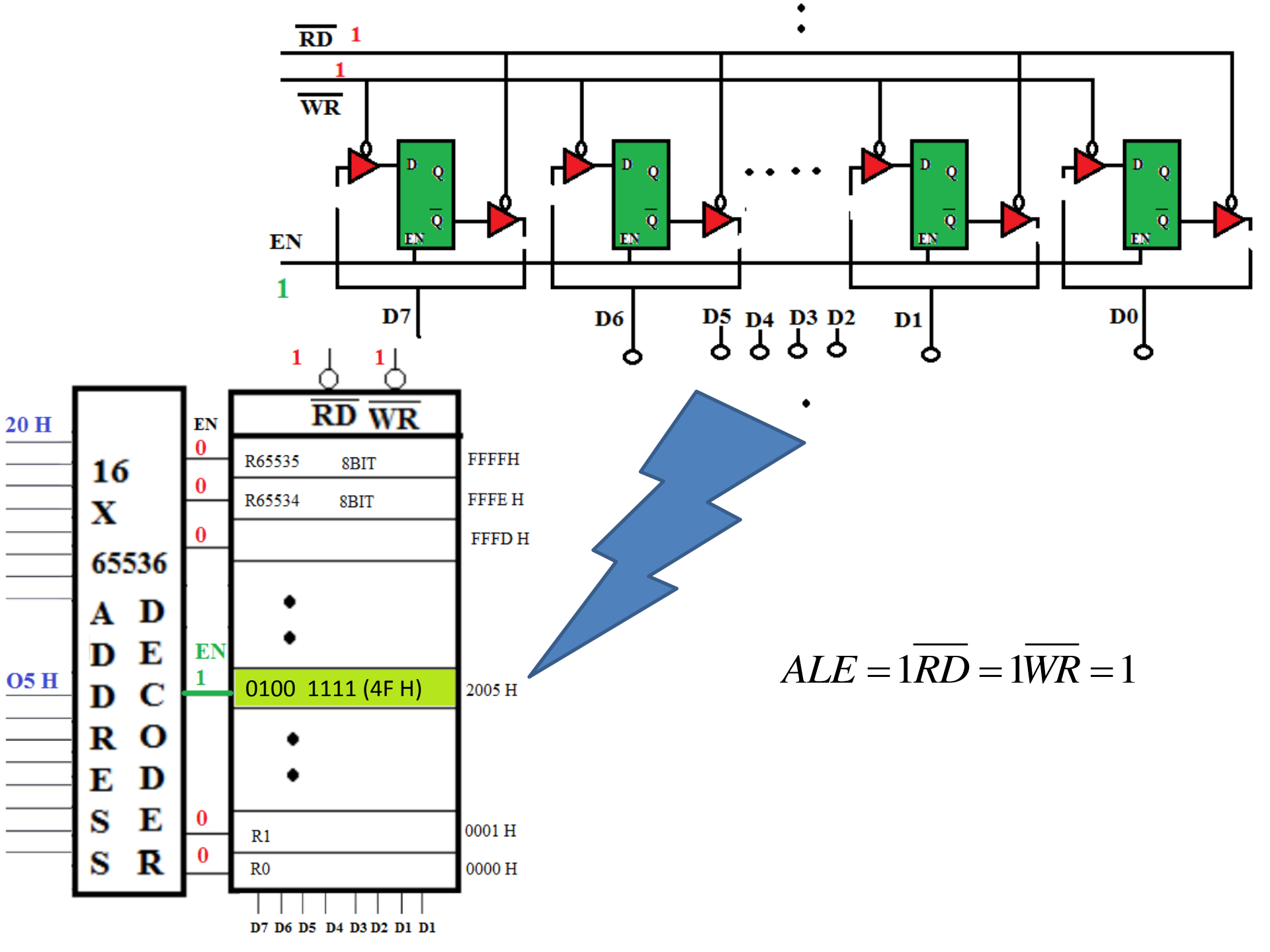
Ignoring Chip Select signal

ENABLE of 2005 H Memory location (Register) gets 1





$$ALE = 1 \overline{RD} = 1 \overline{WR} = 1$$



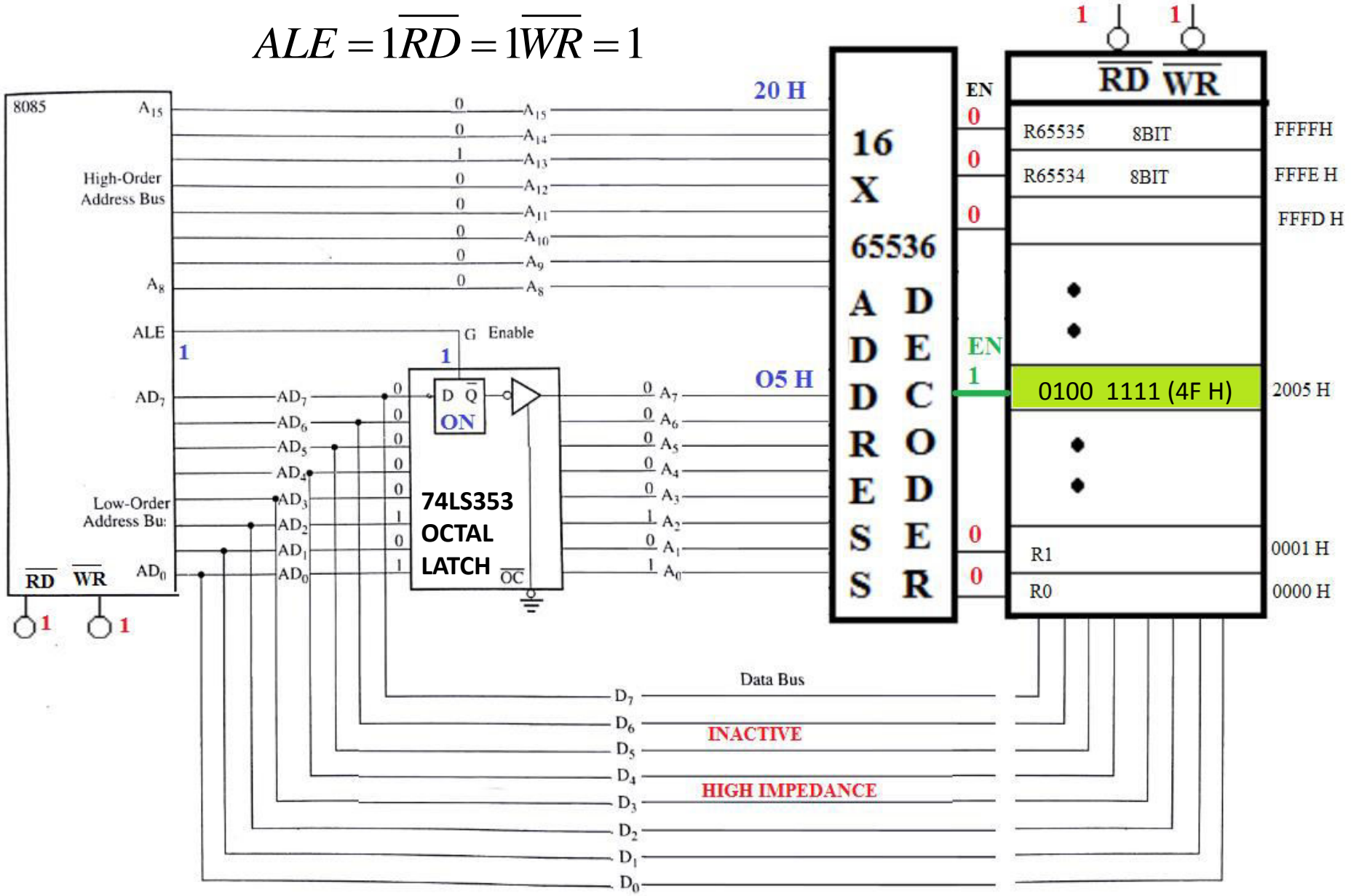
$$ALE = 1 \overline{RD} = 1 \overline{WR} = 1$$

DEMULTIPLEXING THE BUS AD7- AD0

AD7 - AD0 to be used as ADDRESS BUS ALONG WITH A15-A8

Ignoring Chip Select signal

$$ALE = 1 \quad \overline{RD} = 1 \quad \overline{WR} = 1$$

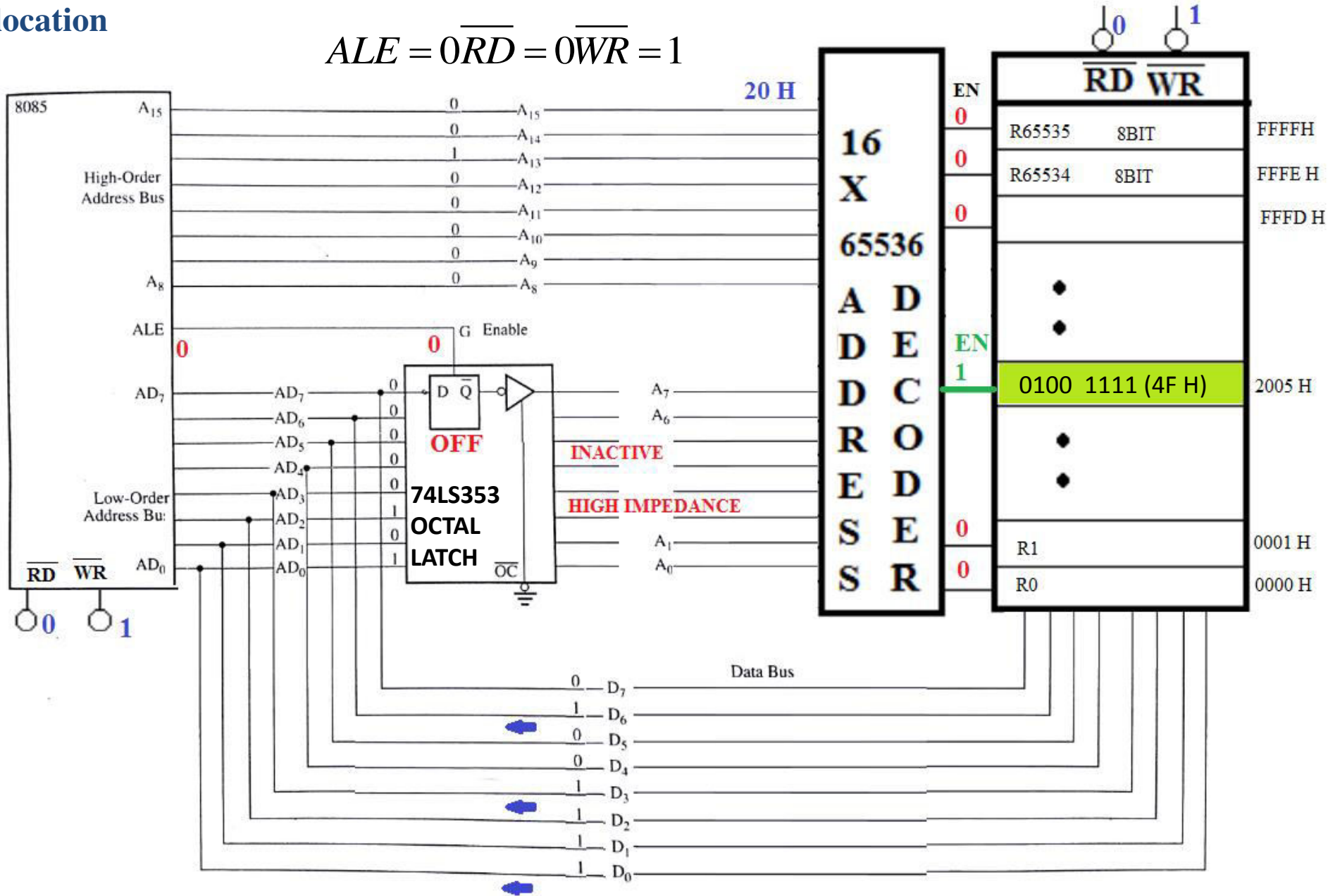


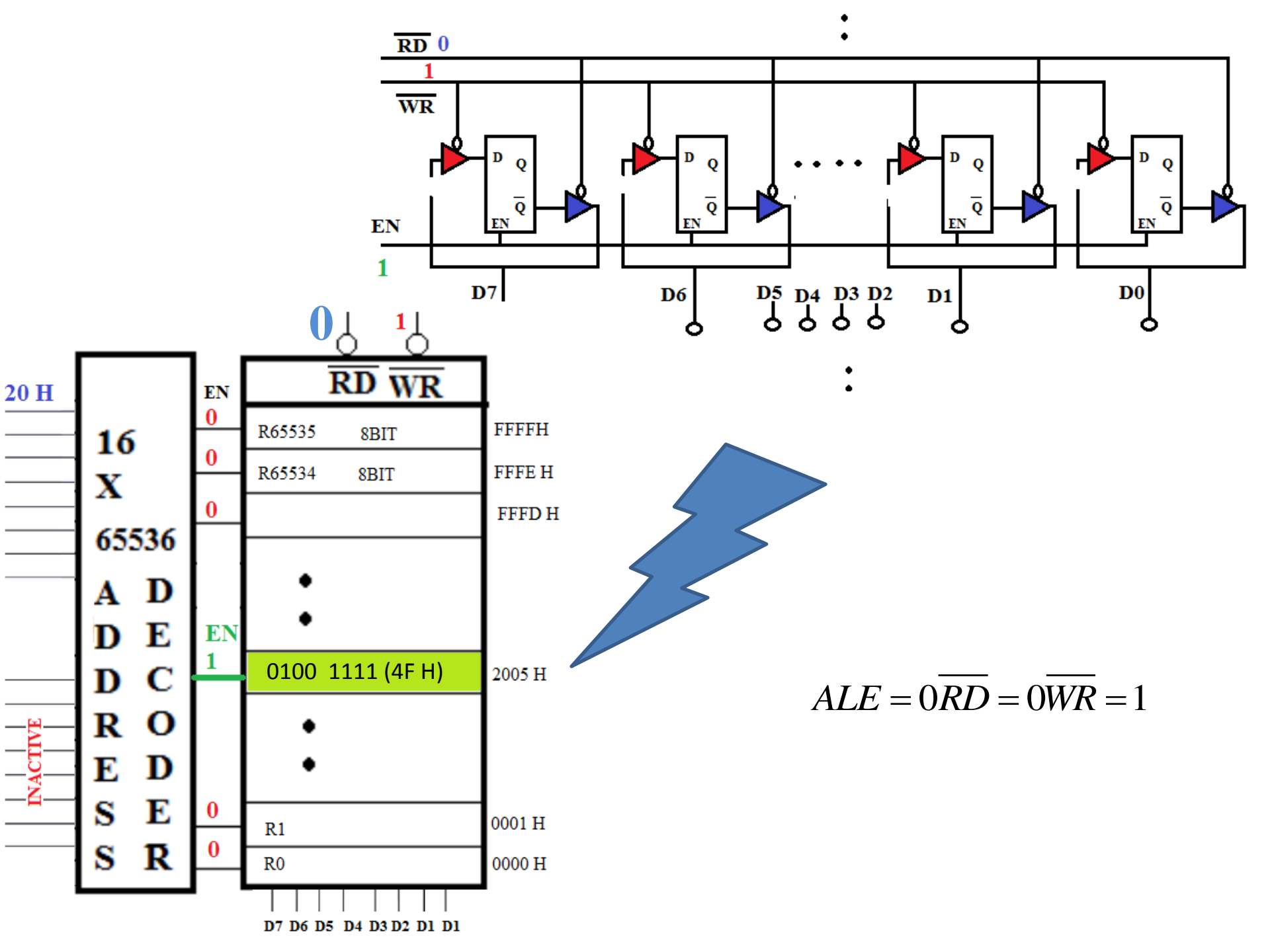
DEMULTIPLEXING THE BUS AD7- AD0

AD7 - AD0 to be used as DATA BUS to read content of 2005 H location

Ignoring Chip Select signal

$$ALE = 0 \quad \overline{RD} = 0 \quad \overline{WR} = 1$$





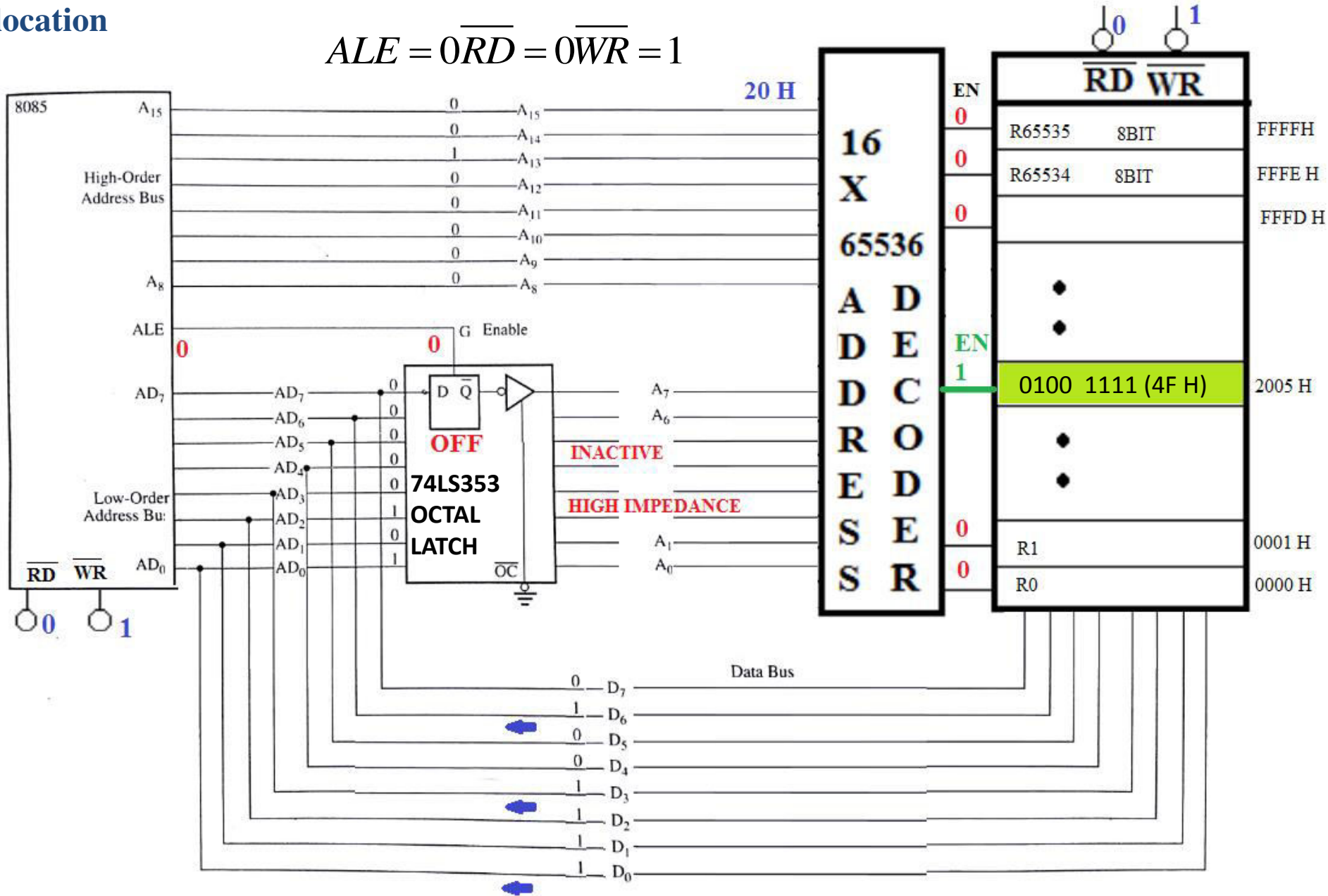
$$ALE = 0 \overline{RD} = 0 \overline{WR} = 1$$

DEMULTIPLEXING THE BUS AD7- AD0

AD7 - AD0 to be used as DATA BUS to read content of 2005 H location

Ignoring Chip Select signal

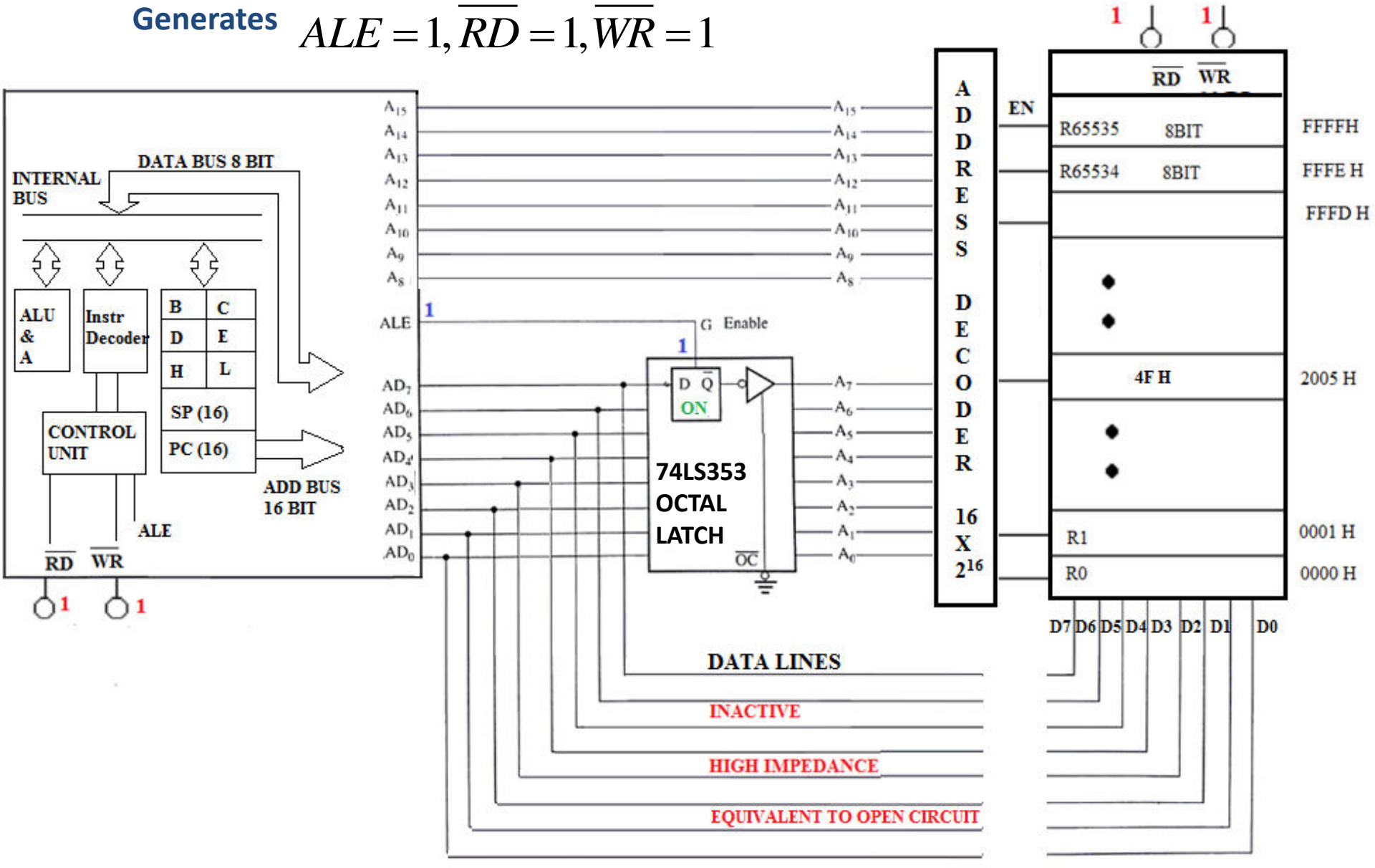
$$ALE = 0 \quad \overline{RD} = 0 \quad \overline{WR} = 1$$



MICROPROCESSOR COMMUNICATION & BUS TIMING
STEP-1 (FIRST CLOCK CYCLE)

Ignoring Chip Select signal

Microprocessor Control Unit
Generates $ALE = 1, \overline{RD} = 1, \overline{WR} = 1$

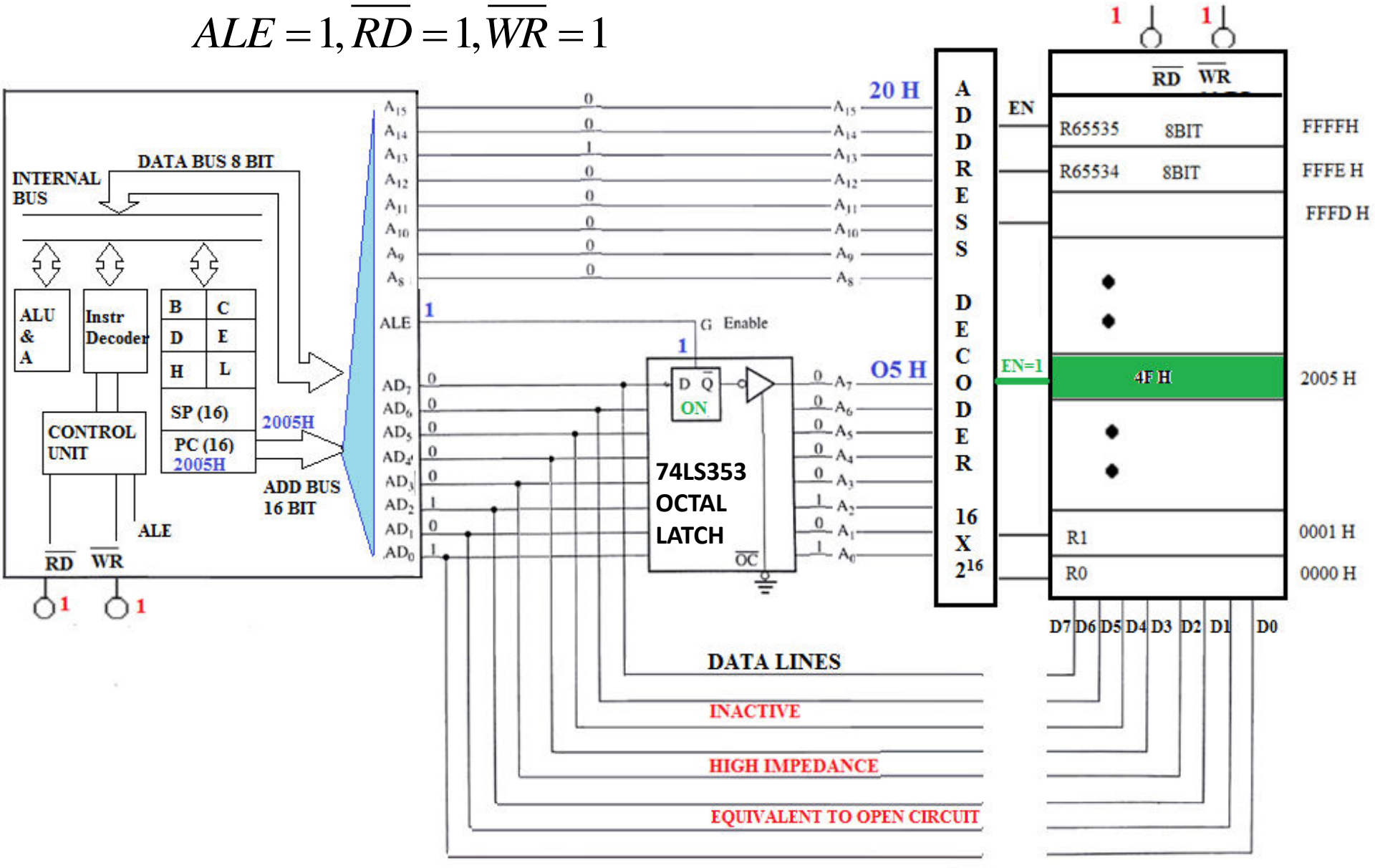


MICROPROCESSOR COMMUNICATION & BUS TIMING
STEP-1 (FIRST CLOCK CYCLE)

Ignoring Chip Select signal

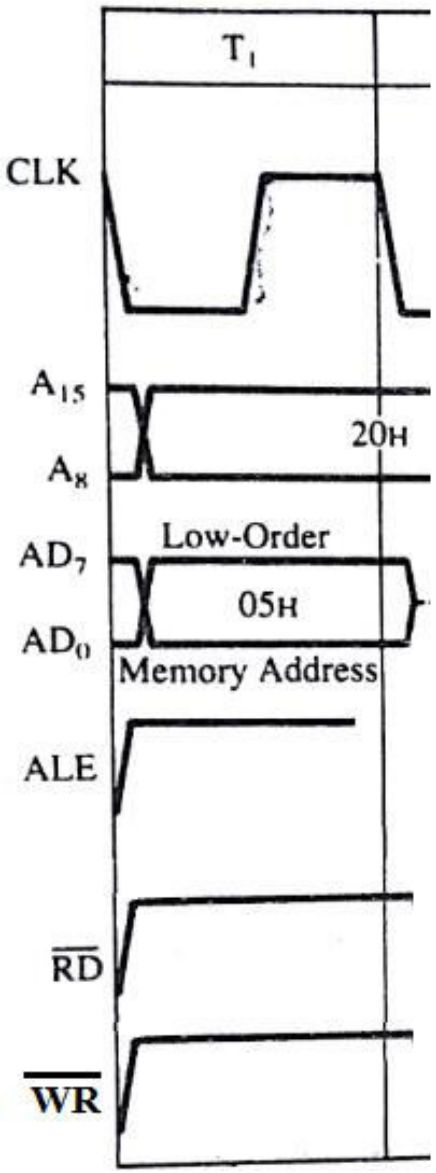
Microprocessor Places 2005 H Address on Address bus (A15 – A0)

$$ALE = 1, \overline{RD} = 1, \overline{WR} = 1$$



MICROPROCESSOR COMMUNICATION & BUS TIMING
STEP-1 (FIRST CLOCK CYCLE)

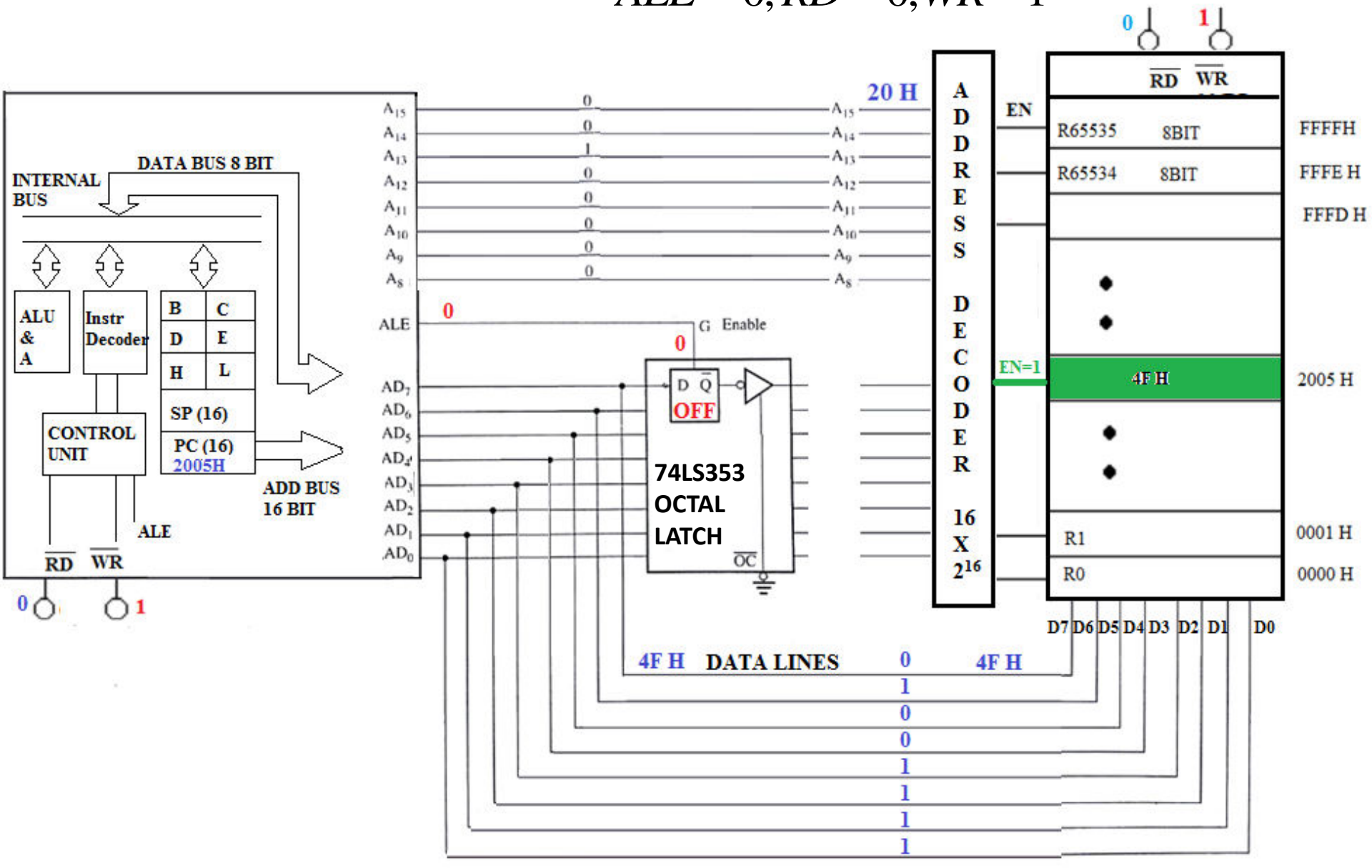
$$ALE = 1, \overline{RD} = 1, \overline{WR} = 1$$



MICROPROCESSOR COMMUNICATION & BUS TIMING
STEP-2 (SECOND CLOCK CYCLE)

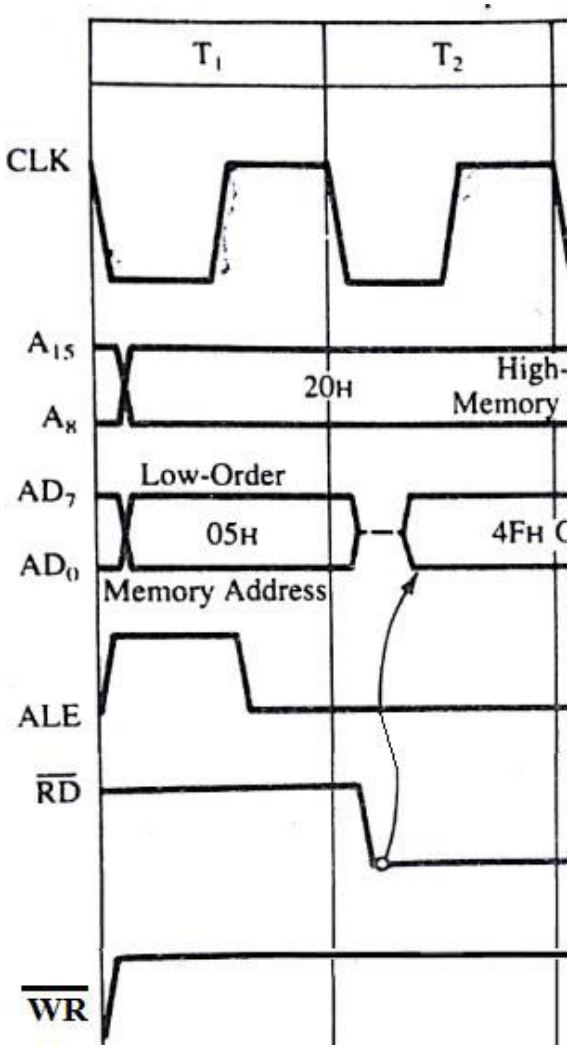
Ignoring Chip Select signal

Microprocessor Control Unit generates: $ALE = 0, \overline{RD} = 0, \overline{WR} = 1$



MICROPROCESSOR COMMUNICATION & BUS TIMING
STEP-2 (SECOND CLOCK CYCLE)

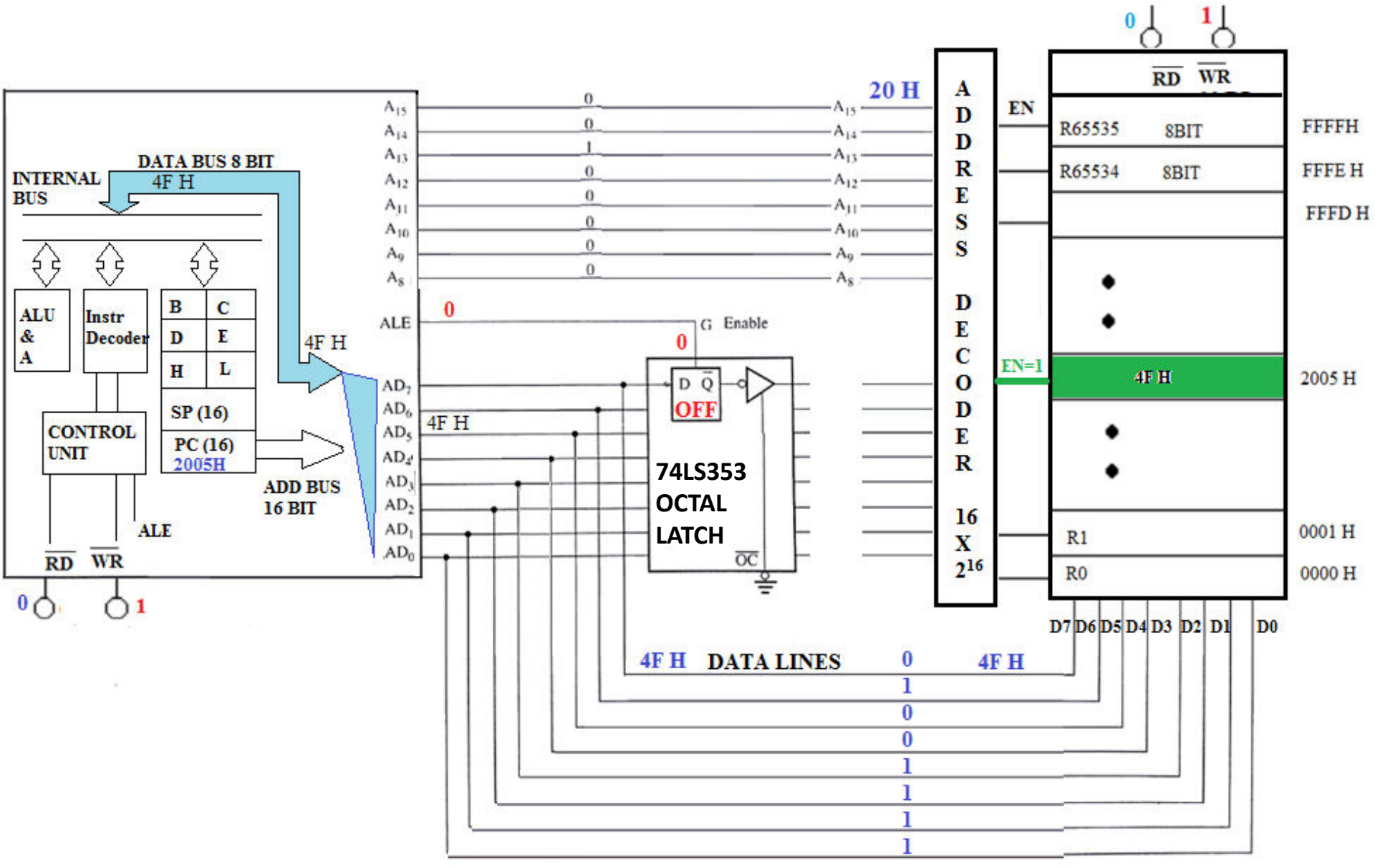
Microprocessor Control Unit generates: $ALE = 0, \overline{RD} = 0, \overline{WR} = 1$



MICROPROCESSOR COMMUNICATION & BUS TIMING
STEP-3 (THIRD CLOCK CYCLE)

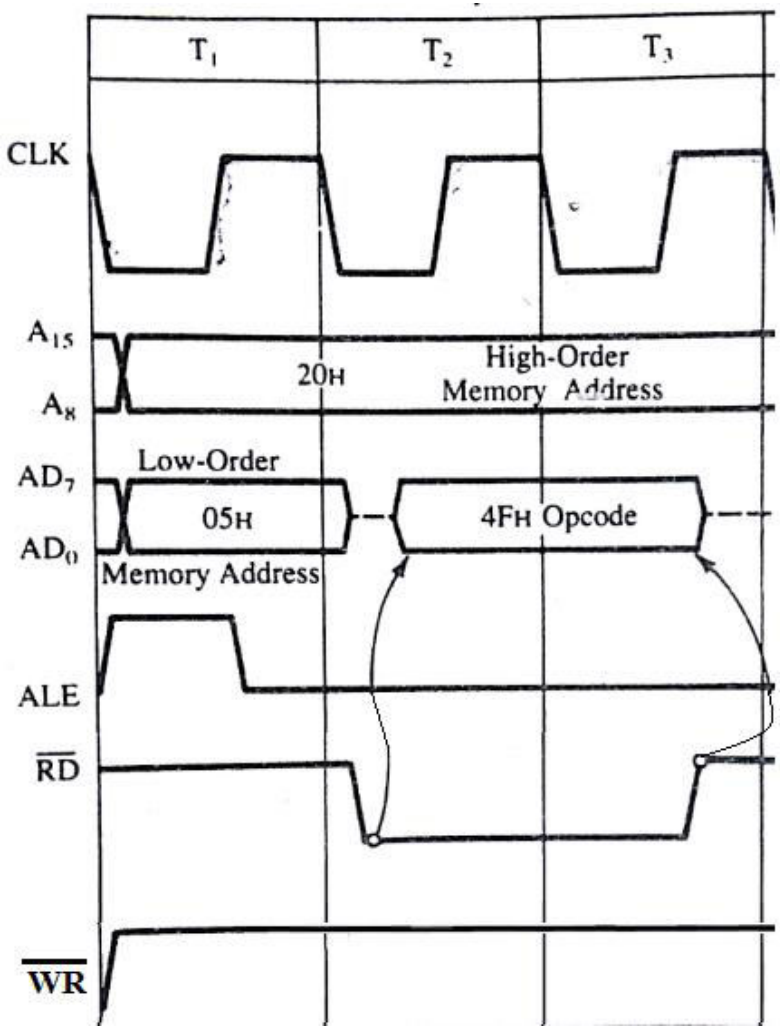
$$ALE = 0, \overline{RD} = 0, \overline{WR} = 1$$

Opcode 4F H is placed on data lines



MICROPROCESSOR COMMUNICATION & BUS TIMING
STEP-3 (THIRD CLOCK CYCLE)

Opcode 4F H is placed on data lines

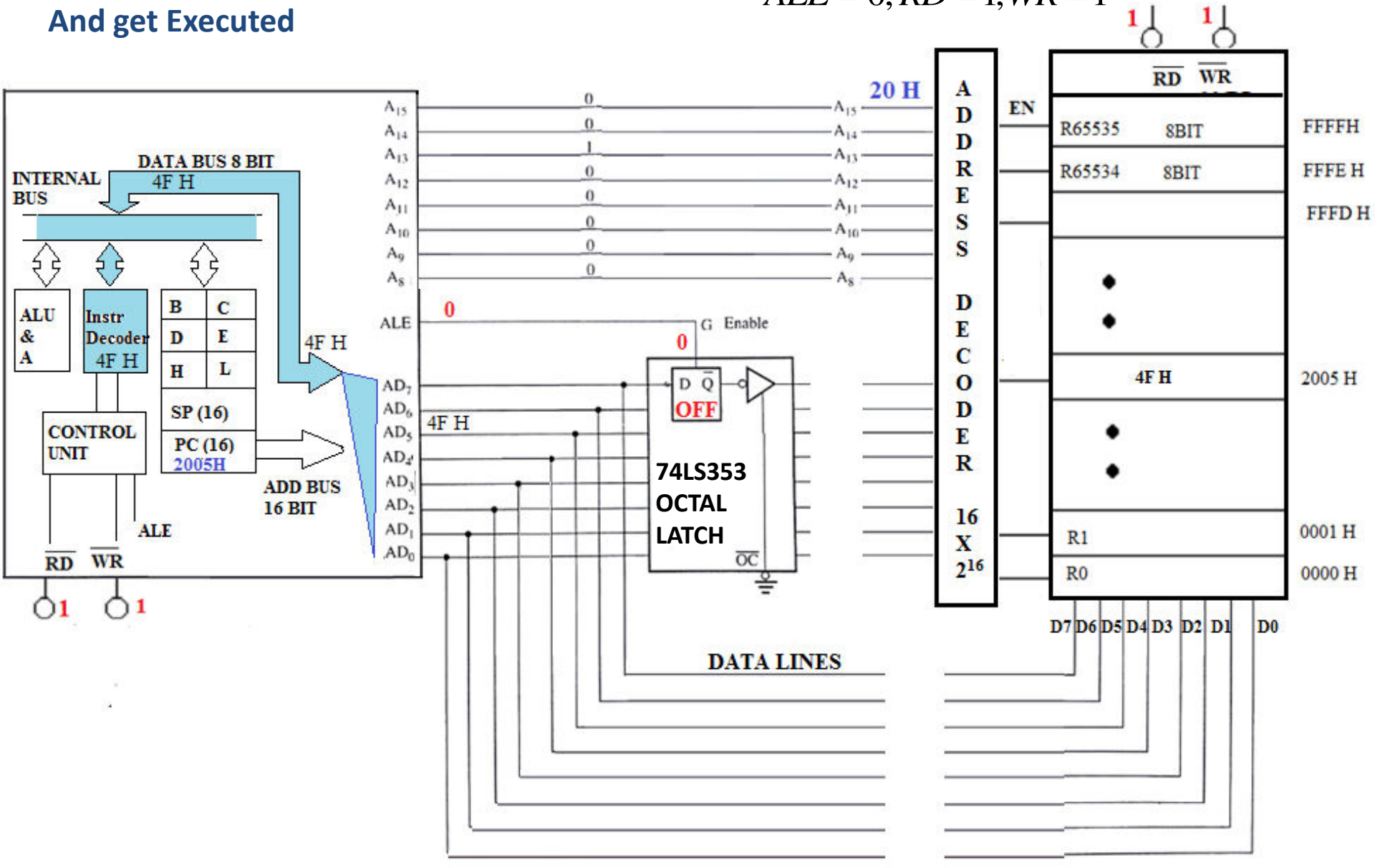


MICROPROCESSOR COMMUNICATION & BUS TIMING
STEP-4 (FOURTH CLOCK CYCLE)

Ignoring Chip Select signal

Opcode 4F H goes to INSTRUCTION DECODER And get Executed

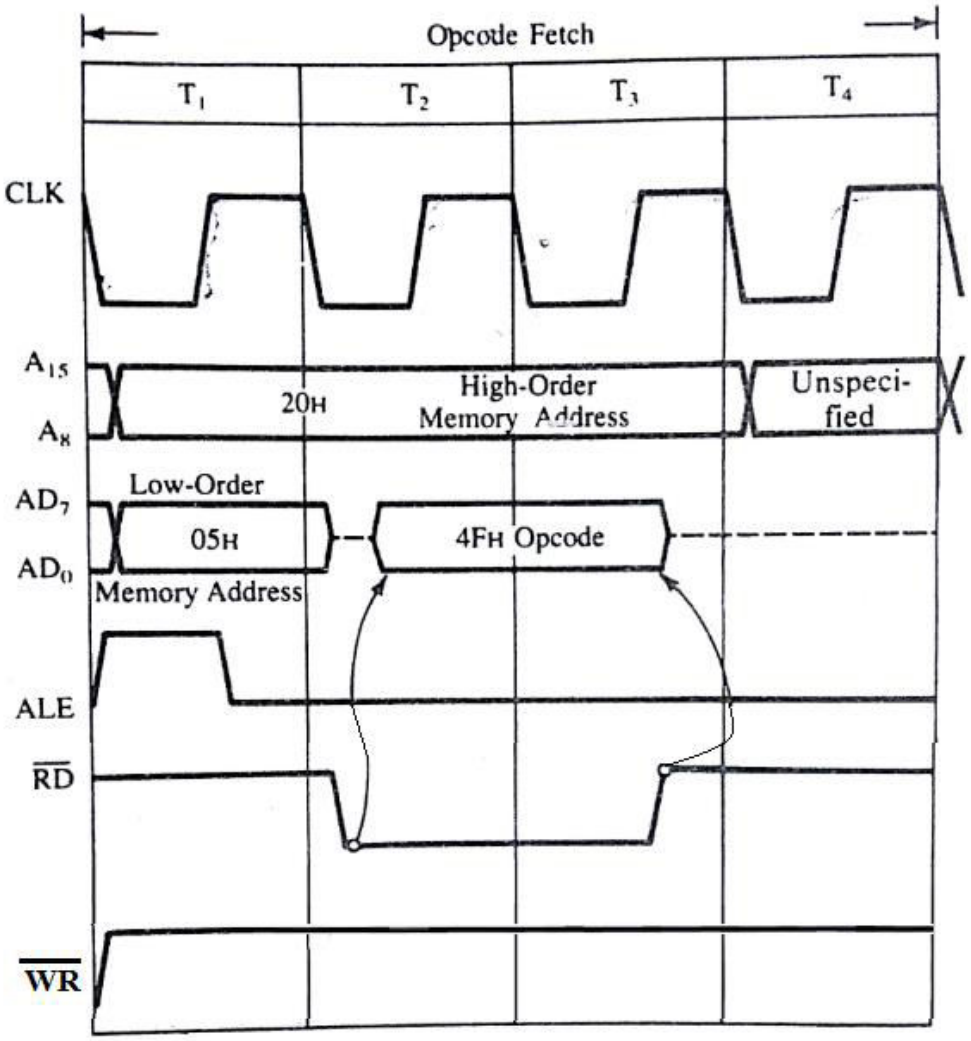
$$ALE = 0, \overline{RD} = 1, \overline{WR} = 1$$



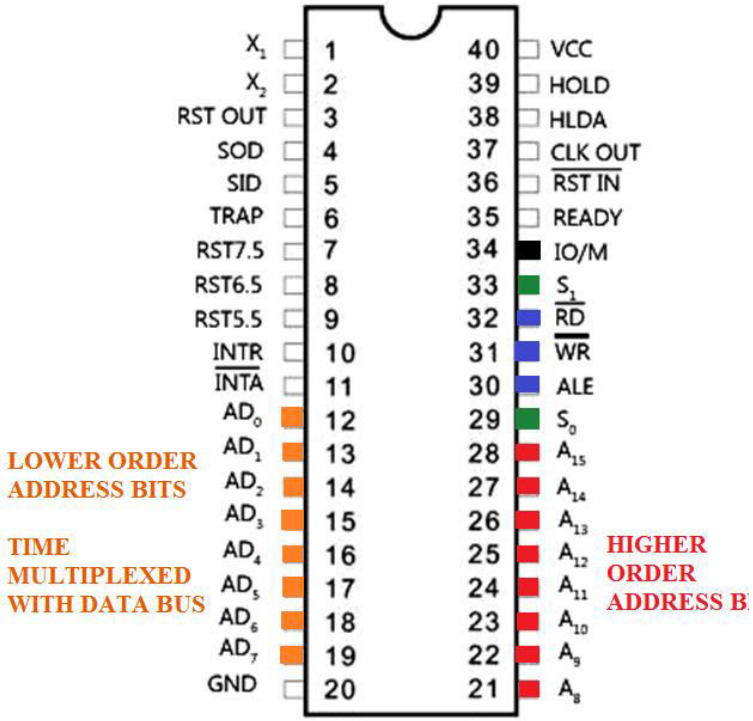
MICROPROCESSOR COMMUNICATION & BUS TIMING
STEP-4 (FOURTH CLOCK CYCLE)

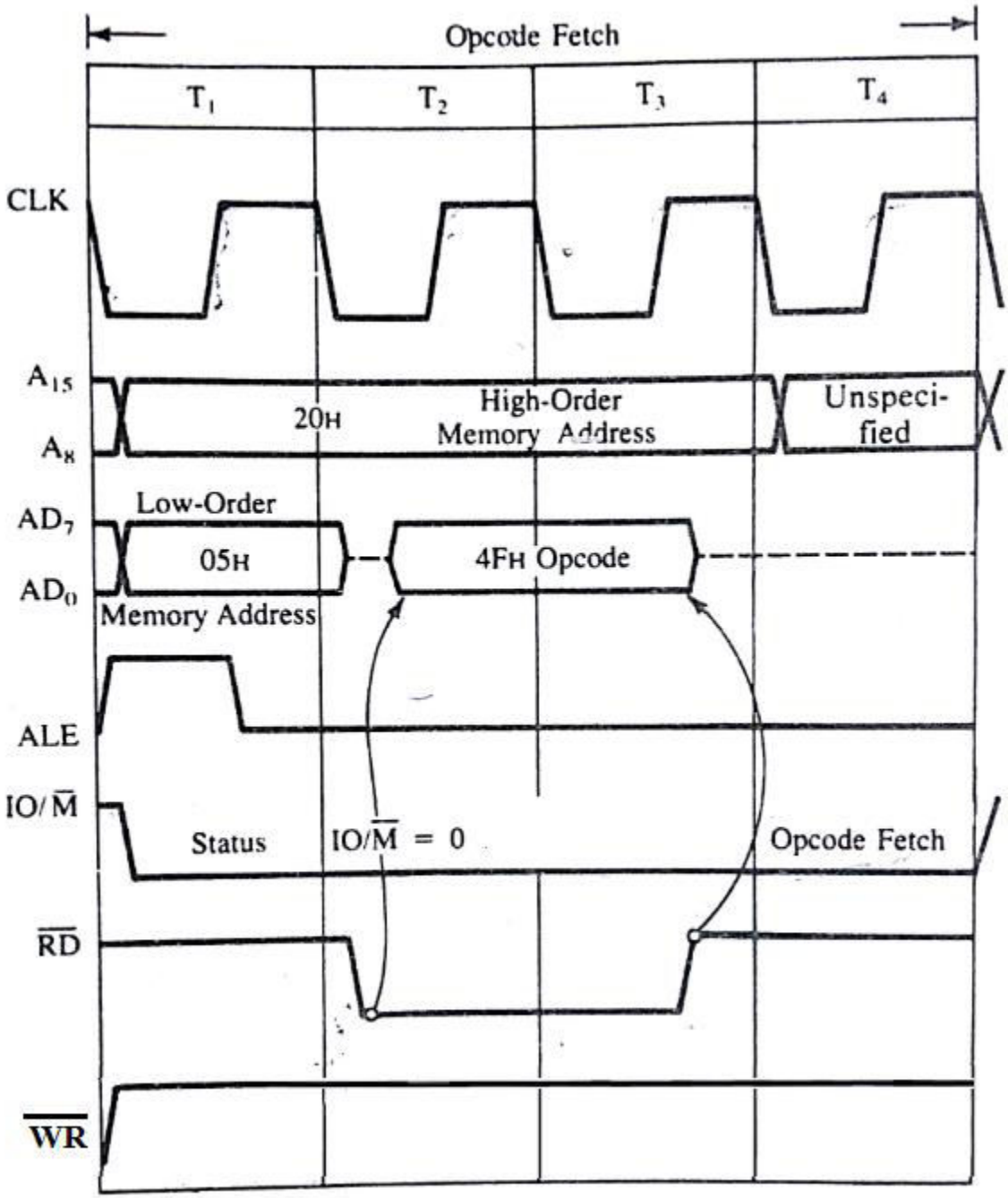
Opcode 4F H goes to INSTRUCTION DECODER And get Executed

$$ALE = 0, \overline{RD} = 1, \overline{WR} = 1$$



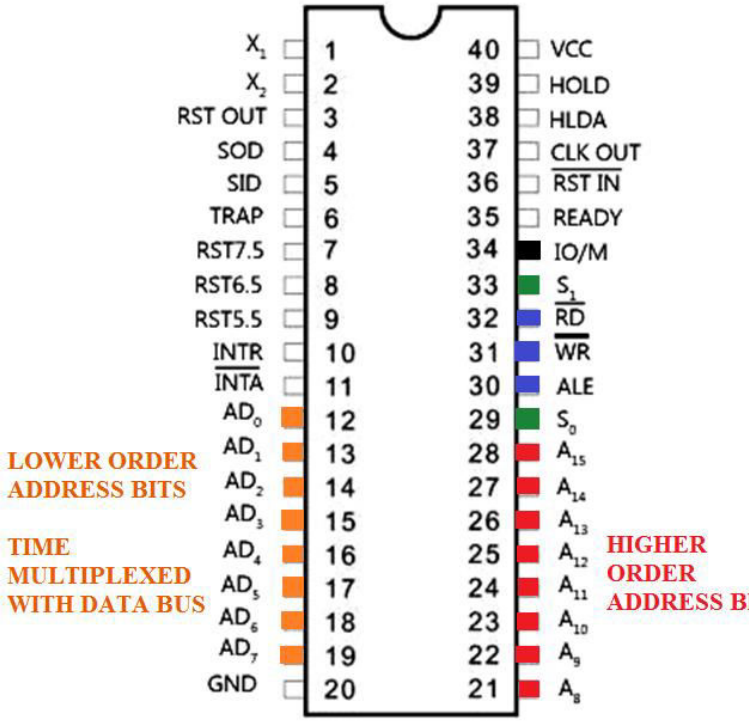
$IO/\overline{M}$ PIN 34

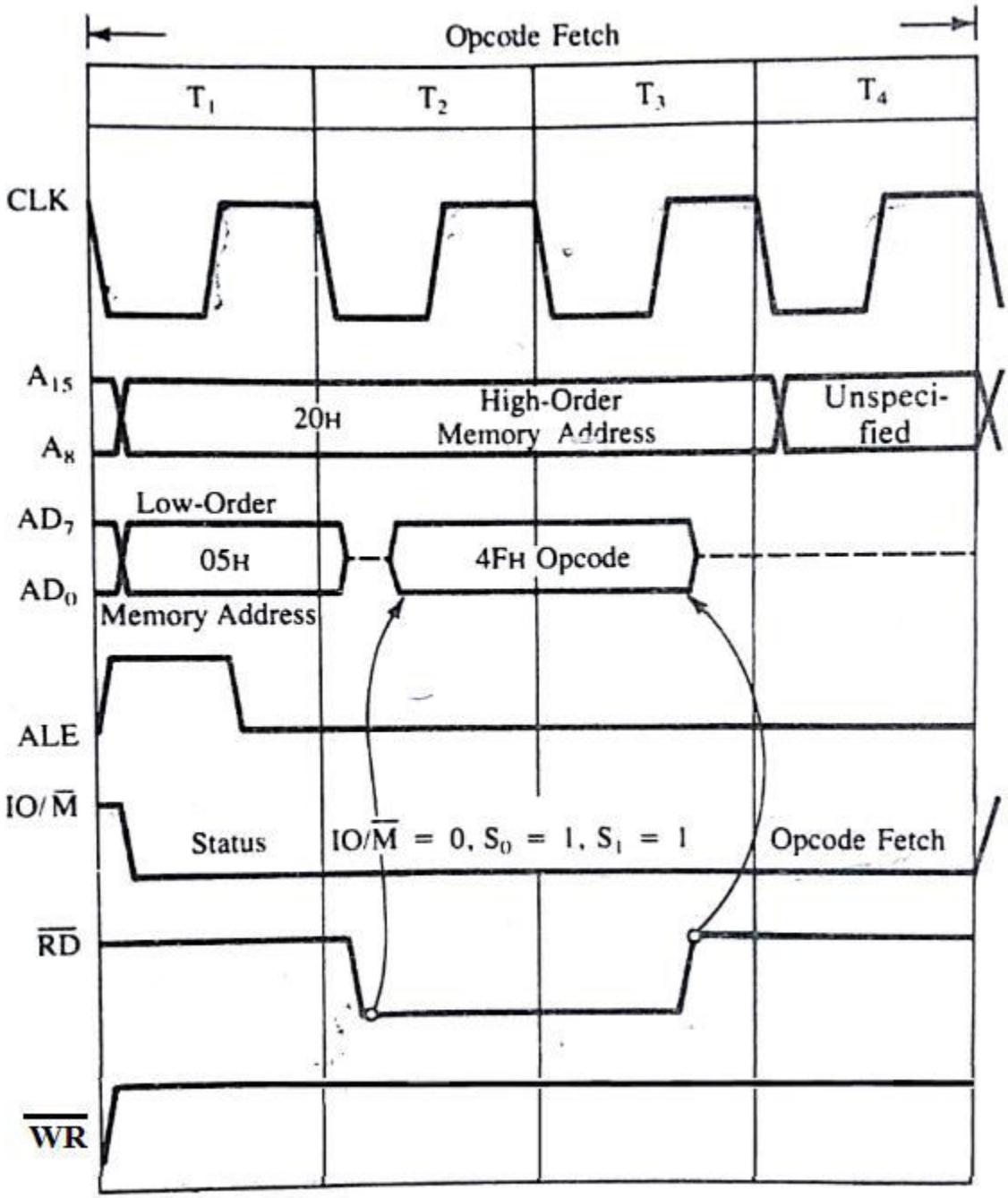




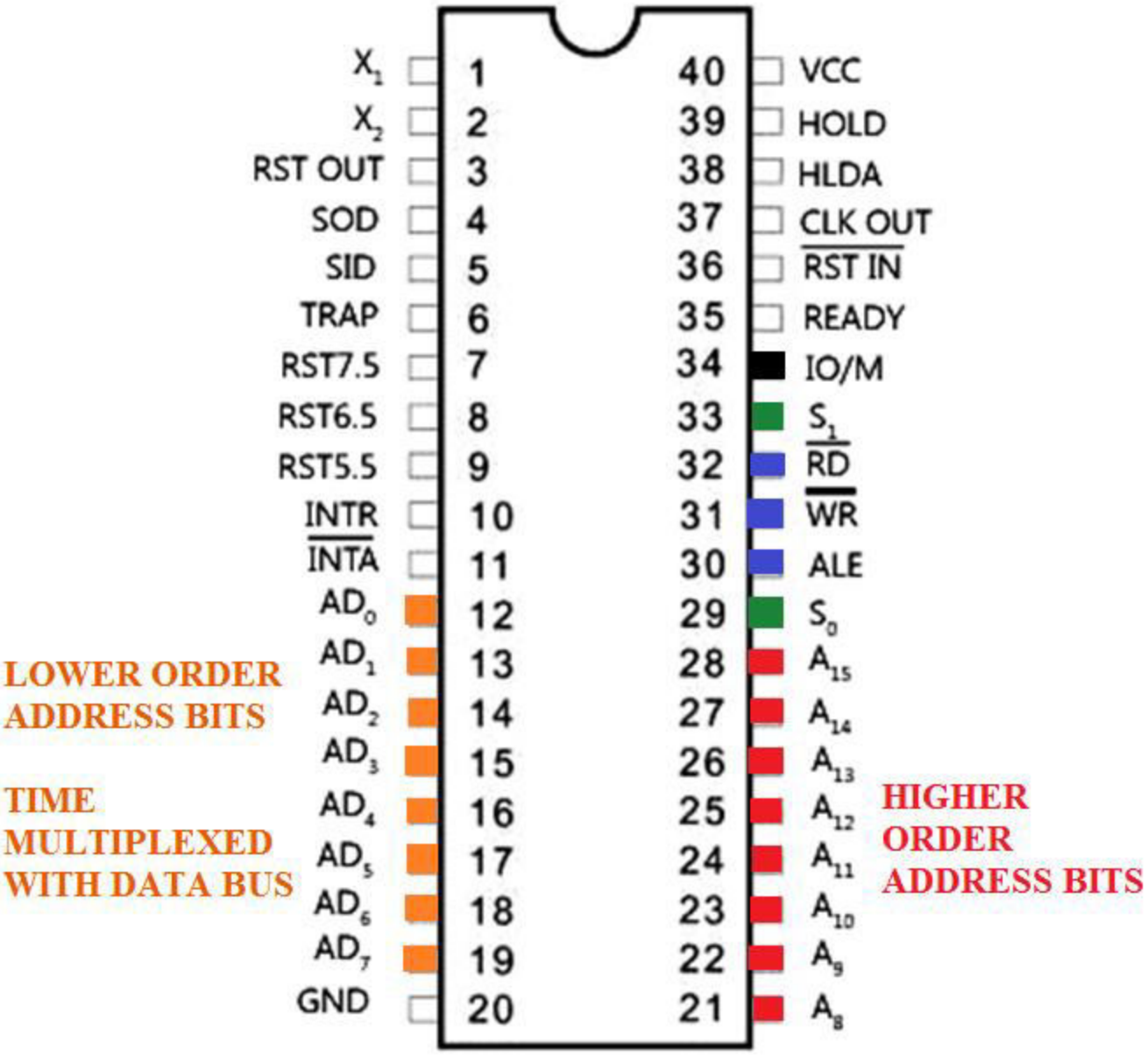
S0 & S1

PIN 29 & 33

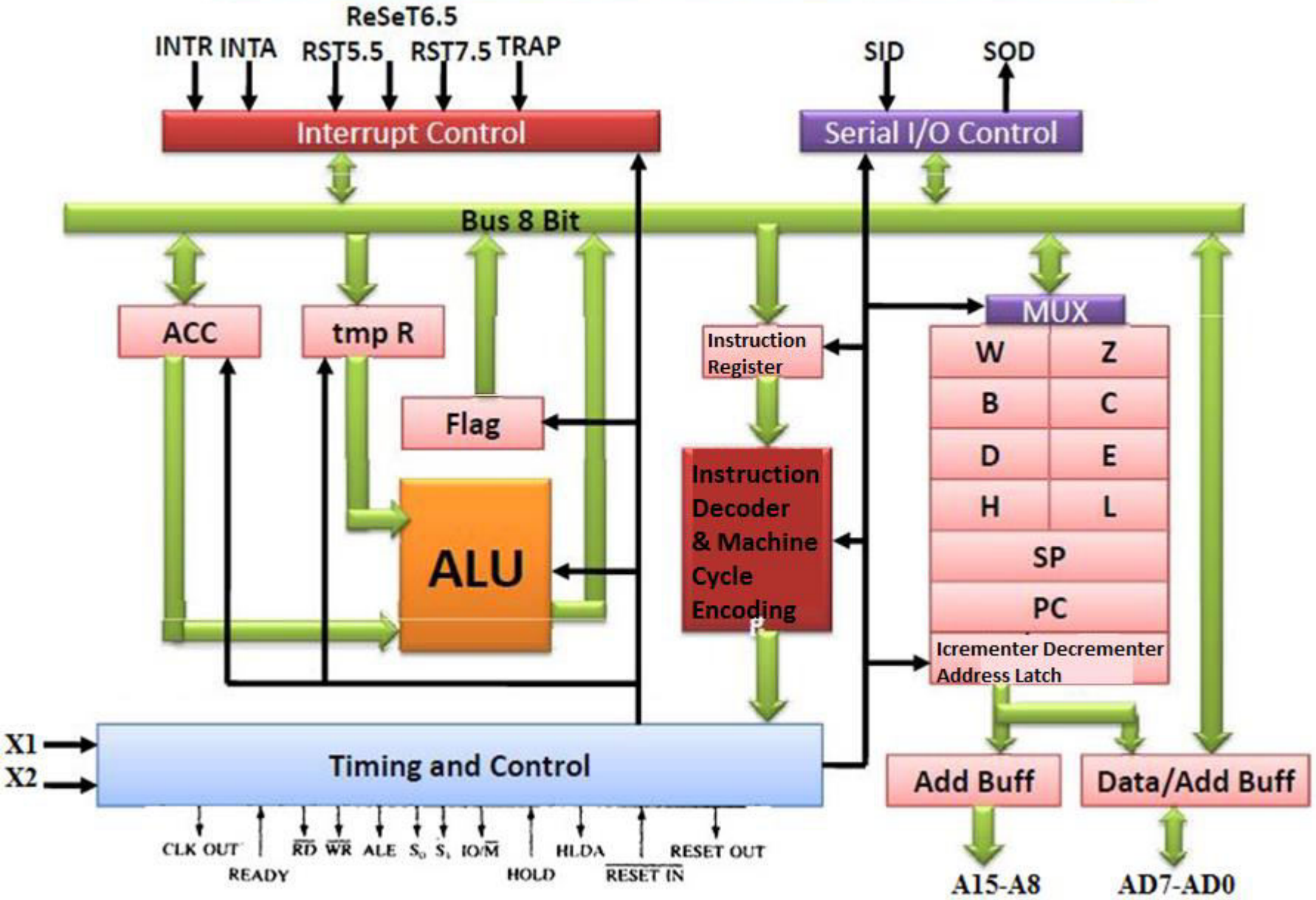




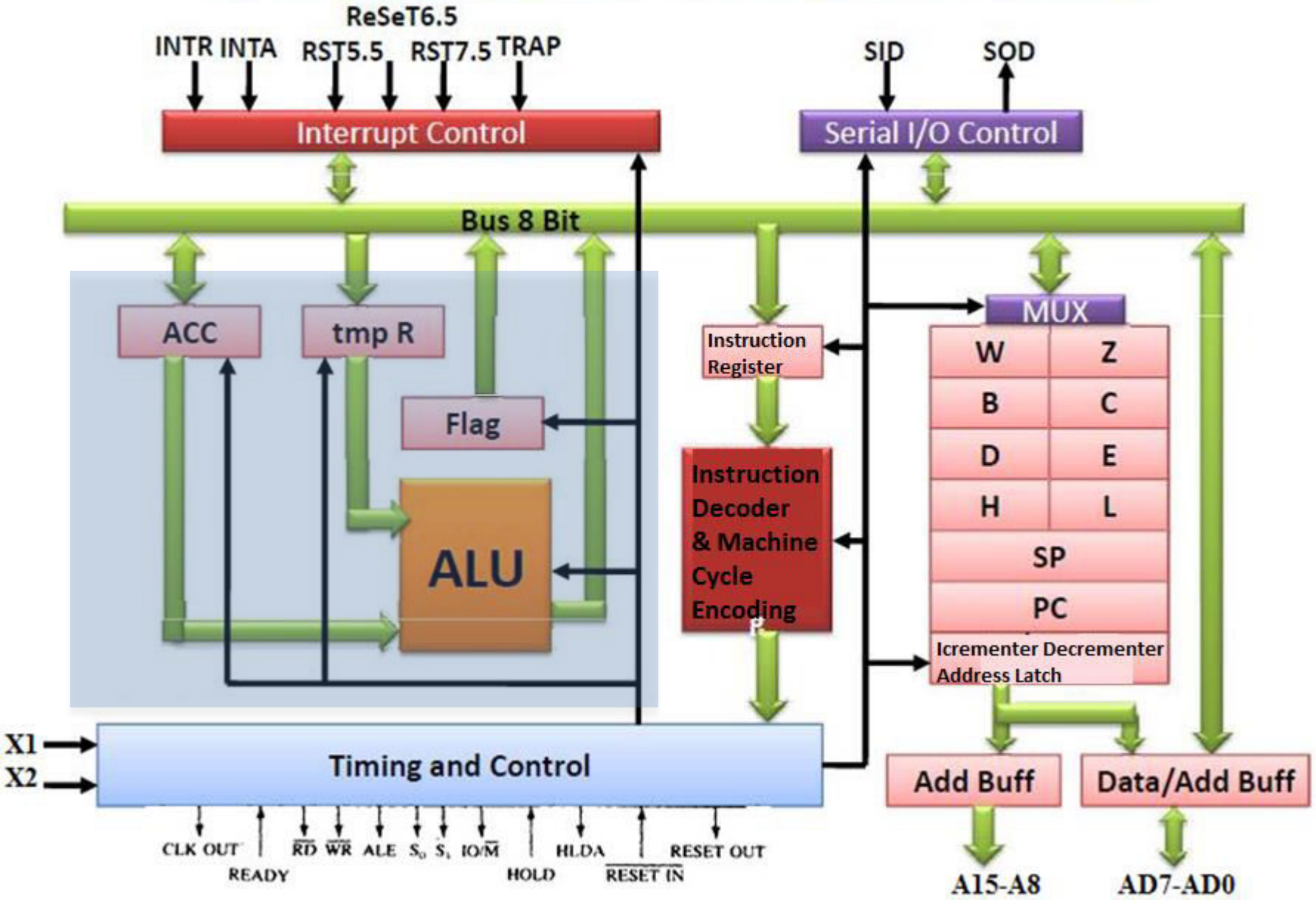
8085 REMAINING PINS



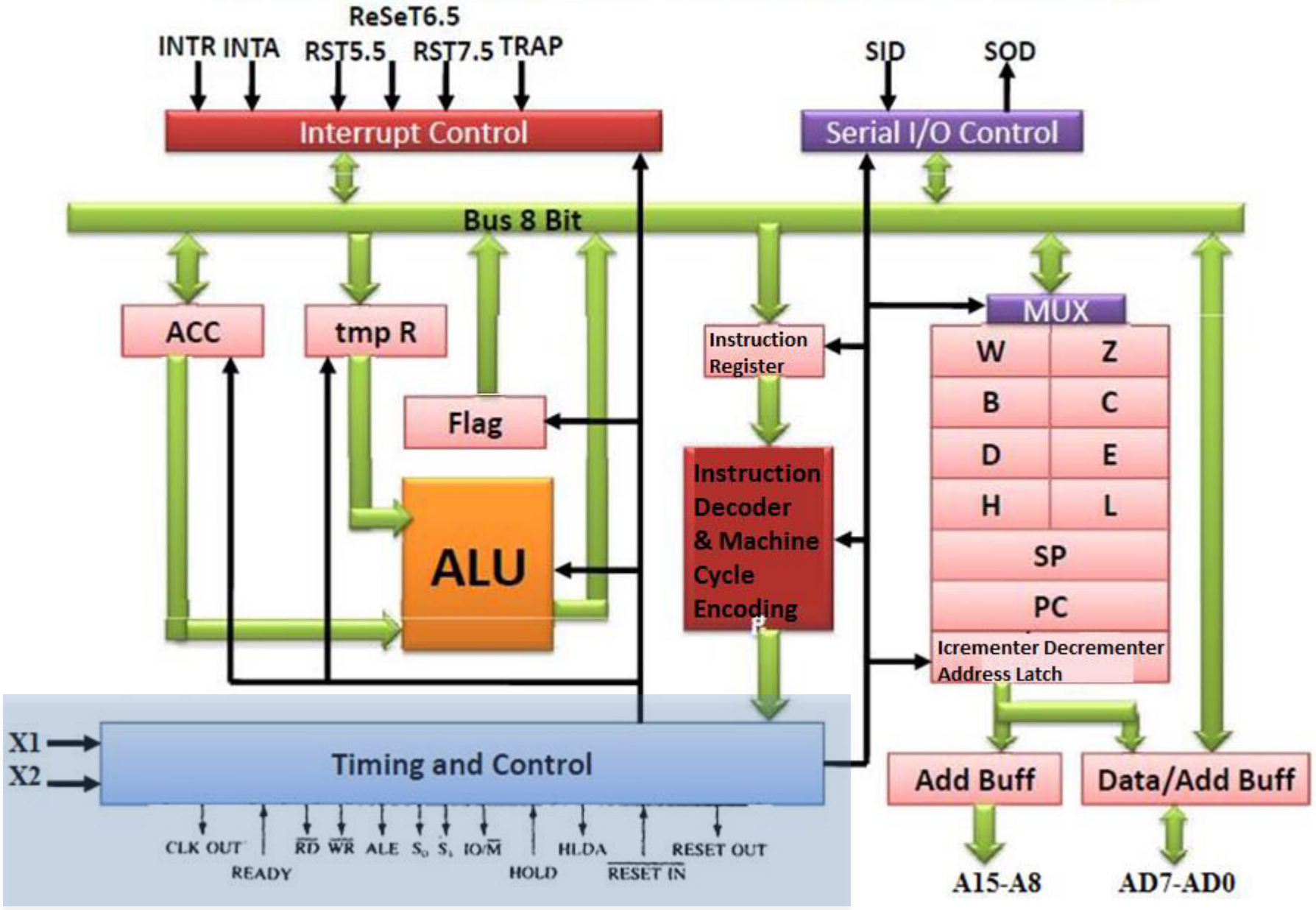
8085 Microprocessor Architecture



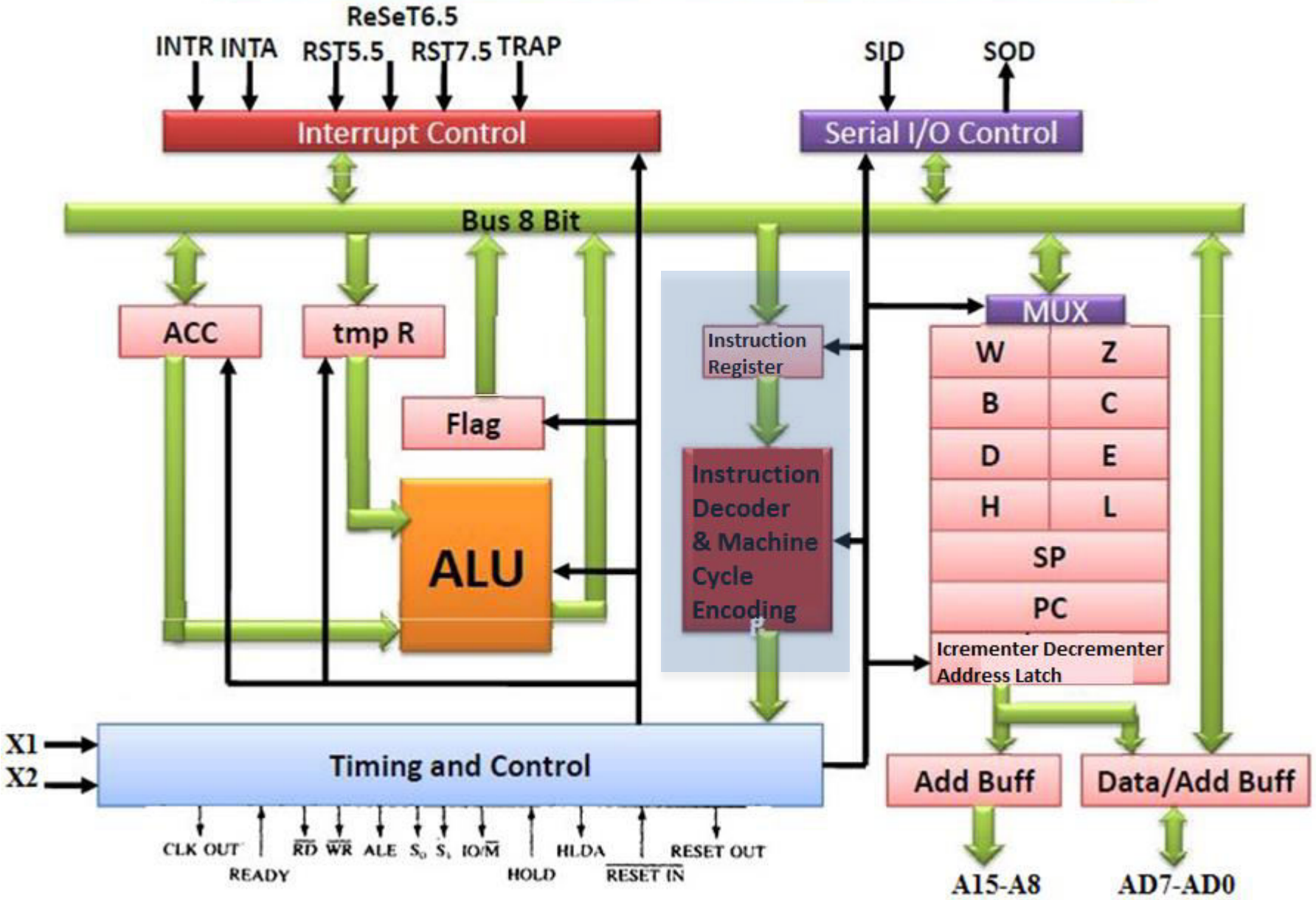
8085 Microprocessor Architecture



8085 Microprocessor Architecture



8085 Microprocessor Architecture



8085 Microprocessor Architecture