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# NAVAL POSTGRADUATE SCHOOL

## Monterey, California


# DIGITAL CONTROL AND INTERFACING FOR A HIGH SPEED SATELLITE COMMUNICATIONS SIGNAL PROCESSOR

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ABSTRACT

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# I. INTRODUCTION

## A. BACKGROUND

This project is one of a series of research projects undertaken by the Naval Postgraduate School (NPS) Satellite Communications Laboratory concerning Navy UHF Satellite Communications. In March of 1977, this laboratory received funding from PME 1Ø6-1 of the Naval Electronic Systems Command (NAVELEX) to develop, design and construct a Satellite Communication (SATCOM) Signal Analyzer at NPS. The purpose of the SATCOM Signal Analyzer is to provide high speed spectrum analysis of the Navy UHF communication satellite transponders while in orbit.

## B. SPECIFIC GOALS

The specific goals in the development of this system are: (1) to provide all necessary equipment to make real-time measurements at NPS; (2) develop satellite signal analysis techniques; (3) to provide equipment design for use in a follow-on version of the Fleet Satellite Monitoring System (FSM) presently in use at the Naval Communication Stations to monitor the GAPFILLER and FLTSAT satellites.

## C. SCOPE OF THIS REPORT

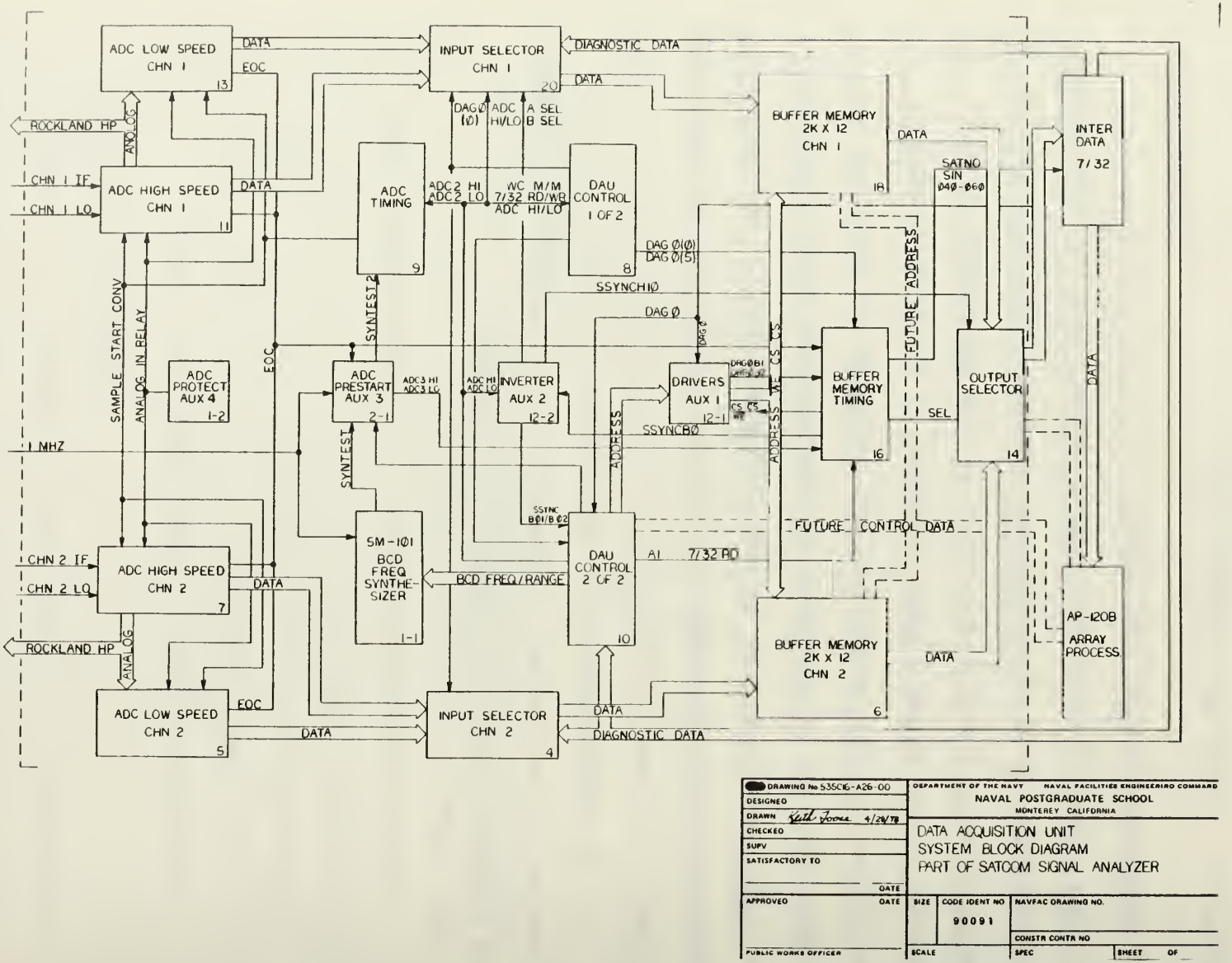
Figure 1 is a simplified block diagram of the SATCOM Signal Analyzer System. This report documents the design and construction of the interface between the Data Acquisi-

tion Unit (DAU) and the Floating Point Systems AP-12ØB Array Processor, shown as a dashed line.

## D. SATELLITE SIGNAL ANALYZER

The SATCOM Signal Analyzer has been constructed around an INTERDATA 7/32 minicomputer system, which provides all the necessary control for most of the equipment in the system. High speed signal processing of data acquired, analog-to-digital converted and buffered in the Data Acquisition Unit is provided by the AP-12ØB Array Processor, as a peripheral device to the INTERDATA 7/32. Additional peripherals are provided for display, control, and software support as shown in Figure 1.

It is recommended that references /1/ and /2/ be digested by the reader to ascertain initial design concepts and implementation preceding this report.

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DATA ACQUISITION UNIT
SYSTEM BLOCK DIAGRAM
PART OF SATCOM SIGNAL ANALYZER

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Figure 1

DAU SYSTEM BLOCK DIAGRAM

## II. DESIGN CONCEPTS

The design goals for the SATCOM Signal Analyzer have been ordered in two major phases. Phase I produced an operational signal analyzer, including a working Data Acquisition Unit (DAU) integrated into the installed system. The first phase is presented in [1] and [2]. Phase II is intended to optimize the system performance within the constraints of the present devices. Phase II involves modifications of the DAU to allow a direct interface with the AP-12ØB. This means data previously acquired and buffered in the DAU, then passed to the 7/32, then to the AP-12ØB for processing will now be sent directly to the AP-12ØB resulting in a considerable savings of system overhead. This will also allow the INTERDATA 7/32 to perform more control functions and greatly increase system throughput rates.

## III. AP/IOP-16 CHARACTERISTICS

The Array Processor, AP-12ØB, has an input/output port (IOP) that provides for a hardware interface design connection to an external device, i.e. the DAU. The internal I/O registers and Direct Memory Access (DMA) converse with an external device via the IOP. The IOP appears to the DAU, or any external device, as a data bus 16 bits wide, an address bus 2Ø bits wide, and control lines /¯3_/, see Figure 2.

The IOP uses a separate DMA priority level compared to that of the AP-12ØB processor and the host interface INTERDATA 7/32. This implies that while the AP-12ØB is accessing memory, the IOP and 7/32 can perform time multiplexed cycle stealing. The memory controller of the AP-12ØB grants the priority of requests as follows: 7/32 highest, IOP next, AP-12ØB processor last. Thus, cycles stolen by the 7/32 and IOP are transparent to an executing AP-12ØB program.

The IOP is comprised of four DMA registers and a data register organized around the Host Data (HD) bus, see Figure 2. All data going from/to the DAU to/from the IOP passes through this HD bus. Note that data from the AP-12ØB memory to the IOP data register passes through the main data (MD) bus. Data from the IOP to AP-12ØB memory goes over the main data input (MDI) bus. Data and DMA control words pass from the AP internal registers to the IOP DMA control registers via the I/O bus. Main data memory addresses are

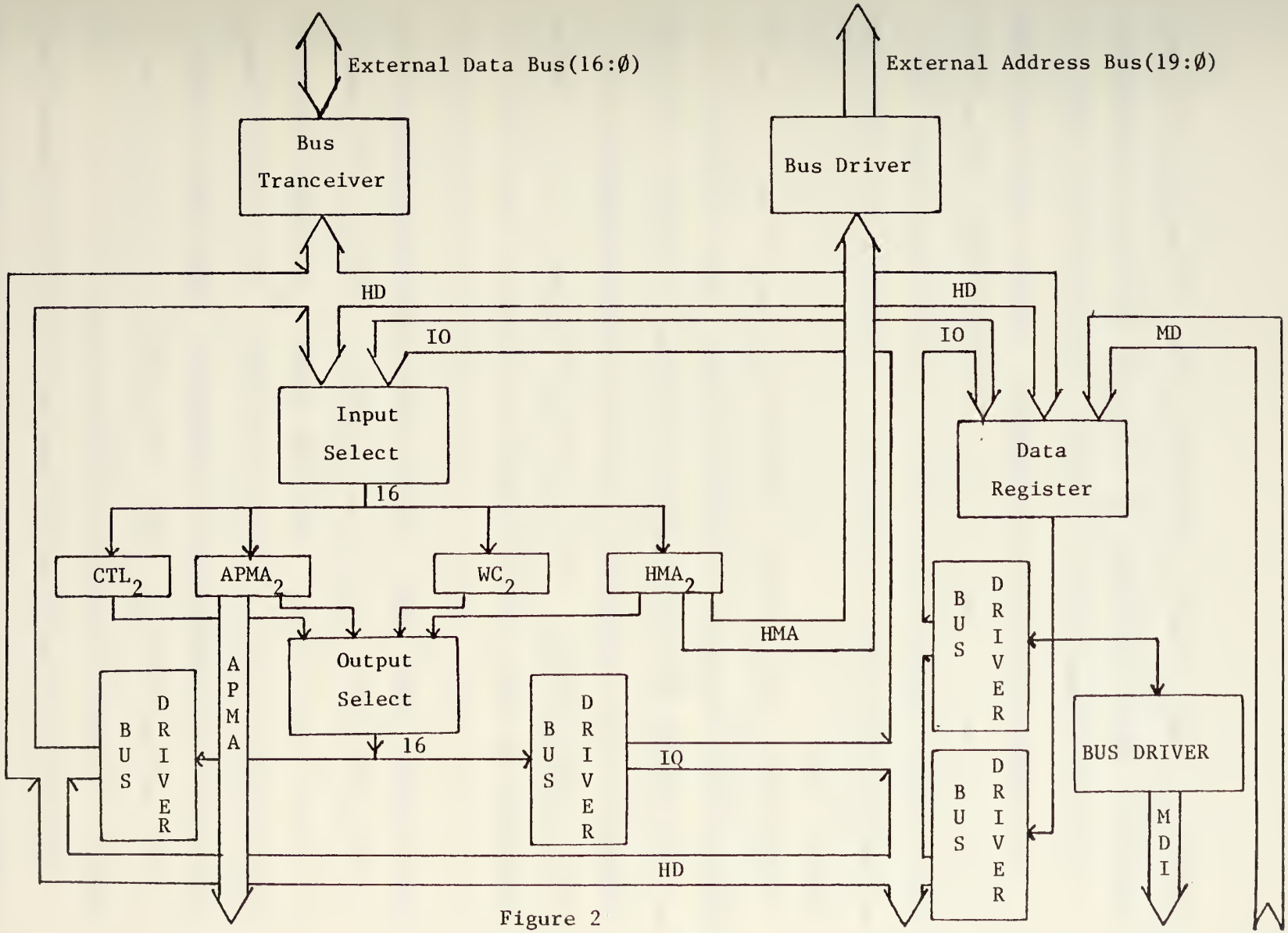



Figure 2

IOP REGISTERS AND DATA PATHS

supplied to the AP main data memory over the memory address (MA) bus. Note that there is a direct path from the External Device Address Register (HMA2) to the external address bus. An important point to remember is that while the 7/32 and the IOP have a common access to the AP-12ØB I/O and MD buses, the two interfaces cannot directly communicate. Intercommunication must be effected by executing AP-12ØB programs [3].

Utilizing the four DMA control registers, the IOP regulates block transfers to/from the DAU. The External Device Address Register (HMA2) maintains the address of the peripheral device or memory for the source/destination of the transferred data. The Word Count register (WC2) counts the number of data words in the DMA process. When WC2 hits zero the DMA transfer stops. Hardware prevents WC2 from counting past zero. The AP-12ØB Memory Address Register (APMA2) points to consecutive locations in Main Data memory during the DMA transfer. The DMA Control Register (CTL2) controls the direction, mode of transfer, and provides status information pertaining to the transfer. HMA2, WC2, APMA2, and CTL2 are all 16 bits wide. A precise functional description of the CTL2 bits is provided in [3].

While either the external device, DAU in this case, or the AP-12ØB can initiate DMA transfers, this design utilizes only DMA transfers initiated from the AP-12ØB. The IOP DMA control registers are accessed by the AP as devices on the

AP internal I/O bus. The AP selects a particular register and loads its address into the Device Address (DA) register. Then when the DA register is set the AP can load the selected register. Note that single word DMA transfers are made by setting WC2=ØØØØØ1.

The rate at which the IOP can DMA transfer words over the external bus depends on the speed of Main Data (MD) Memory. The maximum rate is one 16-bit word/667ns or 1.5 MHz. It is possible for Host interference to cause a delay of up to 5ØØns on an individual cycle. Note that since the Host has a higher priority level to access MD memory, it could conceivably lock out the IOP. However, the 7/32 can transfer at a rate of 1MHz only if it is performing no other operations. Thus the IOP should be able to access MD memory during simultaneous transfers.

The IOP provides 16 data lines, 2Ø address lines, and three control signals to the DAU. These signal names and their functions are listed in Table 1.

The device that initiates the DMA transfer assumes the driver role. The driver places the appropriate address on the address lines, enables data onto the data lines, puts BUSC in the proper state. After allowing a specified time for data and address lines to settle, the driver asserts BUSM to initiate the transfer. Having performed the task as directed, the driven device responds with BUSYN. The driver then removes BUSM upon receiving BUSYN, and after

TABLE I

IOP EXTERNAL BUS SIGNALS

| SIGNAL | FUNCTION |
|---|---|
| BUSD 16-BUSD ØØ (APD 16-APD ØØ) | 16 data transfer lines |
| BUSA 19-BUSA ØØ (APA 19-APA ØØ) | 2Ø external device address lines. Used by the driving device to select a register in the driven device. Note BUSA ØØ is always zero (high). |
| BUSMSYN(BUSM) | BUSMASTER. Driving device synchronization strobe. Initiates data transfer in the driven device. |
| BUSSYN(BUSYN) | BUSYNCHRONIZER. Drive device synchronization strobe. Indicates to the driving device that the driven device has either accepted data or has data ready for the driver to accept. |
| BUSC | BUS CONTROL signal. Used by the driving device to select the direction of transfer. Low ("1") selects driver to driven device. High ("Ø") selects driven to driver. |

Note: With respect to this report, at all times the IOP is the driving device and the DAU is the driven device.

allowing for propagation delay in the cable, releases the data and address lines. When the driven device receives false BUSM (low), it removes BUSYN and the cycle is ready to start again.

For the purposes of this report, the IOP will assume the driver role during all DMA transfers. A diagram of the timing relationships among bus signals is shown in Figure 3. A cycle begins with the IOP driving the address and data lines to a desired state and forcing BUSC true (low on the bus), for transfer from IOP to DAU. After a delay of 1ØØns (minimum) to allow address and data to propagate and stabilize, the IOP drives BUSM true (low on the bus). If the DAU was prepared to accept the data, it would strobe the data into the addressed register and drive BUSYN true (low on the bus). A maximum of 1ØØns after the IOP receives BUSYN true, it removes BUSM, i.e. makes it false (high on the bus). The address lines are held true a minimum of 1ØØns after BUSM goes false to insure against a change while BUSM is still true. The IOP considers the cycle over when it removes the address lines. The external device should remove BUSYN no later than 2ØØns after BUSM goes false to prevent interfacing with the next cycle. BUSM will go true again a minimum of 3ØØns after it goes false. The actual time depends on the number of cycles stolen by Host from AP-12ØB MD memory.

Note that the cycle time is actually dependent on the speed with which the driven device responds with BUSYN.

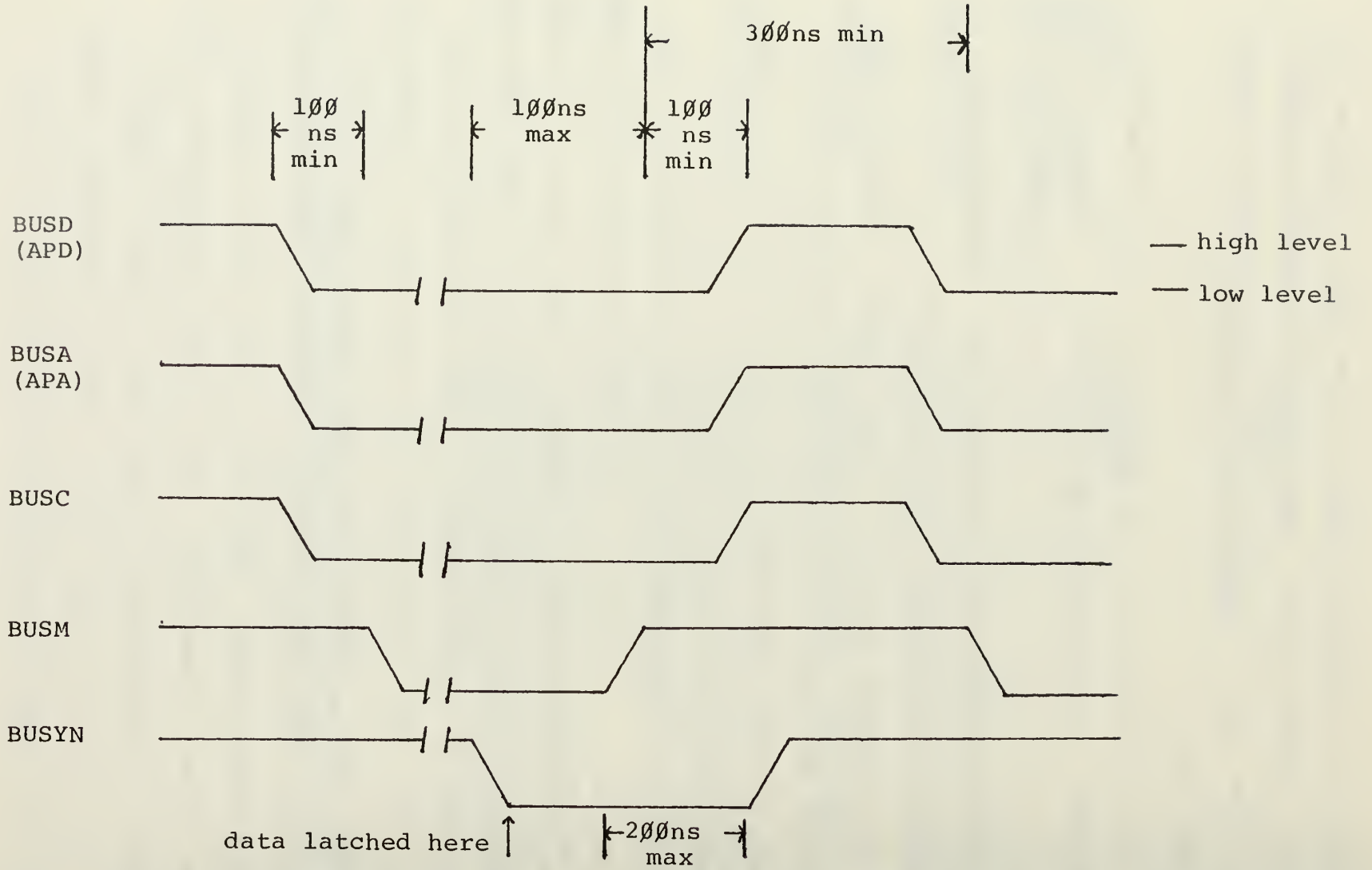



Figure 3

TIMING DIAGRAM IOP TO EXTERNAL DEVICE

This dependency allows DMA transfers to take place at the driven device speed. A time-out circuit is provided in the IOP to prevent "hanging" the IOP forever if the external device fails to respond due to an error /-3-/. The factory installed time-out is 2Ø microseconds. If no response is seen within that time, the entire DMA process is terminated. This time-out may be lengthened or disabled by adjusting the resistor-capacitor timing on chip A-19 of board 237. The resistor, $R_T$, should be kept in the range $5k\Omega < R_T < 5Ø k\Omega$. Defining TW as pulse width, the equation $TW = (Ø,32)(R_T \cdot C_{EXT})(1 + Ø.7/R_T)$ applies for chip A-19 (74123) where Ø.32 is a constant, $R_T$ = kΩ(total), $C_{EXT}$ = picofarad. As of this report, $R_T$ = 39kΩ and $C_{EXT}$ = 33 microfarads resulting in a pulse width TW of 5ØØ miliseconds.

The timing diagram for a DMA transfer from the external device to the IOP under IOP control is shown in Figure 4. First the IOP drives address data onto the bus. BUSC is left false (high on the bus) to indicate the transfer is from the external device to the DAU. A minimum of 1ØØns after the address is driven, BUSM goes true (low on the bus). Upon receiving BUSM true, the external device should drive data onto the bus and return BUSYN, all within 0.5s from the assertion of BUSM. When the IOP receives BUSYN true, the IOP will wait a minimum of 25Øns to allow the data to propagate and settle, before strobing it into the DATA2 Register. When data is latched, the IOP will remove BUSM

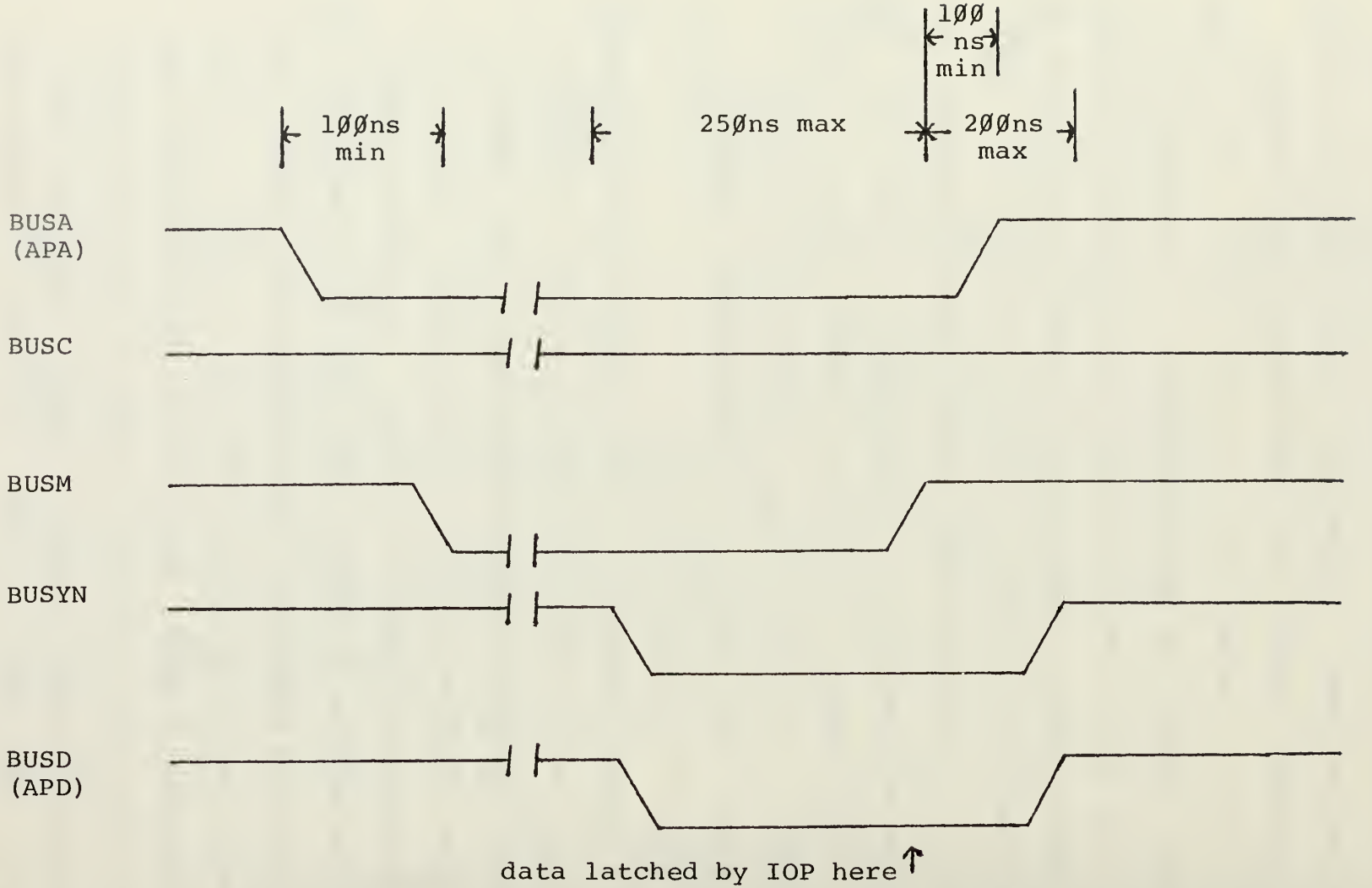



Figure 4

TIMING DIAGRAM EXTERNAL DEVICE TO IOP

and a minimum of 1ØØns later remove the address data from the bus. The external device should remove BUSYN and the data no later than 2ØØns after BUSM goes false. The IOP will drive BUSM true (low on the bus) again no sooner than 3ØØns after it went false.

To assist the reader and system user, a summary of AP/IOP signals and their active states at different DAU system locations is provided in Table II.

All of the external bus signals are open collector bi-directional lines. A signal is considered true when in the low state on the bus. The method recommended by Floating Point Systems for interfacing is shown in Figure 5. The drivers are 7438 open-collector buffers. The receivers are 864Ø bus receivers. One line input to each driver-receiver pair is connected to BUSC or $\overline{\text{BUSC}}$ to appropriately enable or disable the chip for directional control of data flow.

Appendix D contains a wiring pin-out list for the back-plane of the AP. Data is carried to the external device via a Ribbon cable. Figure 6 shows a representation of the AP backplane as viewed from the back of the AP. Note there are two input terminals IN1 and IN2 and two output terminals OUT1 and OUT2 referenced with respect to the AP. Since the SATCOM LAB has only one IOP-16, terminals IN1 and OUT 1 are used. The terminal block referenced on Figure 6 is placed in the OUT1 terminal location. The ribbon cable enters the IN1 location.

TABLE II

SUMMARY OF AP/IOP SIGNALS AND THEIR

STATE AT DIFFERENT DAU SYSTEM LOCATIONS

| | INSIDE AP* | ON BUS CABLE | INSIDE DAU** |
|---|---|---|---|
| BUSC | H=+5=T=1<br>L=GND=F=Ø | L=GND=T=Ø<br>H=+5=F=1 | H=+5=T=1<br>L=GND=F=Ø |
| BUSM | H=+5=T=1<br>L=GND=G=Ø | L=GND=T=Ø<br>H=+5=F=1 | H=+5=T=1<br>L=GND=F=Ø |
| BUSYN | H=+5=T=1<br>L=GND=F=Ø | L=GND=T=Ø<br>H=+5=F=1 | H=+5=T=1<br>L=GND=F=Ø |
| BUSD | H/L=+5/GND=1/Ø | H/L=+5/GND=Ø/1 | H/L=+5/GND=1/Ø |
| BUSA | H/L=+5/GND=1/Ø | H/L=+5/GND=Ø/L | H/L=+5/GND=1/Ø |

H = HIGH

L = LOW

GND = GROUND

T = TRUE

F = FALSE

* → BEFORE LINE DRIVER

** → AFTER LINE RECEIVER

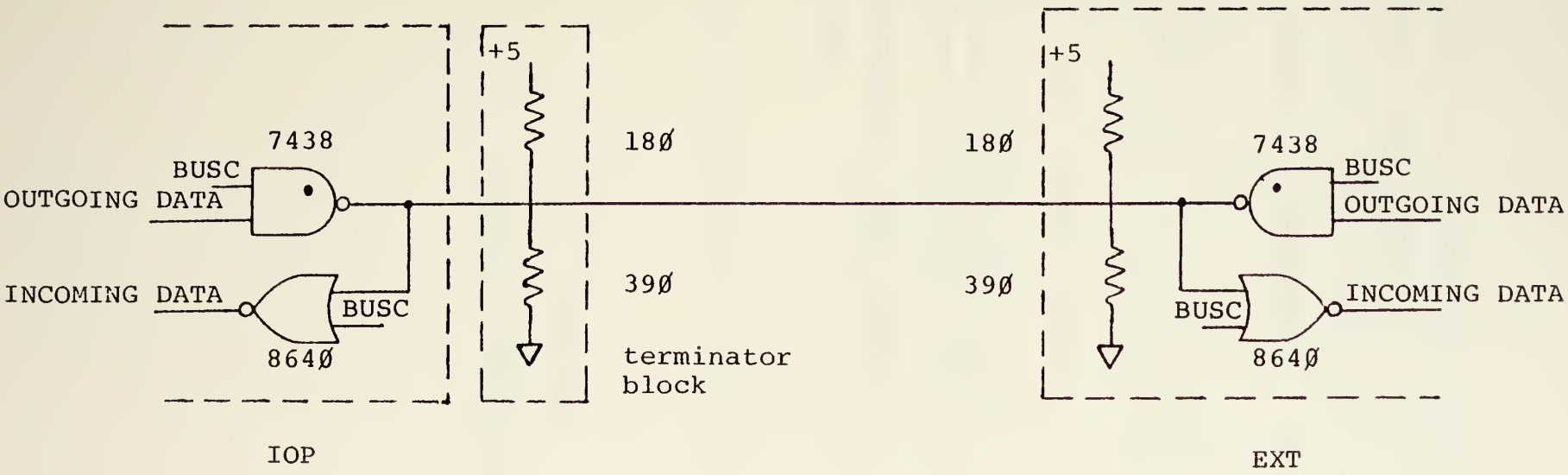



Figure 5

TYPICAL EXTERNAL BUS LINE

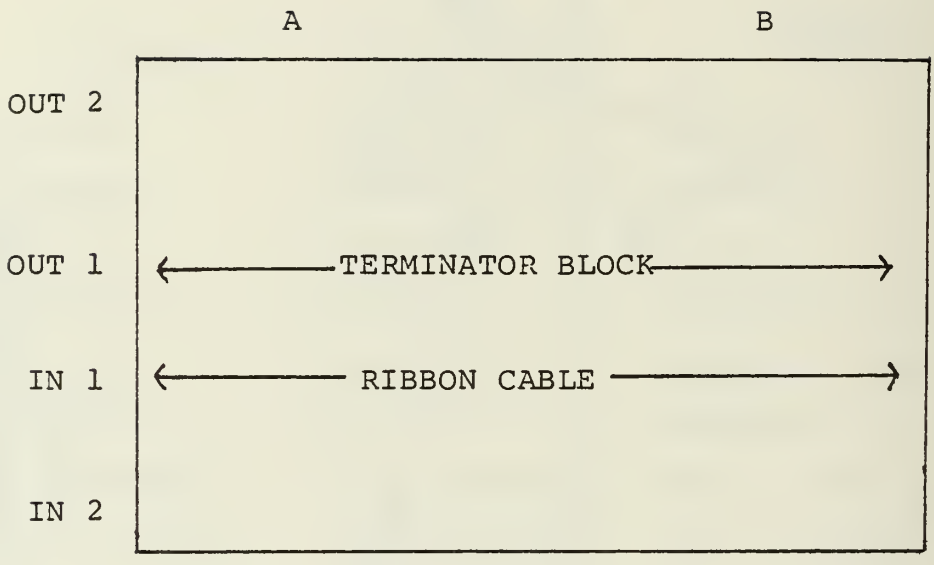
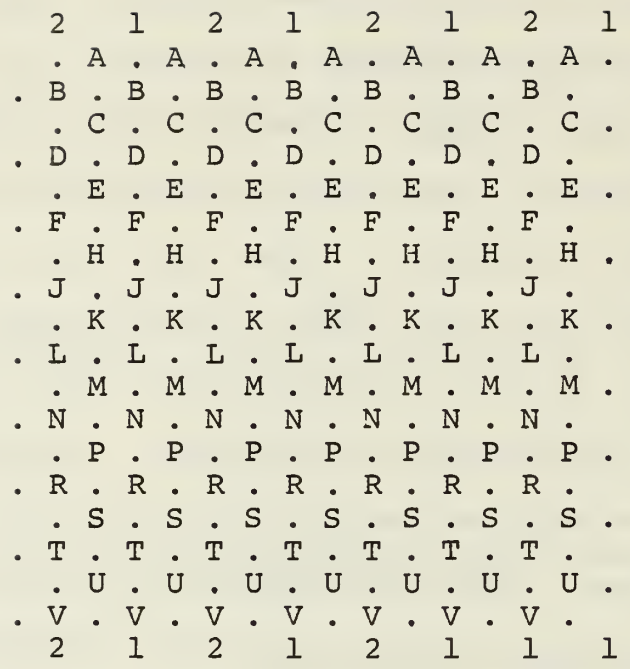



Figure 6

AP BACKPLANE CONNECTOR

The letters on the backplane diagram, Figure 7, correspond to a wiring list internal to the AP /-3-/. For convenience, the IN1 terminal connector can be thought of as an 8Ø pin connector, even numbers on the top and odd on the bottom as shown in Figure 8. Note that the connector in the back of the DAU where the ribbon cable attaches is an 86 pin connector. A plug is placed in pin hole 81-82 for compensation to insure proper connection. Inspection of the ribbon cable reveals an insert at pin locations 37-45 to fit the AP backplane. This means pins 37-45 must not be used in the DAU. Care must be exercised at all times when handling the ribbon cable.



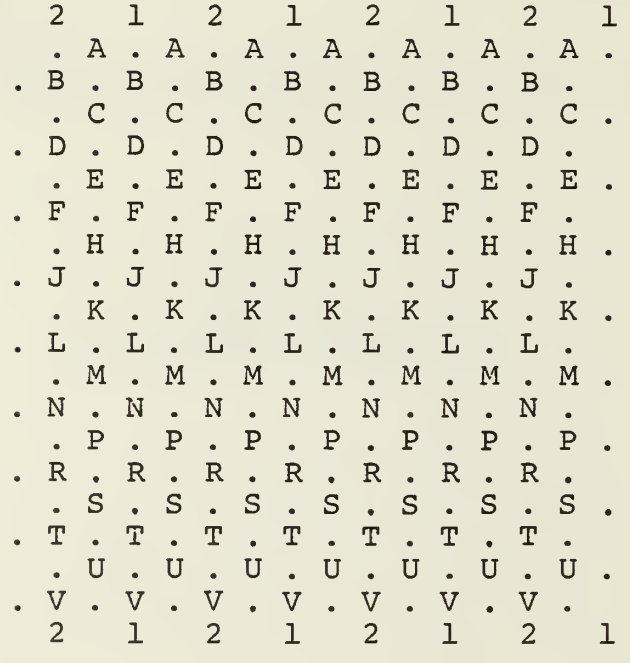




Figure 7

AP-12ØB - BACKPLANE

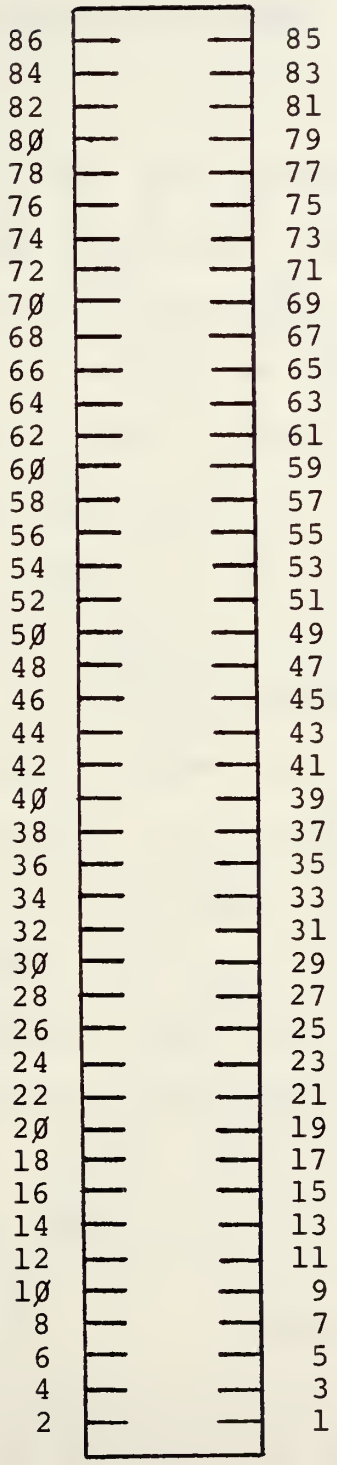



Figure 8

AP-12ØB SIMULATOR BACKPLANE

# IV. DAU MODIFICATIONS

## A. INTRODUCTION

Originally the DAU was setup and controlled solely by the INTERDATA 7/32. The 7/32 passed addresses via COT lines and data via DOT lines to boards 8 and 1Ø, Figures 9 and 1Ø respectively. This data was passed via backplane connectors two (2) and three (3) from the 7/32. The five key internal registers of the DAU: (1) range, (2) frequency, (3) address, (4) word count, and (5) control, were set up by data passed from the 7/32. The internal buffer memory was addressed only from the DAU address register (3). Consequently as data was acquired and then read out, the address register (3) was reset to zero to insure the first point acquired was the first point readout. The Word Count register (4) was set initially for acquisition and then reset when reading out to insure all the data was read. The control register (5) was set as desired to high speed acquisition, low speed acquisition, read, etc. Note that the sample rate was first set in registers (1) and (2) and remains until changed.

## B. MODIFICATION OBJECTIVES

The modification objectives of this report consist of using the AP-12ØB's IOP-16 interface as a smart device to set up and control the internal device registers. So, utilizing the IOP-16 under program control of the AP makes it, the IOP-16, the controller of the DAU from a user program

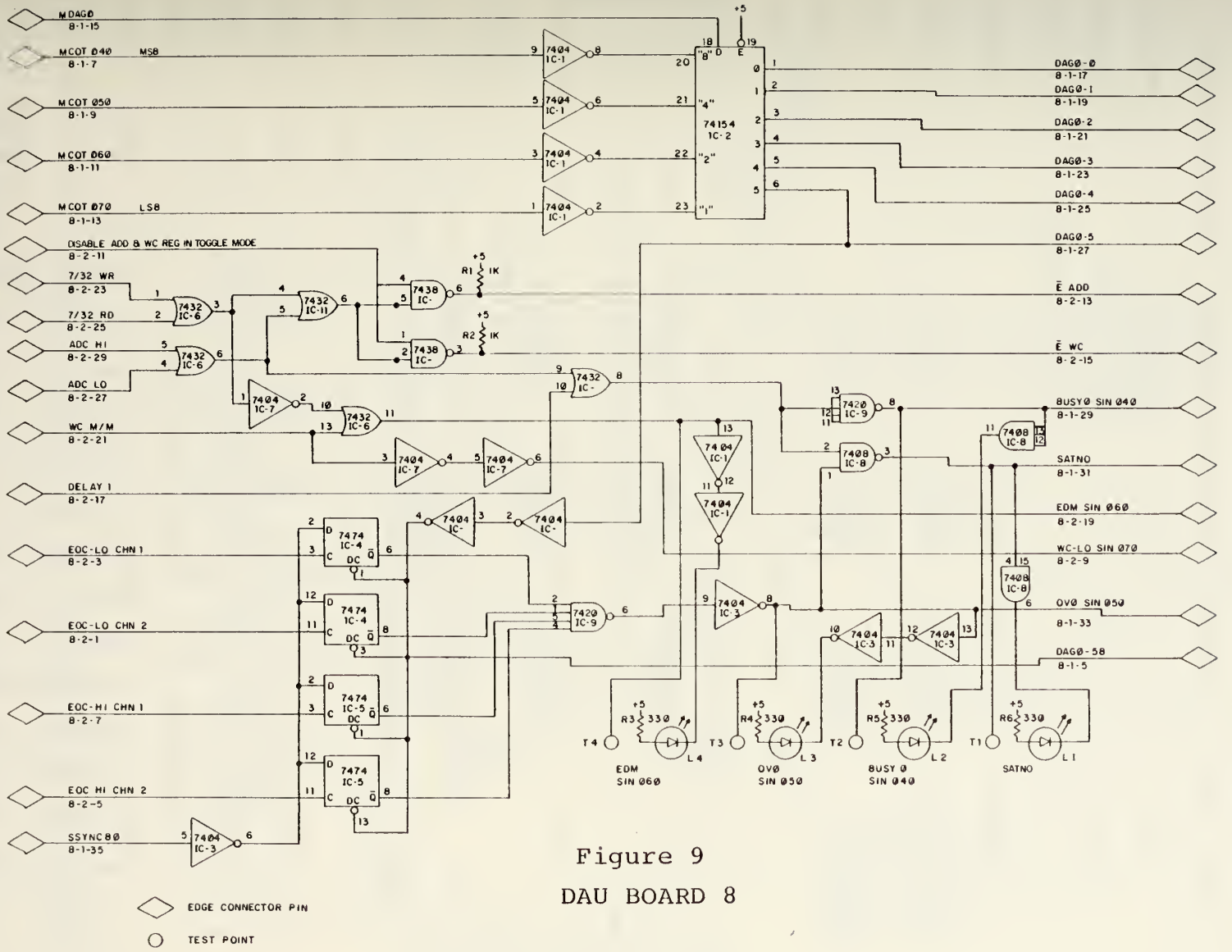



Figure 9

DAU BOARD 8

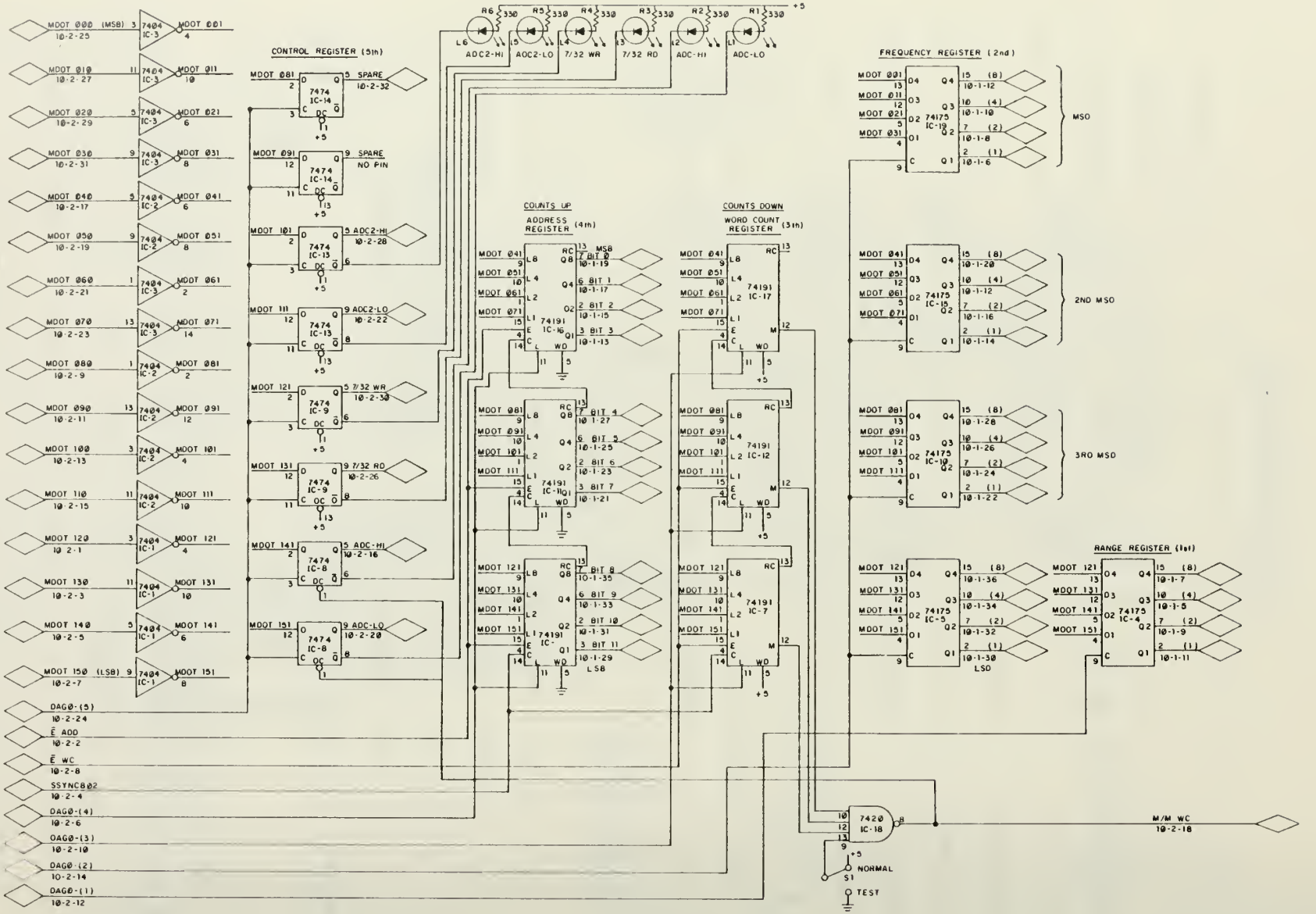



Figure 1Ø

DAU BOARD 1Ø

that can be passed from the 7/32.

Conceptually, to minimize lost processing time in the AP-12ØB, a program using AP Assembly Language can start the DAU into an acquisition mode and continue to process data already stored in the AP main data memory from a previous acquisition. At the same time, the IOP-16 having started the DAU into an acquisition mode, will wait for an end of acquisition signal from the DAU, i.e. word count equals zero in the Block Mode read. Then the most recently acquired data will be stored in AP main data memory in a non-processing block location via DMA transfer. When the AP has finished processing a block of data it will check to see if the new DMA is completed and if so it will start yet a new acquisition and commence processing the most recent DMA transfer from the DAU.

During slow sample rates, i.e. less than 7ØØKHz, the IOP is theoretically capable of transferring out the new data directly after it acquired it on a word by word basis vice a block of words. This is referred to as the Toggle Mode. In this mode data is available to the AP almost immediately after the A/D conversion. For sample rates above 7ØØKHz the data will be transferred out in blocks, i.e. Block Mode, after each block is acquired and stored in buffer memory. The block transfers for high sample rates will not affect AP throughput since the time between "processing" modes is greater than the time between "start

acquisition" for those sample rates. NOTE: The user may select Block Mode at any sample rate independent of speed.

C. ADDITIONAL HARDWARE

1. Overview

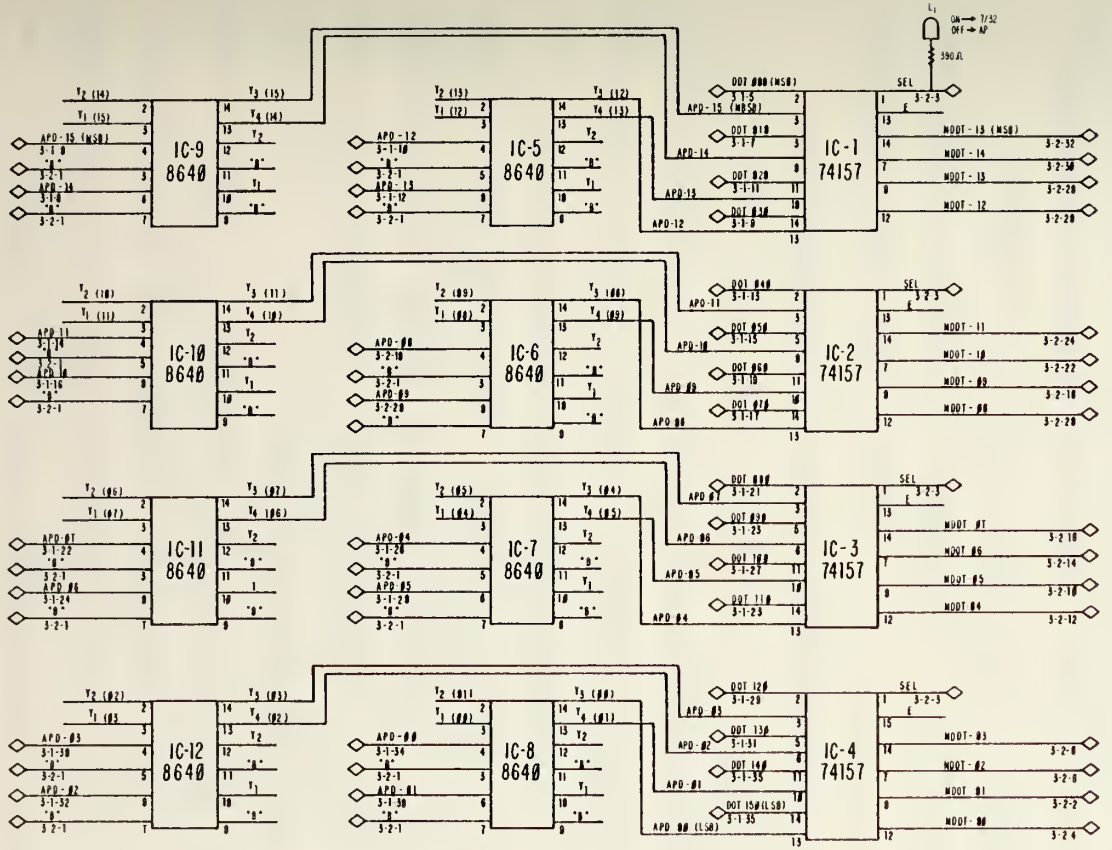
The modifications outlined in this report consist essentially of multiplexing AP/IOP-16 data and address lines with 7/32 data and address lines and providing additional control hardware.

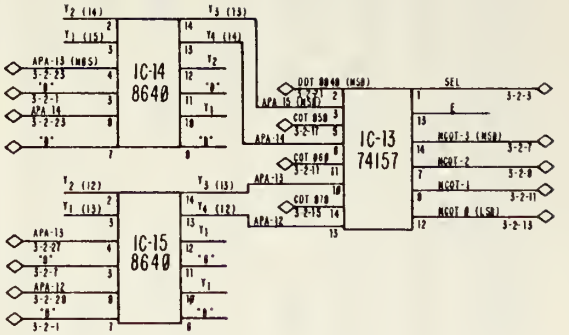
Initially, it should be noted that at the backplane of the DAU the 7/32 lines now enter at connectors one (1) and three (3) vice two (2) and three (3) as in /‾2_/. Connector (1) replaces connector (2) essentially line for line, the reason connector (1) was used was to avoid changing the wire wrap lines on the DAU bottom plane.

Essentially two new boards were added to the DAU and controls were changed on several other boards. These changes will be presented sequentially.

2. Data and Control Lines

DAU Board three (3), Figure 11, consists of multiplexed data and control lines from the AP/IOP-16 and INTERDATA 7/32. As explained in section III the IOP-16 data lines (16 each) enter IC's 5 through 12 which are 864Ø line receivers. Note that each line enters two 864Ø gates so as to invert it (see Figure 12). Within the concept of bi-directional data lines, "B" would be wired to BUSC so as to




NOTE AP DATA LINES 00,01,02, 03 AND AP ADDRESS LINES 12, 13, 14, 15 ENTER THEIR RESPECTIVE IC PINS THROUGH RESISTOR TERMINATION BELOW


AP OR 7/32 DATA AND CONTROL SELECTOR DAU BOARD # 3

Figure 11

DAU BOARD 3

enable or disable the 864Ø receiver appropriately. However, since the DAU "receives" data and addresses on these lines, "B" is wired to ground for simplicity. Should the DAU send data to the AP via these data lines, receiving the data here as it is sent has no effect. Each line must be inverted to be compatible with the 7/32 data lines that previously entered DAU board ten (1Ø), Figure 1Ø. Note that as the data lines enter board ten (1Ø) they are buffered by 74Ø4 hex inverters. Thus to be compatible the IOP-16 data must be inverted prior to the 74Ø4 hex converters on board ten (1Ø). As the IOP-16 data lines leave the 864Ø line receivers they enter IC's (1) through (4) which are 74157 QUAD one of two Data Selectors. The 7/32 data lines from backplane connector (1) also enter IC's (1) through (4). Here a selection is made as to whether the AP or 7/32 will supply data to the DAU internal registers. The selection method will be discussed later. The output of IC's (1) through (4) will be referred to as Master Data Out lines, MDOTØØ-MDOT15 (most significant, MSB). These MDOTØØ through MDOT15 lines now enter board ten (1Ø) as shown in Figure 1Ø. To conform with INTERDATA 7/32 convention, MDOT15 (MSB) becomes MDOTØØ (MSB) on board ten (1Ø).

Originally COT lines from the 7/32 were used to address the DAU internal registers. These COT lines now enter board three (3) at IC-13 at 74157 Quad one of two Data Selector. The AP must also supply four "COT" lines. It

does so in the form of address lines 12 through 15 (MSB). The AP/IOP-16 address lines enter through IC's (14) and (15) 864Ø line receivers. Note as with the data lines, each line enters two 864Ø gates so it is inverted to be compatible with logic on board eight (8), Figure 9. The 7/32 COT lines or AP address lines 12-15 are selected by IC-13. The selection logic will be discussed later. Note as the lines leave IC-13 they are Master Command Out lines (MCOT). Also note on board three (3) MCOT-3 (MSB) is MCOT Ø4Ø (MSB) on board eight (8) to conform with INTERDATA 7/32 convention.

There is a light ($L_1$) on board three (3) to indicate whether the 7/32 (on) or AP (off) is controlling the MDOT and MCOT lines respectively.

3. Control Signals and Address Lines

DAU Board (15) contains a majority of the remaining modifications. Originally the internal buffer memories were addressed by the internal Address Register (3) on board ten (1Ø). Those internal DAU Address lines now come to board (15) to multiplex with AP/IOP-16 address lines. The AP Address lines APAØØ through APA11 enter board (15) through 864Ø line receivers, IC's 1 through 6. Note again each line runs through two 864Ø gates for an inversion (see Figure 12). This results in the lines being compatible with the DAU address lines and the address line drivers on DAU board 12-1, see Figure 13. The AP address lines and DAU address lines meet at IC-9-12, 74154's, QUAD one of two Data Selectors.

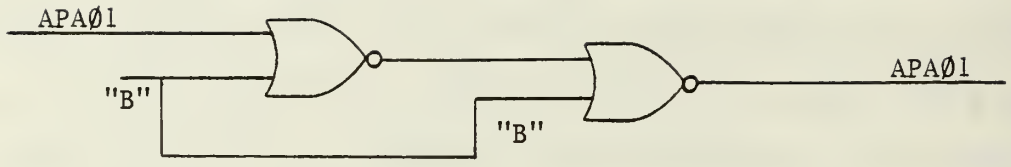



Figure 12

TYPICAL COMBINATIONAL LOGIC FOR AP DATA

AND ADDRESS LINES THROUGH 864Ø RECEIVERS ON DAU BOARD 15

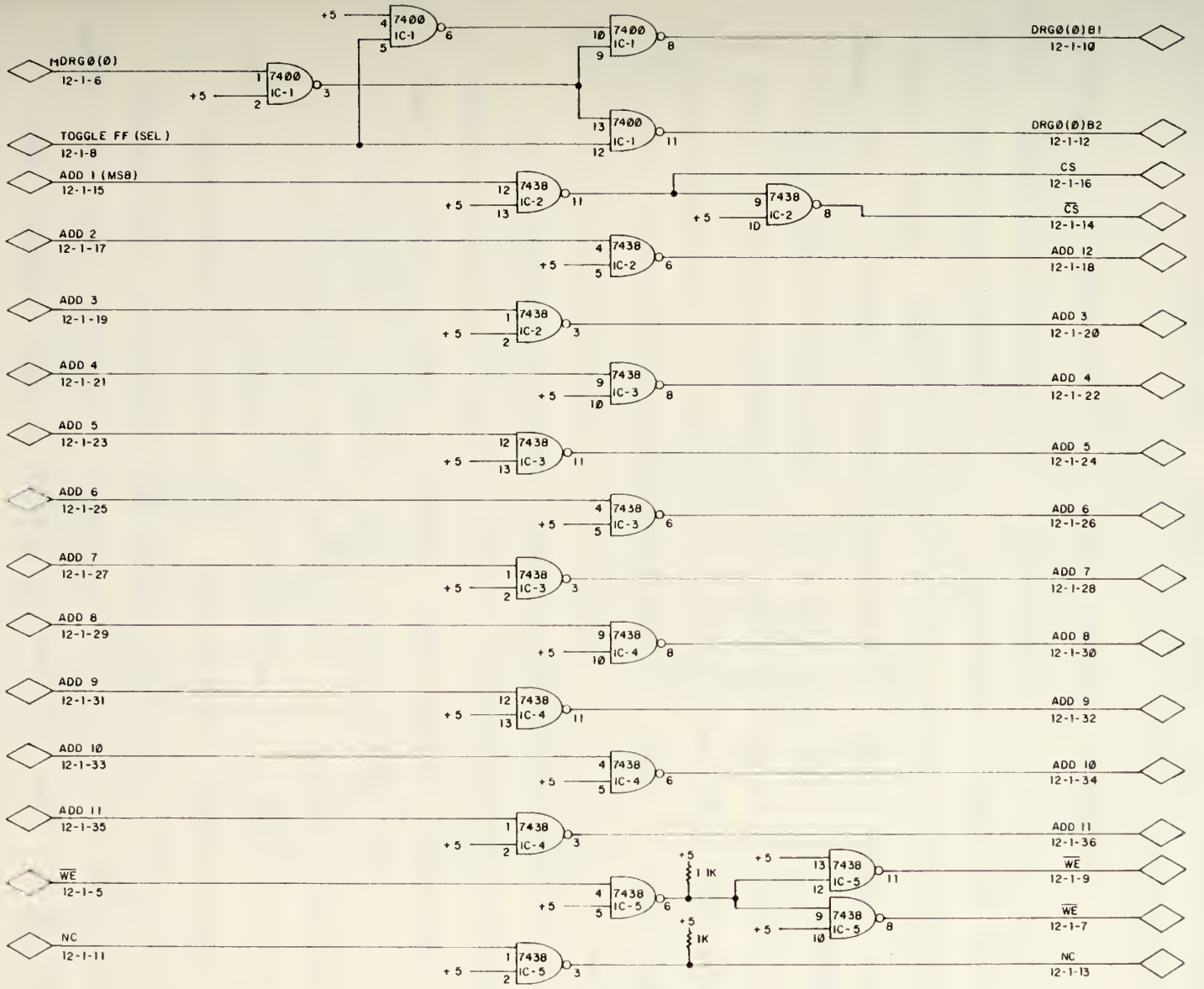



Figure 13

DAU BOARD 12-1

The line then selected addresses the buffer memories through the line drivers on board (12-1). The select line logic will be discussed later.

Probably the most important IC in these new modifications is IC-24, a 74154 one of sixteen data selector. This IC is the Master Controller, i.e. it selects which device of the AP and 7/32 will control the data lines, address lines, and control lines. Note that its five inputs are COT lines Ø4Ø-Ø7Ø and DAGØ from the 7/32. These are the same COT lines that are multiplexed with AP address lines on board three (3), however, these COT lines are not associated with MCOT lines. They are only used to address one of two locations on IC-24, i.e. outputs 6 or 7 (HEX Ø11Ø or Ø111). Due to an initial design deficiency the COT lines were not buffered by HEX inverters 74Ø4's prior to entering IC-24 as required of 7/32 lines. Hence in reality output lines 9 and 8 (HEX 1ØØ1 and HEX 1ØØØ) are used. These perform the same function as if the COT lines had been inverted prior to IC-24. If output (6) is selected by the COT lines, it puts a direct clear signal on IC-23, a D- flip-flop. IC-23 is the Select flip-flop, see Figure 14. It selects either the AP or 7/32 for control. If output (6) is selected the direct clear puts a logic Ø at Q, pin 9. Pin 9 of IC-23 then goes to switch 2, a 4 pole double-throw switch. Switch one (1) and Switch two (2) were installed on board 15 to guarantee use of the DAU under 7/32 control while

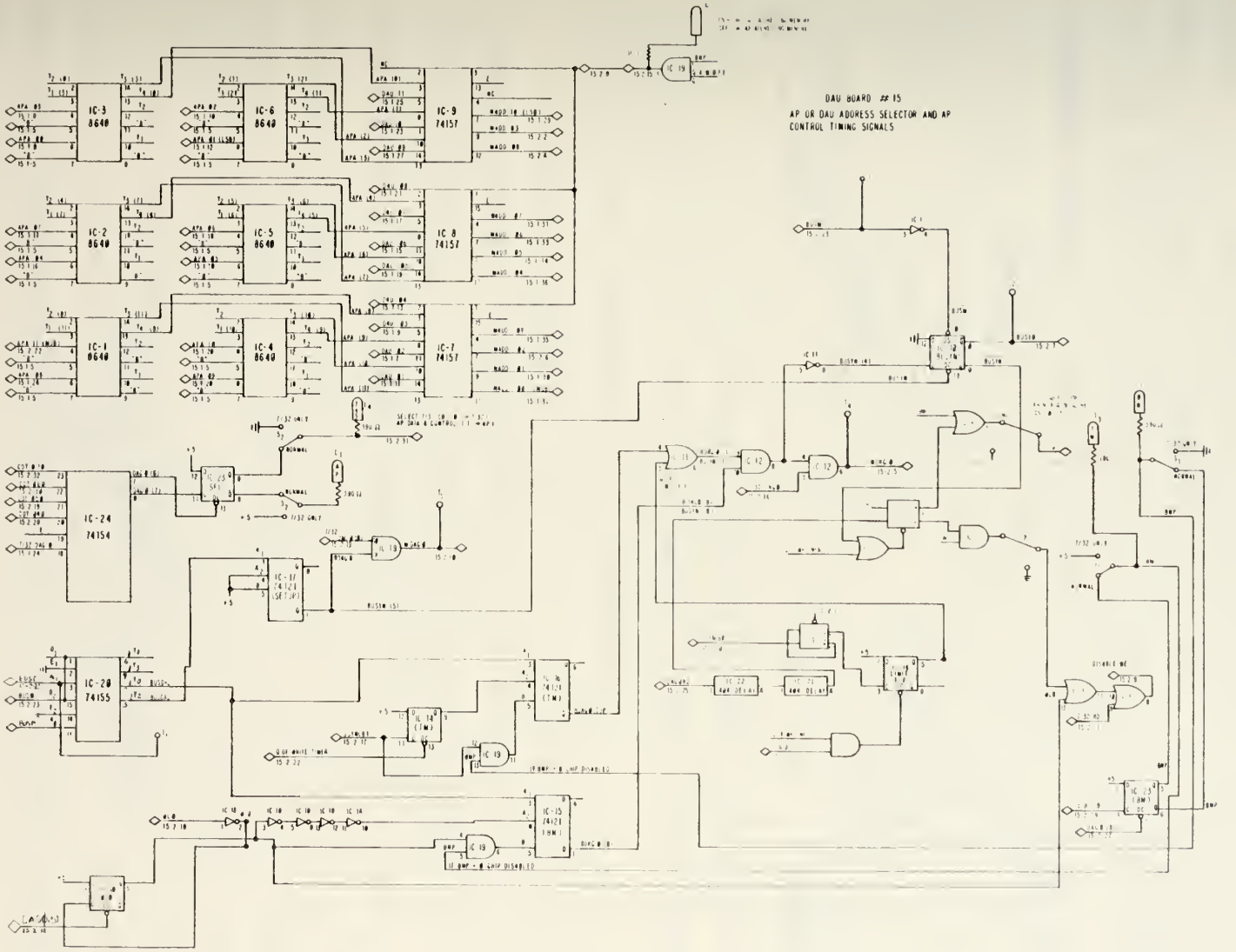



Figure 14

DAU BOARD 15

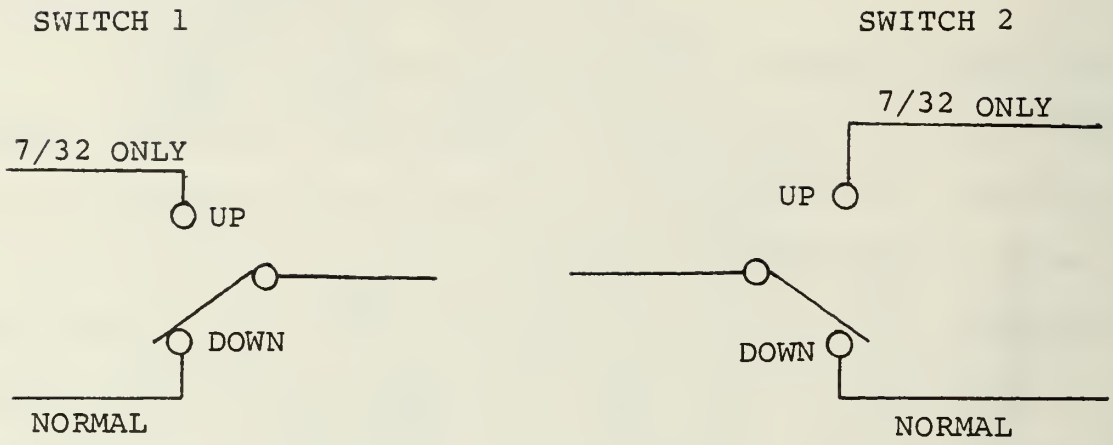



Figure 15

POSITIONS OF CONTROL SWITCHES

1 AND 2 ON DAU BOARD 15

modifications were under static test of AP control (see Figure 15). This feature allows students to exercise the DAU as discussed in references [2] and [3] and enables testing of the AP controls if the switch is toggled. One output of switch $S_2$ goes to pinout 15-2-31 and to light $L_4$. If in normal operation this output is from pin 9 of IC-23. If in 7/32 only guaranteed, the input to pinout 15-2-31 and light $L_4$ is hardwired to ground. Note this lights $L_4$ indicating 7/32 operational control. Pin 8 of IC-23 also goes to one of the poles of $S_2$. In the normal mode it outputs to $L_1$. If in the 7/32 only guaranteed mode, the output to $L_1$ is hardwired to (+5) guaranteeing $L_1$ will be off since $L_4$ would be on indicating 7/32 control.

Should address 7 (HEX Ø111) be selected by the COT lines of IC-24 a clock pulse goes into pin 11 of IC-23 the Select flip-flop. This clocks a logic (1) through to pin 9. So if $S_2$ is in the normal mode, a logic 1 (+5) at pin 9 turns off $L_4$. A logic 1 (+5) at pin 9 means a logic (Ø) (ground) at pin 8. With $S_2$ in normal mode this turns on $L_1$ indicating the AP has control. Thus it can be seen that pinout 15-2-31 (see Figure 14) indicates which device has control. This line connects to pinout 3-2-3 on board (3) to put the MDOT and MCOT selectors under 7/32 or AP control as alluded to earlier.

Two of the most important signals used in the original DAU configuration were DAGØ, Data Available Gated (active

low) as mentioned in /¯1_/ and /¯2_/. DAGØ from the 7/32 was used to setup the acquisition mode and DRGØ to read out acquired data. The only signal available with similar characteristics from the AP/IOP-16 is BUSMASTER (BUSM). Since the AP/IOP-16 has only one signal available, to be compatible with previous DAU operations it had to be capable of creating signals similar in characteristic to DAGØ and DRGØ. This imitation of DAGØ and DRGØ originates at IC-2Ø on board 15, see Figure 14. IC-2Ø is a 74155, Dual one-of-four data distributor.

BUSM enters at pin 1 and pin 15 and pin 1 of IC-2Ø as the data to be passed through the outputs to form signals representing DAGØ and DRGØ. BUSC and $\overline{\text{BUSM}}$ are used as address inputs at pins 3 and 13 respectively. If BUSC is high (+5) and $\overline{\text{BUSM}}$ is low (ground) BUSDAGØ is selected as the output at pin 5 where it is an inverted form of BUSM. If BUSC is low (ground) and $\overline{\text{BUSM}}$ is low (ground) BUSDRGØ is selected as the output at pin 7 where it is an inverted form of BUSM. The desired truth table is shown in Figure 16. With respect to BUSC and BUSM, these signals are inside the DAU after the line receivers and hence have the same logic state as internal to the AP/12ØB prior to the line drivers. NOTE: If BUSM is low (ground) BUSDAGØ and BUSDRGØ are always high (+5). For BUSC and BUSM in Figure 16, Ø = ground and 1 = +5 volts.

| $A_1$ BUSC | $A_\emptyset$ $\overline{\text{BUSM}}$ | DATA BUSM | OUTPUT 1Y2 BUSDAGØ | OUTPUT 1YØ BUSDRGØ |
|---|---|---|---|---|
| Ø | Ø | 1 | 1 | Ø |
| Ø | 1 | Ø | 1 | 1 |
| 1 | Ø | 1 | Ø | 1 |
| 1 | 1 | Ø | 1 | 1 |

Figure 16

TRUTH TABLE FOR BUSDAGØ AND BUSDRGØ

The original 7/32 signal that was used to setup the DAU into an acquisition mode or to load diagnostic data was DAGØ. This signal can be represented by the AP/IOP-16 BUSM when it forms BUSDAGØ. BUSDAGØ is the output of pin 5 of IC-2Ø. BUSDAGØ (pin 5 of IC-2Ø) goes to pin 3 of IC-17, a one shot multivibrator. As BUSDAGØ transitions high to low (+5 to ground) it fires IC-17. This firing forms a negative pulse at output $\overline{Q}$, pin 1 of IC-17. This negative pulse goes as BDAGØ to IC-19 where it "ANDS" with 7/32 DAGØ to form MDAGØ (MASTER DAGØ). MDAGØ replaced 7/32 DAGØ internal to the DAU. Note if 7/32 is active vice AP, MDAGØ is formed by 7/32 DAGØ; if AP is active vice 7/32, MDAGØ is formed by BDAGØ.

The output pin 1 of IC-17 also goes as BUSYN(S) to pin 13 of IC-1Ø, the BUSYN flip-flop. The (S) is representative of "SETUP" mode. BUSYN(S) is a negative pulse that puts a direct clear signal at IC-1Ø. This direct clear puts a "1" at pin 8 of IC-1Ø, which sends an active low signal BUSYN back to the AP. When the AP/IOP-16 receives this BUSYN low, as discussed in section III, it removes BUSM, i.e. brings BUSM to (+5) on the bus. As BUSM is brought to (+5) it is inverted by its receiver. This inversion puts a "Ø" at pin 1Ø of IC-1Ø which direct sets the BUSYN flip-flop, putting a "Ø" at $\overline{Q}$, pin 8 of IC-1Ø. This completes one cycle of the SETUP mode and the DAU is ready for another BUSDAGØ (BUSM) from the AP/IOP-16. Finally note that MDAGØ

at pinout 15-2-2Ø of board (15), Figure 15, goes to pinout 8-1-15, Figure 9, to setup the internal DAU registers. MDAGØ is routed on board 8, Figure 9, to DAGØ (1), DAGØ (2), DAGØ (3), etc., as appropriate.

BUSDRGØ is the other signal formed from BUSM at IC-2Ø pin 7, Figure 15. This signal is formed to be comparible with 7/32 DAGØ. BUSDRGØ leaves pin 7 of IC-2Ø and goes to pin 3 of IC-15 and pin 3 of IC-16, the Block Mode and Toggle Mode one shot multivibrators respectively.

4. Block Mode Read

The Block Mode, as alluded to earlier, is used for high sample rates (can be used for low also < 7ØØ KHz) to transfer data (read) to the AP from the DAU by "blocks" after a block is acquired. The Toggle Mode is used for low sample rates only to DMA transfer data to the AP on a word by word basis as it is acquired. The Toggle Mode cannot be used above 7ØØ KHz, theoretically, because of timing required in the DMA transfer compared with high speed conversion time of the A/D converters. These two modes will be explained separately.

Prior to commencing an acquisition mode, the user must determine how the data is to be read, i.e. Block Mode or Toggle Mode. These modes are selected at IC-23, the BM flip-flop. During the SETUP mode just prior to acquisition, the user sends out a DAGØ(9) pulse or a DAGØ(8) pulse from pin-outs 8-1-34 or 8-1-36, Figure 9 respectively. If DAGØ(9)

is sent pin 3 of IC-23 clocks a "1" at pin 5, Q, the Block Mode Point (BMP). Note this output goes to switch $S_1$. When in the 7/32 only guaranteed mode $S_1$ outputs a (+5) to $L_3$ to turn it off, $L_3$ is the Toggle Mode; $S_1$ outputs a (ground) to $L_2$ to turn it on, $L_2$ is the Block Mode light. The 7/32 "knows" only Block Mode and hence cannot use Toggle Mode ($\overline{BMP}$). If $S_1$ is in the normal position, the AP/IOP-16 can select either BMP or $\overline{BMP}$ by sending DAGØ(9) or DAGØ(8) respectively. Note when BMP is a "1" $\overline{BMP}$ is a "Ø". This will be important in enabling and disabling IC-15 and IC-16.

In the Block Mode the AP/IOP-16 must wait to DMA transfer a "block" of data until the block is fully acquired. The signal that indicates completion of acquisition is WCØ at pinout 15-2-18, Figure 15. WCØ is a status signal from board 8 pinout 8-2-9, Figure 9. WCØ is high (+5) during acquisition and at completion goes low (ground). This high to low transition is inverted by IC-18 pins 1 and 2 on board 15, Figure 15. This inversion forms a low to high transition, $\overline{WC\emptyset}$. $\overline{WC\emptyset}$ is used to clock pin 3 of IC-1Ø, the WCØ flip-flop. Note prior to clocking IC-1Ø had been direct cleared by the "AND" of DAGØ(5) with BUSC at IC-19. This "AND" creates an active low pulse at pin 3 of IC-19 to direct clear IC-23 whenever DAGØ(5) is active or BUSC is low at pin 13 of IC-2Ø. The purpose of this clearing is to insure a "Ø" at $\overline{Q}$, pin 5 of IC-23, prior to the end of an acquisition block, i.e. before WCØ goes low. A review of reference (2)

indicates that DAGØ(5) is the last signal in the SETUP mode, appropriate for clearing IC-23 prior to reading. The importance of having a "Ø" at Q pin 5 of IC-23 prior to $\overline{WCØ}$ clocking at pin 3 is to insure a "1" passes to Q, pin 5 after clocking. When Q, pin 5 of IC-23, goes to a "1" state it "ANDS" with BMP at IC-19. Note BMP was previously set to a "1", if not, pin 6 of IC-19 would be disabled. With a "1" at pin 5 of IC-19, pin 6 of IC-19 will follow the input at pin 4 of IC-19. Thus when Q, pin 5 of IC-1Ø, goes to a "1" state it puts pin 6 of IC-19 to a "1" state and this fires IC-15 for the first time and data is read. Note pin 5 of IC-15 will stay in a "1" state until either BMP goes low or WCØ flip-flop is direct cleared. Also, as Q at pin 5 of IC-1Ø went high, a delayed high was placed on pin 4 of IC-15, a condition required for the initial triggering. Again if Q of WCØ flip-flop goes low, a delayed "Ø" will be placed on pin 4 of IC-15 enabling pin 5 of IC-15 to initiate the first trigger. Successive triggering is enabled by BUSDRGØ at pin 3 of IC-15. As IC-15 is fired, a negative pulse is sent at pin 1 of IC-15 (BDRGØ(B)) where (B) is associated with Block Mode. Pin 1 of IC-15 goes to pin 1Ø of IC-12 where BDRGØ(B) (also BUSYN(B)) "ANDS" with BDRGØ(T) (also BUSYN(T)). When BDRGØ(B) is active, BDRGØ(T) will always be in a "1" state and vice versa. Thus the output, pin 8 of IC-12 follows the active input. Pin 8 of IC-12 goes to pin 4 of IC-12 where it "ANDS" with 7/32 DRGØ to form MDRGØ.

MDRGØ follows the active input, i.e. if 7/32 is active, BDRGØ(B) and BDRGØ(T) are "1"; if AP is active, 7/32 DRGØ is a "1". Pin 8 of IC-12 is also inverted at pins 5 and 6 of IC-11 to form a signal BUSYN(A). BUSYN(A) is a clock signal to clock a "1" to $\overline{Q}$, pin 8 of IC-1Ø. This "1" goes to the AP as BUSYN and remains a "1" until the AP brings BUSM to (+5) which is inverted at its receiver to direct set pin 1Ø of IC-1Ø removing BUSYN in the "handshake" process and ready the AP and DAU for another cycle.

5. Toggle Mode Read

The Toggle Mode design is considerably more complex than the Block Mode. As in the Block Mode, selection of Toggle Mode must be made prior to commencement of an acquisition scheme. With the AP in control, a DAGØ(8) is sent out just prior to the DAGØ(5) that starts acquisition. DAGØ(8) comes from board eight (8) onto board (15) at pinout 15-2-27, where active low pulse proceeds to apply a direct clear signal at pin 1 of IC-23. This direct clear puts a "Ø" at Q, pin 5 of IC-23 and a "1" at $\overline{Q}$, pin 6 of IC-23. The "Ø" at Q and "1" at $\overline{Q}$ turns on the Toggle Mode light, $L_3$, and turns off the Block Mode light, $L_2$, respectively (Figure 15). Note again, if hardwired to 7/32 only operation at $S_1$ the Toggle Mode light is off and Block Mode on.

In the Toggle Mode, the design was for use under 7ØØKHz since the DAU could acquire and not theoretically affect AP processing at this rate and slower rates.

The last signal sent to set up the DAU to acquire data is DAGØ(5). As seen on board 8, Figure 9, this signal sets the internal control register of the DAU, to acquire data. Now as the DAU acquires a word of data and stores it in Buffer Memory, in the Toggle Mode, the AP will read out that same word prior to the next word acquisition. Thus the AP and DAU "toggle" between an acquisition and a read versus acquiring a "block" and reading a "block". As mentioned earlier (Section III) the DMA timeout can be adjusted to suit the user's needs.

The theory behind the Toggle Mode design is that the AP/IOP will set up the DAU using BUSDAGØ signals and after DAGØ(5) is generated the AP/IOP will immediately send out a BUSDRGØ signal waiting to read the first acquired word. As BUSDRGØ goes to a low level, it puts a "Ø" on pin 3 of IC-16, the Toggle Mode one shot multivibrator. Note for the one shot, IC-16, to fire in this configuration, pin 4 must also be low, a "Ø", and pin 5 must be brought from ground ("Ø") to positive (+5). A "Ø" is put at pin 4 by the Toggle Mode flip-flop, IC-14. As a word is acquired, the write timer IC-12 on board 16 fires, putting a positive pulse at Q, pin 6 of IC-12 board 16, and a negative pulse at $\overline{Q}$, pin 1 of IC-12 board 16 (see Figure 17). This negative pulse enters board 15 at pinout 15-2-22 and goes to three different IC gates, i.e. IC-12, IC-13, IC-14. At IC-14 $\overline{Q}$ of the Write Timer is a negative pulse that is used to direct clear, i.e.

put a "Ø" at Q pin 9 of IC-14. This effectively puts a "Ø" at pin 4 of IC-16 board 15.

The Toggle Mode one-shot, IC-16, is now set up for a trigger. With pin 3 low and pin 4 low, a ground to positive transition at pin 5 will fire IC-16. This ground to positive transition is enabled by the signal SSYNCBØ(1) /‾2‾/. SSYNCBØ(1) is a negative pulse that enters board 15 at pin-out 15-2-17. The trailing edge of the pulse clocks IC-14 at pin 3 and the high to low to high transition brings the output pin 11 of IC-19 from high to low to high. This latter transition fires the Toggle Mode one-shot. Conveniently, SSYNCBØ(1) also clocks pin 11 of IC-14 which puts a "1" at Q, pin 9 of IC-14 and effectively at pin 4 of IC-16 to put it in the proper state for the next triggering. Note the propagation delay through IC-14 is sufficiently greater than that through IC-19 to allow the initial firing above.

Since DAU loads its buffer memory in parallel, but the AP/IOP is capable of reading only one channel of data at a time /‾1‾/ and /‾2‾/, the Toggle Mode design must insure there are two read (BDRGØ) pulses before the next acquisition write pulse. Note from the above discussion the SSYNCHBØ(1) pulse has created a "1" at pins 4 and 5 of IC-16. Thus to obtain a pulse at $\overline{Q}$, pin 1 of IC-16, there must be a positive to ground transition at pin 3 of IC-16. This positive to ground transition results from the BUSDRG signal. Note that the BDRGØ(T) pulse creates a BUSYN signal to handshake with

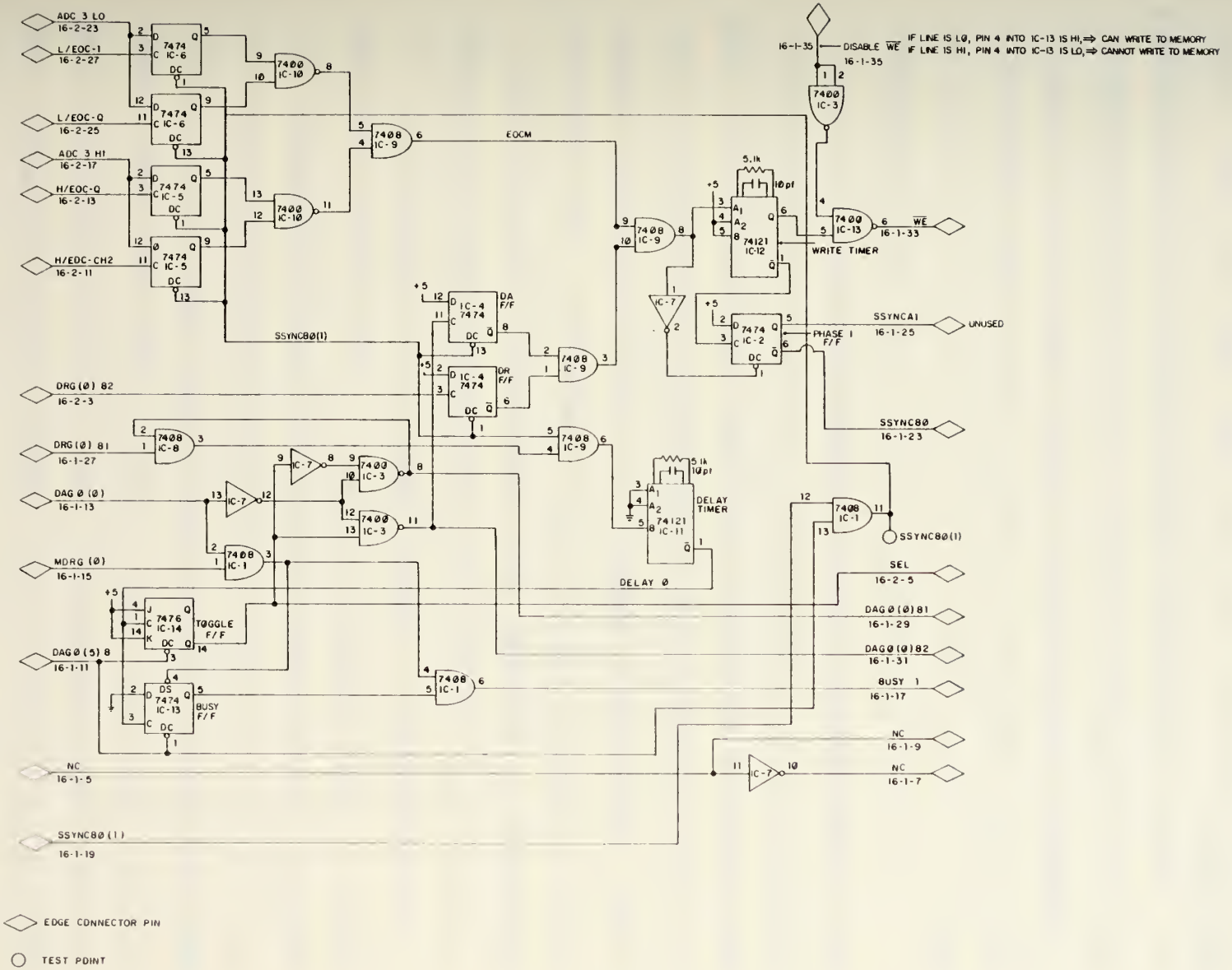



Figure 17

DAU BOARD 16

the AP/IOP in a similar fashion to that of BDRGØ(B) in the block mode.

There are two more important points to discuss before leaving the Toggle Mode design: 1) How to obtain two and only two read pulses from the AP/IOP between word acquisitions; 2) How to avoid a read pulse at an inappropriate time.

The user will always want at least two read pulses after a word acquisition, so the real problem is to insure not more than two read pulses occur after a word acquisition. This problem is handled by the limit flip-flop, IC-14. From $\overline{1}$ and $\overline{2}$ and analysis of DAU board 16, Figure 17, it is seen that two read pulses, i.e. MDRGØ, create one SSYNCBØ pulse. A SSYNCBØ pulse is also created upon word acquisition. The SSYNCBØ pulse comes on to board 15 at pin out 15-2-1Ø and goes to pin 3 of IC-25. This SSYNCBØ signal is divided by two at Q, pin 5 of IC-25. Thus every other SSYNCBØ creates a level change at Q, pin 5 of IC-25. To insure IC-25 starts in the proper state it is preset by a DAGØ(5) pulse at pin 4 of IC-25. The ground to positive level change created by IC-25 is used to clock pin 3 of IC-14, the LIMIT flip-flop. This clocking puts a "1" at Q, pin 5 of IC-14. Note previously Q, pin 5 of IC-14, was at a "Ø" being direct cleared by the DAGØ(5) pulse or the pulse from $\overline{Q}$ of the WRITE TIMER, IC-12 on board 16. Thus Q, pin 5 of IC-14, was in a "Ø" state while the two read pulses were

active. When pin 3 of IC-14 is clocked a "1" is put at Q, pin 5. This "1" "ORS" with the signal from the Toggle Mode one shot at IC-13. Since pin 5 of IC-13 is a "1", the user is guaranteed a "1" at pin 6 of IC-13. This insures a "1" at pin 9 of IC-12 (note pin 1Ø of IC-12 is a "1" because Block Mode is not is use). Thus no more MDRGØ pulses can be created and the user has only two read pulses for each word acquisition.

The second problem was to avoid a read pulse at an inappropriate time. In the Toggle Mode the only appropriate time to read a word is immediately after the word has been written into memory. This time occurs immediately after the write enable pulse ($\overline{WE}$) on IC-13 board 16 Figure 17. From $\overline{1}$ and $\overline{2}$ it should be noted that a $\overline{WE}$ pulse also occurs after every second read pulse (DRGØB2). It is specifically this $\overline{WE}$ pulse that must be disabled so as not to affect the Toggle Mode. This $\overline{WE}$ pulse is eliminated as follows. The $\overline{WE}$ pulse is disabled through pinout 15-2-9 by many possible signals through IC-13 as can be seen on board 15 Figure 15. One input to IC-13 at pin 12 is a signal through $S_2$ from pin 3 of IC-12. When $\overline{BMP}$ is a "1" pin 3 of IC-12 follows the input at pin 1. The input at pin 1 to IC-12 is pin 8, $\overline{Q}$, from IC-25. IC-25 is clocked at pin 11 by a delayed version of DRGØB2. Thus while pin 8 of IC-25, $\overline{Q}$, is in a "1" state, the disable $\overline{WE}$ line at pinout 15-2-9 is high and the buffer memories cannot be written. $\overline{Q}$, pin 8

of IC-25, stays in a "1" state until clocked by the delayed version of DRGØB2, so the $\overline{WE}$ pulse is eliminated. Note that $\overline{Q}$, pin 8 of IC-25, was put in a "1" state by the signal $\overline{Q}$ of the write times. It was this signal that originally wrote good data into memory during acquisition.

Another signal of interest in the Toggle Mode occurs at pinout 15-2-13. Again, from $\overline{1}$ and $\overline{2}$, it is the SSYNCB(2) signal on board 8 that updates the DAU word count and address registers. This updating must be eliminated until after the acquired word has been read. In the Block Mode these registers are updated after each word acquisition so data is stored in appropriate addresses and the word count is decremented. However, in the Toggle Mode if the address and word count are updated prior to the read cycle, undesireable data will be read. The word count and address registers are disabled via pinout 15-2-13. This connection goes onto board 8 at pinout 8-2-11, to two NAND gates, 7438 drivers. The word count and address registers are enabled if output pins 3 and 6 of IC-1Ø are in a "Ø" state. For this to occur inputs 1, 2, 4 and 5 must all be in a "1" state. Note that in the "7/32 only mode", $S_1$ hardwires 8-2-11 and hence inputs 1 and 4 to a 1. In the "normal" mode, $S_1$ allows the output pin 3 of IC-26 to pass to pinout 8-2-11. The output, pin 3 of IC-26 is fed by inputs 1 and 2, BMP and Q, pin 9 of IC-25 respectively. In the Toggle Mode, BMP is a "Ø" thus pin 3 of IC-26 fo-lows pin 1 input. So when Q, pin 9

of IC-25 is a "Ø" SSYNCB(2) cannot update the word count and address registers. This output Q, pin 9 of IC-25 is a "Ø" when cleared by $\overline{Q}$ of the WRITE TIMER, IC-12 on board 16. Thus immediately after a word is written into buffer memory, the address and word count cannot change until the word is read out, i.e. after the second read DRGØB(2) pulse. This is important because now the AP/IOP need not generate address to read data from buffer memory, it need merely follow the address the DAU writes.

For the convenience of monitoring signals and status there are five test points and five lights on board 15. The test points monitor the following signals: $T_1$ → BUSM, $T_2$ → BUSYN, $T_3$ → BUSC, $T_4$ → MDRGØ, $T_5$ → MDAGØ. The lights indicate status as follows: $L_1$ → AP/IOP in control, $L_2$ → Block Mode, $L_3$ → Toggle Mode, $L_4$ → 7/32 in control, $L_5$ → 7/32(on) or AP/IOP(off) addressing buffer memory. On board 3, $L_1$, indicates which device controls the data lines, i.e. 7/32(on) or AP/IOP(off) (see Table 3).

The control (BUSC, BUSM, BUSYN) signals enter the DAU on board 12-2 in a configuration the same as Figure 18. BUSM and BUSYN transit the usual driver/receiver logic compatible with interface design. BUSC must drive many more gates. To increase its fanout, BUSC was sent separately to various locations as shown in Figure 18. The BUSC lines are also driven by standard drivers as shown in Figure 18.

TABLE III

TEST POINTS AND LIGHTS ON DAU BOARD 15

| TEST POINTS | LIGHTS |
|---|---|
| $T_1$ → BUSM | $L_1$ → ON → AP IN CONTROL |
| $T_2$ → BUSYN | $L_2$ → ON → BLOCK MODE |
| $T_3$ → BUSC | $L_3$ → ON → TOGGLE MODE |
| $T_4$ → MDRGØ | $L_4$ → ON → 7/32 IN CONTROL |
| $T_5$ → MDAGØ | $L_5$ → ON → 7/32 ADDRESSING BUFFER MEMORY |
| | $L_5$ → OFF → AP ADDRESSING BUFFER MEMORY |

NOTE: $L_1$ and $L_4$ cannot be on simultaneously

$L_2$ and $L_3$ cannot be on simultaneously

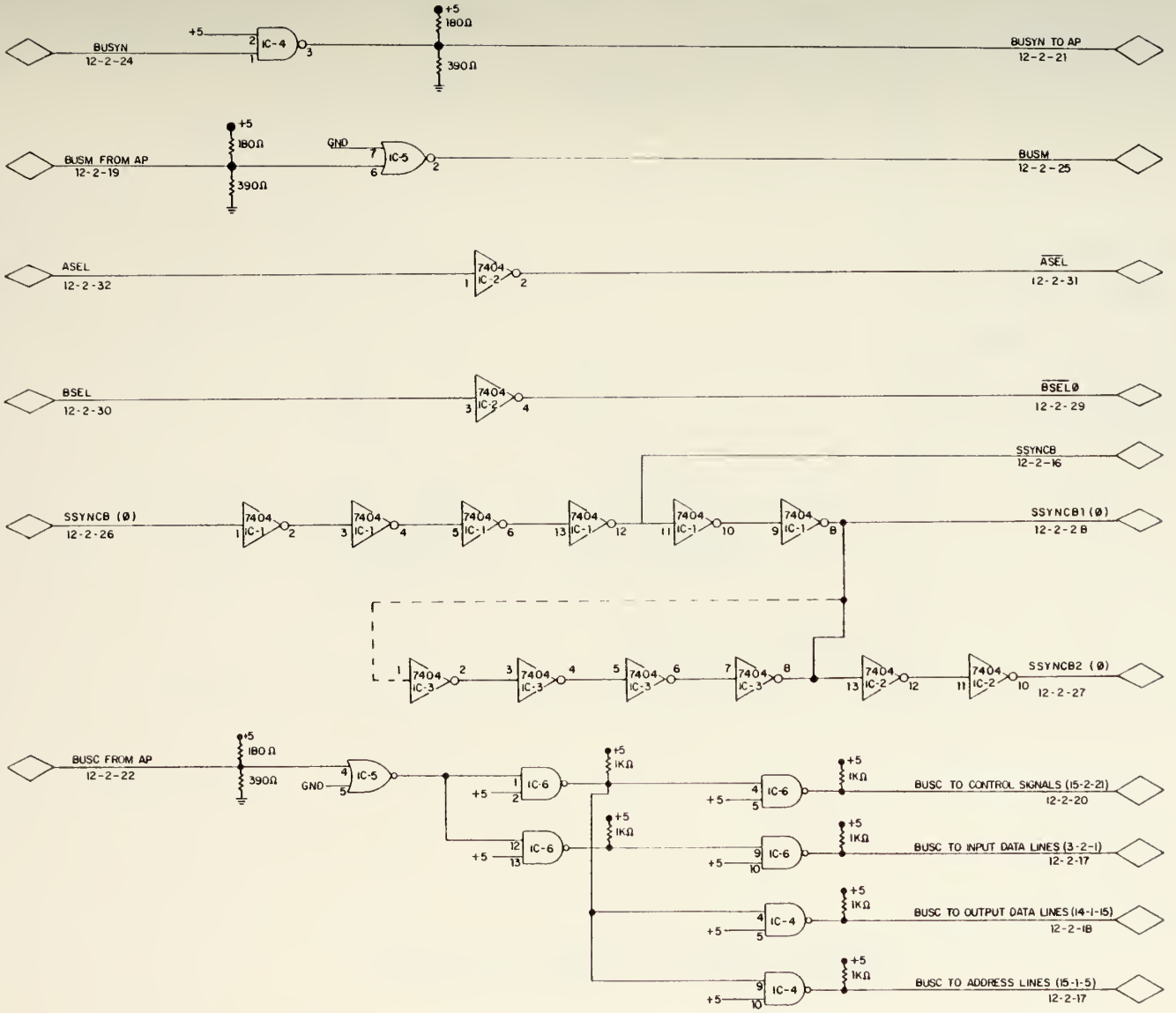



Figure 18

DAU BOARD 12-2

Figures 19 and 2Ø show the Block Mode and Toggle Mode timing diagrams respectively.

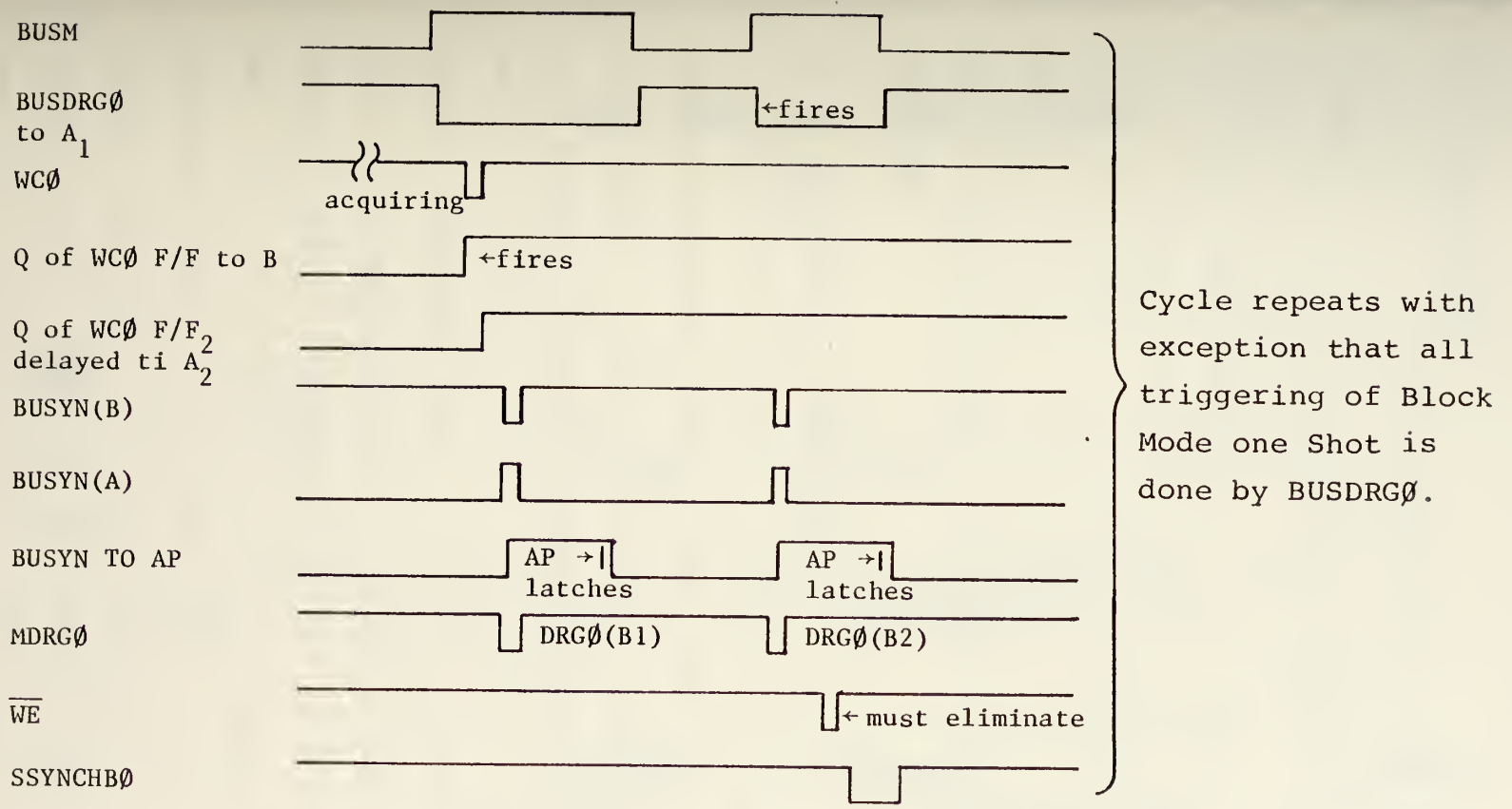



Figure 19

BLOCK MODE READ TIMING DIAGRAM

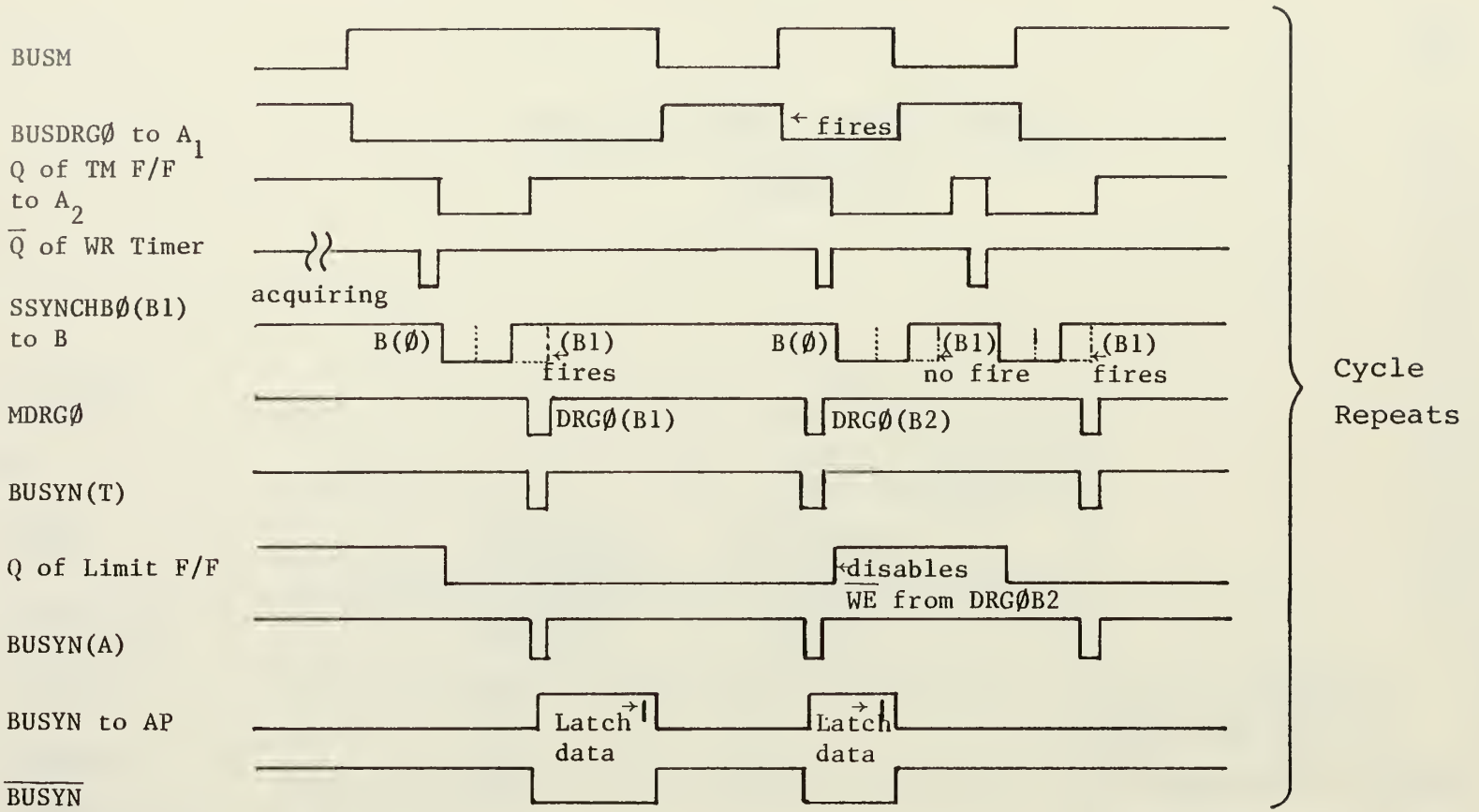



Figure 2Ø

TOGGLE MODE READ TIMING DIAGRAM

## V. FLOATING POINT SYSTEMS AP-12ØB (AP) SIMULATOR

### A. INTRODUCTION

As with any device designed to operate at computer speeds, action takes place in the DAU/IOP interface at speeds which make direct observations nearly impossible. To initially test and design, it is desirable to make essentially "static" tests at speeds observable to the human eye. To this end, and to simulate AP control of the DAU the AP simulator was constructed. When connected to the DAU in place of the AP the simulator effectively represents the AP.

### B. AP SIMULATOR OPERATION

The AP Simulator circuit shown in Figure 21 consists of control signals, bidirectional data lines, and address lines to represent the AP. The control signal BUSC is represented by a single pole double throw switch. One side of the switch is tied to +5 volts the other to ground. The output goes to the data line IC's in the simulator, the BUSC light and to the backplane for transfer to the DAU. The control signal BUSM is represented by a 3 pole double throw switch. Two poles go to debounce Logic as shown in Figure 21. The third pole goes to the BUSM light. The output of the debounce logic goes to the DAU via the ribbon cable. The control signal BUSYN is represented by a light, there is no need for a switch since all transfers will be under AP

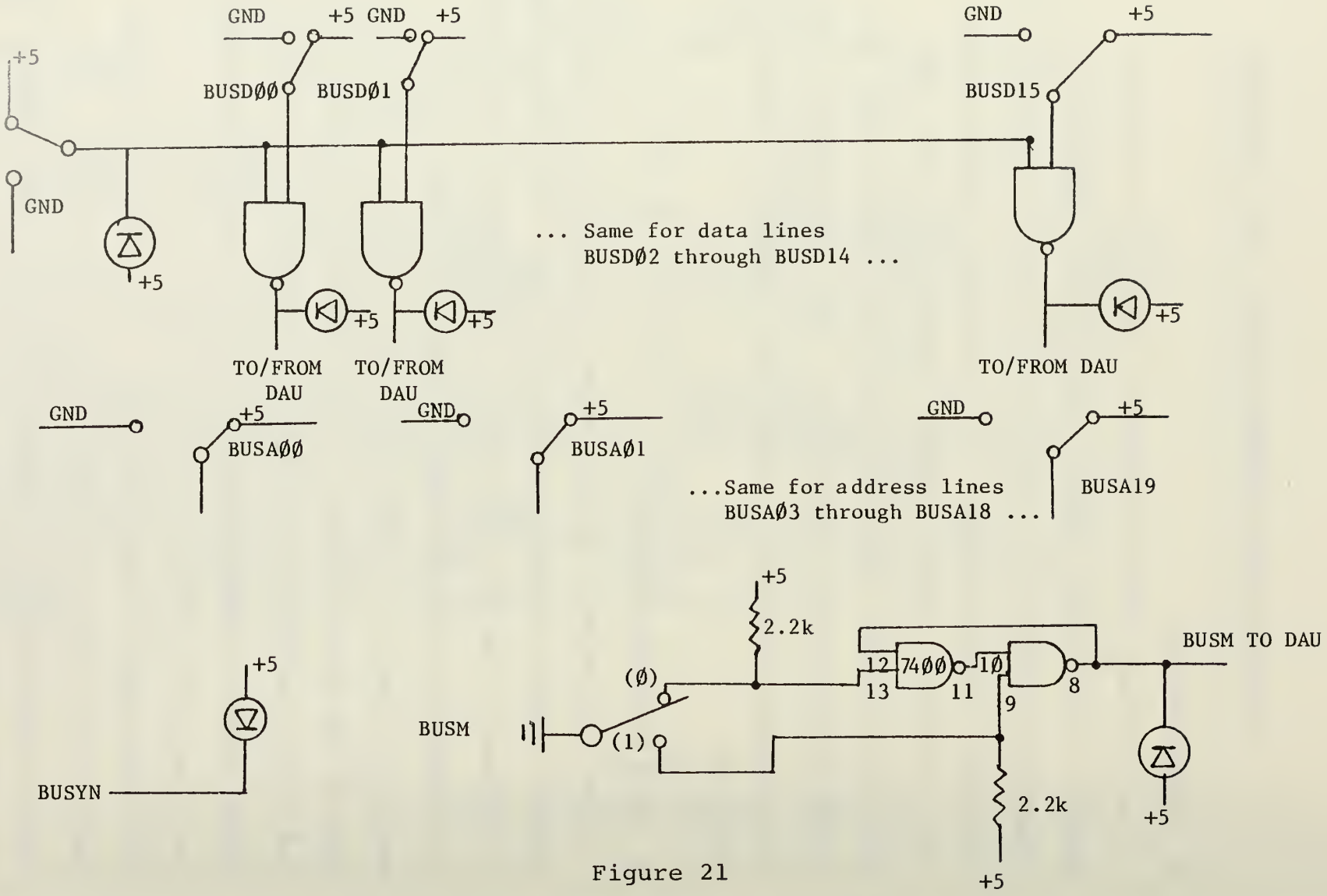



Figure 21

AP SIMULATOR CIRCUIT SCHEMATIC

control the DAU will always be sending back BUSYN. The data lines are represented by single pole double throw switches and 74ØØ Nand gates. One side of the switch is ties to +5 volts and the other is tied to ground. The output of the data switch is one input to a 74ØØ nand gate; the other input is a line from BUSC. The output of the nand gate goes to the respective data line at the backplane and the respective light on the front panel. The lights (LED's) have internal current limiting resistors. Note when BUSC switch is up a +5 is applied to one input of each nand gate. Thus the output will follow the other input, i.e. the data line. Note the output in this case can source approximately 4ØØ microamperes. When BUSC switch is down one input to each gate is at ground, meaning the output will always be a Logical "1". In this case the output can sink 16 miliamperes. The result is a representation of bidirectional data lines, direction dependent on BUSC. The address lines are represented by single pole double throw switches. One input is tied to +5 the other is ties to ground. The output goes directly to the back plane of the simulator. All these lines are summarized in Table IV.

## C. USE OF AP SIMULATOR

The AP Simulator can be used independent of or in conjunction with the DAU Tester [2] to control the DAU. If control is passed to the AP Simulator (see Section IV-C) then it can set up the DAU to acquire data and ultimately read that data as if the AP were actually reading data.

TABLE IV

AP SIMULATOR SUMMARY

I. BUSC - Controls Flow of Data

HI (Light On) at Simulator → Send Mode BUSC will be HI in DAU

LO (Light Off) at Simulator → Receive Mode BUSC will be LO in DAU

II. BUSM - HI (Light On) at Simulator → Transition ↑ → Transition ↑ in DAU Signal Active HI to DAU

III. BUSYN - HI (Light On) at Simulator → Transition ↓ in DAU Signal Active HI in DAU

IV. DATA LINES - HI (Light On) → 1 Sent or Received
LO (Light Off) → Ø Sent or Received

V. ADDRESS LINES - UP ↑ → 1 Sent to DAU Register
DN ↓ → Ø Sent to DAU Register

NOTE: (1) AP-12ØB Address Line Ø is Always LO

(2) AP Simulator Lines 18, 19 N/A

| | SWITCH | LIGHT | CABLE | AFTER LINE RCVR IN DAU |
|---|---|---|---|---|
| BUSC | UP | ON | LO | HI |
| | DN | OFF | HI | LO |
| BUSM | UP | ON | LO | HI |
| | DN | OFF | HI | LO |
| BUSYN | N/A | ON | LO | HI |
| | | OFF | HI | LO |
| DATA | UP | ON | LO | HI |
| | DN | OFF | HI | LO |
| ADDRESS | UP | N/A | LO | HI |
| | DN | | HI | LO |

For example, to set up the registers in the DAU use address lines 12-15 to address the appropriate DAU registers, i.e. range register #1 is addressed by putting line 12 high (HEX 1). Frequency register #2 is addressed by putting address line 13 high (HEX 2). Word count #3 is addressed by putting address lines 12 and 13 high (HEX 3). Word count data is passed over the 16 data lines in conjunction with addressing register 3. Address register #4 in the DAU is addressed by setting AP address line 14 high (HEX 4). Simultaneously the starting address is loaded from the data lines. The control register, #5, is addressed by setting AP address lines 14 and 12 high (HEX 5). Simultaneously the control function is set by appropriate data on the data lines, i.e. high speed analog to digital conversion, low speed analog to digital conversion, diagnostic write, etc. Note also the AP simulator uses a block mode and toggle mode with respect to reading (see Section IV-C). These mode are set by putting AP address lines 15 and 12 (HEX 9) or 15 along (HEX 8) high respectively. In all cases the appropriate register is addressed and data strobed into the DAU by first addressing the register, setting the data, put BUSC switch up (send mode) and enabling BUSM (bring switch down). Note that the data is latched into the DAU at the proper register when the BUSYN light goes on at the AP Simulator panel. To remove the BUSYN light, bring the BUSM switch up again. This process is continued until the appropriate re-

gisters are loaded with the desired data.

The AP simulator can be used with the DAU tester to statically check an acquisition of data and a block mode read as follows. Initially use the DAU Tester. Set the DAU word count register to ØØØ8 HEX. This implies we will load in eight words (note one word goes into Channel I and Channel II by pushing the DAGØ switch twice). Set the DAU address register to ØØØØ HEX. Set the DAU control register to 7/32 WR ØØØ8 HEX and the DAU is set up to receive diagnostic data. Now load the eight desired words by appropriately selecting the data lines. As the word count register counts down and hits ØØØØ, a signal is set to transfer control of the buffer memory address lines from the DAU tester to the AP simulator. This can be noted by observing light (5) on DAU Board #15, it should be on when the 7/32 is addressing buffer memory and off when the AP is addressing buffer memory. The word count equals zero status can also be observed by monitoring the status in line (7).

When control of the buffer memory address lines switches from 7/32 to the AP the data previously written in can be read out as follows. Set the BUSC switch down for receive mode. Next set the desired location in memory to read with the address lines. In this example start at ØØØØ and work to address ØØØ8 using address lines Ø through 11. The data read will show on the data lines and should correspond to what was loaded by the DAU tester. To read a word from

channel one drive the BUSM switch down, the data will then appear and the BUSYN light should come on. Repeat without changing address to read from channel two. This process is summarized in Table V.

TABLE V

AP SIMULATOR OPERATION

| Mode | | Address Lines Switches | Data Lines Switches | BUSC Switch | BUSM Switch | Comments |
|---|---|---|---|---|---|---|
| SETUP DAU | 1 | 12 UP | ØØØ6 HEX | UP | DN | When BUSYN lights data set in DAU, bring BUSM up to remove BUSYN |
| | 2 | 13 UP | 2ØØØ HEX | UP | DN | " Sets in 2ØØKHz |
| | 3 | 12,13 UP | Ø4ØØ HEX | UP | DN | " Sets WC to 1Ø24 |
| | 4 | 14 UP | ØØØØ HEX | UP | DN | Sets ADD to ØØØØ |
| | 5 | 14,15 UP | ØØ22 HEX | UP | DN | High Speed ACQ |
| | | | ØØ11 HEX | UP | DN | Lo Speed ACQ |
| BLOCK MODE READ | 1 | Load data with DAU Tester as described in text and reference (1). | | | | |
| | 2 | To desired location | observe | DN | DN | When BUSYN lights a word is read to remove BUSYN, bring BUSM high. |

## VI. AP SOFTWARE

Programming the AP-12ØB in Array Processor Assembly Language (APAL) is discussed in references [4] - [7]. In particular references [4] and [5], offer examples of programming techniques. The programmer inexperienced in assembly language will find a great deal of time required to diagnose and understand these manuals. References [6] and [7] list the language commands used by the AP-12ØB assembler. However, few examples are noted and again the uniniated programmer will find initial efforts very cumbersome but not impossible.

A sample program that can be used to set up the DAU in an acquisition mode is listed in Appendix A.

# VII. CONCLUSION

The interface between the Data Acquisition Unit and the AP-12ØB Array Processor has been designed and constructed for digital control. The interface has passed static testing satisfactorily. The interface has demonstrated the ability to command the DAU to acquire data under software program control. Implementation of this interface will enable further increases in efficiency in digital spectrum analysis performed by the SATCOM Signal Analyzer.

# APPENDIX A

## SOFTWARE PROGRAM

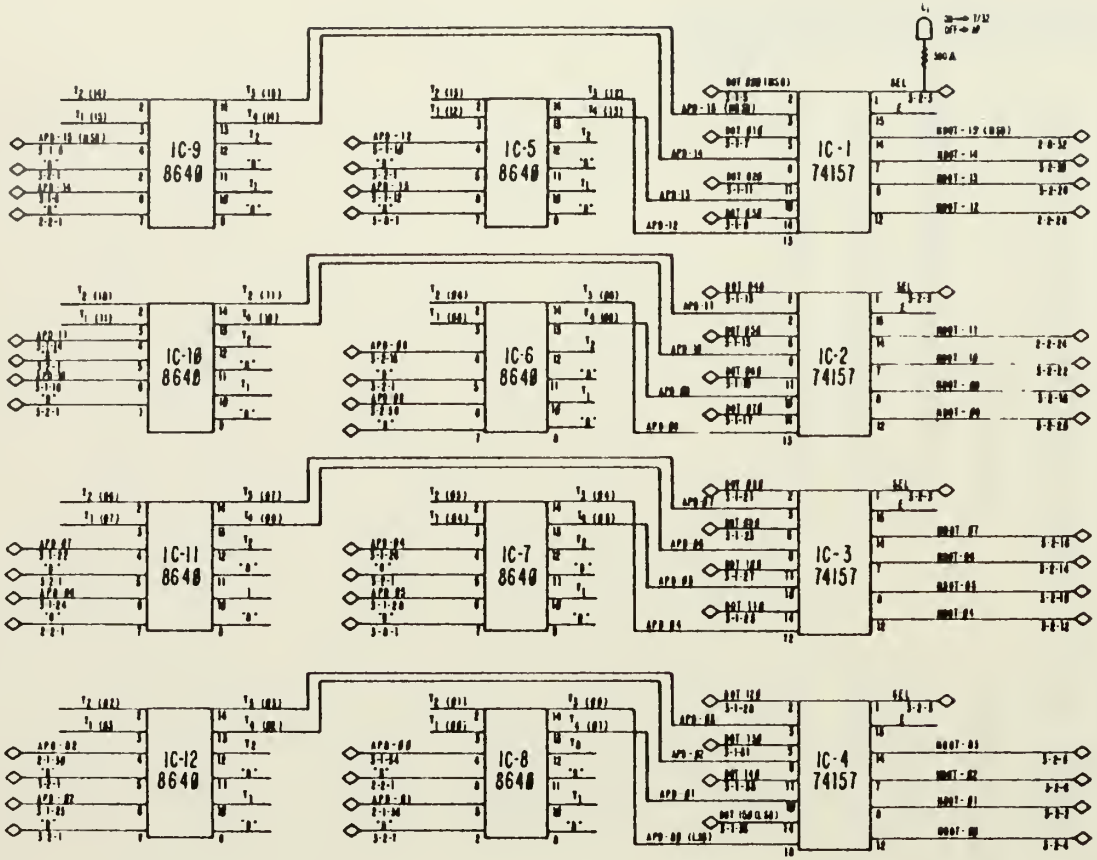
```
C
C                          SIMUL1
C
C
C     PROGRAM TO TEST AP/IOP DATA XFER TO DAU
C
C       INTEGER WC2V,APMA2V,HMA2V,CLT2V
        INTEGER*2 IVAL,IREG,DAUTO
C
C
C     SET UP DAU FOR AP CONTROL
C
C
        WRITE(6,600)
600     FORMAT(/,'INPUT D; INPUT REG NR; 6=7/32, 7=AP,
       FORMAT(I1,1X,I1)')
        READ (5,500) IVAL, IREG
500     FORMAT(I1,1X,I1)
        CALL DAUREG(IVAL,IREG)
C
C
C     CLEAR AP
C
C
        CALL APCLR
C
C
C     PUT DATA INTO AP MAIN MEMORY
C
C
2       WRITE(6,602)
602     FORMAT(/,'INPUT DATA TO SETUP DAU INTERNAL REG (Z4)')
        READ (5,501)DAUTO
501     FORMAT(Z4)
        CALL APPUT(DAUTO,0,1,1)
        CALL APWD
C
C
C     SET UP IOP FOR XFER
C
C
3       WRITE (6,603)
603     FORMAT(/,'INPUT DATA TO SETUP IOP XFER, (4(Z4,1X)')
        READ(5,502) WC2V,APMA2V,HMA2V,CTL2V
502     FORMAT(4(z4,1X)
 1      CALL TAP2A(8,WC2V,11,APMA2V,9,HMA2V,10,CTL2V)
        CALL APWR
        GO TO 2
        END
```

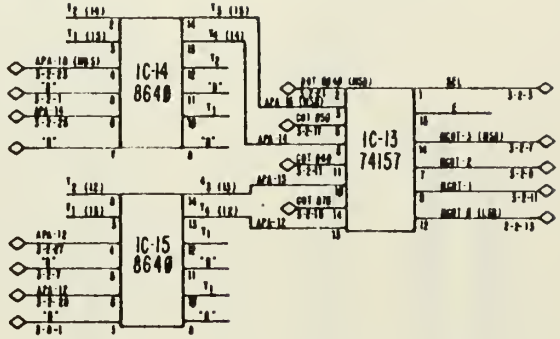
```
$TITLE TAP2A
$ENTRY TAP2A,8
WC2 = 0
WC2V = 1
APMA2 = 2
APMA2V = 3
HMA2 = 4
HMA2V = 5
CTL2 = 6
CTL2V = 7
TAP2A: MOV WC2,WC2;DB=SPFN;LDDA  "POINT TO WC2 REGISTER
NOP
MOV WC2V,WC2V;DB=SPFN;OUT        "SET WC2 TO ØØØ1
NOP
MOV APMA2,APMA2;DB=SPFN;LDDA     "POINT TO APMA2 REGISTER
NOP
MOV APMA2V,APMA2V;DB=SPFN;OUT    "SET APMA2 TO DESIRED LOCA-
NOP                                                    TION
MOV HMA2,HMA2;DB=SPFN;LDDA       "POINT TO HMA2 REGISTER
NOP
MOV HMA2V,HMA2v;DB=SPFN;OUT      "SET HMA2 TO DESIRED LOCA-
NOP                                                    TION
MOV CTL2,CTL2;DB=SPFN;LDDA       "POINT TO CTL2 REGISTER
NOP
MOV CTL2V,CTL2V;DB=SPFN;OUT      "SET CTL2 TO DMA WRITE
NOP
RETURN
$END
```

# APPENDIX B

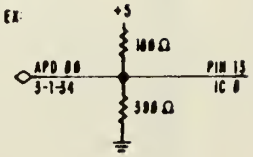
## DAU CIRCUIT BOARD SCHEMATICS

These must be used in conjunction with those in [2].



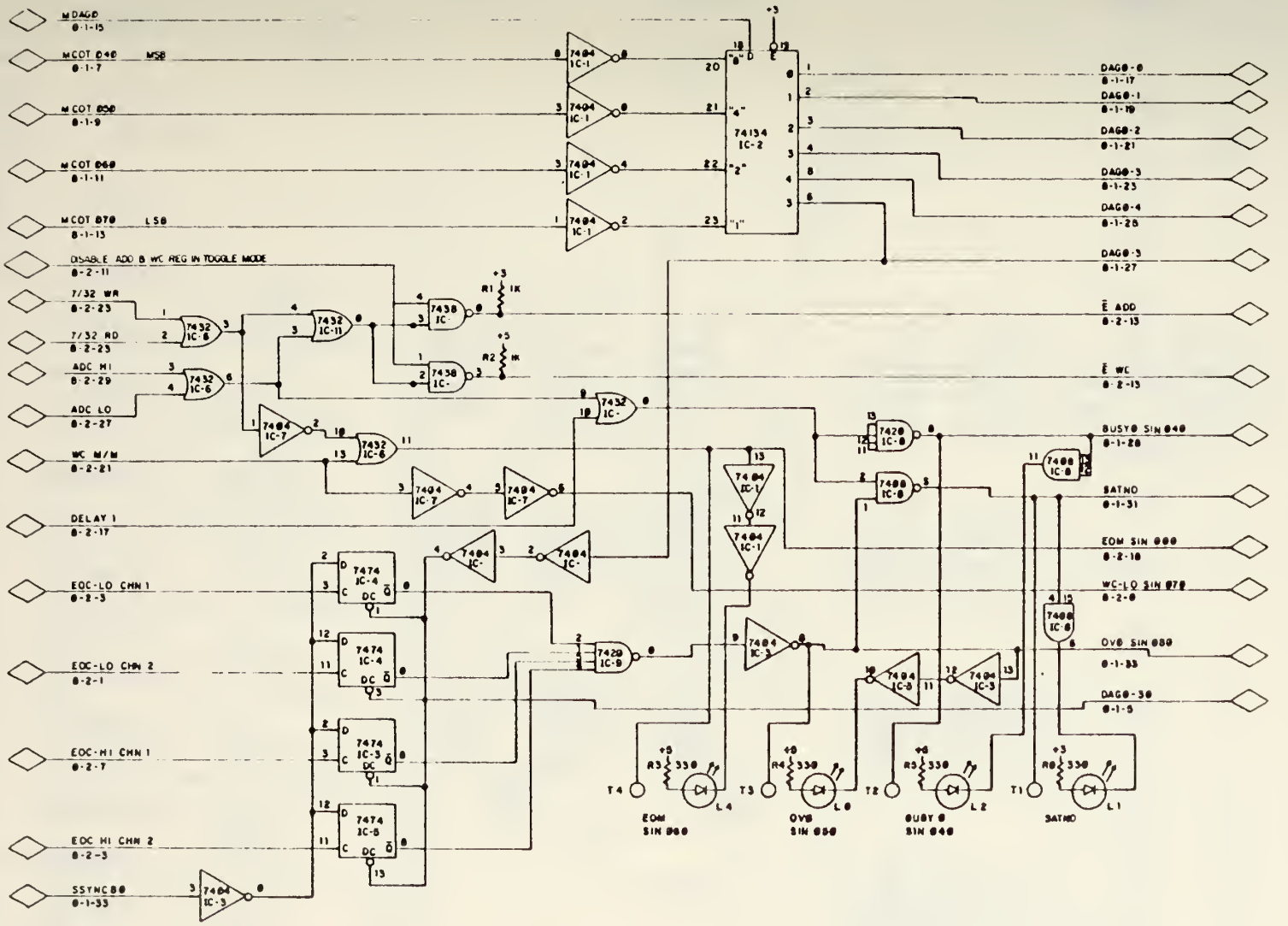




NOTE AP DATA LINES 00, 01, 02, 03 AND AP ADDRESS LINES 12, 13, 14, 15 ENTER THEIR RESPECTIVE IC PINS THROUGH RESISTOR TERMINATION BELOW

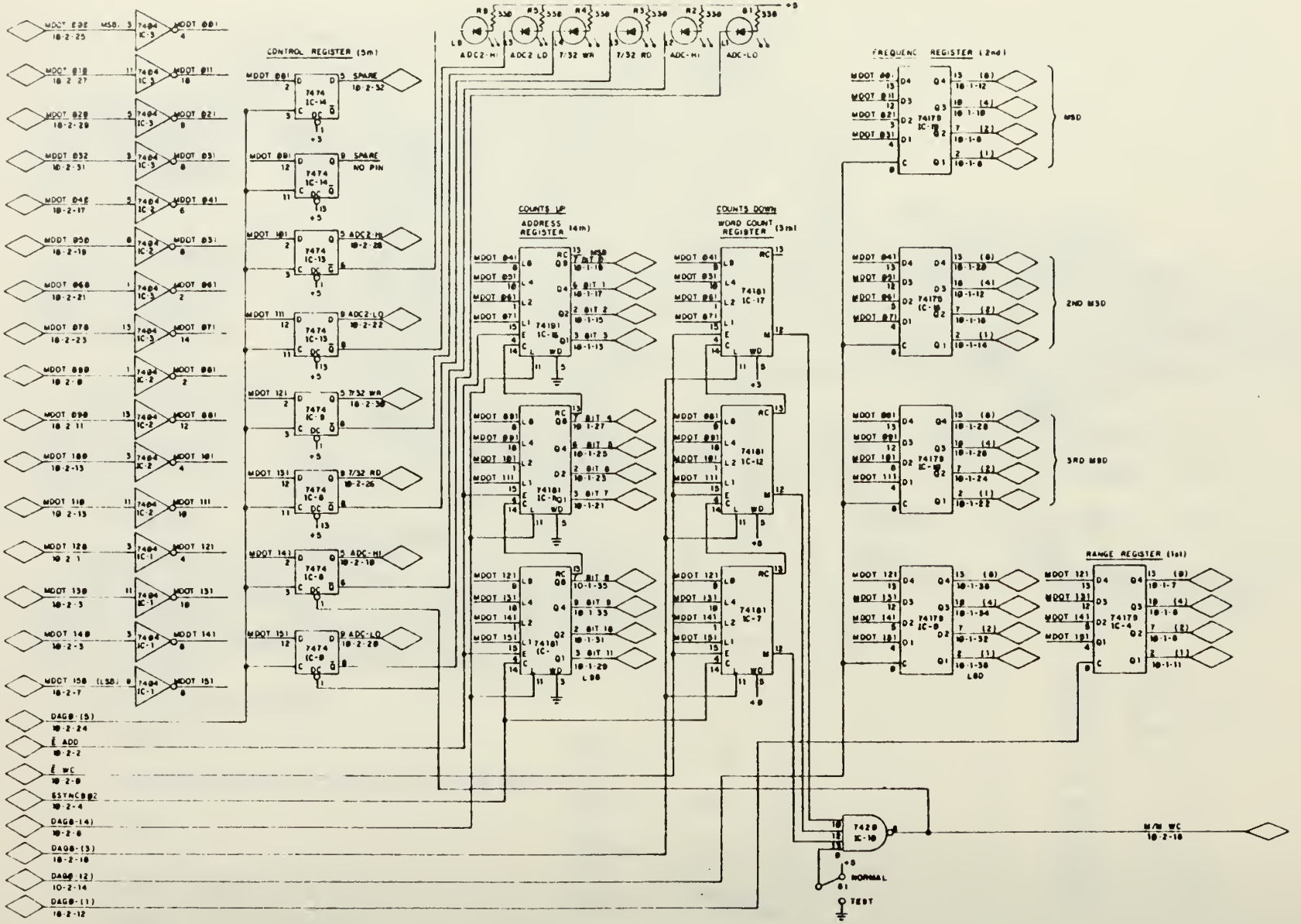


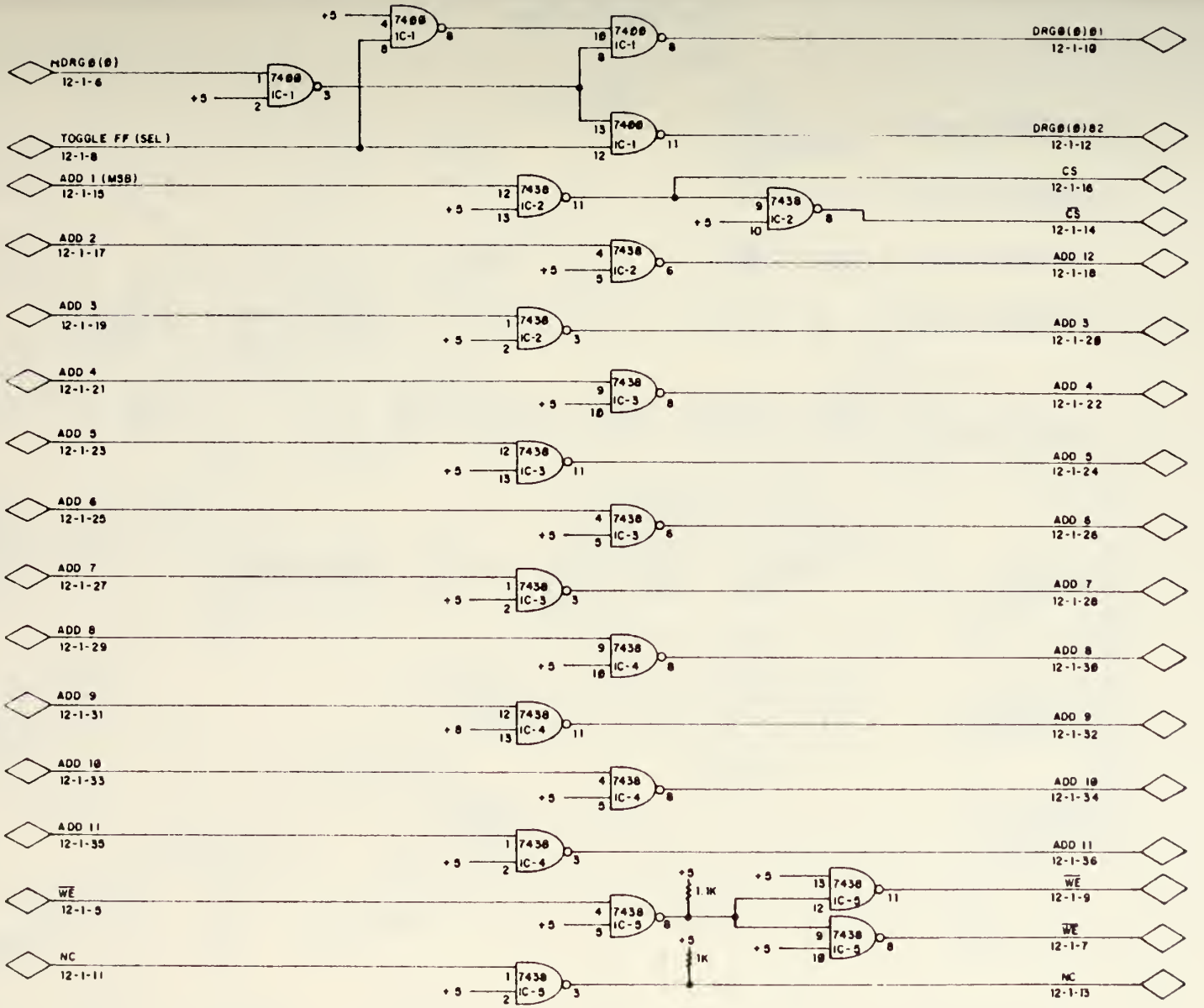

AP OR 7/32 DATA AND CONTROL SELECTOR DAU BOARD # 3

DAU BOARD 3

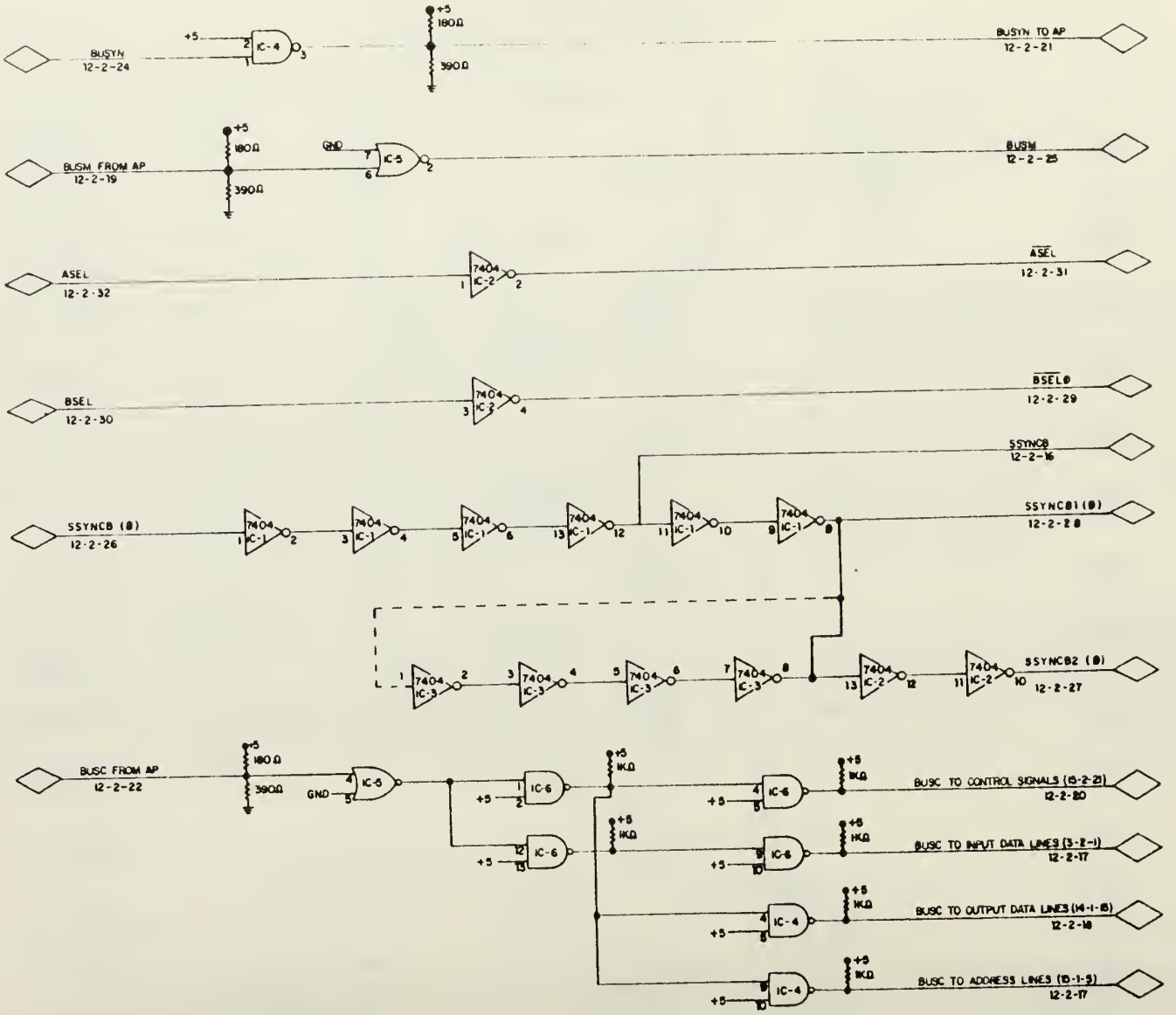

MDAG0 0-1-15
MCOT 040 MSB 0-1-7
MCOT 050 0-1-9
MCOT 060 0-1-11
MCOT 070 LSB 0-1-13
DISABLE ADD B WC REG IN TOGGLE MODE 0-2-11
7/32 WR 0-2-23
7/32 RD 0-2-25
ADC HI 0-2-29
ADC LO 0-2-27
WC M/M 0-2-21
DELAY 1 0-2-17
EOC-LO CHN 1 0-2-3
EOC-LO CHN 2 0-2-1
EOC-HI CHN 1 0-2-7
EOC HI CHN 2 0-2-5
SSYNC80 0-1-33
7404 IC-1
7404 IC-7
7404 IC-3
7404 IC-5
7404 IC-1
7404 IC-7
7404 IC-3
7404 IC-5
74154 IC-2
7432 IC-6
7432 IC-11
7432 IC-6
7432 IC-
7438 IC-
7438 IC-
7474 IC-4
7474 IC-4
7474 IC-3
7474 IC-8
7429 IC-8
7420 IC-8
7408 IC-8
7408 IC-8
7408 IC-8
R1 1K
R2 1K
R3 330
R4 330
R5 330
R6 330
DAG0-0 0-1-17
DAG0-1 0-1-19
DAG0-2 0-1-21
DAG0-3 0-1-23
DAG0-4 0-1-25
DAG0-5 0-1-27
E ADD 0-2-13
E WC 0-2-15
BUSY0 SIN 040 0-1-29
SATN0 0-1-31
EOM SIN 000 0-2-10
WC-LO SIN 070 0-2-0
OV0 SIN 080 0-1-33
DAG0-30 0-1-5
T4 EOM SIN 060
T3 OV0 SIN 050
T2 BUSY 0 SIN 040
T1 SATN0
L4
L0
L2
L1
EDGE CONNECTOR PIN
TEST POINT

DAU BOARD 8

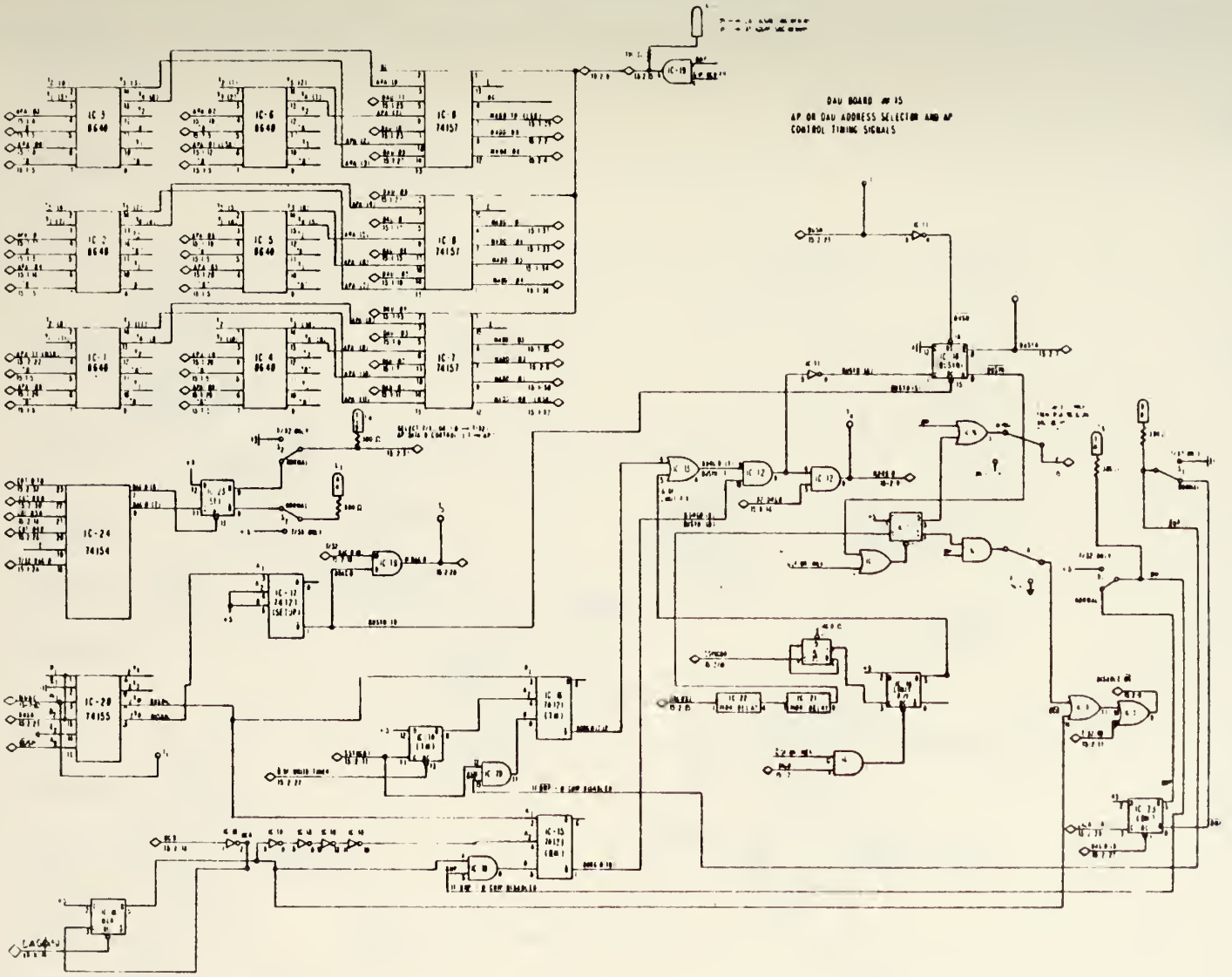

CONTROL REGISTER (5ml)
FREQUENC REGISTER (2nd)
COUNTS UP
ADDRESS REGISTER (14m)
COUNTS DOWN
WORD COUNT REGISTER (5ml)
RANGE REGISTER (1st)
MSD
2ND MSD
3RD MSD
LSD
NORMAL
TEST
M/W WC
10-2-10
DAU BOARD 10



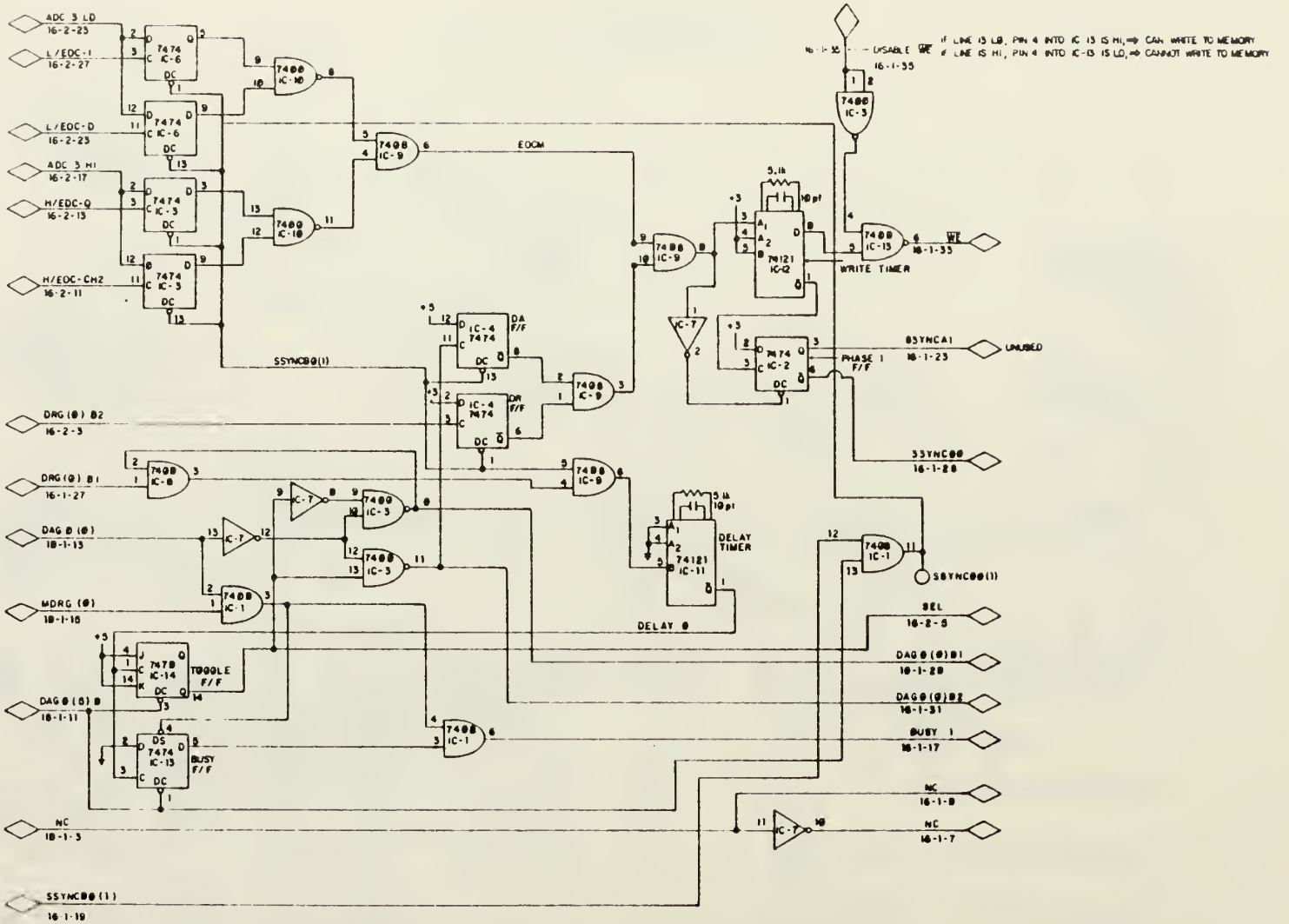

DAU BOARD 12-1




DAU BOARD 12-2


DAU BOARD # 15
AP OR DAU ADDRESS SELECTOR AND AP
CONTROL TIMING SIGNALS

DAU BOARD 15

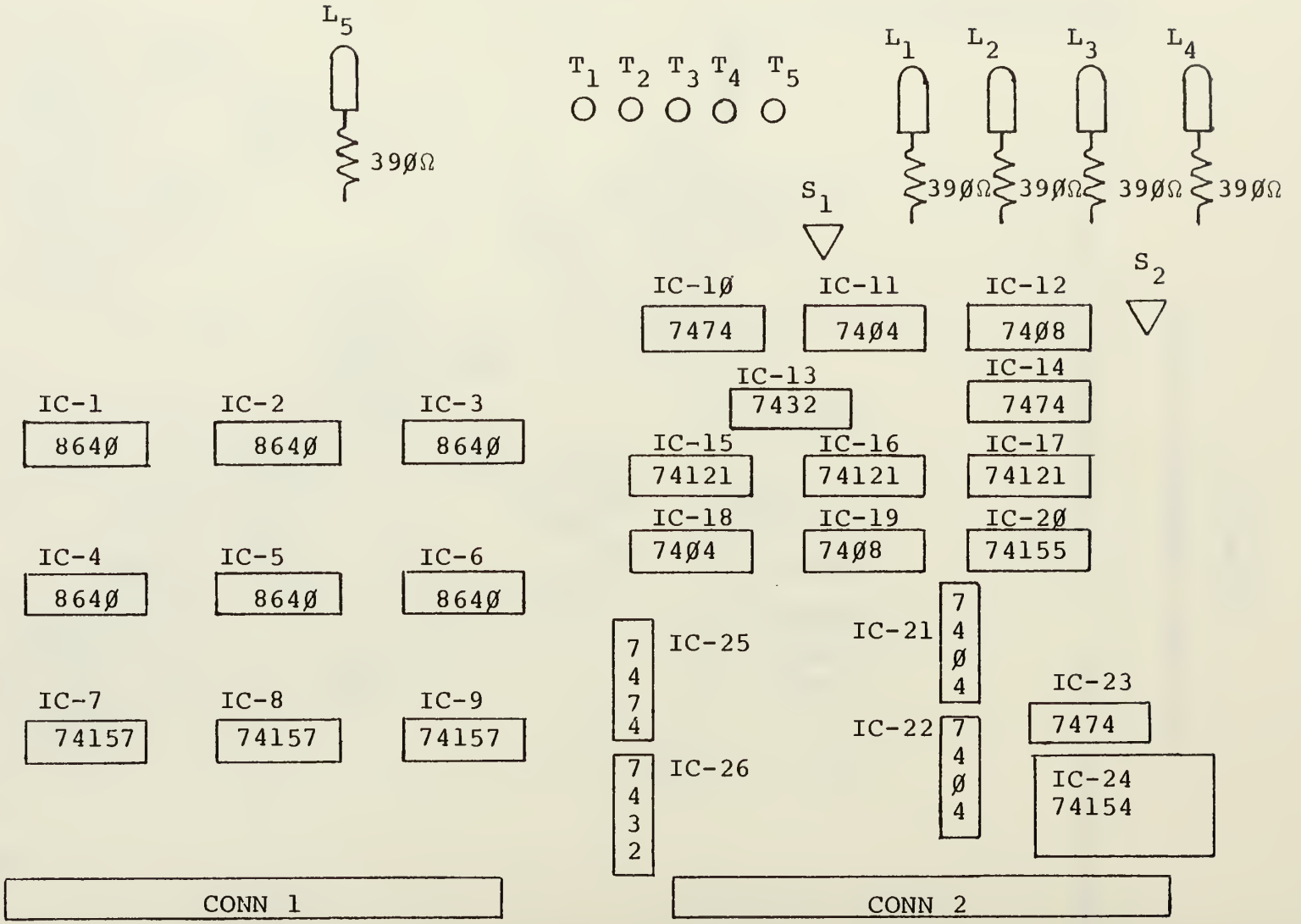

ADC 3 LD
16-2-25
L/EDC-I
16-2-27
L/EDC-D
16-2-23
ADC 3 HI
16-2-17
H/EDC-Q
16-2-13
H/EDC-CH2
16-2-11
7474 IC-6
7474 IC-5
7474 IC-3
7408 IC-10
7408 IC-9
EOCM
SSYNCB0(1)
DAG(0) B2
16-2-3
DAG(0) B1
16-1-27
DAG 0 (0)
16-1-13
MDAG (0)
16-1-10
DAG 0 (0) B
16-1-11
NC
16-1-5
SSYNCB0 (1)
16-1-19
7408 IC-8
7408 IC-3
7408 IC-1
7408 IC-14
TOGGLE F/F
7474 IC-13
BUSY F/F
IC-4 7474
DA F/F
DB F/F
IC-7
5.1k
10 pf
74121 IC-12
WRITE TIMER
74121 IC-11
DELAY TIMER
DELAY 0
7474 IC-2
PHASE 1 F/F
B3YNCA1
16-1-23
UNUSED
B3YNC00
16-1-28
S0YNCB0(1)
SEL
16-2-8
DAG 0 (0) B1
16-1-29
DAG 0 (0) B2
16-1-31
BUSY 1
16-1-17
NC
16-1-8
NC
16-1-7
16-1-35
WE
IF LINE IS LO, PIN 4 INTO IC 13 IS HI, ⇒ CAN WRITE TO MEMORY
IF LINE IS HI, PIN 4 INTO IC-13 IS LO, ⇒ CANNOT WRITE TO MEMORY
EDGE CONNECTOR PIN
TEST POINT

DAU BOARD 16

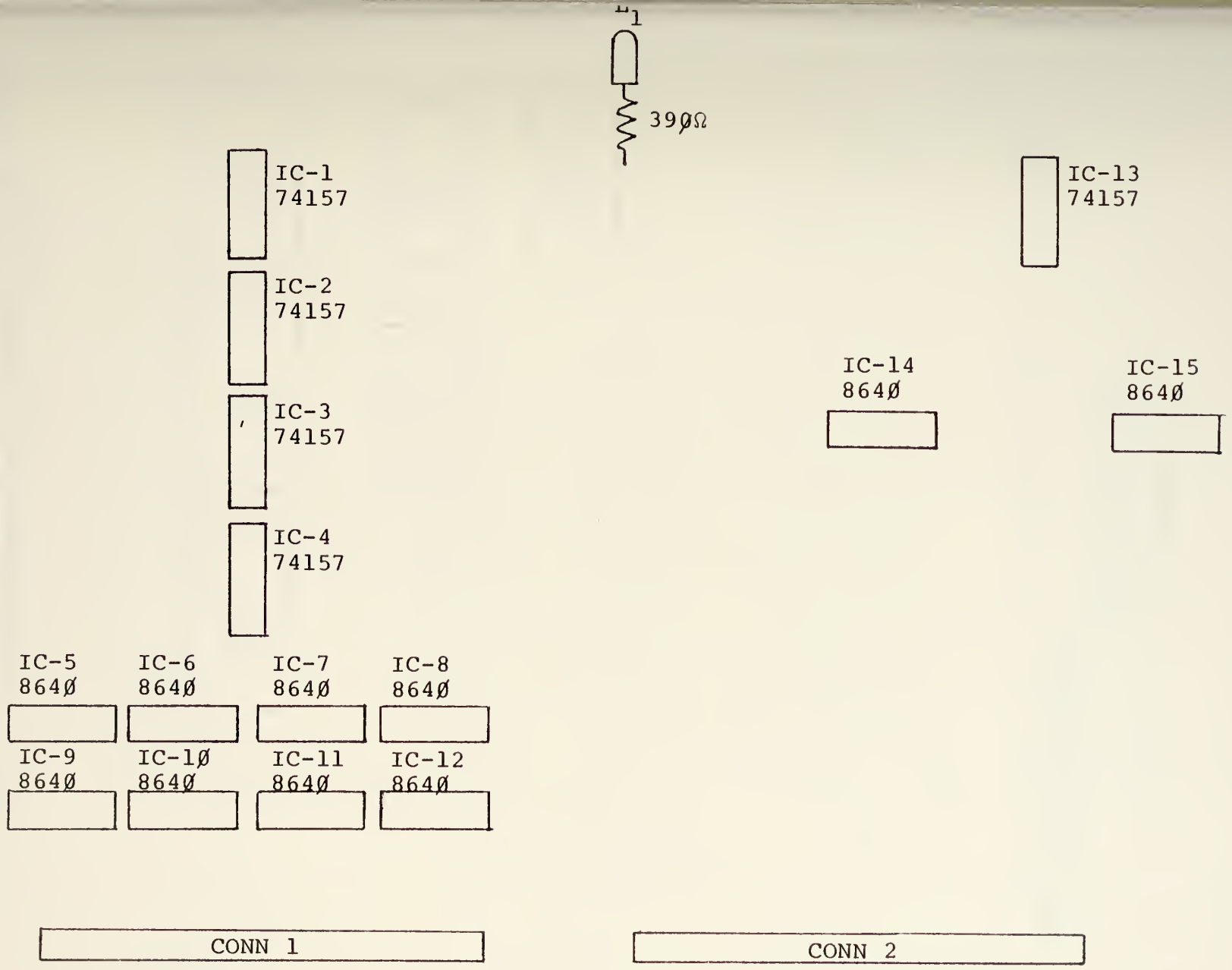
# APPENDIX C

## DAU BOARD COMPONENT LAYOUTS

These must be used in conjunction with those in [2].

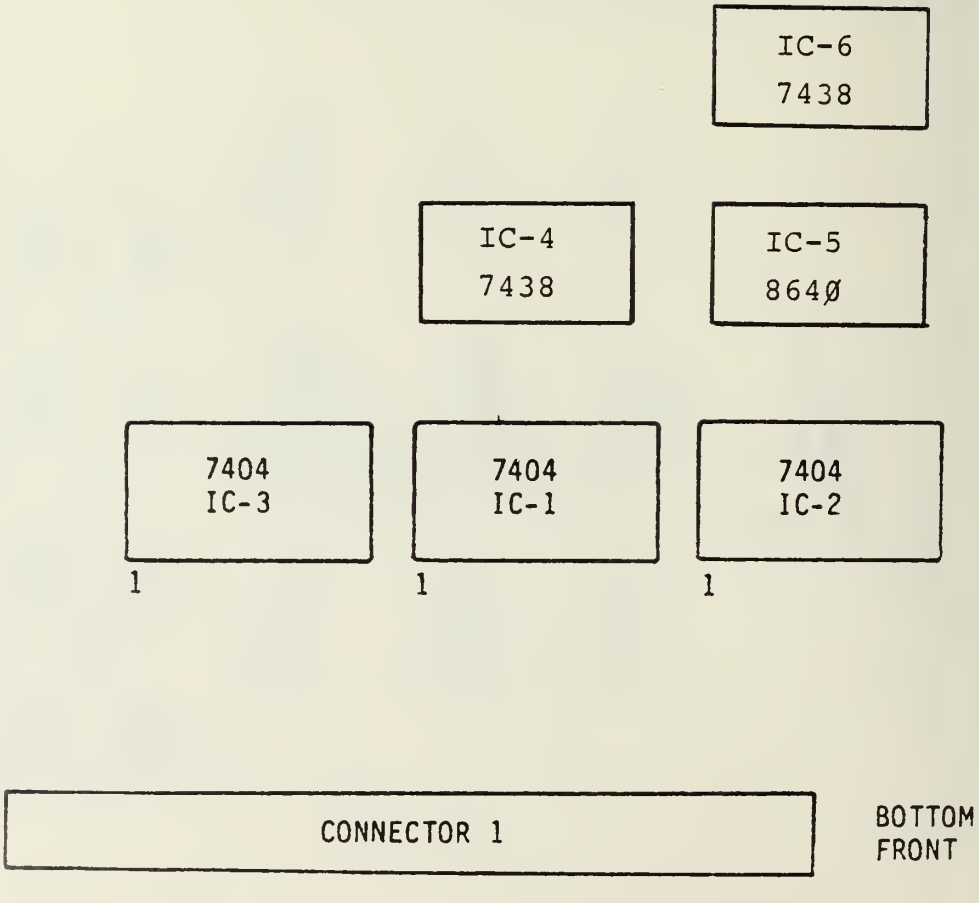



AP Or 7/32 Address Line Selector And AP Interface Signals




AP Or 7/32 Data And Control Selector Component Layout

DAU AUXILIARY BOARD 2



# APPENDIX D

## DAU WIRING LISTS

These must be used in conjunction with those in [2].

| CONNECTOR #1 TOP | | | CONNECTOR #1 BOTTOM | | |
|---|---|---|---|---|---|
| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
| 3-1-2 | +5 | +5 | 3-1-1 | GND | G |
| 3-1-4 | +5 | +5 | 3-1-3 | GND | G |
| 3-1-6 | AP DATA (MSB) 15 OUT | B-4-21 | 3-1-5 | 732 DATA Ø (MSB) | B-1-48 |
| 3-1-8 | AP DATA 14 | B-4-20 | 3-1-7 | 732 DATA 1 | B-1-46 |
| 3-1-1Ø | AP DATA 12 | B-4-18 | 3-1-9 | 732 DATA 3 | B-1-42 |
| 3-1-12 | AP DATA 13 | B-4-19 | 3-1-11 | 732 DATA 2 | B-1-44 |
| 3-1-14 | AP DATA 11 | B-4-17 | 3-1-13 | 732 DATA 4 | B-1-4Ø |
| 3-1-16 | AP DATA 1Ø | B-4-16 | 3-1-15 | 732 DATA 5 | B-1-38 |
| 3-1-18 | AP DATA 8 | B-4-14 | 3-1-17 | 732 DATA 7 | B-1-34 |
| 3-1-2Ø | AP DATA 9 | B-4-15 | 3-1-19 | 732 DATA 6 | B-1-36 |
| 3-1-22 | AP DATA 7 | B-4-13 | 3-1-21 | 732 DATA 8 | B-1-17 |
| 3-1-24 | AP DATA 6 | B-4-12 | 3-1-23 | 732 DATA 9 | B-1-16 |
| 3-1-26 | AP DATA 4 | B-4-1Ø | 3-1-25 | 732 DATA 11 | B-1-14 |
| 3-1-28 | AP DATA 5 | B-4-11 | 3-1-27 | 732 DATA 1Ø | B-1-15 |
| 3-1-3Ø | AP DATA 3 | B-4-9 | 3-1-29 | 732 DATA 12 | B-1-13 |
| 3-1-32 | AP DATA 2 | B-4-8 | 3-1-31 | 732 DATA 13 | B-1-12 |
| 3-1-34 | AP DATA Ø (LSB) | B-4-6 | 3-1-33 | 732 DATA 15 (LSB) | B-1-1Ø |
| 3-1-36 | AP DATA 1 | B-4-7 | 3-1-35 | 732 DATA 14 | B-1-11 |



WIRING LIST BOARD #3

| CONNECTOR #2 TOP | | | CONNECTOR #2 BOTTOM | | |
|---|---|---|---|---|---|
| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
| 3-2-2 | MDOT 1 | 1Ø-2-5 | 3-2-1 | "B" to 864Ø RCVR | 12-2-17<br>3-2-31 |
| 3-2-4 | MDOT (LSB) Ø | 1Ø-2-7 | 3-2-3 | SELECT 732 or IOP | 15-2-31 |
| 3-2-6 | MDOT 2 | 1Ø-2-3 | 3-2-5 | NC | NC |
| 3-2-8 | MDOT 3 | 1Ø-2-1 | 3-2-7 | MCOT (MSB) 3 | 8-1-7 |
| 3-2-1Ø | MDOT 5 | 1Ø-2-13 | 3-2-9 | MCOT 2 | 8-1-9 |
| 3-2-12 | MDOT 4 | 1Ø-2-15 | 3-2-11 | MCOT 1 | 8-1-11 |
| 3-2-14 | MDOT 6 | 1Ø-2-11 | 3-2-13 | MCOT Ø (LSB) | 8-1-13 |
| 3-2-16 | MDOT 7 | 1Ø-2-9 | 3-2-15 | 732 COT Ø7Ø (LSB) | B-1-6 |
| 3-2-18 | MDOT 9 | 1Ø-2-21 | 3-2-17 | 732 COT Ø6Ø | B-1-7 |
| 3-2-2Ø | MDOT 8 | 1Ø-2-23 | 3-2-19 | 732 COT Ø5Ø | B-1-8 |
| 3-2-22 | MDOT 1Ø | 1Ø-2-19 | 3-2-21 | 732 COT (MSB) Ø4Ø | B-1-9 |
| 3-2-24 | MDOT 11 | 1Ø-2-17 | 3-2-23 | AP ADDR (MSB) 15 | B-4-72 |
| 3-2-26 | MDOT 13 | 1Ø-2-29 | 3-2-29 | AP ADDR 14 | B-4-71 |
| 3-2-28 | MDOT 12 | 1Ø-2-31 | 3-2-27 | AP ADDR 13 | B-4-7Ø |
| 3-2-3Ø | MDOT 14 | 1Ø-2-27 | 3-2-20 | AP ADDR (LSB) 12 | B-4-69 |
| 3-2-32 | MDOT 15 (MSB) | 1Ø-2-25 | 3-2-31 | "B" to 864Ø RCVR | 3-2-1 |
| 3-2-34 | +5 | +5 | 3-2-33 | GND | G |
| 3-2-36 | +5 | +5 | 3-2-35 | GND | G |



WIRING LIST BOARD #3

| CONNECTOR #1 TOP | | | CONNECTOR #1 BOTTOM | | |
|---|---|---|---|---|---|
| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
| 15-1-2 | +5 | +5 | 15-1-1 | GND | G |
| 15-1-4 | +5 | +5 | 15-1-3 | GND | G |
| 15-1-6 | AP ADDR LINE 3 | B-4-6Ø | 15-1-5 | "B" TO 8640 RCVRS | 12-2-15 |
| 15-1-8 | AP ADDR LINE Ø | NC | 15-1-7 | DAU ADDR LINES 6 | 1Ø-1-15 |
| 15-1-1Ø | AP ADDR LINE 2 | B-4-59 | 15-1-9 | DAU ADDR LINES 7 | 1Ø-1-13 |
| 15-1-12 | AP ADDR LINE (LSB) 1 | B-4-58 | 15-1-11 | DAU ADDR LINES (MSB) (CS) 5 | 1Ø-1-17 |
| 15-1-14 | AP ADDR LINE 7 | B-4-64 | 15-1-13 | DAU ADDR LINES 8 | 1Ø-1-27 |
| 15-1-16 | AP ADDR LINE 4 | B-4-61 | 15-1-15 | DAU ADDR LINES 1Ø | 1Ø-1-23 |
| 15-1-18 | AP ADDR LINE 6 | B-4-63 | 15-1-17 | DAU ADDR LINES 11 | 1Ø-1-21 |
| 15-1-2Ø | AP ADDR LINE 5 | B-4-62 | 15-1-19 | DAU ADDR LINES 9 | 1Ø-1-25 |
| 15-1-22 | AP ADDR LINE (MSB) (CS) 11 | B-4-68 | 15-1-21 | DAU ADDR LINES 12 | 1Ø-1-35 |
| 15-1-24 | AP ADDR LINE 8 | B-4-65 | 15-1-23 | DAU ADDR LINES 14 | 1Ø-1-31 |
| 15-1-26 | AP ADDR LINE 1Ø | B-4-67 | 15-1-25 | DAU ADDR LINES (LSB) 15 | 1Ø-1-29 |
| 15-1-28 | AP ADDR LINE 9 | B-4-66 | 15-1-27 | DAU ADDR LINES 13 | 1Ø-1-33 |
| 15-1-3Ø | MADDR OUT MA1 | 12-1-17 | 15-1-29 | MASTER ADDR OUT (LSB) MA1Ø | 12-1-35 |
| 15-1-32 | MADDR OUT (MSB) MAØ | 12-1-15 | 15-1-31 | MASTER ADDR OUT MA7 | 12-1-29 |
| 15-1-34 | MADDR OUT MA5 | 12-1-25 | 15-1-33 | MASTER ADDR OUT MA6 | 12-1-27 |
| 15-1-36 | MADDR OUT MA4 | 12-1-23 | 15-1-35 | MASTER ADDR OUT MA3 | 12-1-21 |



WIRING LIST BOARD #15

| CONNECTOR #2 TOP | | | CONNECTOR #2 BOTTOM | | |
|---|---|---|---|---|---|
| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
| 15-2-2 | MADDR OUT MA9 | 12-1-33 | 15-2-1 | NC | NC |
| 15-2-4 | MADDR OUT MA8 | 12-1-31 | 15-2-3 | NC | NC |
| 15-2-6 | MADDR OUT MA2 | 12-1-19 | 15-2-5 | MDRGØ OUT | 16-1-15<br>12-1-6 |
| 15-2-8 | BM or TM SELECT | 15-2-15 | 15-2-7 | BUSYN TO IOP | 12-2-24 |
| 15-2-1Ø | $\overline{\text{SSYNCHB}}$ | 12-2-16 | 15-2-9 | DISABLE $\overline{\text{WE}}$ LINE | 16-1-35 |
| 15-2-12 | DAGØ (5) IN | 16-1-11 | 15-2-11 | 732 RD LINE | 1Ø-2-26 |
| 15-2-14 | NC | NC | 15-2-13 | Q OF LIMIT F/F | 8-2-11 |
| 15-2-16 | 732 BRG Ø (BACKPLANE) | B-1-4 | 15-2-15 | BM OR TM "SELECT" | 15-2-8 |
| 15-2-18 | WC Ø | 8-2-9 | 15-2-17 | SSYNCH B1 | 12-2-28 |
| 15-2-2Ø | MDAG Ø OUT | 8-1-15 | 15-2-19 | 732 DAGØ Ø | 15-2-24 |
| 15-2-22 | $\overline{\text{Q}}$ OF WRITE TIMER | 16-2-7 | 15-2-21 | BUSC | 12-2-2Ø |
| 15-2-24 | 732 DAG Ø (BACKPLANE) | B-1-5 | 15-2-23 | BUSM | 12-2-25 |
| 15-2-26 | COT Ø4Ø | B-1-9 | 15-2-24 | DRGØB 2 | 16-2-3 |
| 15-2-28 | COT Ø5Ø | B-1-8 | 15-2-27 | DAGØ(8)OUT | 8-1-36 |
| 15-2-3Ø | COT Ø6Ø | B-1-7 | 15-2-29 | DAGØ(9)OUT | 8-1-34 |
| 15-2-32 | COT Ø7Ø | B-1-6 | 15-2-31 | "SELECT" 732 OR IOP | 3-2-3 |
| 15-2-34 | +5 | +5 | 15-2-33 | GND | G |
| 15-2-36 | +5 | +5 | 15-2-35 | GND | G |



WIRING LIST BOARD #15

CONNECTOR (1)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 8-1-2 | +5 | +5 | 8-1-1 | Gnd | Gnd |
| 8-1-4 | +5 | +5 | 8-1-3 | Gnd | Gnd |
| 8-1-6 | NC | NC | 8-1-5 | DAGØ(5) B Out | 16-1-11 |
| 8-1-8 | NC | NC | 8-1-7 | MCOT Ø4Ø In | 3-2-7 |
| 8-1-10 | NC | NC | 8-1-9 | MCOT Ø5Ø In | 3-2-9 |
| 8-1-12 | NC | NC | 8-1-11 | MCOT Ø6Ø In | 3-2-11 |
| 8-1-14 | NC | NC | 8-1-13 | MCOT Ø7Ø In | 3-2-13 |
| 8-1-16 | NC | NC | 8-1-15 | MDAG Ø In | 15-2-20 |
| 8-1-18 | NC | NC | 8-1-17 | DAG Ø-(Ø) Out | 16-1-13 |
| 8-1-20 | NC | NC | 8-1-19 | DAG Ø-(1) Out | 10-2-12 |
| 8-1-22 | NC | NC | 8-1-21 | DAG Ø-(2) Out | 10-2-14 |
| 8-1-24 | NC | NC | 8-1-23 | DAG Ø-(3) Out | 10-2-10 |
| 8-1-26 | NC | NC | 8-1-25 | DAG Ø-(4) Out | 10-2-6 |
| 8-1-28 | NC | NC | 8-1-27 | DAG Ø-(5) Out | 10-2-24 |
| 9-1-30 | NC | NC | 8-1-29 | SIN Ø4Ø Out | B-3-5 |
| 8-1-32 | NC | NC | 8-1-31 | SATNO Out | B-1-3 |
| 8-1-34 | DAGØ(9)OUT | 15-2-29 | 8-1-33 | ØVØ SIN Ø5Ø Out | B-3-4 |
| 8-1-36 | DAGØ(8)OUT | 15-2-27 | 8-1-35 | SSYNØBØ In | 12-2-27 |

DATA ACQUISITION CONTROL CIRCUIT (1 of 2)
DAU BOARD #8

CONNECTOR (2)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 8-2-2 | NC | NC | 8-2-1 | EOC-LO CHN 2 In | 5-1-34 |
| 8-2-4 | NC | NC | 8-2-3 | EOC-LO CHN 1 In | 13-1-34 |
| 8-2-6 | NC | NC | 8-2-5 | EOC-HI CHN 2 In | 7-1-34 |
| 8-2-8 | NC | NC | 8-2-7 | EOC-LO CHN 1 In | 11-1-34 |
| 8-2-10 | NC | NC | 8-2-9 | WCØ | 15-2-18 |
| 8-2-12 | NC | NC | 8-2-11 | Q of LIMIT F/F | 15-2-13 |
| 8-2-14 | NC | NC | 8-2-13 | $\overline{E}$ Add Out | 10-2-2 |
| 8-2-16 | NC | NC | 8-2-15 | $\overline{E}$ WC Out | 10-2-8 |
| 8-2-18 | NC | NC | 8-2-17 | Busy In | 16-1-17 |
| 8-2-20 | NC | NC | 8-2-19 | EOM SIN Ø6Ø In | B-3-3 |
| 8-2-22 | NC | NC | 8-2-21 | WC M/M In | 10-2-18 |
| 8-2-24 | NC | NC | 8-2-23 | 7/32 WR In | 10-2-30 |
| 8-2-26 | NC | NC | 8-2-25 | 7/32 RD In | 10-2-26 |
| 8-2-28 | NC | NC | 8-2-27 | ADC2-LO-In | 10-2-20 |
| 8-2-30 | NC | NC | 8-2-29 | ADC2-HI-In | 10-2-16 |
| 8-2-32 | NC | NC | 8-2-31 | NC | NC |
| 8-2-34 | +5 | +5 | 8-2-33 | Gnd | Gnd |
| 8-2-36 | +5 | +5 | 8-2-35 | Gnd | Gnd |

DATA ACQUISITION CONTROL CIRCUIT (1 of 2)
DAU BOARD #8

CONNECTOR (1)

| FROM | FUNCTION | | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|---|
| 10-1-2 | +5 | | +5 | 10-1-1 | Gnd | Gnd |
| 10-1-4 | +5 | | +5 | 10-1-3 | Gnd | Gnd |
| 10-1-6 | Freq Sel Bit 1 | | 1-2-33 | 10-1-5 | Range Out Bit 4 | 1-2-35 |
| 10-1-8 | Freq Sel Bit 2 | MSD | 1-2-21 | 10-1-7 | Range Out Bit 8 | NC |
| 10-1-10 | Freq Sel Bit 4 | OUT | 1-2-31 | 10-1-9 | Range Out Bit 2 | 1-2-40 |
| 10-1-12 | Freq Sel Bit 8 | | 1-2-29 | 10-1-11 | Range Out Bit 1 | 1-2-38 |
| 10-1-14 | Freq Sel Bit 1 | 2ND | 1-2-24 | 10-1-13 | Add Out Bit 3 | 15-1-9 |
| 10-1-16 | Freq Sel Bit 2 | MSD | 1-2-23 | 10-1-15 | Add Out Bit 2 | 15-1-7 |
| 10-1-18 | Freq Sel Bit 4 | OUT | 1-2-27 | 10-1-17 | Add Out Bit 1 | 15-1-11 |
| 10-1-20 | Freq Sel Bit 8 | | 1-2-25 | 10-1-19 | Add Out Bit 0 MSB | NC |
| 10-1-22 | Freq Sel Bit 1 | 3RD | 1-2-16 | 10-1-21 | Add Out Bit 7 | 15-1-17 |
| 10-1-24 | Freq Sel Bit 2 | MSD | 1-2-9 | 10-1-23 | Add Out Bit 6 | 15-1-15 |
| 10-1-26 | Freq Sel Bit 4 | OUT | 1-2-11 | 10-1-25 | Add Out Bit 5 | 15-1-19 |
| 10-1-28 | Freq Sel Bit 8 | | 1-2-13 | 10-1-27 | Add Out Bit 4 | 15-1-13 |
| 10-1-30 | Freq Sel Bit 1 | | 1-2-19 | 10-1-29 | Add Out Bit 11 LSB | 15-1-25 |
| 10-1-32 | Freq Sel Bit 2 | LSD | 1-2-7 | 10-1-31 | Add Out Bit 10 | 15-1-23 |
| 10-1-34 | Freq Sel Bit 4 | OUT | 1-2-3 | 10-1-33 | Add Out Bit 9 | 15-1-27 |
| 10-1-36 | Freq Sel Bit 8 | | 1-2-4 | 10-1-35 | Add Out Bit 8 | 15-1-21 |

DATA ACQUISITION CONTROL CIRCUIT (2 of 2)
DAU BOARD #10

CONNECTOR (2)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 10-2-2 | $\overline{E}$ Add In | 8-2-13 | 10-2-1 | 7/32 In DOT 12Ø | 3-2-8 |
| 10-2-4 | SSYNCB In | 8-1-35 | 10-2-3 | 7/32 In DOT 13Ø | 3-2-6 |
| 10-2-6 | DAGØ (4) In | 8-1-25 | 10-2-5 | 7/32 In DOT 14Ø | 3-2-2 |
| 10-2-8 | $\overline{E}$ WC In | 8-2-15 | 10-2-7 | 7/32 In DOT 15Ø | 3-2-4 |
| 10-2-10 | DAGØ (3) In | 8-1-23 | 10-2-9 | 7/32 In DOT Ø8Ø | 3-2-16 |
| 10-2-12 | DAGØ (1) In | 8-1-19 | 10-2-11 | 7/32 In DOT Ø9Ø | 3-2-14 |
| 10-2-14 | DAGØ (2) In | 8-1-21 | 10-2-13 | 7/32 In DOT 1ØØ | 3-2-10 |
| 10-2-16 | ADC-HI Out | 2-1-24, 12-2-32 8-2-29 | 10-2-15 | 7/32 In DOT 11Ø | 3-2-12 |
| 10-2-18 | M/M WC Out | 8-2-21 | 10-2-17 | 7/32 In DOT Ø4Ø | 3-2-24 |
| 10-2-20 | ADC-L0 Out | 12-2-30, 2-1-26 8-2-27 | 10-2-19 | 7/32 In DOT Ø5Ø | 3-2-22 |
| 10-2-22 | ADC2-L0 Out | 2-1-16 | 10-2-21 | 7/32 In DOT Ø6Ø | 3-2-18 |
| 10-2-24 | DAGØ (5) In | 8-2-27 | 10-2-23 | 7/32 In DOT Ø7Ø | 3-2-20 |
| 10-2-26 | 7/32 RD Out | 8-2-25, 16-1-35 | 10-2-25 | 7/32 In DOT ØØØ | 3-2-32 |
| 10-2-28 | ADC2-Hi Out | 9-1-33, 2-1-18 | 10-2-27 | 7/32 In DOT Ø1Ø | 3-2-30 |
| 10-2-30 | 7/32 WR Out | 8-2-23 | 10-2-29 | 7/32 In DOT Ø2Ø | 3-2-26 |
| 10-2-32 | Spare DOT Ø8Ø | NC | 10-2-31 | 7/32 In DOT Ø3Ø | 3-2-28 |
| 10-2-34 | +5 | +5 | 10-2-33 | Gnd | Gnd |
| 10-2-36 | +5 | +5 | 10-2-35 | Gnd | Gnd |

DATA ACQUISITION CONTROL CIRCUIT (2 of 2)

DAU BOARD #1Ø

CONNECTOR (1)

| PIN | FUNCTION | TO | PIN | FUNCTION | TO |
|---|---|---|---|---|---|
| 12-1-2 | +5 | | 12-1-1 | Gnd | |
| 12-1-4 | +5 | | 12-1-3 | Gnd | |
| 12-1-6 | DRGØ | 16-1-15/15-2-5 | 12-1-5 | $\overline{We}$ In | 16-1-33 |
| 12-1-8 | Toggle FF IN (SEC) | 16-2-5 | 12-1-7 | $\overline{We}$ Out | 6-1-33 |
| 12-1-10 | DRG(Ø) B1 Out | 16-1-27 | 12-1-9 | $\overline{We}$ Out | 18-1-33 |
| 12-1-12 | DRG(Ø) B2 Out | 16-2-3 | 12-1-11 | NC | |
| 12-1-14 | $\overline{CS}$ | 6/18-2-2 | 12-1-13 | NC | |
| 12-1-16 | CS | 6/18-2-4 | 12-1-15 | Add In Bit 1 MSB | 15-1-32 |
| 12-1-18 | Add Out Bit 2 MSB | 6/18-1-31 | 12-1-17 | Add In Bit 2 MSB | 15-1-30 |
| 12-1-20 | Add Out Bit 3 | 6/18-1-29 | 12-1-19 | Add In Bit 3 | 15-2-6 |
| 12-1-22 | Add Out Bit 4 | 6/18-1-27 | 12-1-21 | Add In Bit 4 | 15-1-35 |
| 12-1-24 | Add Out Bit 5 | 6/18-1-25 | 12-1-23 | Add In Bit 5 | 15-1-36 |
| 12-1-26 | Add Out Bit 6 | 6/18-1-23 | 12-1-25 | Add In Bit 6 | 15-1-34 |
| 12-1-28 | Add Out Bit 7 | 6/18-1-21 | 12-1-27 | Add In Bit 7 | 15-1-33 |
| 12-1-30 | Add Out Bit 8 | 6/18-1-19 | 12-1-29 | Add In Bit 8 | 15-1-31 |
| 12-1-32 | Add Out Bit 9 | 6/18-1-17 | 12-1-31 | Add In Bit 9 | 15-2-4 |
| 12-1-34 | Add Out Bit 10 | 6/18-1-15 | 12-1-33 | Add In Bit 10 | 15-2-2 |
| 12-1-36 | Add Out Bit 11 LSB | 6/18-1-13 | 12-1-35 | Add In Bit 11 LSB | 15-1-29 |

DAU BOARD 12-1 DRIVERS

CONNECTOR (2)

| PIN | FUNCTION | TO | PIN | FUNCTION | TO |
|---|---|---|---|---|---|
| 12-2-2 | NC | NC | 12-2-1 | NC | NC |
| 12-2-4 | NC | NC | 12-2-3 | NC | NC |
| 12-2-6 | NC | NC | 12-2-5 | NC | NC |
| 12-2-8 | NC | NC | 12-2-7 | NC | NC |
| 12-2-10 | NC | NC | 12-2-9 | NC | NC |
| 12-2-12 | NC | NC | 12-2-11 | NC | NC |
| 12-2-14 | NC | NC | 12-2-13 | NC | NC |
| 12-2-16 | $\overline{\text{SSYNCB}\emptyset}$(OUT) | 15-2-10 | 12-2-15 | BUSC | 15-1-5 |
| 12-2-18 | NC | NC | 12-2-17 | BUSC | 3-2-1 |
| 12-2-20 | BUSC | 15-2-21 | 12-2-19 | NC | NC |
| 12-2-22 | NC | NC | 12-2-21 | NC | NC |
| 12-2-24 | BUSYN TO AP | 15-2-7 | 12-2-23 | NC | NC |
| 12-2-26 | SSYNCBØ In | 16-1-23 | 12-2-25 | BUSM | 15-2-23 |
| 12-2-28 | SSYNCBØ(1) Out | 14-1-19<br>16-1-19/15-2-17 | 12-2-27 | SSYNCBØ(2) Out | 8-1-35 |
| 12-2-30 | ADC-Lo | 10-2-20 | 12-2-29 | $\overline{\text{BSEL}}$ Out | 4-1-12 |
| 12-2-32 | ADC-Hi | 10-2-16 | 12-2-31 | $\overline{\text{ASEL}}$ Out | 4-1-10 |
| 13-2-34 | +5 | | 12-2-33 | Gnd | Gnd |
| 12-2-36 | +5 | | 12-2-35 | Gnd | Gnd |

DAU BOARD 12-2 INVERTERS AND AUXILIARY SIGNALS

CONNECTOR (1)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 16-1-2 | +5 | +5 | 16-1-1 | Gnd | Gnd |
| 16-1-4 | +5 | +5 | 16-1-3 | Gnd | Gnd |
| 16-1-6 | NC | NC | 16-1-5 | A1 In | 10-1-17 |
| 16-1-8 | NC | NC | 16-1-7 | NC | NC |
| 16-1-10 | NC | NC | 16-1-9 | NC | NC |
| 16-1-12 | NC | NC | 16-1-11 | DAG Ø (5) B In | 8-1-5 |
| 16-1-14 | NC | NC | 16-1-13 | DAG Ø (Ø) In | 8-1-17 |
| 16-1-16 | NC | NC | 16-1-15 | MDRG Ø (Ø) In | 12-1-6, B-1-4, 15-2-5 |
| 16-1-18 | NC | NC | 16-1-17 | Busy 1 Out | 8-2-17 |
| 16-1-20 | NC | NC | 16-1-19 | SSYNCBØ In | 12-2-28 |
| 16-1-22 | NC | NC | 16-1-21 | NC | NC |
| 16-1-24 | NC | NC | 16-1-23 | SSYNC BØ Out | 12-2-26 |
| 16-1-26 | NC | NC | 16-1-25 | SSYNC A1 Out | NC |
| 16-1-28 | NC | NC | 16-1-27 | DRG (Ø) B1 In | 12-1-10 |
| 16-1-30 | NC | NC | 16-1-29 | DAG (Ø) B1 Out | 20-2-26 |
| 16-1-32 | NC | NC | 16-1-31 | DAG (Ø) B2 Out | 4-2-26 |
| 16-1-34 | NC | NC | 16-1-33 | $\overline{WE}$ Out | 12-1-5 |
| 16-1-36 | NC | NC | 16-1-35 | 7/32 RD In | 10-2-26 |

BUFFER MEMORY TIMING CIRCUIT
DAU BOARD #16

CONNECTOR (2)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 16-2-2 | NC | NC | 16-2-1 | NC | NC |
| 16-2-4 | NC | NC | 16-2-3 | DRG (Ø) B2 In | 12-1-12 |
| 16-2-6 | NC | NC | 16-2-5 | Sel Out | 12-1-8, 14-1-17 |
| 16-2-8 | NC | NC | 16-2-7 | NC | NC |
| 16-2-10 | NC | NC | 16-2-9 | NC | NC |
| 16-2-12 | NC | NC | 16-2-11 | EOC Hi Chn 2 In | 7-1-34, 2-1-28 |
| 16-2-14 | NC | NC | 16-2-13 | EOC Hi Chn 1 In | 11-1-34, 2-1-34 |
| 16-2-16 | NC | NC | 16-2-15 | NC | NC |
| 16-2-18 | NC | NC | 16-2-17 | ADC3 Hi In | NC |
| 16-2-20 | NC | NC | 16-2-19 | ADC3 Hi In | 2-1-22 |
| 16-2-22 | NC | NC | 16-2-21 | ADC3 Lo In | NC |
| 16-2-24 | NC | NC | 16-2-23 | ADC3 Lo In | 2-1-20 |
| 16-2-26 | NC | NC | 16-2-25 | EOC Lo Chn 2 In | 5-1-34, 2-1-32 |
| 16-2-28 | NC | NC | 16-2-27 | EOC Lo Chn 1 In | 13-1-34, 2-1-30 |
| 16-2-30 | NC | NC | 16-2-29 | NC | NC |
| 16-2-32 | NC | NC | 16-2-31 | NC | NC |
| 16-2-34 | +5 | +5 | 16-2-33 | Gnd | Gnd |
| 16-2-36 | +5 | +5 | 16-2-35 | Gnd | Gnd |

BUFFER MEMORY TIMING CIRCUIT
DAU BOARD #16

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| B-1-14 | DOT 11Ø | 3-1-25 | B-1-31 | DOT 11Ø RET | Gnd |
| B-1-15 | DOT 1ØØ | 3-1-27 | B-1-32 | DOT 1ØØ RET | Gnd |
| B-1-16 | DOT Ø9Ø | 3-1-23 | B-1-33 | DOT Ø9Ø RET | Gnd |
| B-1-17 | DOT Ø8Ø | 3-1-21 | B-1-50 | DOT Ø8Ø RET | Gnd |
| B-1-34 | DOT Ø7Ø | 3-1-17 | B-1-35 | DOT Ø7Ø RET | Gnd |
| B-1-36 | DOT Ø6Ø | 3-1-19 | B-1-37 | DOT Ø6Ø RET | Gnd |
| B-1-38 | DOT Ø5Ø | 3-1-15 | B-1-39 | DOT Ø5Ø RET | Gnd |
| B-1-4Ø | DOT Ø4Ø | 3-1-13 | B-1-41 | DOT Ø4Ø RET | Gnd |
| B-1-42 | DOT Ø3Ø | 3-1-9 | B-1-43 | DOT Ø3Ø RET | Gnd |
| B-1-44 | DOT Ø2Ø | 3-1-11 | B-1-45 | DOT Ø2Ø RET | Gnd |
| B-1-46 | DOT Ø1Ø | 3-1-7 | B-1-47 | DOT Ø1Ø RET | Gnd |
| B-1-48 | DOT ØØØ | 3-1-5 | B-1-49 | DOT ØØØ RET | Gnd |
| B-1-1 | DIN ØØØ | 14-1-24 | B-1-18 | DIN ØØØ RET | Gnd |
| B-1-2 | SCLR Ø | NC | B-1-19 | SCLR Ø RET | Gnd |
| B-1-3 | SATNO Ø | 8-1-31 | B-1-2Ø | SATNO Ø RET | Gnd |
| B-1-4 | DRG Ø | 15-2-16 | B-1-21 | DRG Ø RET | Gnd |
| B-1-5 | DAG Ø | 15-2-19, 15-2-24 | B-1-22 | DAG Ø RET | Gnd |
| B-1-6 | COT Ø7Ø | 15-2-32, 3-2-15 | B-1-23 | COT Ø7Ø RET | Gnd |
| B-1-7 | COT Ø6Ø | 15-2-3Ø, 3-2-17 | B-1-24 | COT Ø6Ø RET | Gnd |
| B-1-8 | COT Ø5Ø | 15-2-28, 3-2-19 | B-1-25 | COT Ø5Ø RET | Gnd |
| B-1-9 | COT Ø4Ø | 15-2-26, 3-2-21 | B-1-26 | COT Ø4Ø RET | Gnd |
| B-1-1Ø | DOT 15Ø | 3-1-33 | B-1-27 | DOT 15Ø RET | Gnd |
| B-1-11 | DOT 14Ø | 3-1-35 | B-1-28 | DOT 14Ø RET | Gnd |
| B-1-12 | DOT 13Ø | 3-1-31 | B-1-29 | DOT 13Ø RET | Gnd |
| B-1-13 | DOT 12Ø | 3-1-29 | B-1-3Ø | DOT 12Ø RET | Gnd |



DAU BACKPLANE CONNECTOR #1

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| B-4-6 | BUSD (LSB) ØØ | 3-1-34 | B-4-57 | BUSA ØØ | (NOT USED)<br>15-1-8 |
| B-4-7 | BUSD Ø1 | 3-1-36 | B-4-58 | BUSA (LSB) Ø1 | 15-1-12 |
| B-4-8 | BUSD Ø2 | 3-1-32 | B-4-59 | BUSA Ø2 | 15-1-1Ø |
| B-4-9 | BUSD Ø3 | 3-1-3Ø | B-4-6Ø | BUSA Ø3 | 15-1-6 |
| B-4-1Ø | BUSD Ø4 | 3-1-26, 14-2-2 | B-4-61 | BUSA Ø4 | 15-1-16 |
| B-4-11 | BUSD Ø5 | 3-1-28, 14-2-4 | B-4-62 | BUSA Ø5 | 15-1-2Ø |
| B-4-12 | BUSD Ø6 | 3-1-24, 14-2-8 | B-4-63 | BUSA Ø6 | 15-1-18 |
| B-4-13 | BUSD Ø7 | 3-1-22, 14-2-6 | B-4-64 | BUSA Ø7 | 15-1-14 |
| B-4-14 | BUSD Ø8 | 3-1-18, 14-2-22 | B-4-65 | BUSA Ø8 | 15-1-24 |
| B-4-15 | BUSD Ø9 | 3-1-2Ø, 14-2-24 | B-4-66 | BUSA Ø9 | 15-1-28 |
| B-4-16 | BUSD 1Ø | 3-1-16, 14-1-16 | B-4-67 | BUSA 1Ø | 15-1-26 |
| B-4-17 | BUSD 11 | 3-1-14, 14-1-14 | B-4-68 | BUSA (MSB-CS)11 | 15-1-22 |
| B-4-18 | BUSD 12 | 3-1-1Ø, 14-1-3Ø | B-4-69 | BUSA 12 | 3-2-29 |
| B-4-19 | BUSD 13 | 3-1-12, 14-1-32 | B-4-7Ø | BUSA 13 | 3-2-27 |
| B-4-2Ø | BUSD 14 | 3-1-8, 14-1-36 | B-4-71 | BUSA 14 | 3-2-25 |
| B-4-21 | BUSD (MSB) 15 | 3-1-6, 14-1-34 | B-4-72 | BUSA 15 | 3-2-23 |
| B-4-35<br>B-4-79 | GND | GND | B-4-75 | BUSC | 12-2-22 |
| B-4-1 | +5 | +5 | B-4-80 | BUSM | 12-2-19 |
| | | | B-4-78 | BUSYN | 12-2-21 |

DAU BACKPLANE CONNECTOR #4 (AP)

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| AC1 | BUSD ØØ | B-4-6 | BH2 | BUSA ØØ | B-4-57 |
| AD2 | BUSD Ø1 | B-4-7 | BH1 | BUSA Ø1 | B-4-58 |
| AD1 | BUSD Ø2 | B-4-8 | BJ2 | BUSA Ø2 | B-4-59 |
| AE2 | BUSD Ø3 | B-4-9 | BJ1 | BUSA Ø3 | B-4-6Ø |
| AE1 | BUSD Ø4 | B-4-1Ø | BK2 | BUSA Ø4 | B-4-61 |
| AF2 | BUSD Ø5 | B-4-11 | BK1 | BUSA Ø5 | B-4-62 |
| AF1 | BUSD Ø6 | B-4-12 | BL2 | BUSA Ø6 | B-4-63 |
| AH2 | BUSD Ø7 | B-4-13 | BL1 | BUSA Ø7 | B-4-64 |
| AH1 | BUSD Ø8 | B-4-14 | BM2 | BUSA Ø8 | B-4-65 |
| AJ2 | BUSD Ø9 | B-4-15 | BM1 | BUSA Ø9 | B-4-66 |
| AJ1 | BUSD 1Ø | B-4-16 | BN2 | BUSA 1Ø | B-4-67 |
| AK2 | BUSD 11 | B-4-17 | BN1 | BUSA 11 | B-4-68 |
| AK1 | BUSD 12 | B-4-18 | BP2 | BUSA 12 | B-4-69 |
| AL2 | BUSD 13 | B-4-19 | BP1 | BUSA 13 | B-4-7Ø |
| AL1 | BUSD 14 | B-4-2Ø | BR2 | BUSA 14 | B-4-71 |
| AM2 | BUSD 15 | B-4-21 | BR1 | BUSA 15 | B-4-72 |
| | | | BS2 | BUSA 16 | B-4-73 |
| | | | BS1 | BUSA 17 | B-4-74 |
| | | | BT2 | BUSC | B-4-75 |
| | | | BV1 | BUSM | B-4-8Ø |
| | | | BU1 | BUSYN | B-4-78 |

AP BACKPLANE

| FROM | FUNCTION | TO | FROM | FUNCTION | TO |
|---|---|---|---|---|---|
| 2 | +5 | +5 | 1 | GND | G |
| 4 | +5 | +5 | 3 | GND | G |
| 6 | DATA IN Ø | DSW Ø | 5 | DATA OUT 1 | L-1, B-7 |
| 8 | DATA IN 1 | DSW 1 | 7 | DATA OUT Ø | L-Ø, B-6 |
| 1Ø | DATA IN 2 | DSW 2 | 9 | DATA OUT 2 | L-2, B-8 |
| 12 | DATA IN 3 | DSW 3 | 11 | DATA OUT 3 | L-3, B-9 |
| 14 | DATA IN 4 | DSW 4 | 13 | DATA OUT 5 | L-5, B-11 |
| 16 | DATA IN 5 | DSW 5 | 15 | DATA OUT 4 | L-4, B-1Ø |
| 18 | DATA IN 6 | DSW 6 | 17 | DATA OUT 6 | L-6, B-12 |
| 2Ø | DATA IN 7 | DSW 7 | 19 | DATA OUT 7 | L-7, B-13 |
| 22 | DATA IN 8 | DSW 8 | 21 | DATA OUT 8 | L-8, B-14 |
| 24 | DATA IN 9 | DSW 9 | 23 | DATA OUT 9 | L-9, B-15 |
| 26 | DATA IN 1Ø | DSW 1Ø | 25 | DATA OUT 11 | L-11, B-17 |
| 28 | DATA IN 11 | DSW 11 | 27 | DATA OUT 1Ø | L-1Ø, B-16 |
| 3Ø | DATA IN 12 | DSW 12 | 29 | DATA OUT 12 | L-12, B-18 |
| 32 | DATA IN 13 | DSW 13 | 31 | DATA OUT 13 | L-13, B-19 |
| 34 | DATA IN 14 | DSW 14 | 33 | DATA OUT 15 | L-15, B-21 |
| 36 | DATA IN 15 | DSW 15 | 35 | DATA OUT 14 | L-14, B-2Ø |
| 38 | BUSC | L-BUSC<br>BUSC 75 | 37 | BUSMI N | BUSM |
| 4Ø | BUSMI N | BUSM | 39 | BUSM OUT | L-BUSM, 8Ø |
| 42 | +5 | +5 | 41 | GND | G |
| 44 | +5 | +5 | 43 | GND | G |

DSW = DATA Switch

L = LIGHT

AP SIMULATOR WIRING

| FROM | FUNCTION | TO |
|---|---|---|
| B-57 | BUSA ØØ | ASW Ø |
| B-58 | BUSA Ø1 | ASW 1 |
| B-59 | BUSA Ø2 | ASW 2 |
| B-6Ø | BUSA Ø3 | ASW 3 |
| B-61 | BUSA Ø4 | ASW 4 |
| B-62 | BUSA Ø5 | ASW 5 |
| B-63 | BUSA Ø6 | ASW 6 |
| B-64 | BUSA Ø7 | ASW 7 |
| B-65 | BUSA Ø8 | ASW 8 |
| B-66 | BUSA Ø9 | ASW 9 |
| B-67 | BUSA 1Ø | ASW 1Ø |
| B-68 | BUSA 11 | ASW 11 |
| B-69 | BUSA 12 | ASW 12 |
| B-7Ø | BUSA 13 | ASW 13 |
| B-71 | BUSA 14 | ASW 14 |
| B-72 | BUSA 15 | ASW 15 |
| B-73 | BUSA 16 | ASW 16 |
| B-74 | BUSA 17 | ASW 17 |
| B-75 | BUSC | (L & SW) BUSC |
| B-8Ø | BUSM | PIN 39 |
| B-78 | BUSYN | (L) BUSYN |

ASW = ADDRESS SWITCH
L = LIGHT

SIMULATOR BACKPLANE

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