# Gate Power

Please send corrections (or suggestions) to youngwlim@hotmail.com.

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# Dynamic Power Reduction Techniques

Circuit Parallelization
Voltage Scaling-based  Techniques
Circuit Technology-independent Techniques
Circuit Technology-dependent Techniques

# Circuit Parallelization

Memory Parallelization
Parallelized Shift Register
Serial-Parallel Converter
Linear Feedback Shift Registers
Double Edge Triggered FlipFlops

# Voltage Scaling-based Techniques

Multiple Voltage Techniques
Low Voltage Swing

# Circuit Technology-independent Techniques

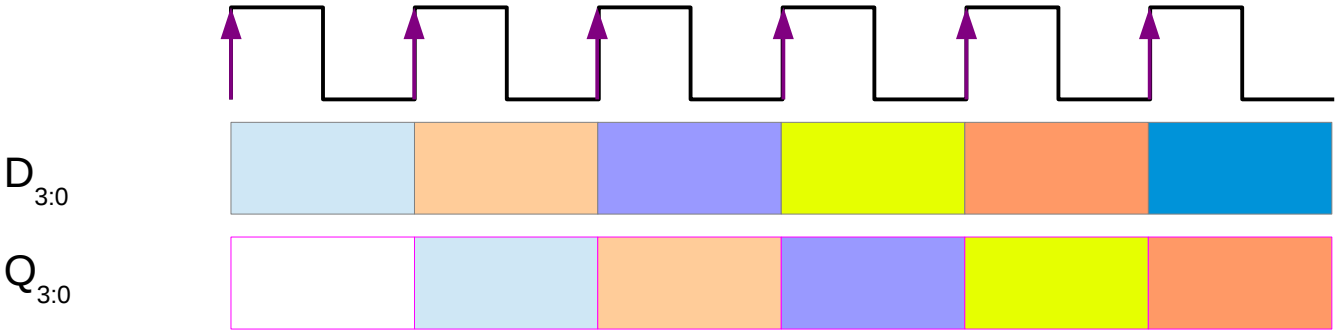
Precomputation
Retiming
Synthesis of FSMs with Gated Clocks

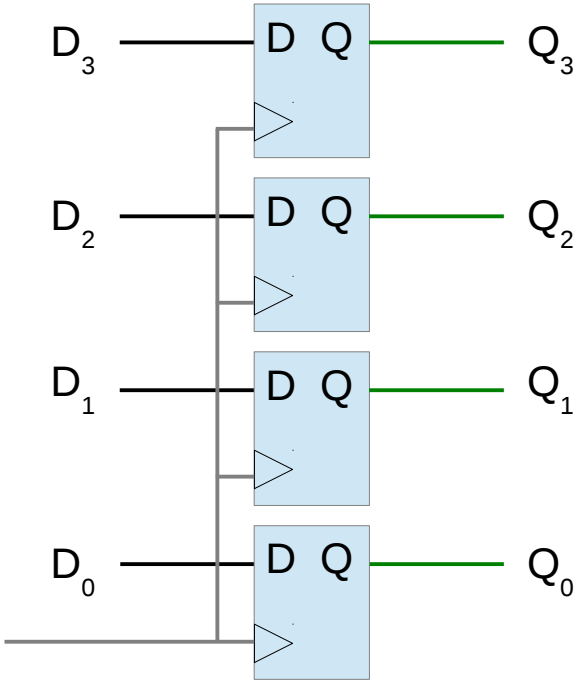
# Circuit Technology-dependent Techniques

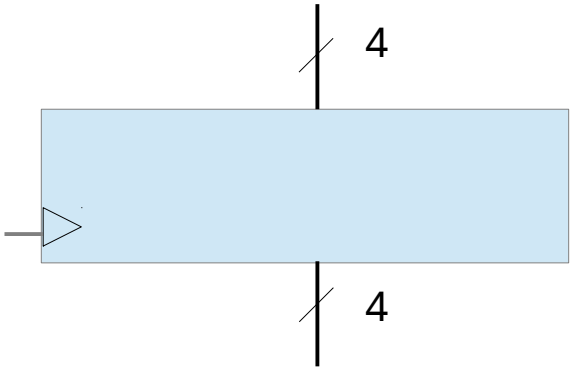
Path Balancing
Technology Decomposition
Technology Mapping

# Pass Transistor Circuits

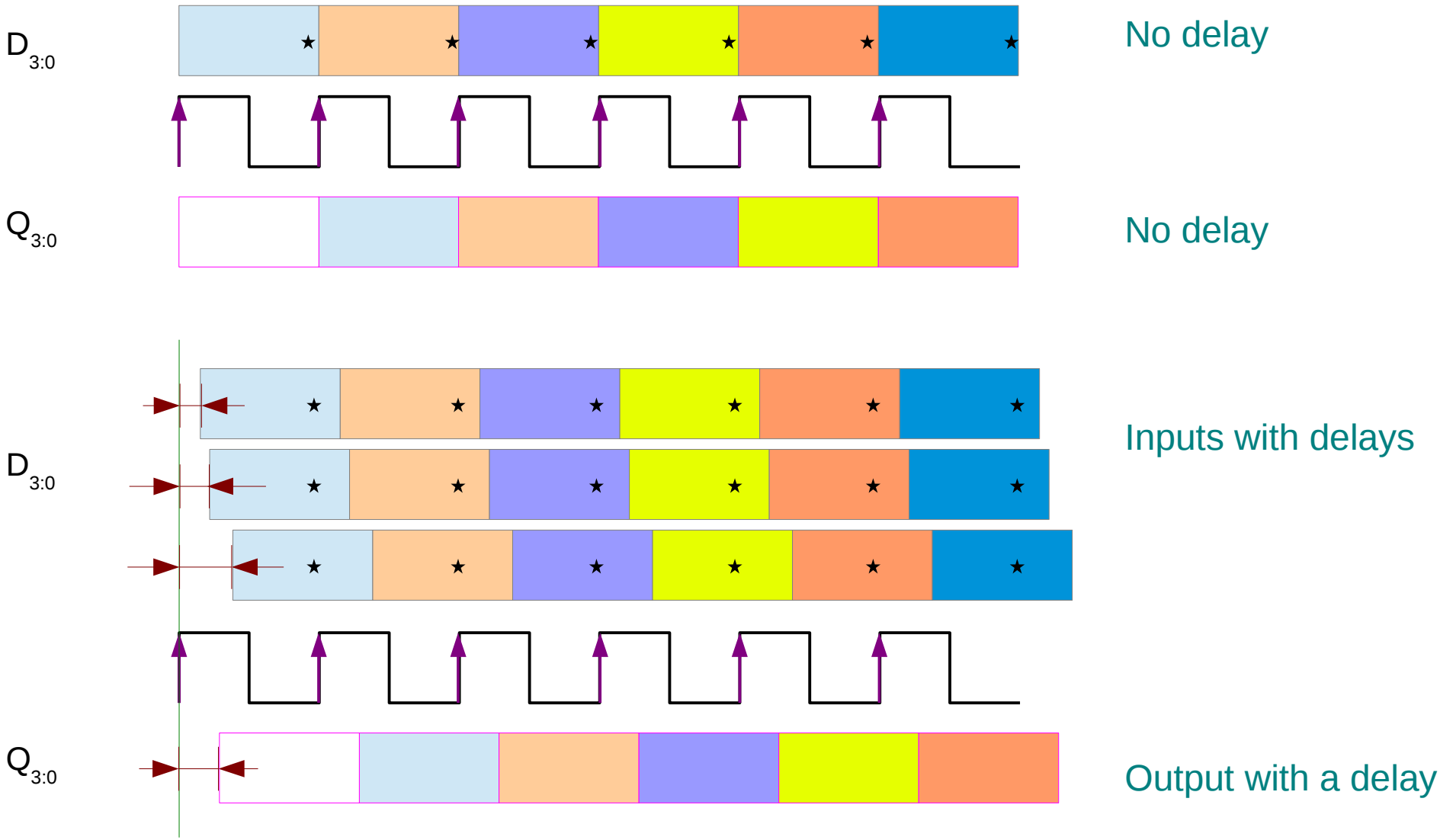
# FF Timing (Ideal)



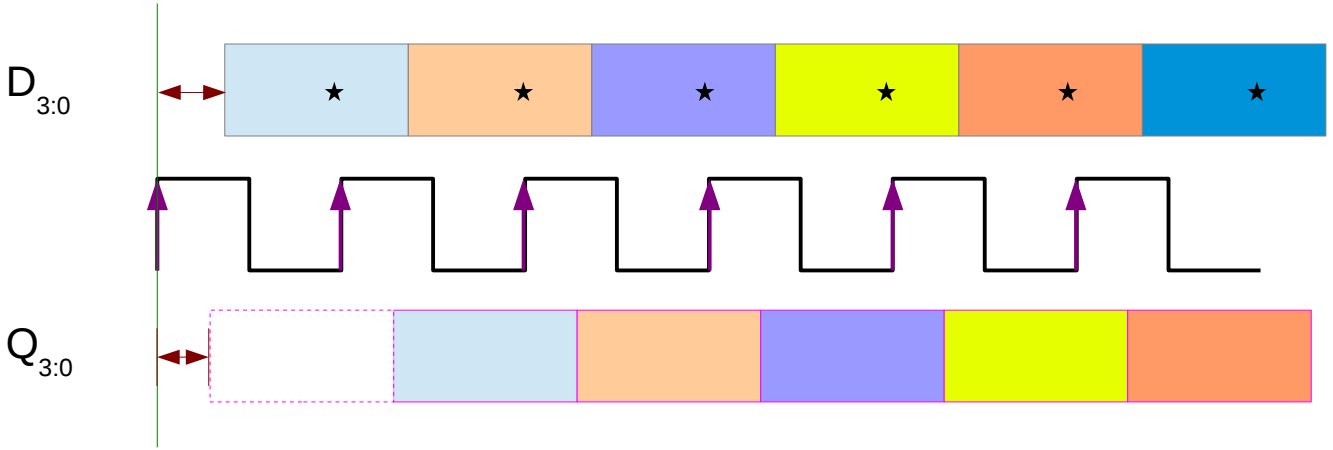



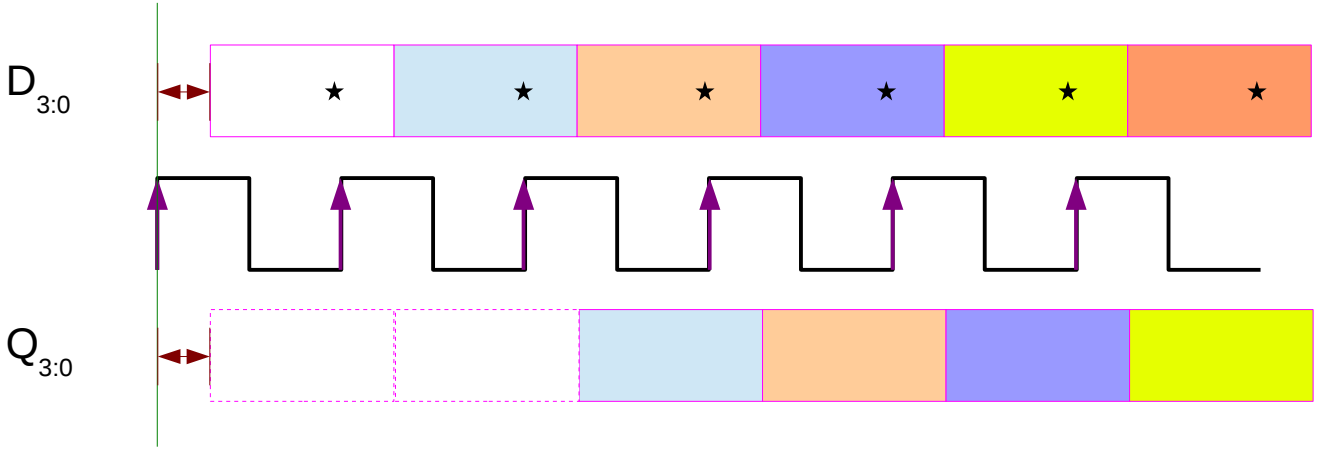



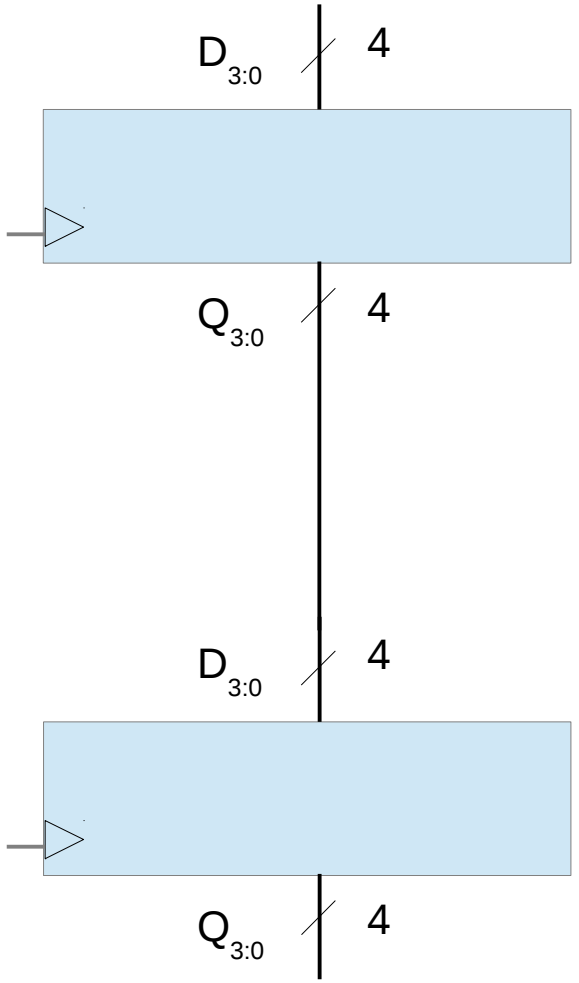
# FF Timing (Delay)



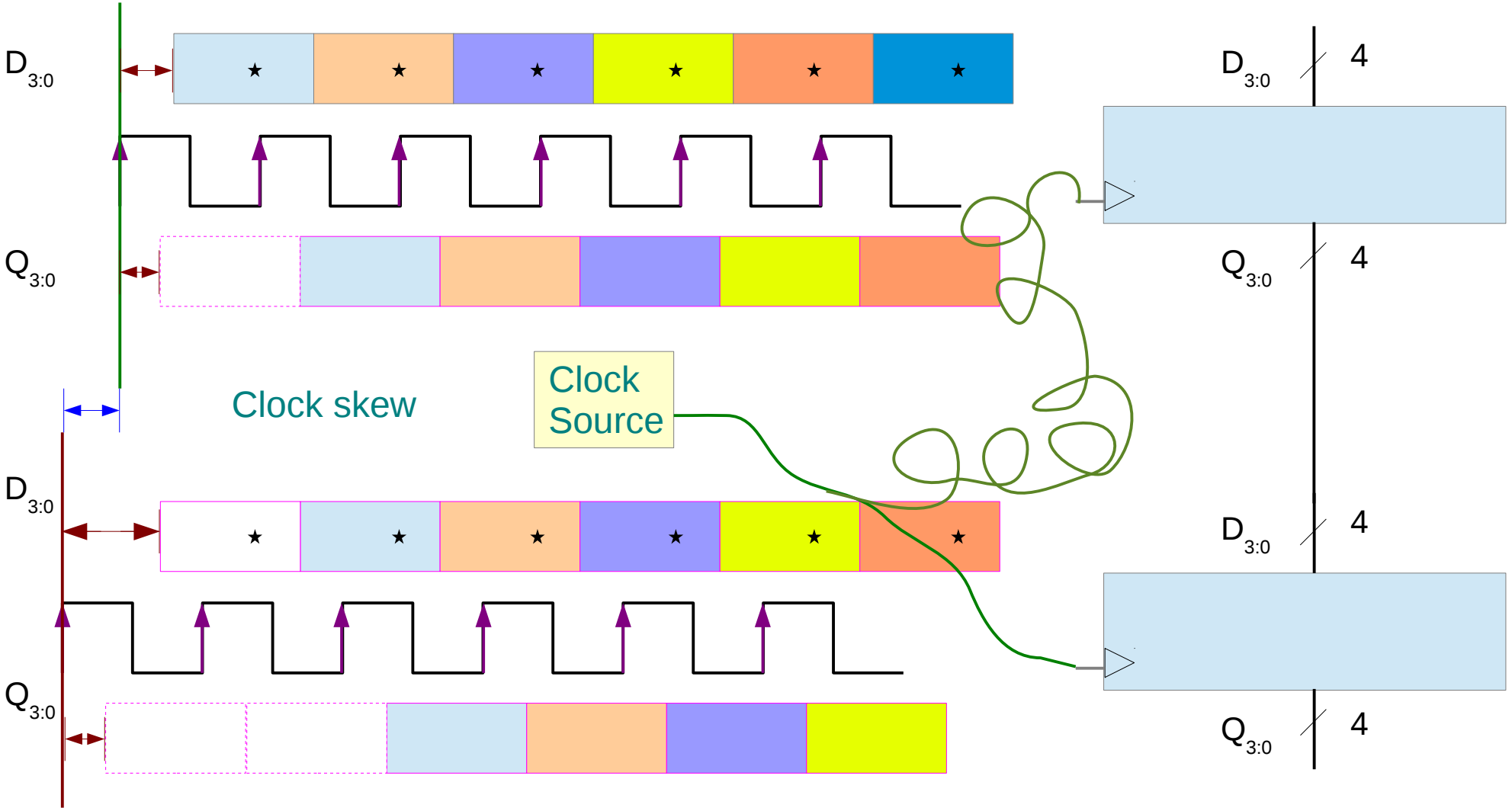
# FF Timing (Delay)



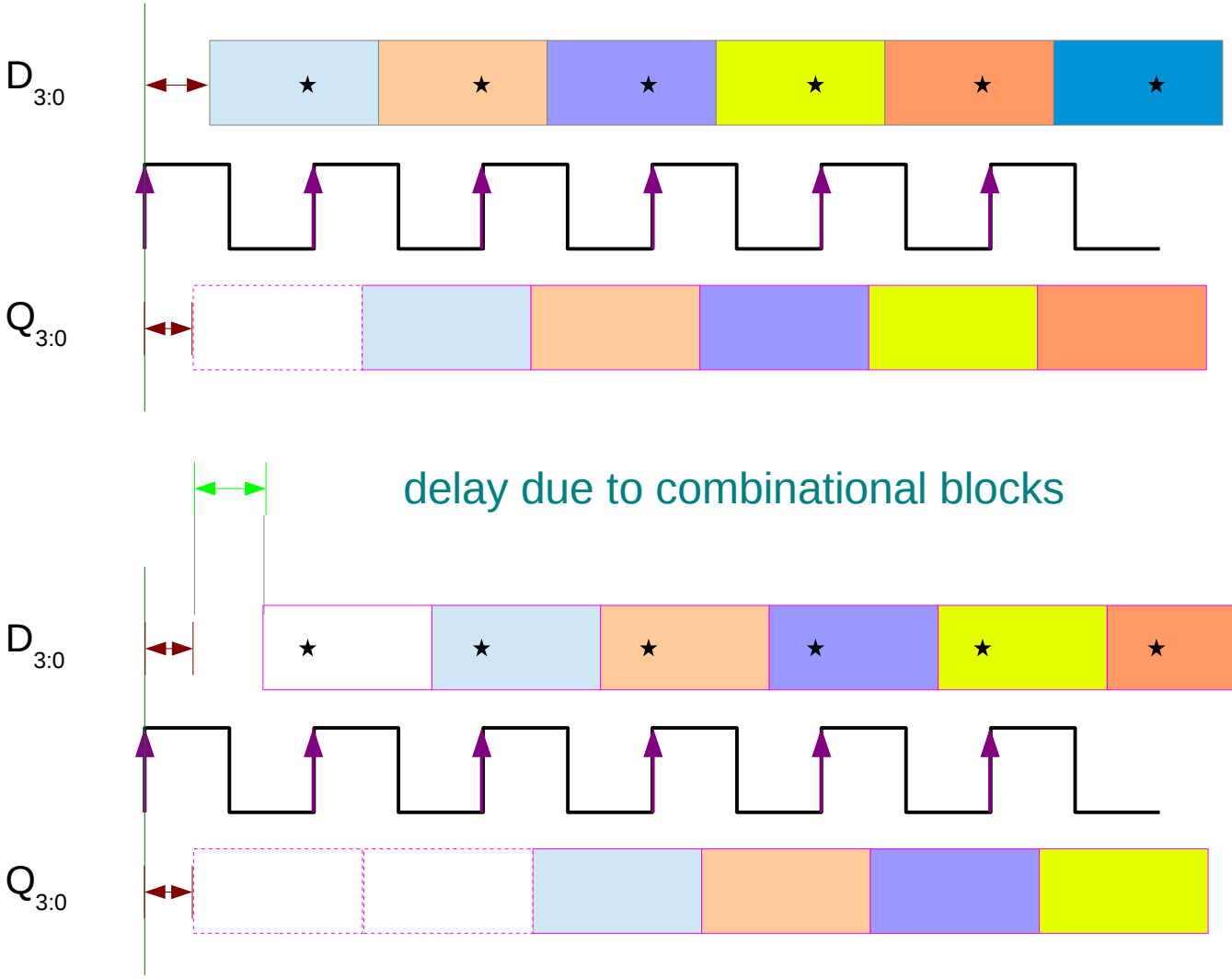



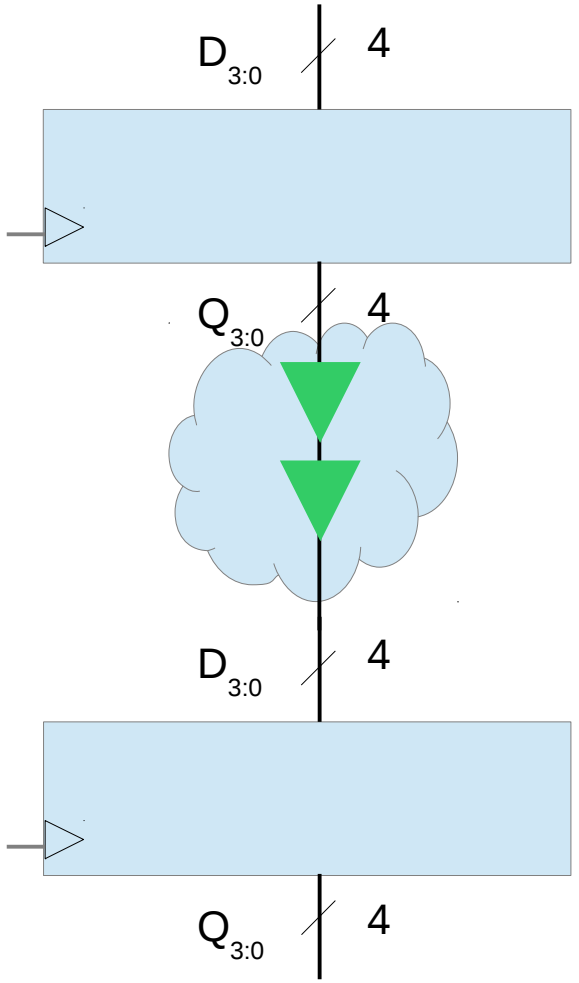



# Clock Skew

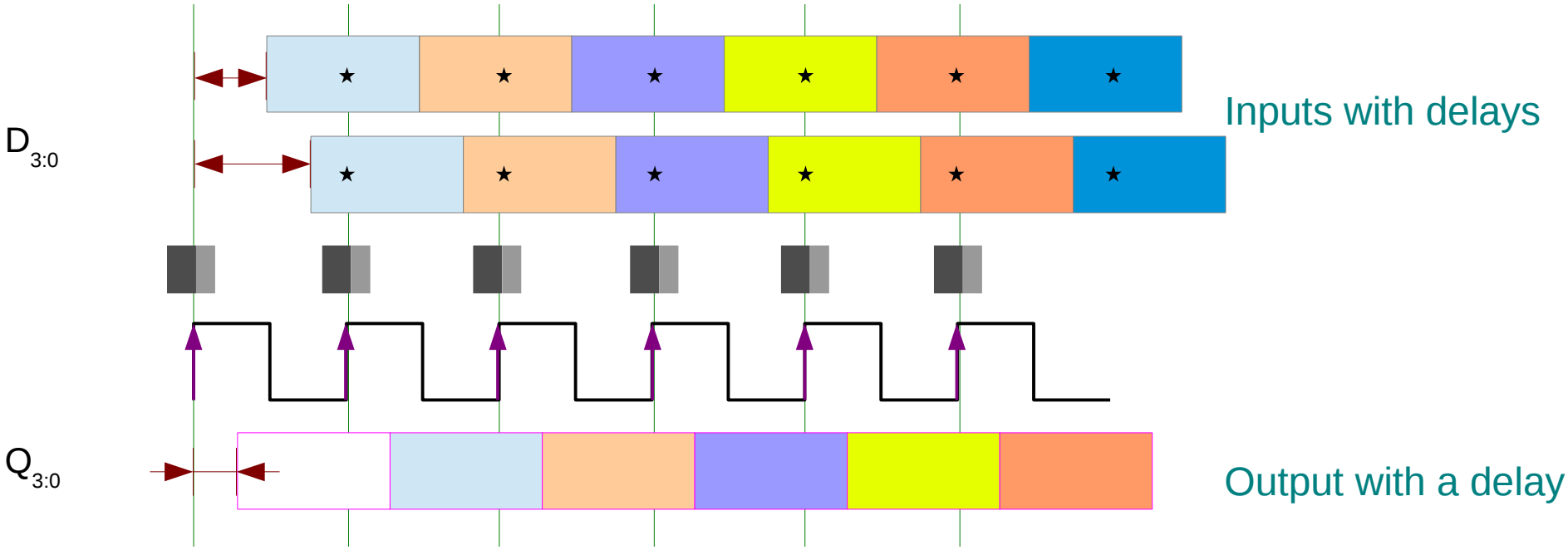


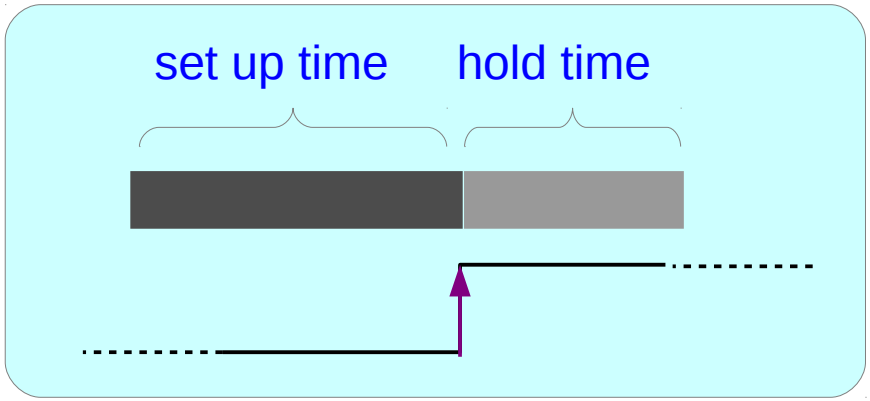
# Path Delay


D3:0
Q3:0
delay due to combinational blocks
D3:0
Q3:0

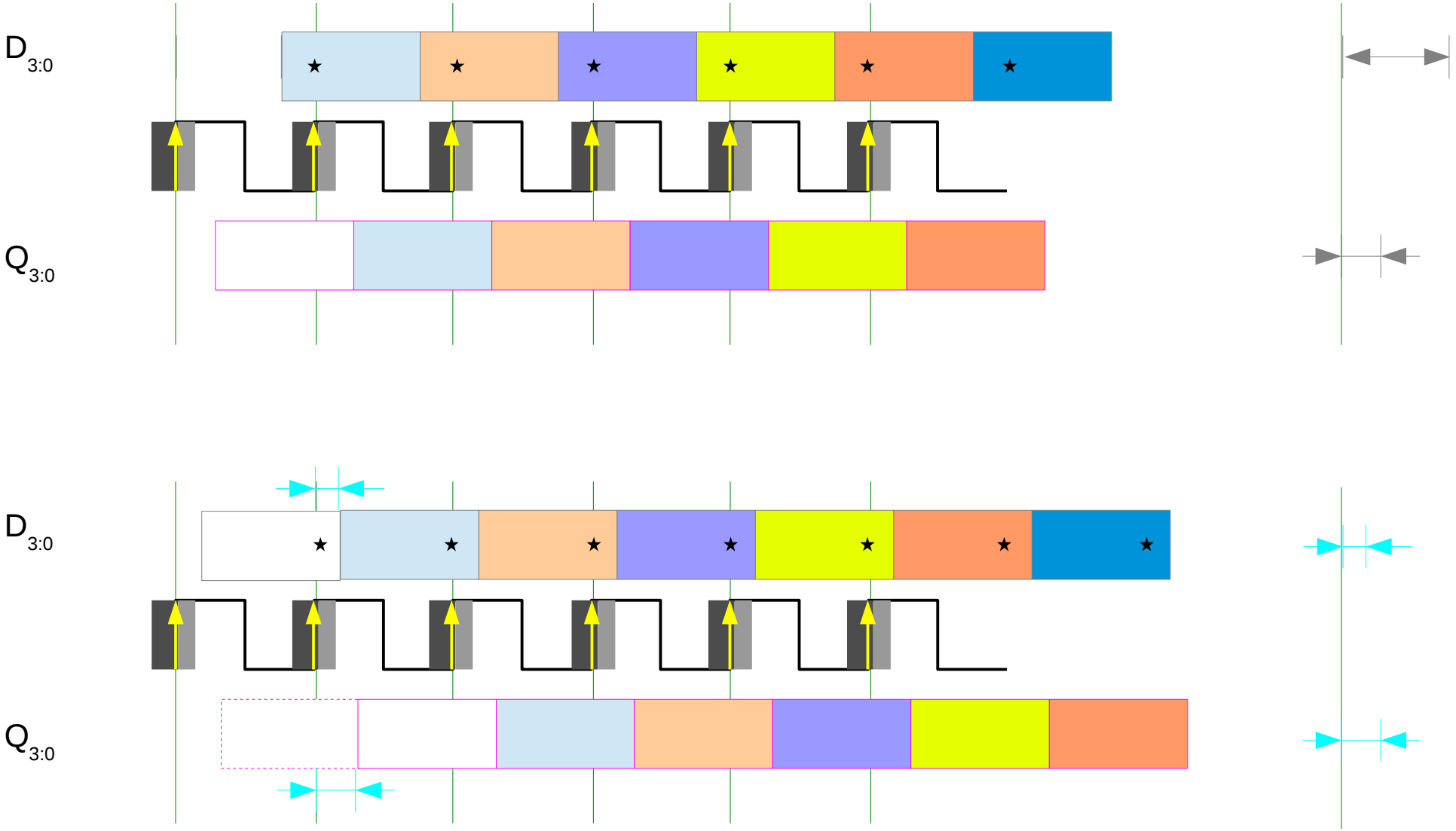

D3:0
4
Q3:0
4
D3:0
4
Q3:0
4

# Setup & Hold Time (1)

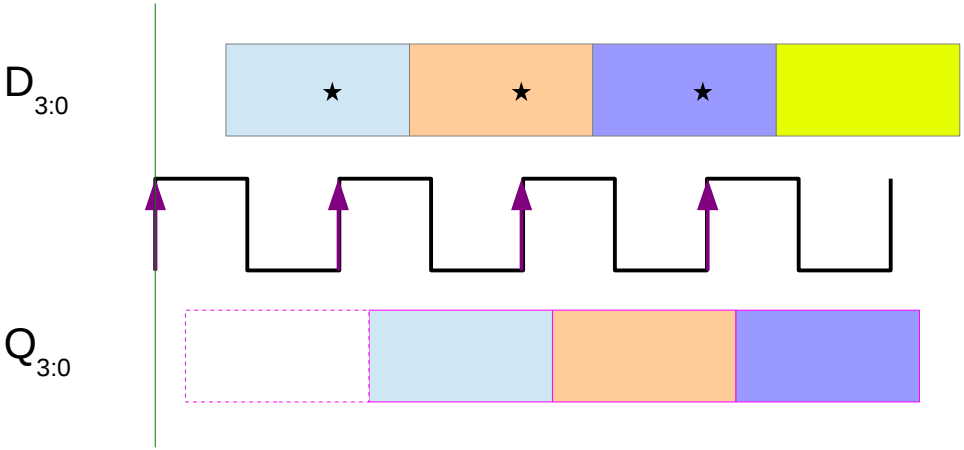


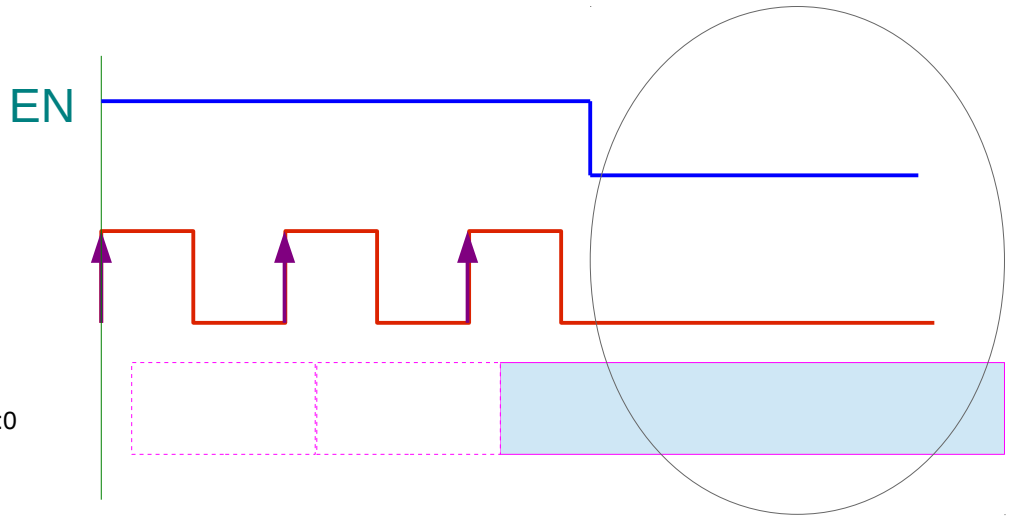



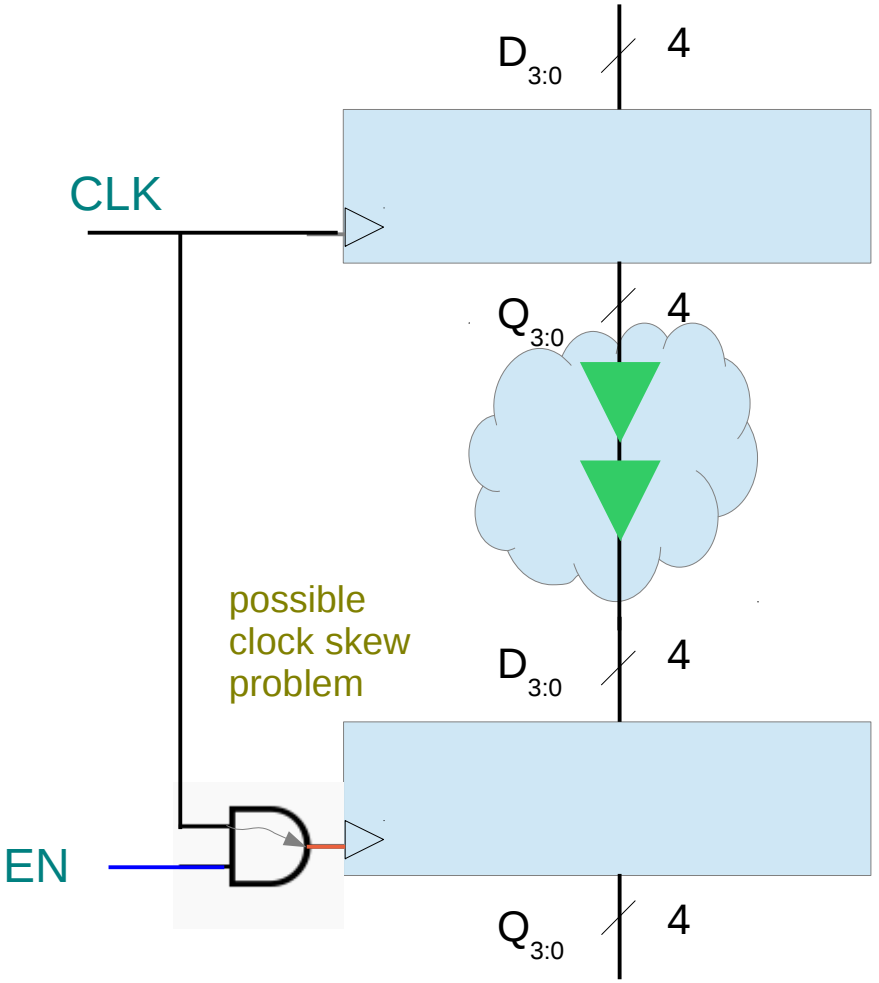
# Setup & Hold Time (2)



# Clock Gating



## References


[1] http://en.wikipedia.org/
[2] http://www.allaboutcircuits.com/
[3] W. Wolf, “Modern VLSI Design : Systems on Silicon
[4] N. Weste, D. Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”
[5] J. P. Uyemura, “Introduction to VLSI Circuits and Systems”