NAVAL POSTGRADUATE SCHOOL
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2 FSK/QPSK TRANSMITTER AND RECEIVER:
DESIGN AND PERFORMANCE

by

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and

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December 1987

Thesis Advisor: Glen A. Myers

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2 FSK/QPSK Transmitter and Receiver: Design and Performance

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ABSTRACT

This research considers a particular form of M-ary signaling called 2 FSK/QPSK. It is a unique way of combining two modulation methods to produce an 8-ary signaling technique whose noise performance is shown to be significantly better than 8-PSK. A transmitter and receiver for 2 FSK/QPSK is designed, built, tested and analyzed. Theoretical and experimental results are compared using a plot of probability of bit error versus signal-to-noise ratio (SNR). Known theoretical performance of 8-PSK is used for comparison. Results show a 5 dB theoretical improvement in SNR and a 3 dB experimental improvement of 2 FSK/QPSK relative to 8-PSK.

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A	Sinusoid Amplitude
AVM	Analog Voltage Multiplier
BW	Bandwidth
C	Capacitor
C_1, C_2	Output Voltage of Integrate and Dump Circuit
dB	Decibels
DL	Display Line
E_b	Energy Per Bit
E_s	Energy Per Symbol
FSR	Feedback Shift Register
f_1, f_2	One of Two FSK System Frequencies
Hz	Cycles Per Seconds (Hertz)
k	Bits Per Symbols
M	Number of States
MKR	Marker
μF	Microfarads
N	Noise Power
N_0	Noise Power Spectral Density
n(t)	Additive White Gaussian Noise (bandpass)
Ω	Ohms
P_e	Probability of Bit Error
R	Resistor
R_{xx}	Autocorrelation Function
r_b	Bit Data Rate
S	Signal Power
SNR	Signal-to-Noise Ratio

S_1, S_2	Output Voltage of Integrate and Dump Circuit
$s(t)$	Transmitted/Received Signal in Channel
σ^2	variance
T_s	Symbol Period
t	time
V	Volts
ω_1, ω_2	One of Two FSK System Frequencies in Radians/Sec.
$x(t)$	Lowpass Gaussian Noise Voltage
$y(t)$	Lowpass Gaussian Noise Voltage

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I. INTRODUCTION AND BACKGROUND

A. INTRODUCTION

Digital technology has created a growing need to transmit binary digits or bits. These may be sent over guided channels (twisted pair, coaxial cable, fiber), or wireless transmission may occur.

Wireless communication is bandpass signaling which uses a sinusoidal carrier occupying a specific frequency band. There are two common choices of bandpass signaling available when transmitting binary data.

1. Binary signaling requires two states of the carrier representing a one and a zero.

2. M-ary signaling groups k bits to define symbols which are each assigned to one of $M = 2^k$ carrier states.

This research considers a particular form of M-ary signaling.

B. BACKGROUND

With M-ary signaling, M symbols are sent. Each symbol is represented by a particular "state" of the carrier. Carrier states differ in amplitude, frequency or phase or combinations thereof. Each symbol is transmitted at a rate

of $1/T_s$ symbols/sec where T_s is the symbol interval. Since there are $k = \log_2 M$ bits per symbol, the bit rate is k/T_s bits/sec. The advantage of M-ary signaling over binary schemes is conservation of bandwidth which is determined by the switching rate of the carrier.

M-ary bandpass signaling is represented in several common forms such as binary phase shift keying (BPSK) when M = 2, quadrature phase shift keying (QPSK) when M = 4, eight-phase shift keying (8-PSK) and frequency shift keying (MFSK). With BPSK two phases (0 and π) of a sinusoidal carrier are used to represent two bits. QPSK uses four phases of a fixed frequency sinusoidal carrier to represent four different symbols. An example is shown in Figure 1.1. Frequency Shift Keying (MFSK), assigns M symbols to M carriers differing in frequency. An example is shown in Figure 1.2.

A well known and widely used method of M-ary signaling is 8-PSK. An example of a signal constellation of 8-PSK is shown in Figure 1.3. This communication scheme is similar to QPSK except that eight phases of the carrier represent eight different symbols. An 8-PSK system is compared with the subject of this research because the performance of 8-PSK is known, it is popular and it is an 8-ary system.

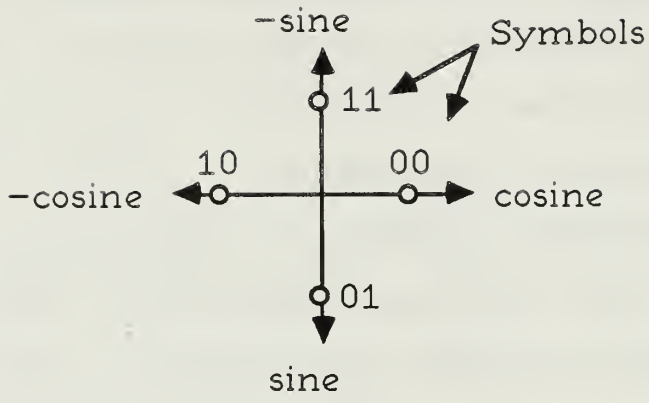


Figure 1.1 Diagram of the QPSK Signal Constellation

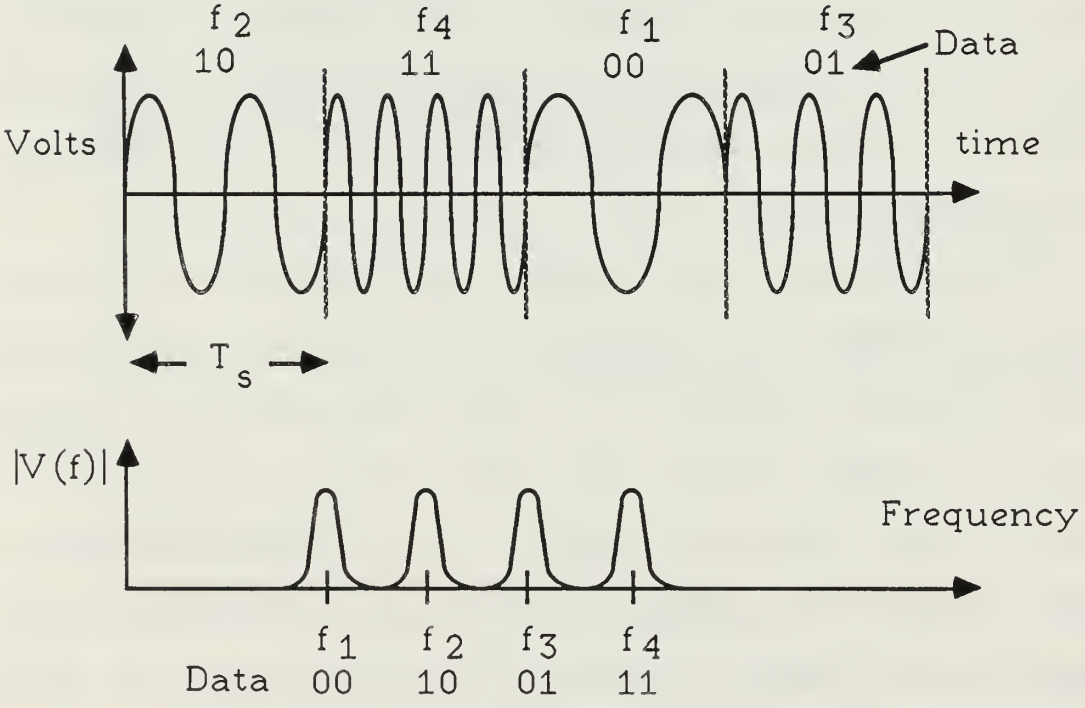


Figure 1.2 Diagram of the Time Domain and Frequency Spectrum of FSK

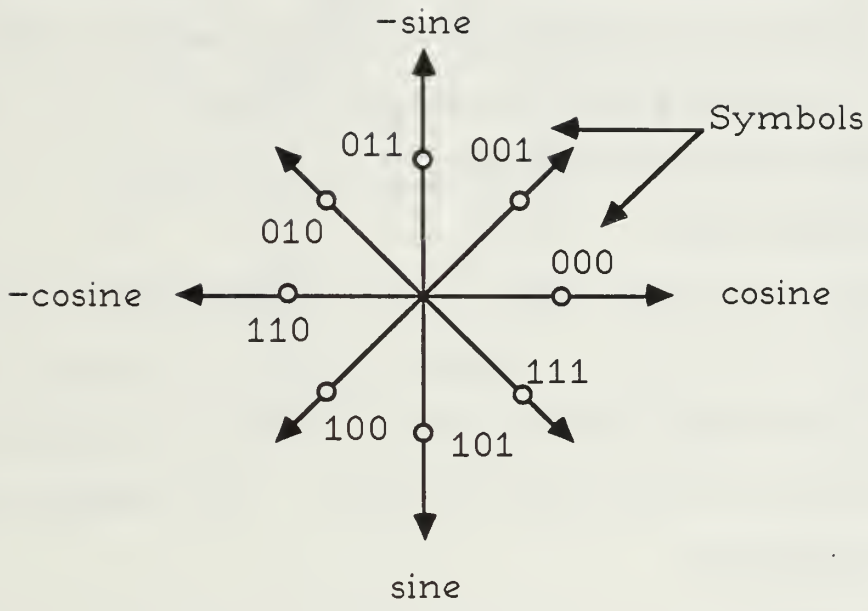


Figure 1.3 Diagram of the Signal Constellation of 8-PSK

1. 2 FSK/QPSK

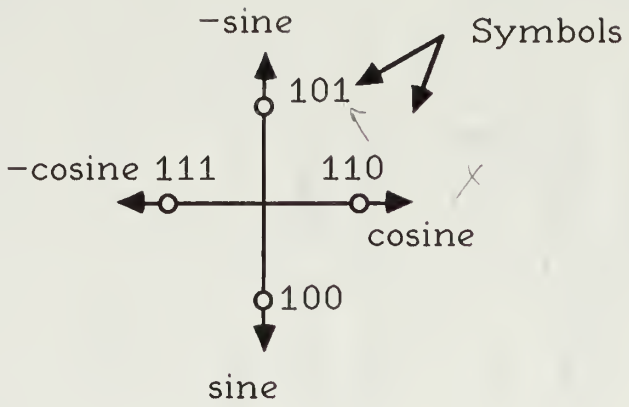
The modulation of the carrier waveform identifies the communication method as PSK or FSK. The methods of interest here are FSK and QPSK used together to create a composite modulation form. The system considered in this research uses two frequencies of the carrier with each having four possible phases as shown in Figure 1.4. This is called 2 FSK/QPSK in this report.

2. Transmitter

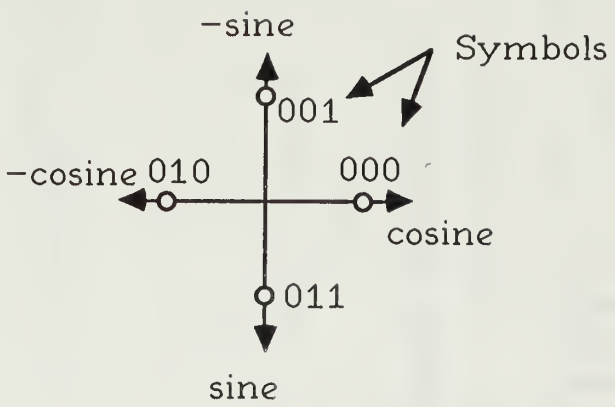
The transmitter design of the 2 FSK/QPSK system is a multiplexer as shown in Figure 1.5. The inputs to the multiplexer are eight different carriers; each is selected by a particular group of three bits of data. The selected carrier is then transmitted.

3. Channel

An ideal channel would carry the message to the receiver without errors. In practice, noise from the environment is added to the signal. This noise creates errors. A practical channel is modeled by adding Gaussian noise to the signal as shown in Figure 1.6. To simulate the action of an intermediate frequency (IF) amplifier in a typical superheterodyne receiver, the noise is bandpass filtered and amplified before addition with the signal.



Frequency 1



Frequency 2

Figure 1.4 Diagram of the 2 FSK/QPSK Signal Constellation

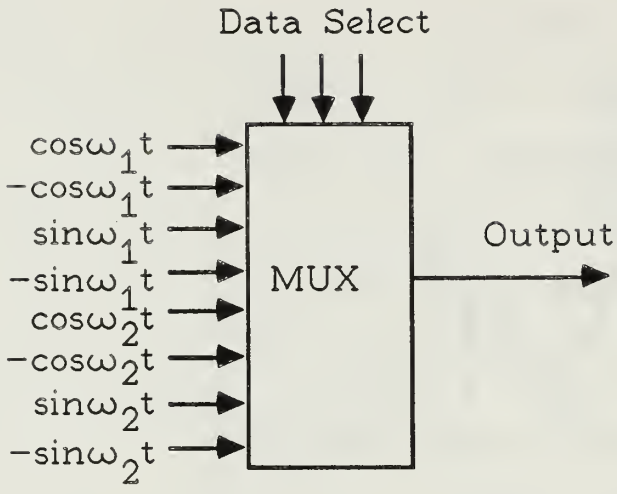


Figure 1.5 Design of the 2 FSK/QPSK Transmitter

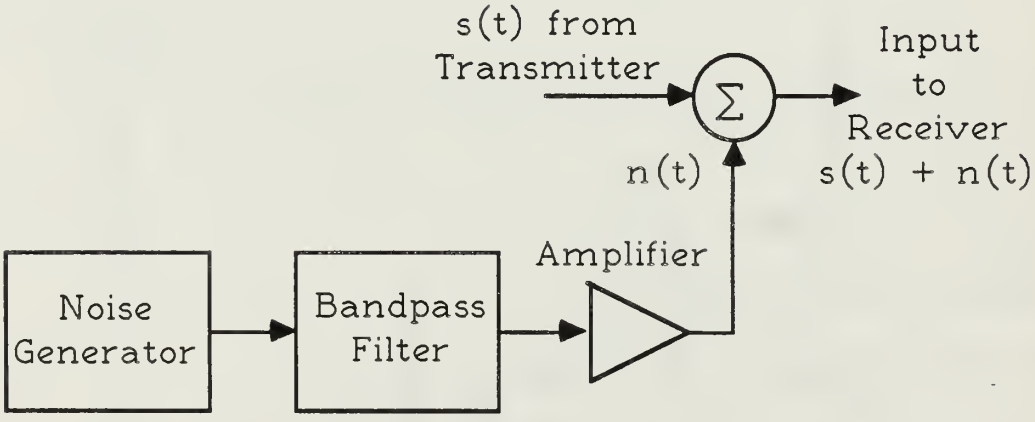


Figure 1.6 Design of the Channel Model

4. Receiver

Recovery of the bits of the 2 FSK/QPSK system is accomplished using a coherent receiver shown in Figure 1.7. There are three parts to the receiver: the demodulator, the integrate and dump circuit and the decoder. Demodulation occurs in four separate mixers having different local oscillators. Integration of the mixer output over the symbol period produces voltages which are summed in three channels of the decoder. The decoder uses a decision circuit in each channel to recover the bits directly. The entire receiver requires mixers, integrators, sample and dump pulses, summers, sample and hold circuits and comparators.

C. PLAN OF THE REPORT

This report presents a description of the research, the experimental system, test results, analysis, experimental performance and the conclusions.

The system design and description of the experimental hardware are considered in three parts; the transmitter, channel and receiver. Chapter II contains a description of system operation. Subsystems and bit error detection circuits are detailed in Chapter III, and test results are documented.

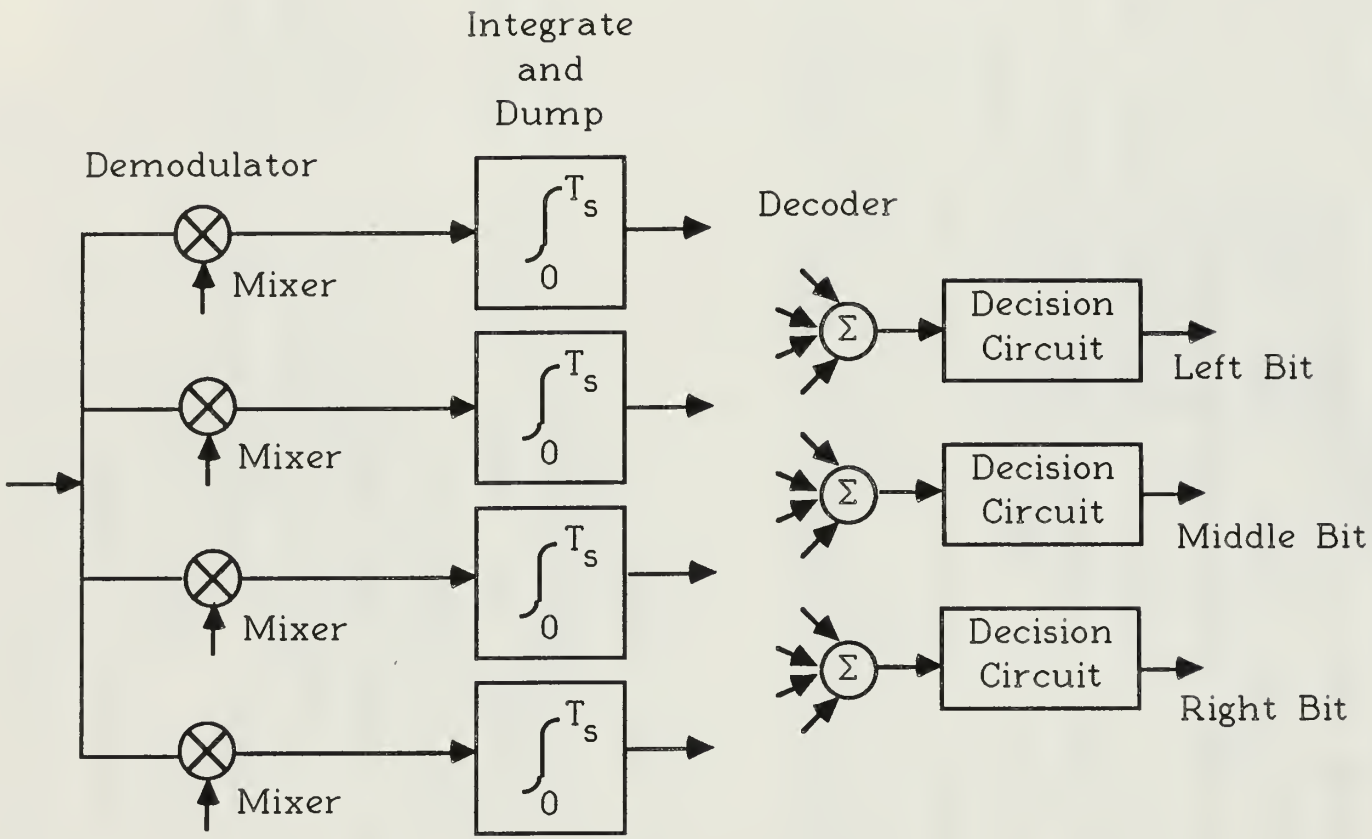


Figure 1.7 Design of the Coherent Receiver

In Chapter IV, the performance of the experimental system is compared with theory. The performance of the experimental system is compared with the theoretical performance of an 8-PSK system. Conclusions are drawn from these comparisons. Appendix A contains circuit schematics. Appendix B is a noise analysis of the 2 FSK/QPSK system.

II. DESCRIPTION OF RESEARCH

This chapter presents the theory of operation of the 2 FSK/QPSK system.

A. OBJECTIVE

This research measures and compares the performance of the 2 FSK/QPSK system by designing, building and testing a system. Performance is measured as probability of bit error versus receiver input signal to noise ratio. This same performance measure is determined analytically. These results are compared with the theoretical performance of an 8-PSK system.

B. SYSTEM DESIGN AND THEORY OF OPERATION

The experimental system consists of the transmitter, channel, receiver and bit error detection subsystems. These are discussed in this section.

1. Transmitter

An analog carrier is modulated by pseudo random data. Both the carrier and the random data are generated in the transmitter subsystem shown in Figure 2.1. Three data bits are transmitted as a symbol. Therefore, there are $2^3 = 8$ symbols and, hence, 8 carrier states. These

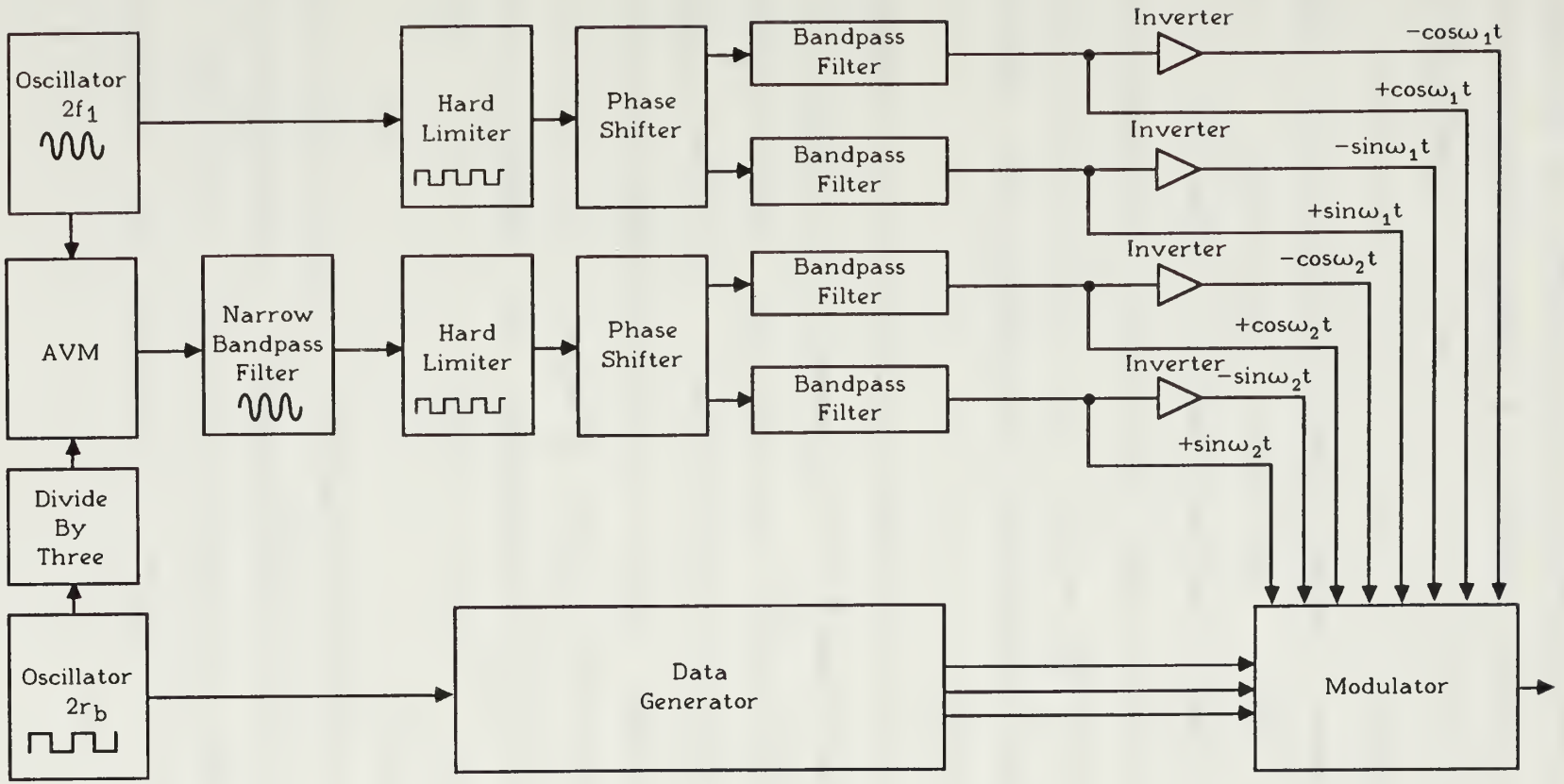


Figure 2.1 Block Diagram of the Transmitter

eight states are generated continuously in parallel. A multiplexer (analog switch) is used to implement the selection (transmission) of the carrier state corresponding to the symbol sent.

The pseudo random data is produced by a feedback shift register (FSR). The FSR has eight stages. Therefore, the output binary sequence repeats after $2^8 - 1 = 255$ symbols. The clock rate is the symbol rate of transmission. Three outputs of the possible eight from the FSR define the symbol. These three outputs are applied to the control lines of the multiplexer.

Two oscillators produce a square wave of frequency $1/T_s$ Hz and a sinusoid of frequency f_1 Hz where T_s is the duration of the symbol and f_1 is one carrier frequency. The square wave is the symbol clock. These two signals are mixed to generate another carrier of frequency $f_2 = f_1 + 1/T_s$ Hz. Then four phases of each of these carriers are created using digital techniques. The result is the eight carrier states.

2. Channel

In a typical communication system, noise is added to the signal prior to demodulation. In this experiment, this noise effect is duplicated by using a Gaussian noise generator and a summer. Broadband noise is filtered to

represent the action of an intermediate-frequency (IF) amplifier in a superheterodyne receiver.

3. Receiver

The receiver shown in Figure 2.2 consists of mixers, integrators, summers, and circuitry to recover the data bits.

Four mixers are used to demodulate the signal received from the channel. The coherent references required for the mixers are taken directly from the transmitter in this research. The output of each mixer is integrated over the symbol interval and then summed with like voltages from three other channels to recover one of the bits of the symbol. Summing four voltages permits use of a zero threshold for bit recovery. The output of each summer produces a positive or negative voltage, representing a binary one and a binary zero respectively. The bit is recovered directly using a comparator. This circuitry is repeated with appropriate inputs to the summer to directly recover the remaining two bits of the symbol.

Errors in data recovery are determined by comparing on a bit by bit basis each of the transmitted symbol components with the appropriate outputs of the three comparators. Counters record the errors and the total number of bits sent. The bit error ratio (BER) formed from these counts is the probability of bit error.

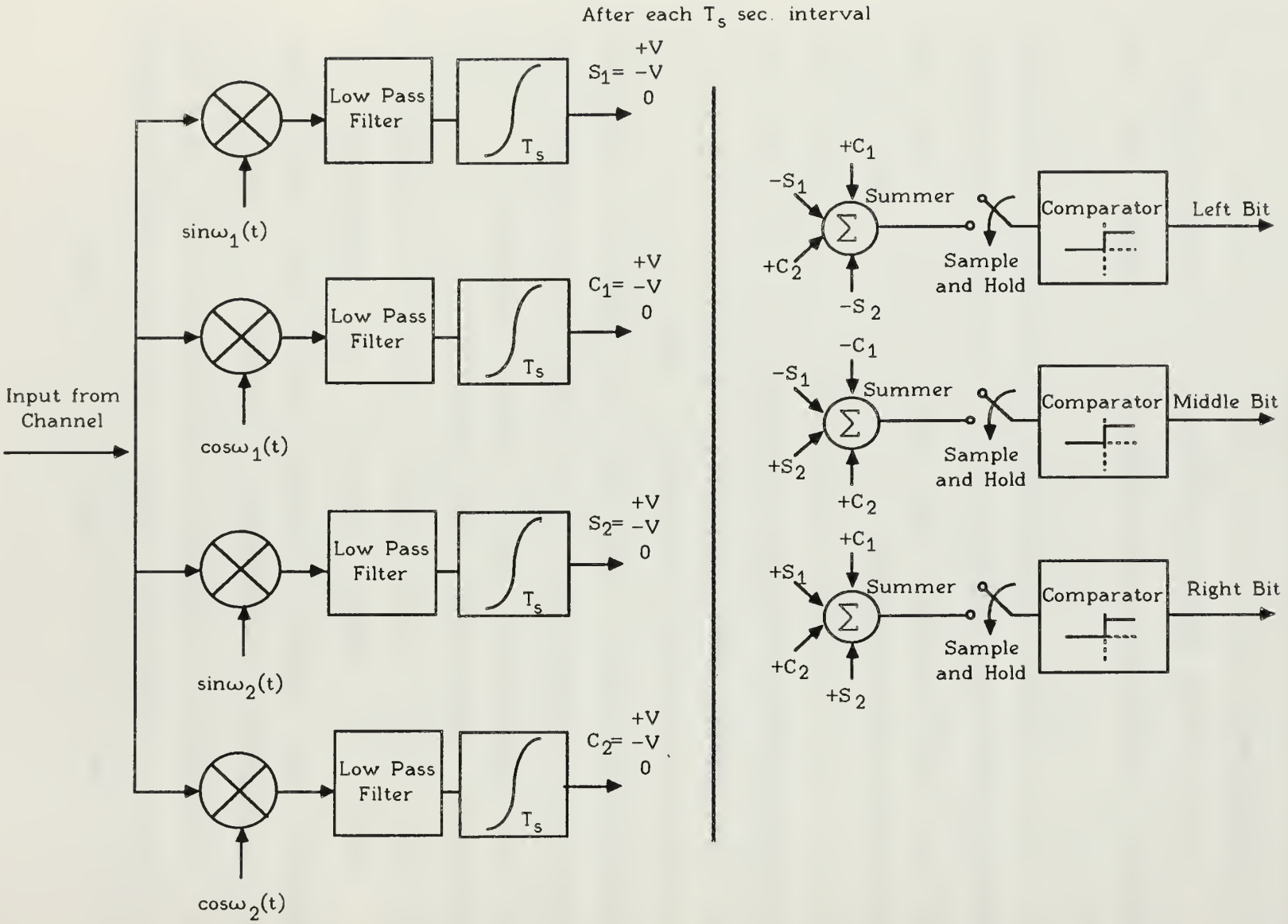


Figure 2.2 Block Diagram of the Zero Threshold Receiver

C. PERFORMANCE RESULTS

The analysis in Appendix B shows the 2 FSK/QPSK system to require about 5 db less signal power than 8-PSK for the same bit error ratio. Experimental results differ from theory by about 2 db.

III. EXPERIMENTAL SYSTEM AND RESULTS

The experimental system was built, using standard linear and TTL integrated circuits, on "bread boards" and interfaced with various test equipment. The system consists of the transmitter, channel, receiver and bit error detection subsystems. This chapter discusses the design and operation of each subsystem.

A. TRANSMITTER

The transmitter consists of the data generator and the modulator as shown in Figure 2.1.

1. Data Generator

In a 2 FSK/QPSK system, symbols are sent. Each symbol represents one of eight different combinations of three simultaneous data bits. To accurately test the system, it is desirable to have the symbols occur in a random manner. Therefore, it is necessary to generate a data stream of random bits at a rate of $r_b/3$ bits per second and convert them to symbols. This is accomplished using a feedback shift register (FSR) as shown in Figure 3.1. The FSR is clocked externally by a square wave oscillator having a frequency of 4 kHz = $2r_b$.

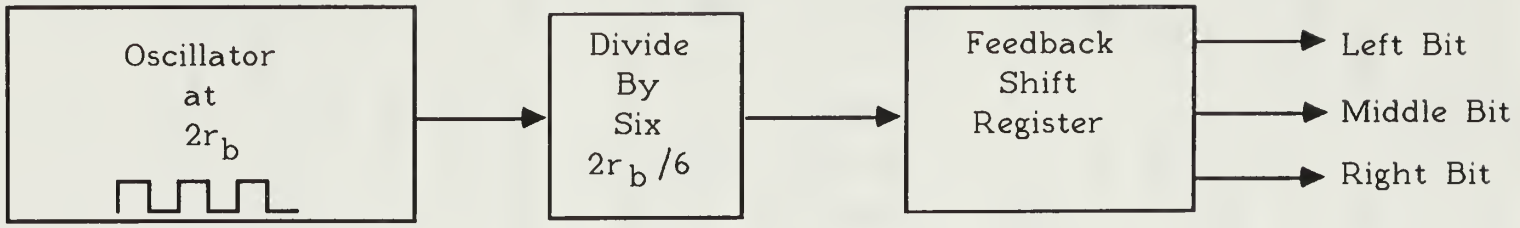


Figure 3.1 Block Diagram of the Data Generator

The feedback shift register produces a pseudo-random data stream. An all zero state in the data stream is not allowed because of the use of exclusive-or (XOR) gates in the FSR. Should a FSR erroneously register all zeroes, the FSR must be reset so that the psuedo random sequence can continue. To reset the FSR, an "all zeroes detector" circuit is implemented.

Three bits select any one of eight analog carriers at the system bit rate ($r_b/3$). This is accomplished by using an analog switch (multiplexer).

2. Modulator

Digital data is used to modulate analog carriers in an M-ary bandpass signaling scheme. In this research, the analog carrier consists of one of two sinusoids of differing frequencies, each having four possible phases. The method by which these two sinusoids and their phases are generated is described in this section.

a. Sinusoid of Frequency f_1 Hz

The sinusoid of frequency f_1 Hz is generated by hard limiting and filtering a sinusoid of twice the frequency, $2f_1$ Hz. A double frequency is chosen to provide sine and cosine terms as discussed in the description of the phase shifter. Figure 3.2 illustrates the generation of a sinusoid of frequency f_1 Hz.

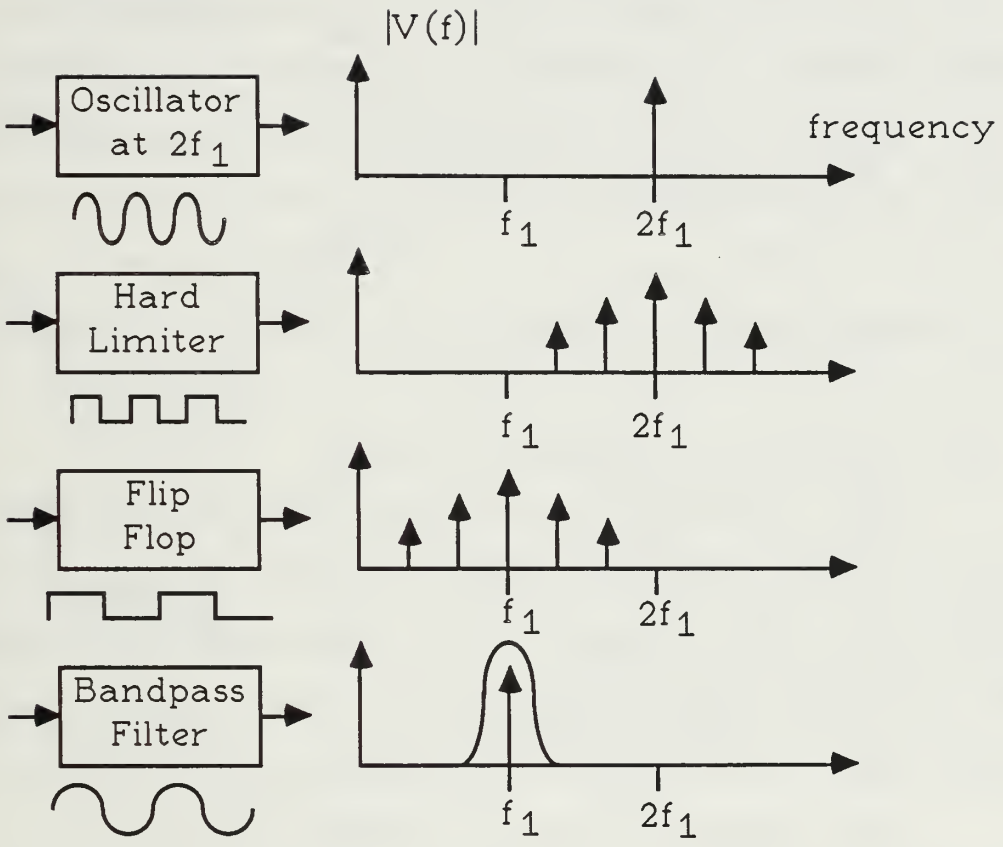


Figure 3.2 Frequency Spectra

In Figure 3.2, an oscillator at frequency $2f_1$ Hz creates a sinusoid which is applied to a hard limiter producing a square wave of frequency $2f_1$. The square wave frequency is divided by two by an edge-triggered flip flop. The resulting square wave of frequency f_1 Hz is bandpass filtered to produce the desired sinusoid of frequency f_1 Hz, which is referred to as v_1 throughout the remainder of this paper. Generating v_1 provides only one of the carriers necessary for the 2 FSK/QPSK system. The other is provided by generation of a sinusoid of frequency f_2 Hz.

b. Sinusoid of Frequency f_2 Hz

The process of producing v_2, a sinusoid of frequency f_2 Hz, is more involved than the process of producing v_1. The sinusoid v_2 is generated by mixing, filtering, hard limiting, phase shifting, and again filtering two analog waveforms. Figure 3.3 illustrates this process.

Two analog waveforms are multiplied using an analog voltage multiplier (AVM). The waveforms shown in Figure 3.4, a sinusoid and a square wave, are generated by two oscillators set at frequencies $2f_1$ Hz and $2r_b/3$ Hz respectively. The product signal, also shown in Figure 3.4, is bandpass filtered at a center frequency of $2f_1-2r_b/3$ Hz. Filtering recovers a sinusoid at frequency $2f_1-2r_b/3 = 2f_2$ Hz.

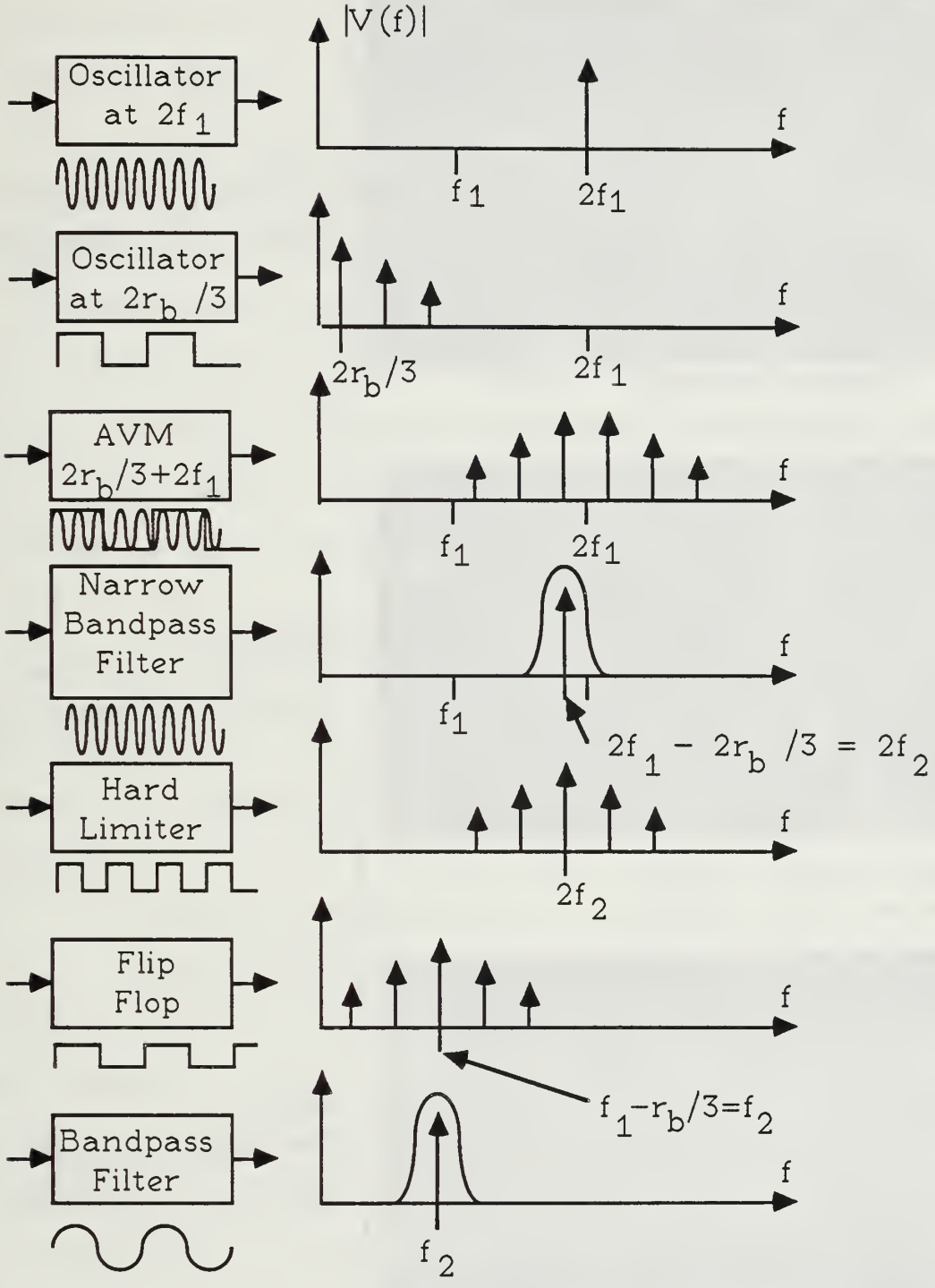
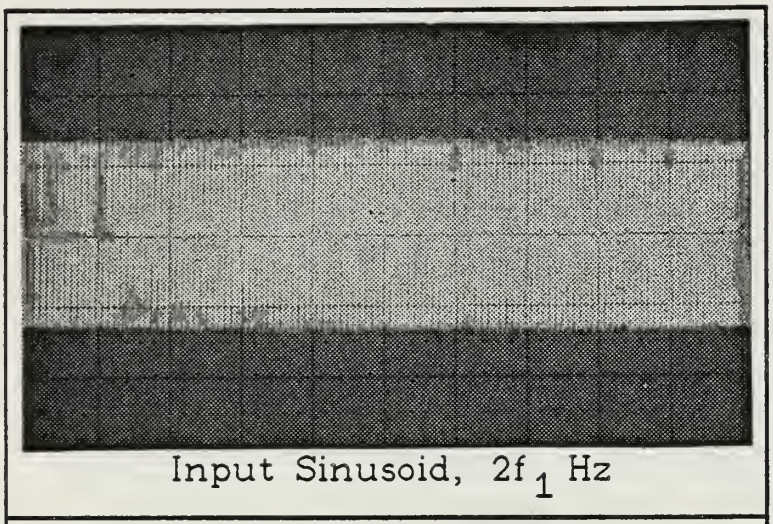
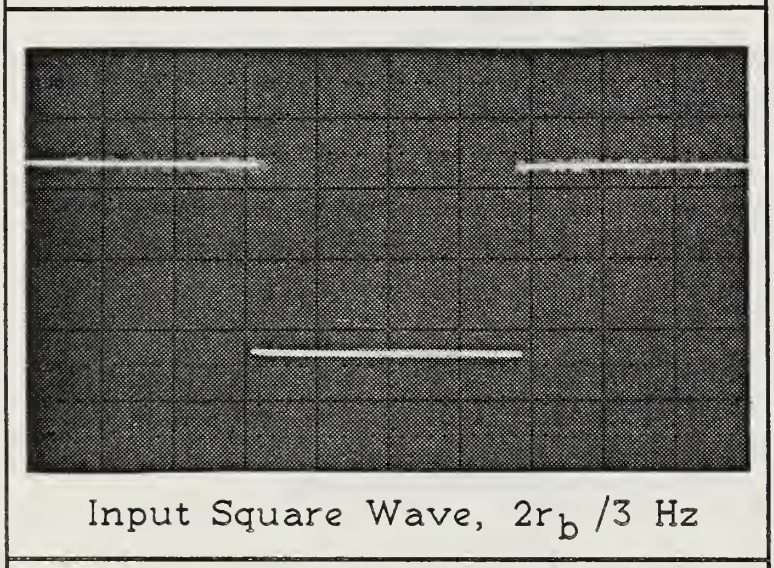


Figure 3.3 Frequency Spectra



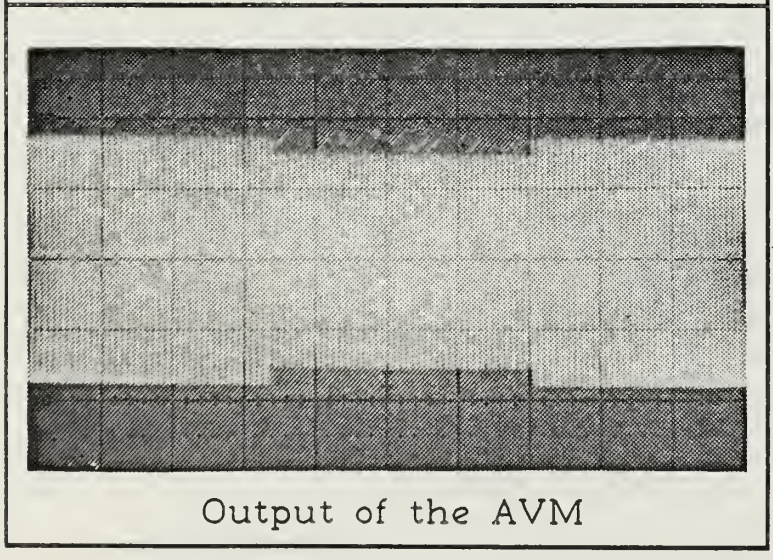
Input Sinusoid, $2f_1$ Hz

Scale
Vertical: 5 V/div
Horiz: 0.1 msec/div



Input Square Wave, $2r_b/3$ Hz

Scale
Vertical: 5 V/div
Horiz: 0.1 msec/div



Output of the AVM

Scale
Vertical: 5 V/div
Horiz: 0.1 msec/div

Figure 3.4 Waveforms of the Transmitter AVM

The remaining process is similar to that found in the generation of v_1. Hard limiting produces a square wave of frequency $2f_2$ Hz. The square wave frequency is divided by two using an edge-triggered flip flop. The resulting square wave, of frequency f_2 Hz, is bandpass filtered to produce the desired sinusoid v_2 of frequency $f_1 - r_b/3 = f_2$ Hz. Four different phases of each of these two sinusoids are then created using a phase shifter.

Observe that $f_2 - f_1 = r_b/3$ = symbol rate = $1/T_s$. This condition guarantees that v_1 and v_2 are orthogonal on any symbol interval of Ts seconds. That is,

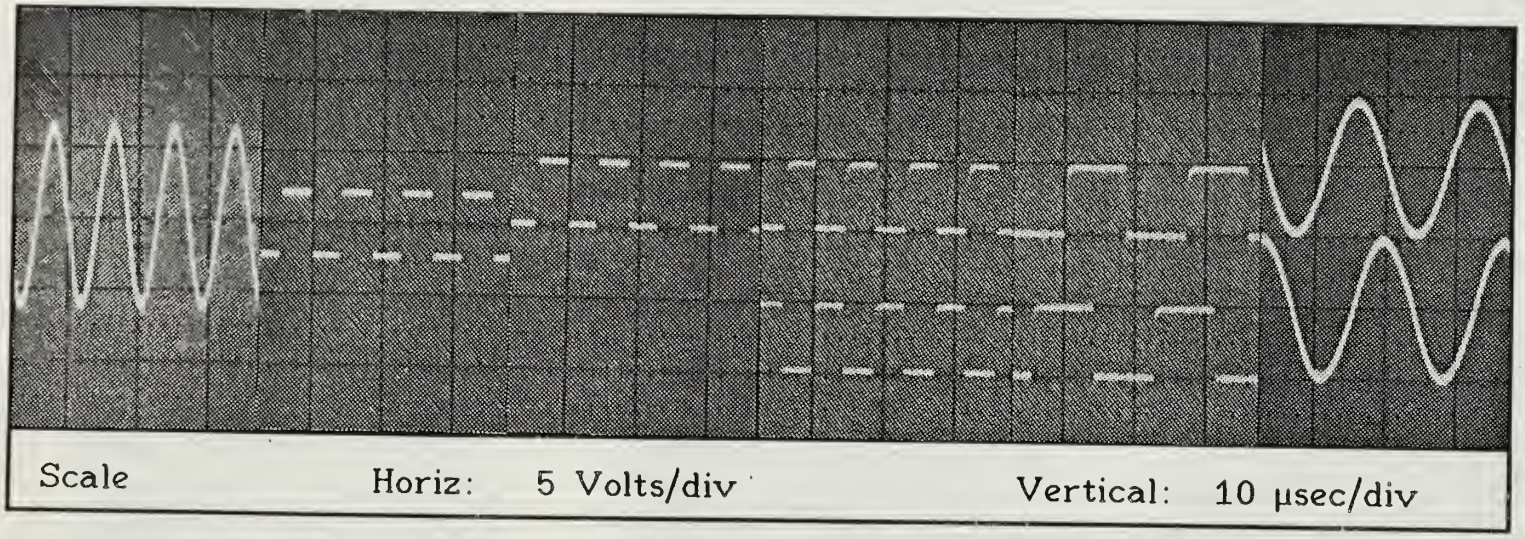
$$\int_0^{T_s} v_1(t)v_2(t)\,dt \rightarrow \int_0^{T_s} \cos 2\pi(f_1-f_2)t \;\; dt$$

which is the area of one cycle of a sinusoid. This area is always zero, independent of the "phase" of that cycle on the interval.

c. Phase Shifter

The 2 FSK/QPSK system requires the four phases of v_1 and v_2 to be generated and available for modulation. Phase shifting v_1 and v_2 is accomplished through the use of a hard limiter, a bipolar to unipolar converter, an inverter, flip flops and bandpass filters. The process of shifting the phase of v_1 and v_2 is illlustrated in Figure 3.5.

Phase shifting is performed by converting the analog signal to a digital form, phase shifting the digital signal, and



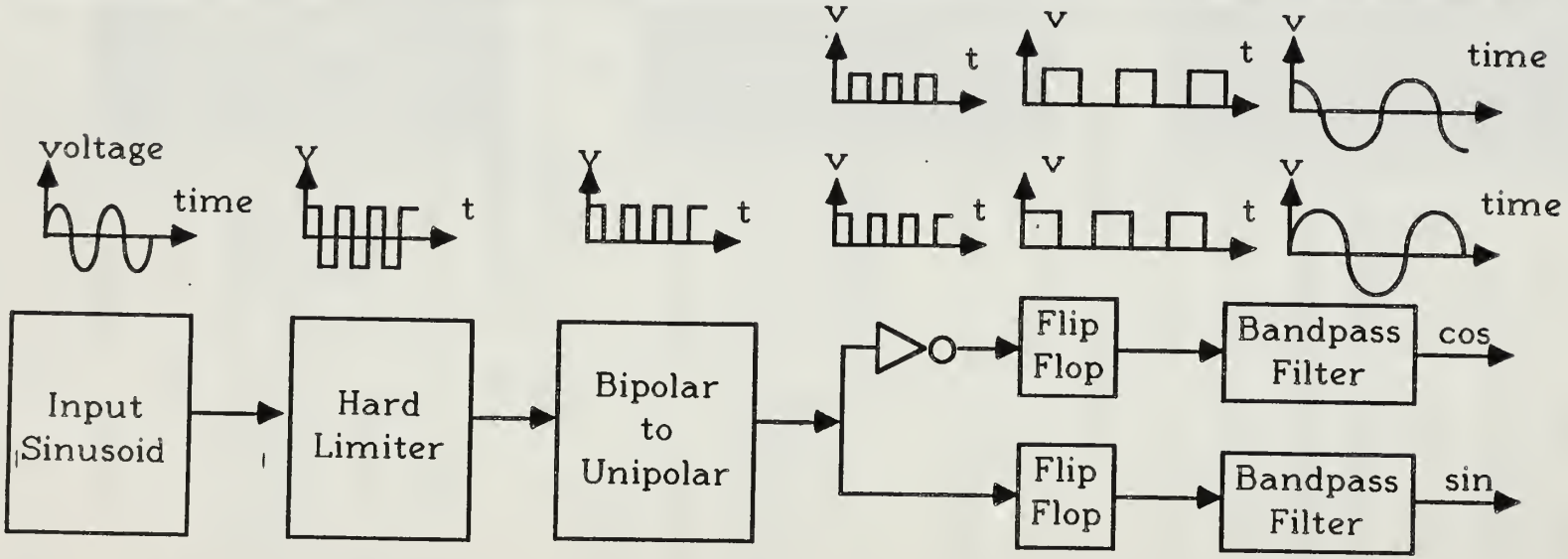


Figure 3.5 Block Diagram of the Phase Shifter

converting the digital signal back to an analog signal. A sinusoid, at a frequency of either $2f_1$ Hz or $2f_2$ Hz is hard limited. A sinusoid of twice the desired frequency is used because the flip flops divide by two to produce a phase shift. In this case, hard limiting is analog-to-digital conversion.

The square wave is converted to digital form for TTL compatibility. The digital square wave is inverted causing a 180 degree phase shift from the original digital square wave. In turn, the original and inverted digital waveforms are fed into leading-edge-triggered flip flops, causing a 90 degree phase difference. A 90 degree phase shift occurs because the flip flops act as divide-by-two circuits, thereby halving the frequencies and the 180 degree phase shift.

The phase shifted digital square waves are bandpass filtered, representing a conversion back to analog. The sinusoids produced represent the sine and cosine signals at frequency f_1 Hz or f_2 Hz. The other signals, -sine and -cosine, are produced using analog inverters.

The end result is that eight carriers, represented by eight unique states of phase and frequency, are available for transmission.

3. Multiplexer

Eight carriers are fed into a 3 x 8 multiplexer so that the data is transmitted by selecting one of the carriers

with the psuedo random data symbols. The bit assignment is shown in Table 3.1. An analog multiplexer represents a switch whose output is selected by the symbol appearing at the data selection inputs. Carriers are modulated in this manner at the symbol rate = $r_b/3$ symbols per second.

B. CHANNEL

The channel is depicted in Figure 3.6. A Gaussian noise generator is used to provide a method of judging the performance of the system in the presence of random noise. The noise is bandlimited by a bandpass filter, amplified and summed with the signal. After filtering and summing, the noise plus signal voltage is applied to the demodulator.

C. RECEIVER

Analog signals are received via the channel for demodulation and decoding so that bits may be recovered. The entire process requires mixers, integrators, sample and dump pulses, summers, sample and hold circuits and comparators. These are all components of three subsystems: the demodulator, the integrate and dump circuitry, and the bit detection system. A description of these three subsystems follows.

1. Demodulator

Demodulation occurs when the analog signals are received and simultaneously mixed with four different local

TABLE 3.1 BIT ASSIGNMENT FOR MULTIPLEXING

Code Word			
Left Bit	Middle Bit	Right Bit	Code Assignment
0	0	0	$-\cos\omega_2 t$
0	0	1	$+\sin\omega_1 t$
0	1	0	$-\cos\omega_1 t$
0	1	1	$+\sin\omega_2 t$
1	0	0	$-\sin\omega_2 t$
1	0	1	$+\cos\omega_1 t$
1	1	0	$-\sin\omega_1 t$
1	1	1	$+\cos\omega_2 t$

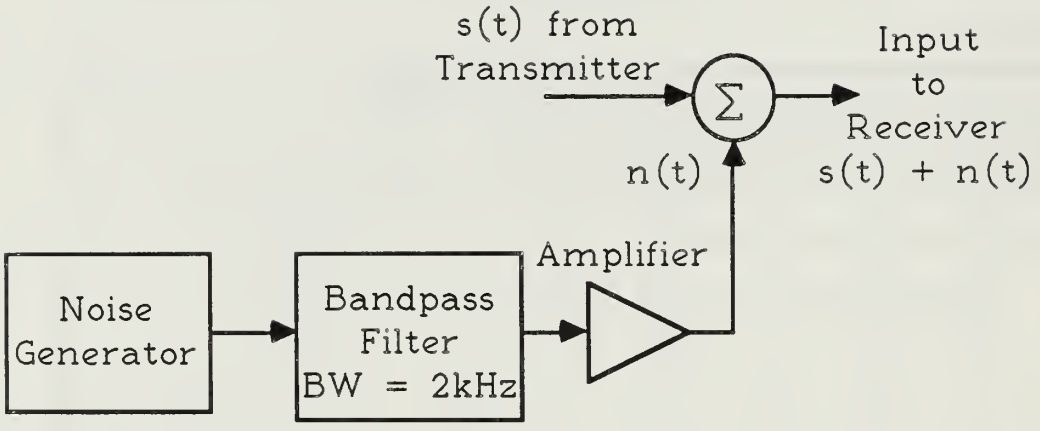


Figure 3.6 Block Diagram of the Channel Model

oscillators (LO's). This demodulation is achieved through the use of AVM's as mixers and the sinusoids $\cos\omega_1 t$, $\sin\omega_1 t$, $\cos\omega_2 t$, and $\sin\omega_2 t$ as LO's as shown in Figure 2.2. The output of each mixer is low pass filtered and integrated over the symbol interval of T_s sec.

2. Integrate and Dump Circuit

Integration of the mixer outputs over the symbol interval produces any one of three voltage levels, depending upon which analog symbol is sent. Regardless of which analog symbol is sent, the output of one of the four integrate and dump circuits at the end of one symbol interval is always a positive or negative voltage. The remaining three integrate and dump outputs are zero volts. The outputs of the mixer and integrate and dump are described on a case by case basis.

There are eight different possible combinations produced at the output of each of the mixers. In turn, each of these produces a particular output in the integration process. We examine all cases in which the received signal is mixed with the LO of $\sin\omega_1 t$.

Case 1. Assume that $\sin\omega_1 t$ is received. The analytical expression for the output of the mixer is

$$\sin\omega_1(t)\sin\omega_1(t) = \frac{1}{2}\left(1-\cos 2\omega_1 t\right). \qquad (3.1)$$

The trigonometric expression in Equation 3.1 produces a DC term and double frequency term. The time domain descriptions of the output of the mixer and the integrate and dump are shown in Figure 3.7. In all cases, a received signal identical to the LO voltage integrates to a positive voltage over the symbol interval T_s sec. The result of integrating the double frequency term is negligible because $f_1 >> 1/T_s$.

Case 2. Assume that $-\sin\omega_1 t$ is received. The analytic expression for the output of the mixer is

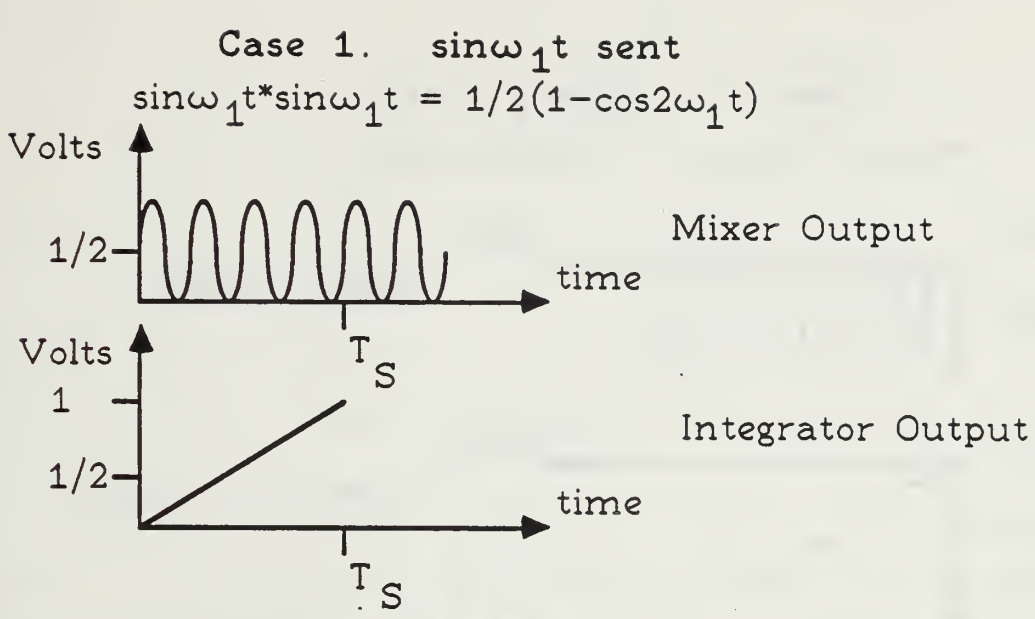
$$-\sin\omega_1(t)\sin\omega_1(t) = -\frac{1}{2}\left(1-\cos 2\omega_1(t)\right). \quad (3.2)$$

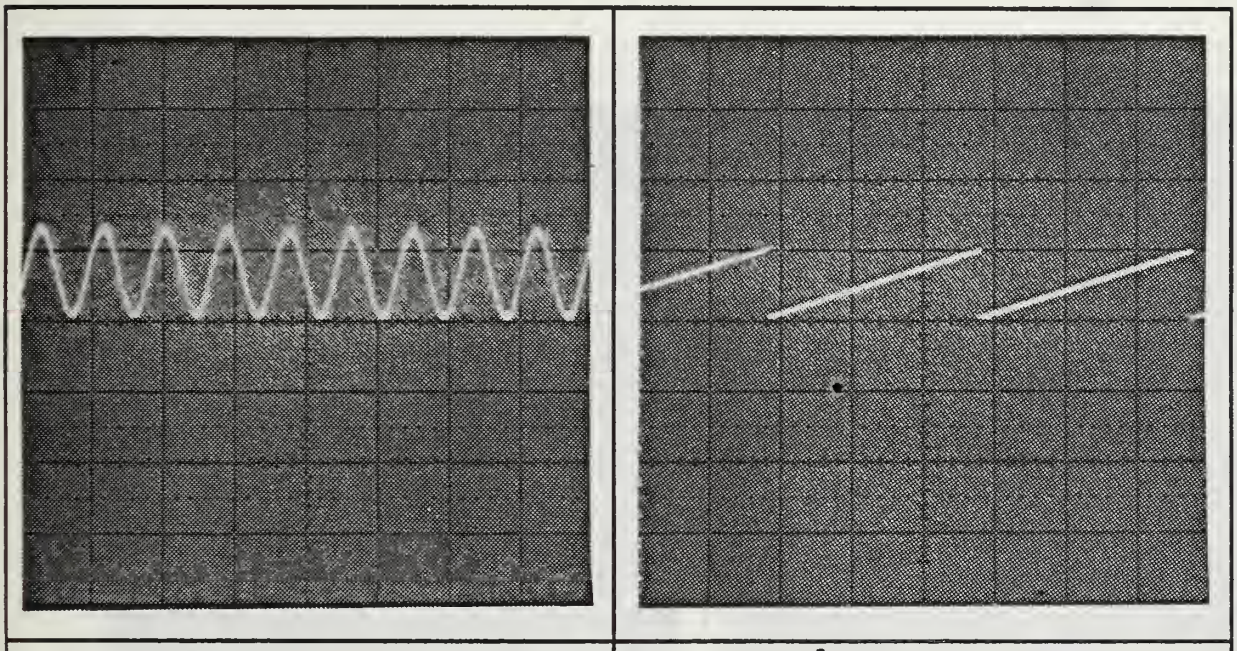
As in Case 1, a DC term and double frequency term are produced. The time domain descriptions are shown in Figure 3.8. In this case, a received sinusoid which is different in phase by 180 degrees from the LO voltage produces a negative voltage at the output of the integrate and dump circuit.

Cases 3 and 4. Assume that $\pm\cos\omega_1 t$ is received. The analytic expression for this case is

$$\pm\cos\omega_1(t)\sin\omega_1(t) = \pm\frac{1}{2}\left(\sin 2\omega_1(t)\right). \quad (3.3)$$

The trigonometric expression in Equation 3.3 produces a double frequency term. Integrated over T_s sec. the double frequency term attenuates to zero because the



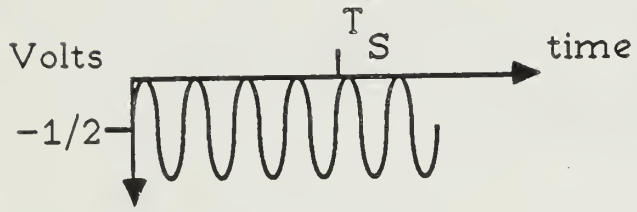


Mixer	Integrator
Vert: 2 V/div	Vert: 5 V/div
Horiz: 10 μsec/div	Horiz: 0.5 msec/div

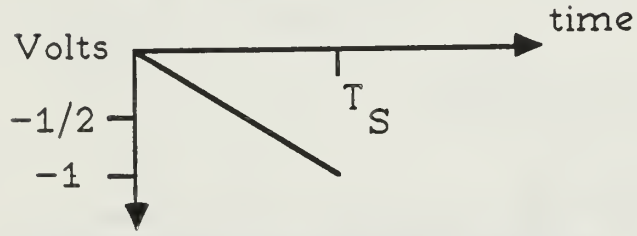
Figure 3.7 Case 1. Mixer and Integrator Output

Case 2. $-\sin\omega_1 t$ sent

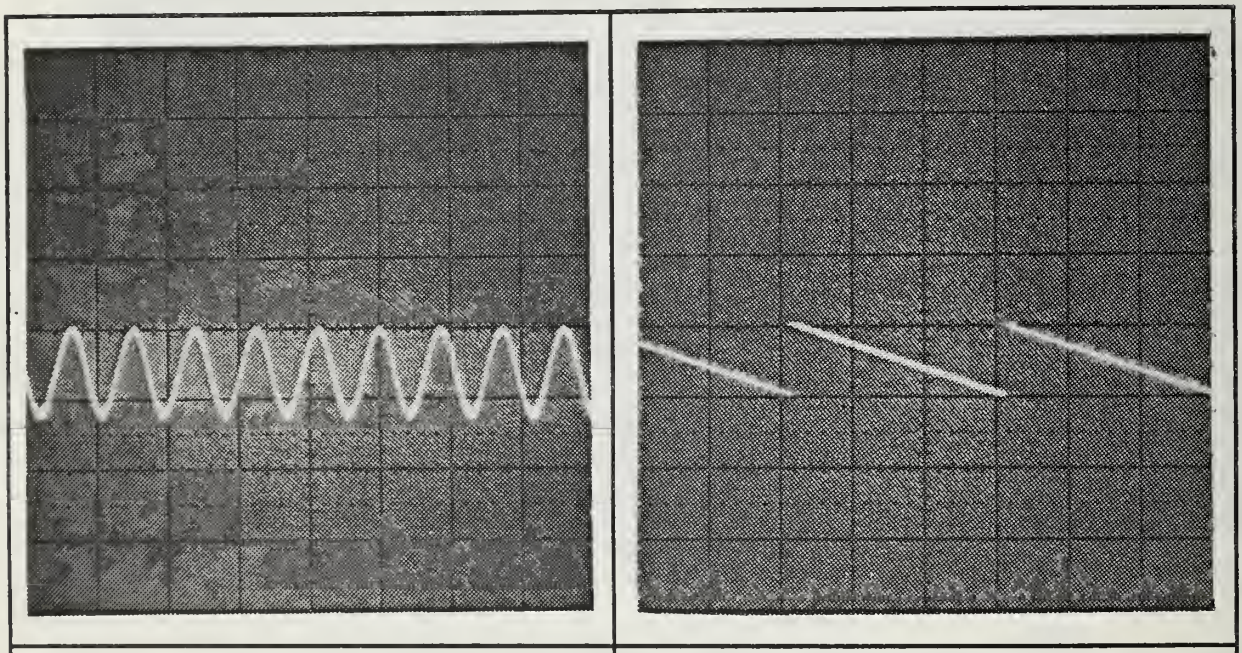
$-\sin\omega_1 t * \sin\omega_1 t = -1/2(1-\cos 2\omega_1 t)$



Mixer Output



Integrator Output



Mixer	Integrator
Vert: 2 V/div	Vert: 5 V/div
Horiz: 10 μsec/div	Horiz: 0.5 msec/div

Figure 3.8 Case 2. Mixer and Integrator Output

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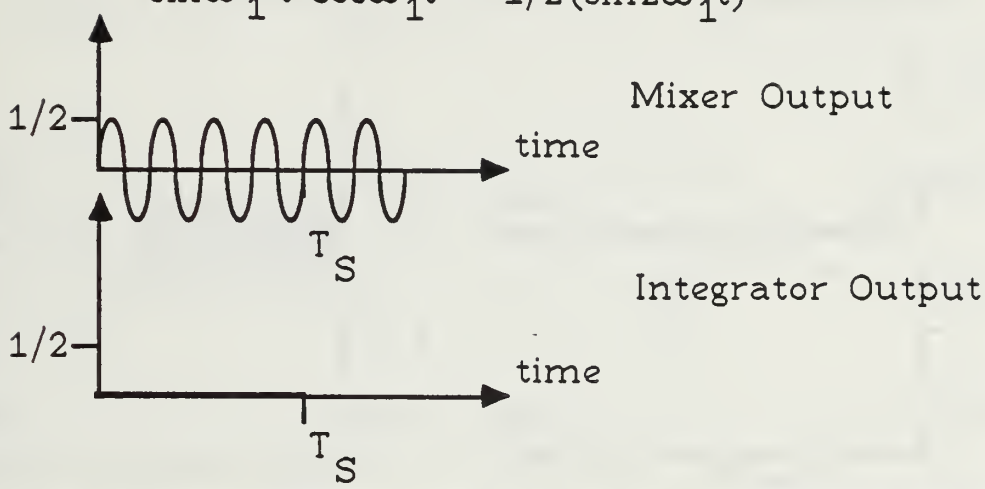
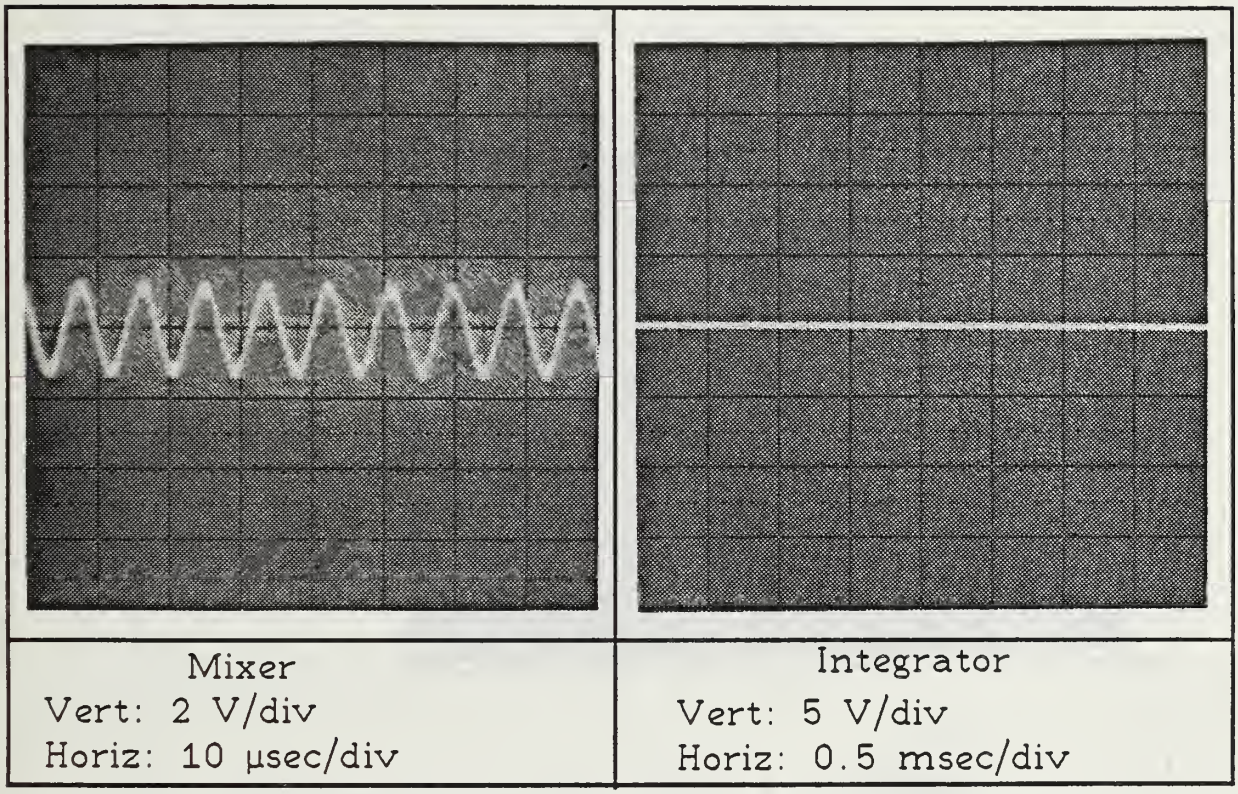




Mixer	Integrator
Vert: 2 V/div	Vert: 5 V/div
Horiz: 10 µsec/div	Horiz: 0.5 msec/div

Figure 3.9 Case 3 and 4. Mixer and Integrator Output

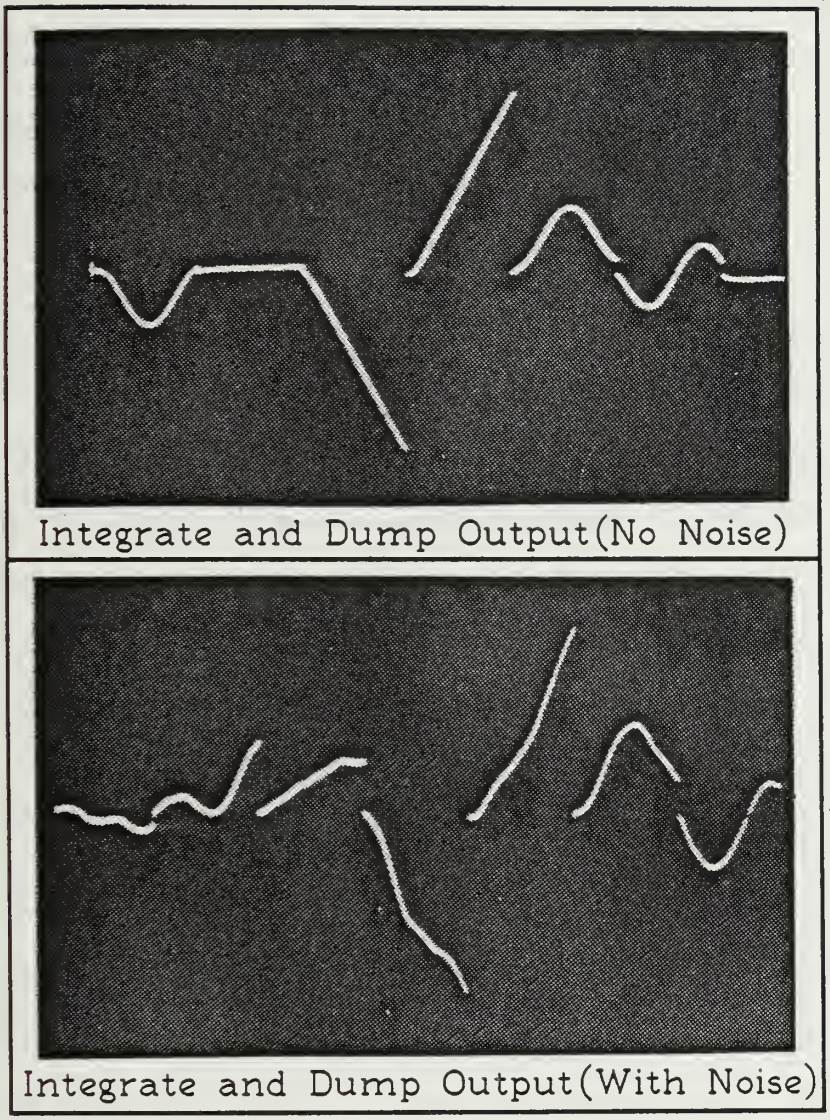


Figure 3.11 Integrate and Dump Outputs
With and Without Noise Added

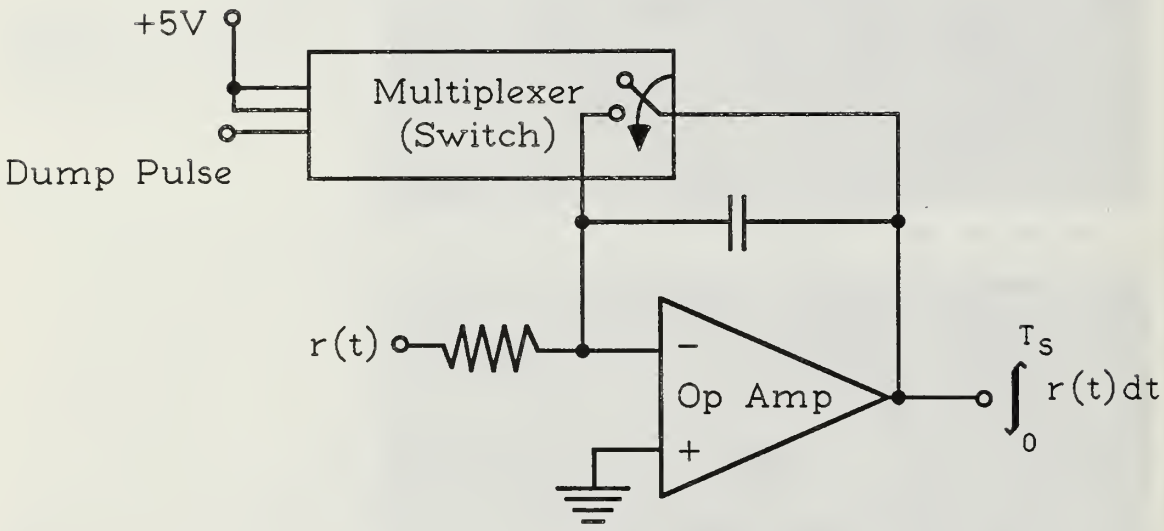


Figure 3.12 Diagram of the Integrator

maximum value (no noise case). This insures optimum bit detection. The sample and dump pulse duration is small compared to the symbol interval (integration period). After the sample pulse, the dump pulse is used to begin the integration process again for one symbol interval. The dump pulse is made dependent upon the trailing edge of the sample pulse as shown in Figure 3.13.

Both pulses are produced by a dual one-shot which is clocked at the symbol rate = $r_b/3$ symbols per second. This clock rate allows integration over an entire symbol interval and sampling at the symbol rate. Sampling is triggered on the leading edge of each clock cycle by the first one-shot. The trailing edge of the sample pulse triggers the dump pulse which, in turn, reinitiates the integration process every T_s sec.

3. Bit Recovery

The recovery of bits in the demodulation scheme involves symbol assignments, a mapping scheme and decision circuitry. Symbols are assigned to the eight different carriers and each one produces a voltage at the output of one of the integrate and dump circuits. The integrate and dump outputs are then summed in a direct bit detection scheme based upon a zero voltage decision threshold. Bits are recovered from the bit detection scheme using decision circuitry.

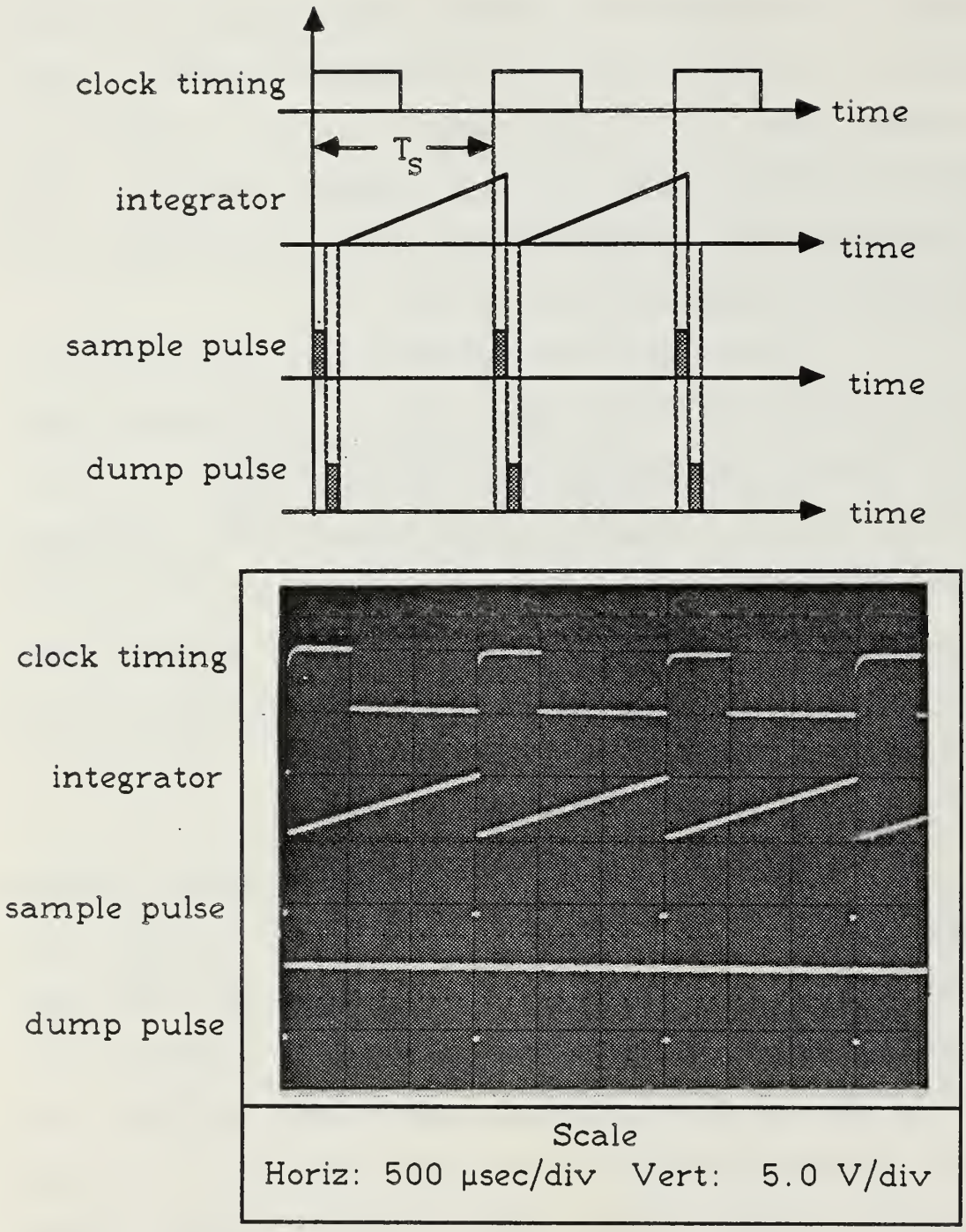


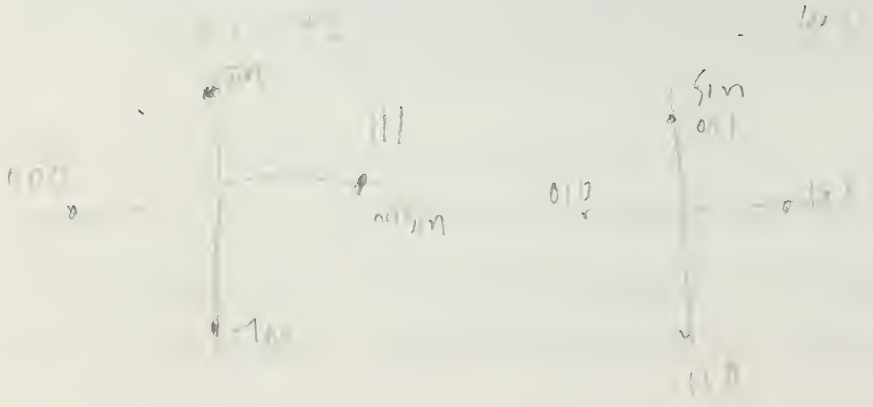
Figure 3.13 Timing Diagram of Sample and Dump Pulses

The integrate and dump output voltage combinations shown in Table 3.2 are the result of symbol assignments made in the first two columns where C_1, S_1, C_2 and S_2 represent the channel integrate and dump circuit outputs shown in Figure 2.2. In Table 3.2, symbols 0, + and − all represent maximum voltage levels at the time the integrator is dumped. For any given symbol interval a positive or negative voltage is at the output of one of the integrate and dumps. The remaining three integrate and dump output voltages are zero. The three possible voltages at the output of the integrate and dump circuits provide a voltage ambiguity when recovering data bits of ones and zeros. This ambiguity is eliminated by a logical analysis of the integrate and dump outputs C_1, S_1, C_2 and S_2. The last three columns of Table 3.2, physically realized by three four-input summers, constitutes a mapping scheme derived from an analysis of the ambiguities. The summers combine the integrate and dump outputs to produce positive or negative voltages on which decisions are made and bits are detected. Output of the summers with and without the influence of noise are illustrated in Figure 3.14.

The three summer outputs are applied to the decision circuitry as shown in Figure 3.15. The decision subsystem consists of sample and hold and comparator circuits. The positive or negative voltage produced by the

TABLE 3.2 INTEGRATOR OUTPUT TO SUMMER MAPPING

Symbol Assignment		Integrator Voltages				Summer Voltages		
Symbols	Signals	C_1	S_1	C_2	S_2	C_1-S_1 + C_2-S_2 Left Bit	C_2-C_1 + S_2-S_1 Middle Bit	C_1+S_1 + C_2+S_2 Right Bit
000	$-\cos\omega_2 t$	0	0	−	0	−	−	−
001	$+\sin\omega_1 t$	0	+	0	0	−	−	+
010	$-\cos\omega_1 t$	−	0	0	0	−	+	−
011	$+\sin\omega_2 t$	0	0	0	+	−	+	+
100	$-\sin\omega_2 t$	0	0	0	−	+	−	−
101	$+\cos\omega_1 t$	+	0	0	0	+	−	+
110	$-\sin\omega_1 t$	0	−	0	0	+	+	−
111	$+\cos\omega_2 t$	0	0	+	0	+	+	+



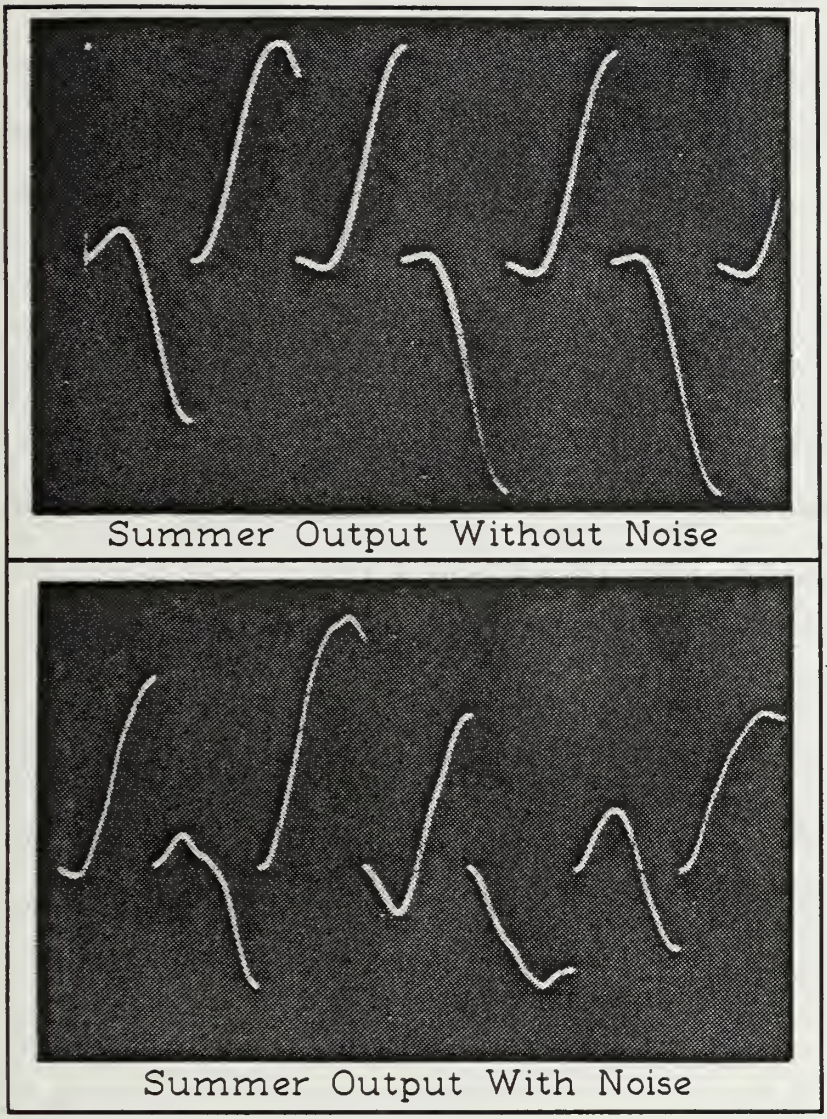


Figure 3.14 Output of a Four-Input Summer, With and Without Noise Added

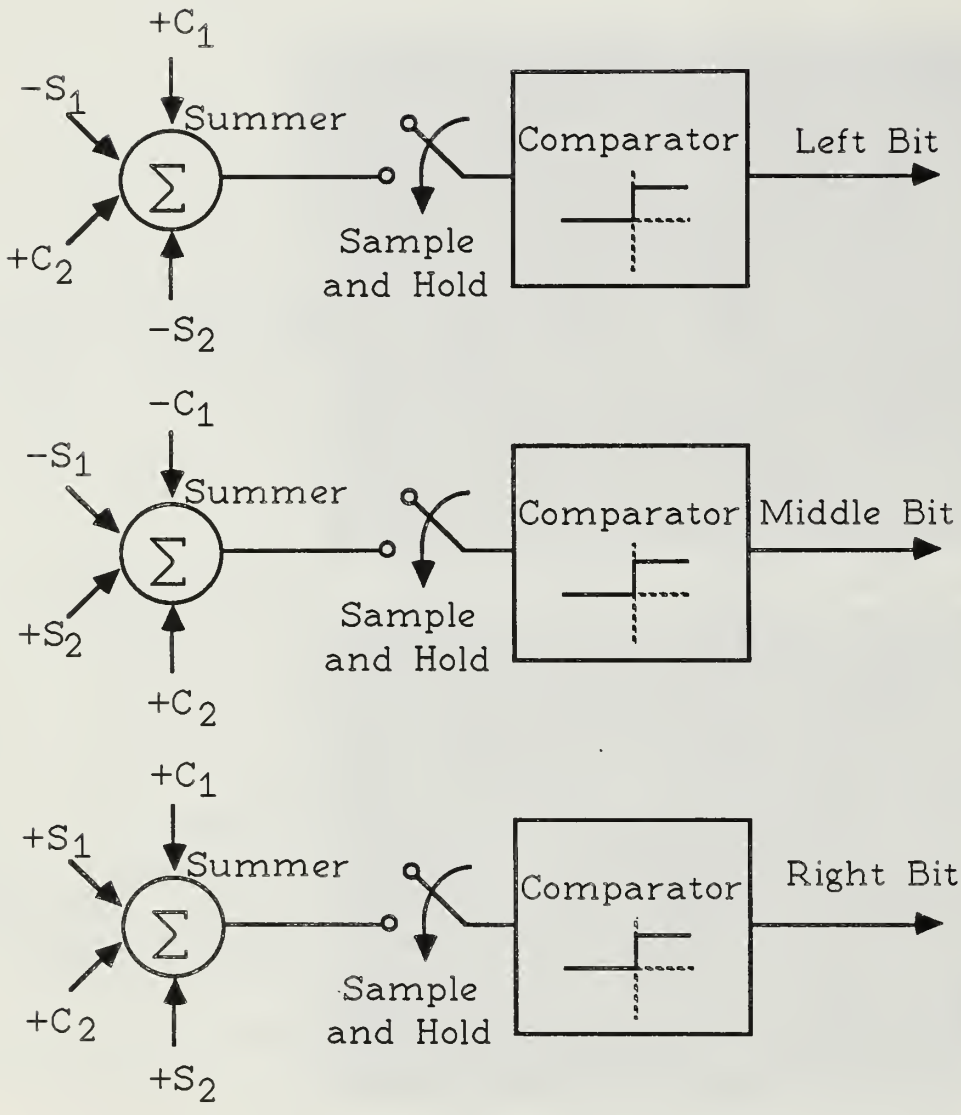


Figure 3.15 Block Diagram of Decoding Circuitry

four-input summer is held at a constant voltage by a sample and hold circuit for one symbol interval of T_s sec. Based upon a zero threshold, the comparator decides a positive voltage is a one and a negative voltage is a zero. From the output of the comparator the bits are recovered directly.

D. BIT ERROR DETECTION CIRCUIT

Performance of a system is judged by the number of errors made when random Gaussian noise is added. The errors are detected by comparing the recovered data with a delayed version of the transmitted data. A delay in the transmitted data is necessary to compensate for delays experienced in the receiver. From this comparison, the bit error detection circuit counts the number of errors for each bit channel and the number of symbols sent. Three bits are sent simultaneously. Therefore the bit rate in each channel is equal to the symbol rate so that the symbol counter is also used as a bit counter. The ratio of errors to symbols sent is the bit error ratio (BER) which is a measure of system quality.

The bit error detection circuit for this system is shown in Figure 3.16. The transmitted data is compared with the recovered data on a bit by bit basis using an XOR gate. If the data bits are the same, the XOR stays low. Before the

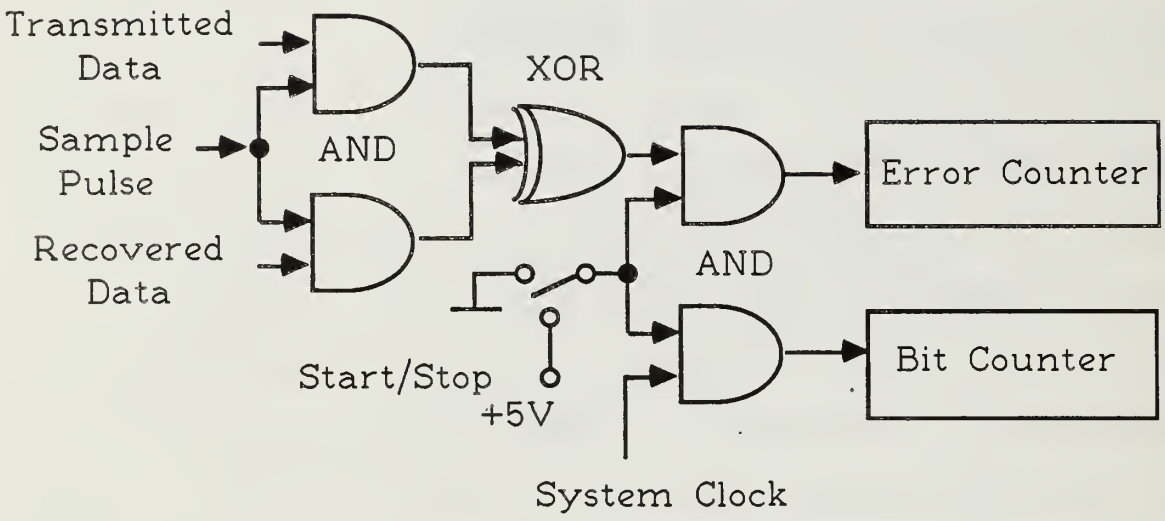


Figure 3.16 Block Diagram of the Error Detection Circuit

data is compared, each data pulse is strobed using AND gates. The strobe is identical in nature to the sample and dump pulse described earlier. Data is strobed at the center of each pulse to eliminate errors due to the edges (switching times) of the pulse. If the bits differ, an error is counted. The error detection circuit is stopped and started by an external switch and another set of AND gates as shown in Figure 3.16.

E. TEST RESULTS

Errors are counted for various levels of noise injected into the channel. This variable noise level is used to change the system signal-to-noise ratio (SNR). Communication system performance is presented as a plot of probability of error P_e = BER versus SNR. The resulting curve is compared to that of a more conventional system. Here, the 2 FSK/QPSK system is compared to an 8-PSK system. An 8-PSK system is chosen because 8-PSK system performance is known, it is similar to the 2 FSK/QPSK system, and 8-PSK is popular.

1. SNR versus P_e

The experimental data taken for varying levels of SNR is shown in Table 3.3. SNR is measured using a true RMS voltmeter. The signal power S and the signal plus noise power (S+N) at the output of the channel summer are

TABLE 3.3 EXPERIMENTAL DATA

S/N (dB)	P_e Left Bit LB	P_e Middle Bit MB	P_e Right Bit RB	P_e Total = $1/3(P_{e_{LB}}+P_{e_{MB}}+P_{e_{RB}})$
3	2.80×10^{-2}	2.09×10^{-2}	2.06×10^{-2}	2.32×10^{-2}
4	1.30×10^{-2}	9.16×10^{-3}	9.56×10^{-3}	1.06×10^{-2}
5	6.08×10^{-3}	4.67×10^{-3}	4.82×10^{-3}	5.44×10^{-3}
6	3.56×10^{-3}	2.06×10^{-3}	2.46×10^{-3}	2.70×10^{-3}
7	1.20×10^{-3}	6.07×10^{-4}	1.01×10^{-3}	9.39×10^{-4}
8	6.47×10^{-4}	3.44×10^{-4}	4.03×10^{-4}	4.65×10^{-4}
9	2.72×10^{-4}	9.53×10^{-5}	1.48×10^{-4}	1.72×10^{-4}
10	3.33×10^{-5}	1.11×10^{-5}	2.88×10^{-5}	2.44×10^{-5}
11	1.00×10^{-5}	6.67×10^{-7}	7.33×10^{-6}	6.00×10^{-6}

measured using a true RMS voltmeter. The noise power is then determined by subtracting the signal power S from S+N. The SNR = $\frac{S}{N}$ or in db,

$$SNR(dB) = 10 \log(\frac{S}{N}).$$

The probability of error P_e of the system is calculated by first determining the probability of bit error in each bit recovery channel for various values of SNR and then averaging the three channel results.

Probability of bit error P_e for each channel is calculated by dividing the total bit count by the error count for that particular SNR.

$$P_e = \frac{\text{error count}}{\text{bit count}}$$

The counts are obtained from the error detection circuit. The three bit recovery channels combine to produce P_e where LB is the left bit, MB is the middle bit and RB is the right bit.

$$P_e = \frac{1}{3}(P_{e_{LB}}+P_{e_{MB}}+P_{e_{RB}})$$

This is calculated for a SNR from 3 to 11 db. The data is plotted in terms of P_e versus SNR. Figure 3.17 illustrates the characteristic waterfall curves for the 2 FSK/QPSK system and the 8-PSK case. The 8-PSK curve is a basis for comparison.

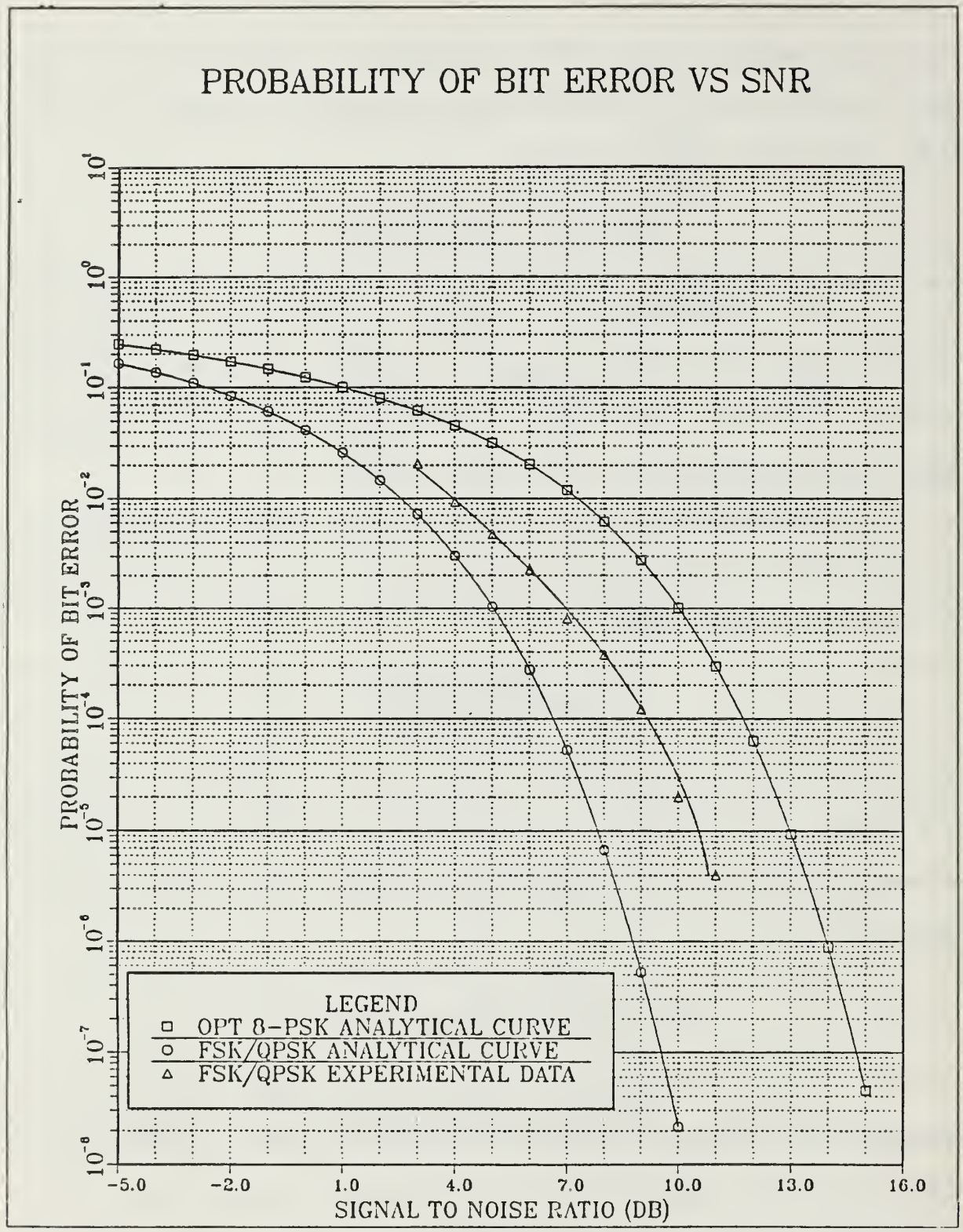


Figure 3.17 Probability of Bit Error Versus Signal-to-Noise Ratio

2. Comparison

Figure 3.17 shows a 5 db improvement of the experimental system relative to the theoretical 8-PSK system. The experimental system differs from the theory of Appendix B by 1.5 db to 2.5 db.

3. Results

The theoretical noise performance of the 2 FSK/QPSK system is derived in Appendix B and plotted in Figure 3.17. The results for 8-PSK are also given in that figure [Ref. 1]. Finally, the measured performance, averaged over the three bits of the symbol, is also plotted in Figure 3.17.

IV. CONCLUSIONS AND RECOMMENDATIONS

A. CONCLUSIONS

The analytic results of the 2 FSK/QPSK system shows a 5 dB power advantage relative to 8-PSK. This advantage is caused by the use of a third parameter (dimension) in the constellation diagrams. This parameter is frequency and it allows a "separation" of the carrier states which cannot be realized with 8-PSK. It is well known from decision theory that increasing the distance between "signals" reduces probability of error.

The experimental results differ from theory by 1.5 db to 2.5 db over the range of SNR used. This discrepancy is caused by differences in the four demodulation channels in the operating receiver. Considerable time may be required to adjust the circuitry until all four channels have nearly identical performance. Such adjustment is required before the experimental results will duplicate the theoretical results.

B. RECOMMENDATIONS

It is recommended that extensions of this work include adjusting the circuitry to obtain closer agreement between measurement and theory. Further, work should proceed on

the design and implementation of circuitry to derive carrier and bit synchronization from the received noisy signal.

APPENDIX A

CIRCUIT SCHEMATICS

This section contains schematic diagrams of the subsystems and individual circuits of the 2 FSK/QPSK system. Standard Linear and TTL integrated circuits are used. Specifications for all integrated circuits can be found in References 2, 3 or 4. Unless stated otherwise, resistor values are in kΩ, capacitor values are in μF and op-amps and comparators are powered by voltage supplies of +14 and -14 volts. Most op-amp applications use LF356N high speed op-amps because of the high slew rates required for frequency operation in the 50 to 150 kHz range.

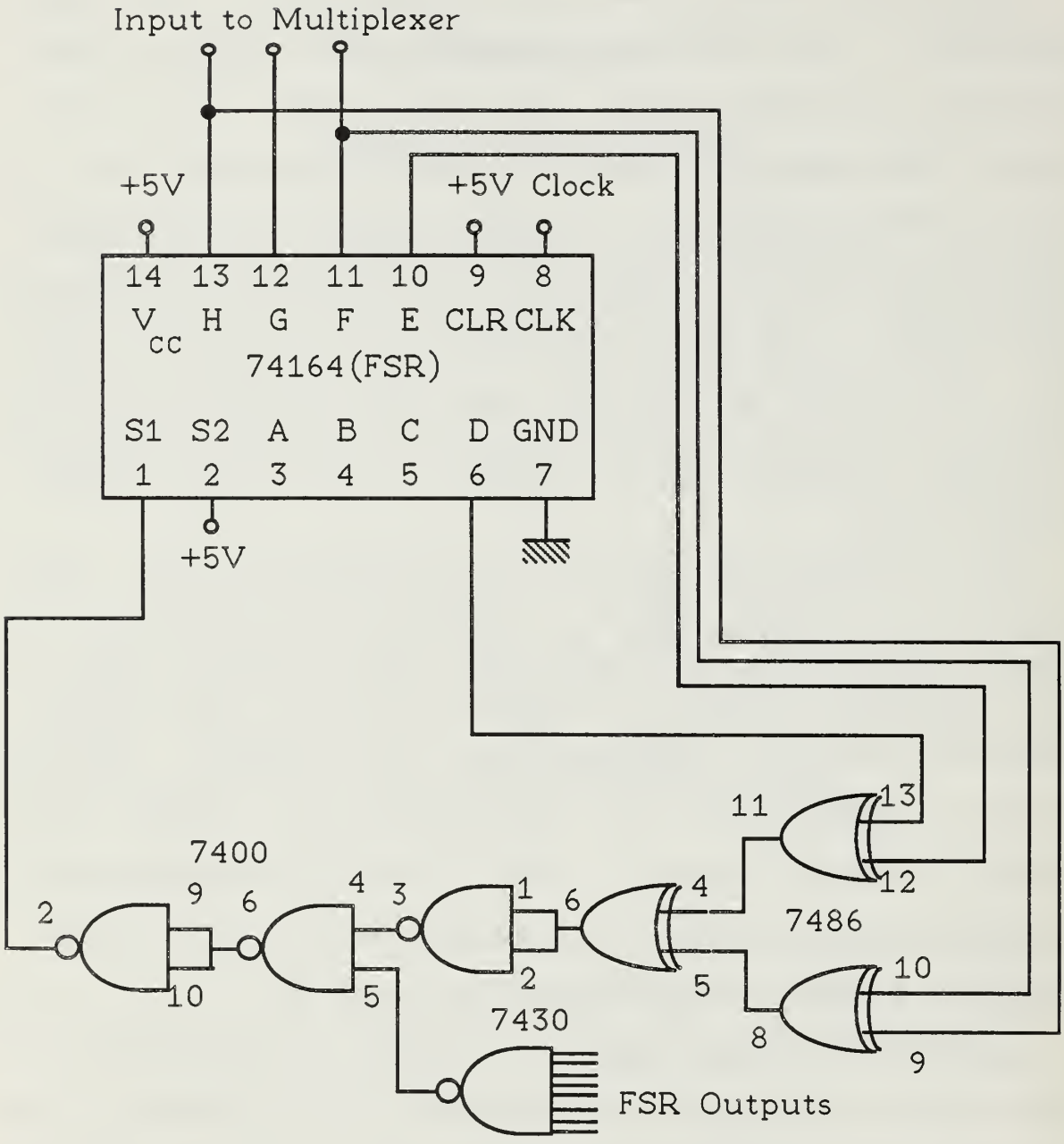
A. TRANSMITTER

The transmitter consists of the data generator, modulator and phase shifter subsystems as shown in Figure 3.1. Hard limiters, bandpass filters, an AVM and several frequency dividers are used. Two oscillators feed the system to produce the modulated carriers and generate data. One oscillator produces a sinusoid of frequency $2f_1$ = 115.366 kHz. The other oscillator produces a square wave of frequency $2r_b$ = 4.000 kHz.

Figure A.1 shows the circuit schematic for the data generator. The 74LS164 feedback shift register (FSR) produces a psuedo random data stream [Ref. 2:p. 280]. Because XOR gates are used as feedback components, the all zeroes state is disallowed. Combinational logic using NAND gates detects the all zeroes state and reinitiates the FSR data stream. The FSR is clocked at a rate of $r_b/3 = 667$ Hz. The clock is derived from the system oscillator producing a square wave of frequency $2r_b$ Hz and a divide-by-six circuit.

The divide-by-six circuit is shown in Figure A.2. The bipolar square wave from the oscillator is converted to a TTL compatible unipolar square wave in the MC1489 monolithic quad line receiver [Ref. 3:p. 5-120]. Division by six is realized by the configuration of a single 7492 counter integrated circuit. This circuit is clocked by the unipolar square wave of frequency $2r_b$ Hz, thereby producing a square wave of frequency $r_b/3$ Hz.

A divide-by-three circuit is necessary in the transmitter because one of the inputs to the AVM which produces v_2 is a square wave of frequency $2r_b/3$ Hz, one third of the square wave oscillator frequency. The divide-by-three circuit consisting of a dual JK edge-triggered flip flop is shown in Figure A.3.



All Zeros Detector

Figure A.1 Circuit Diagram of the Data Generator

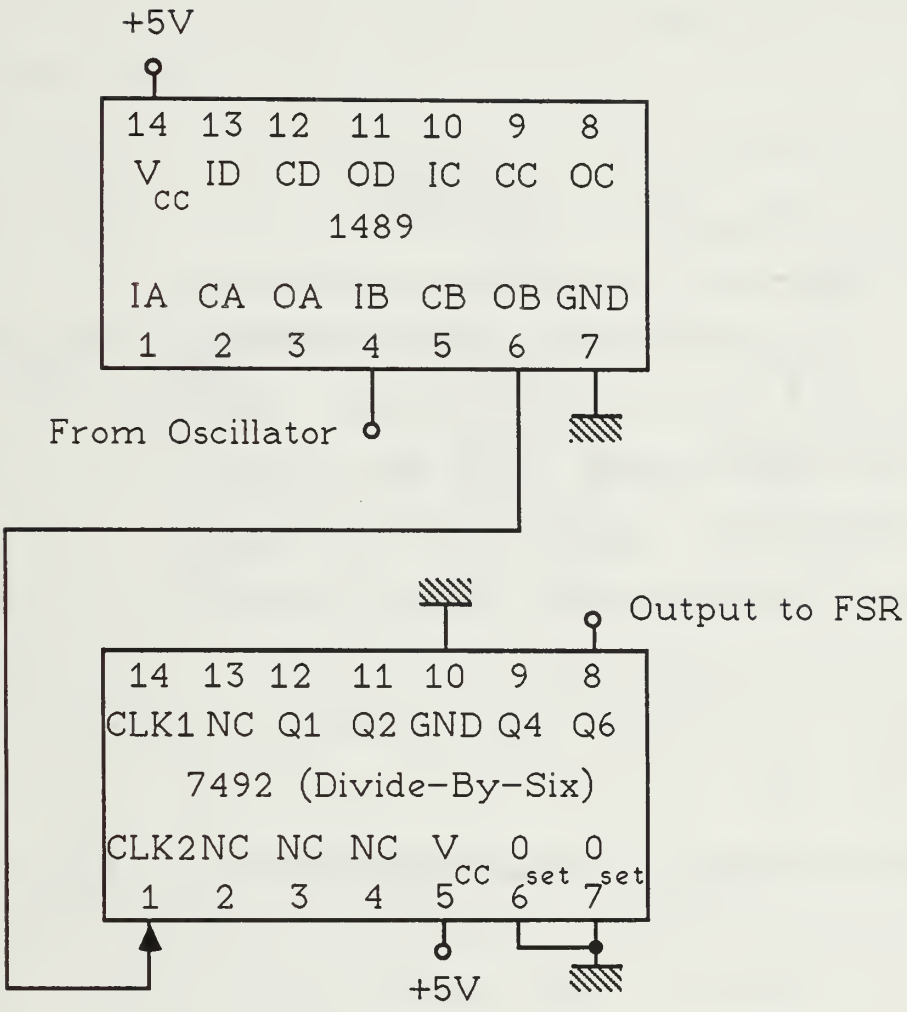


Figure A.2 Diagram of the Divide-By-Six Circuit

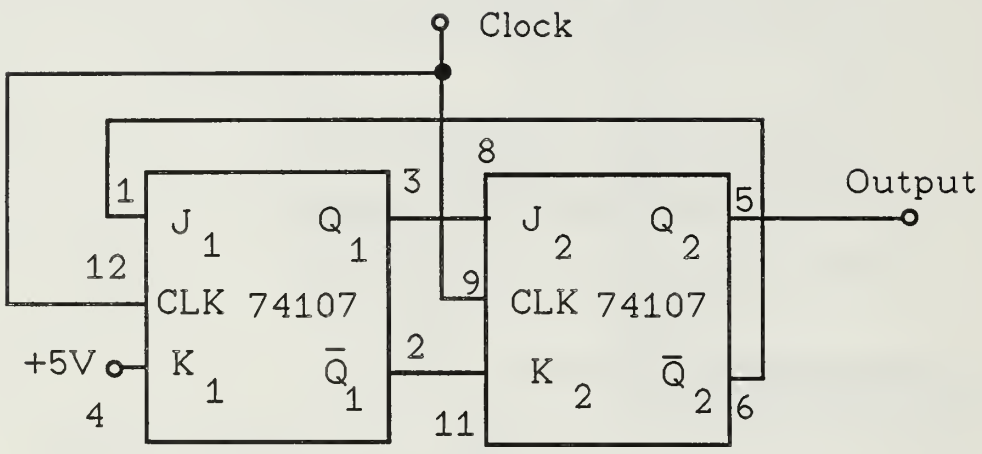


Figure A.3 Diagram of the Divide-By-Three Circuit

Figure A.4 is a schematic diagram of the hard limiter. The hard limiter is an LM710 high speed voltage comparator. It requires voltage biasing of +14 volts and −7 volts. This arrangement converts an analog sinusoid into a digital square wave.

Two types of filters are shown in the transmitter block diagram (Figure 2.1). A bandpass filter and a narrow bandpass filter are both variations of the biquadratic bandpass filter realization shown in Figure A.5. The biquadratic bandpass filter design permits simplicity, flexibility and accuracy in the design process. [Ref. 5]

The narrow bandpass filter design requires a 3 dB bandwidth of 2 kHz and a center frequency of 114.031 kHz, $2f_1 - 2r_b/3$ Hz. To achieve this, the design consists of six stages of the filter realization shown in Figure A.5 where R = 270Ω, C = 0.005 μF and R_5 = 27 kΩ. The frequency response for the narrow bandpass filter is shown in Figures A.6 and A.7. Figure A.8 shows the narrow bandpass filter frequency response superimposed over the spectrum of the output of the mixer to illustrate the filter effectiveness.

The bandpass filters in the phase shifter have a 3 dB bandwidth of 34.2 kHz and a center frequency of 57.683 or 57.016 kHz (f_1 or f_2 Hz). The filter design consists of a single stage of the circuit shown in Figure A.5 where R =

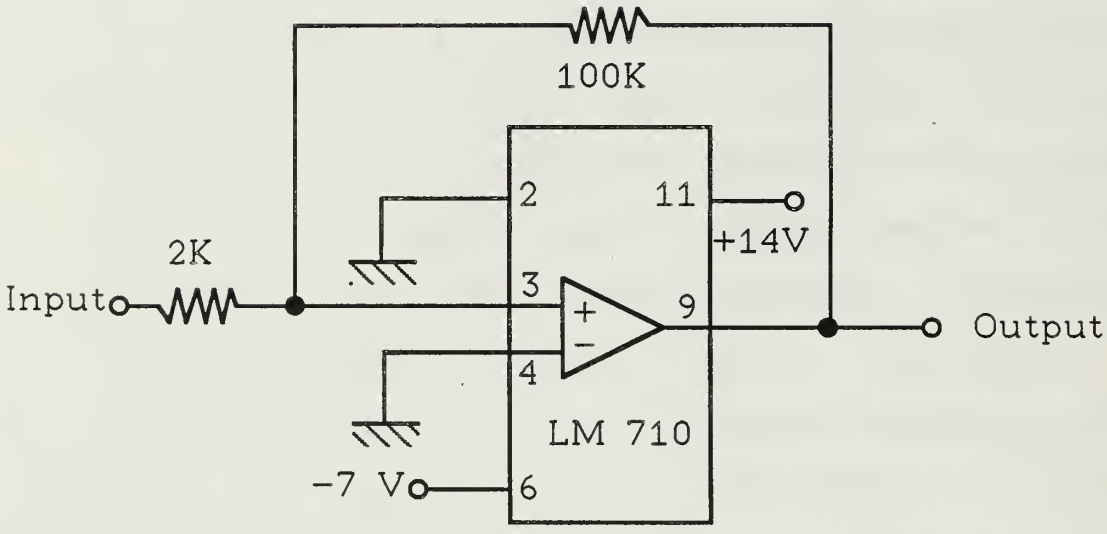


Figure A.4 Circuit Diagram of the Hard Limiter

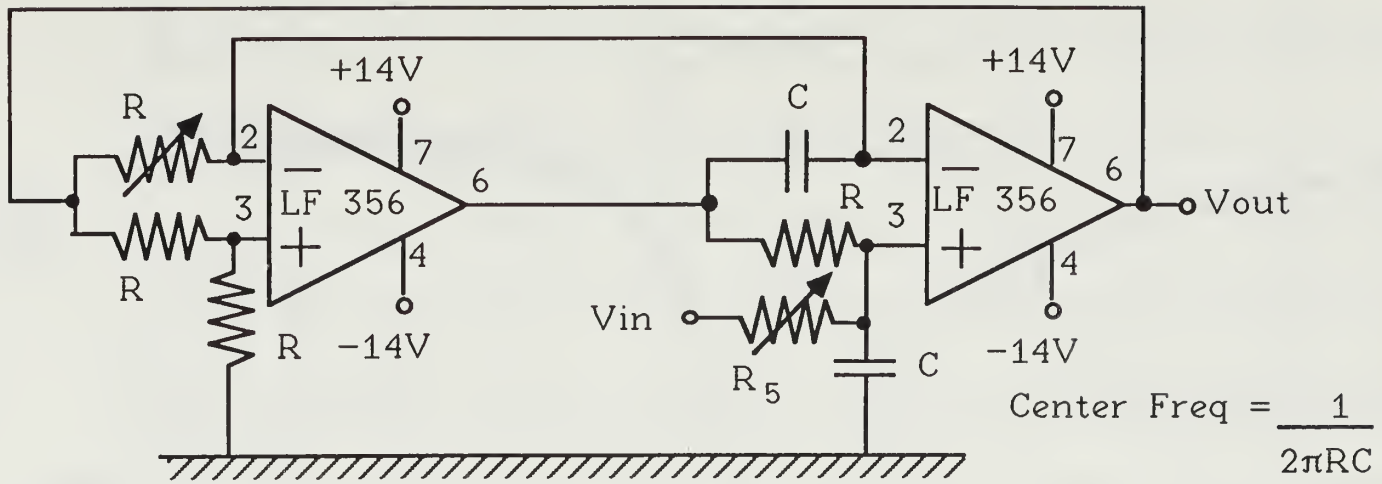


Figure A.5 Circuit Diagram of a Single Stage of the Biquadratic Bandpass Filter

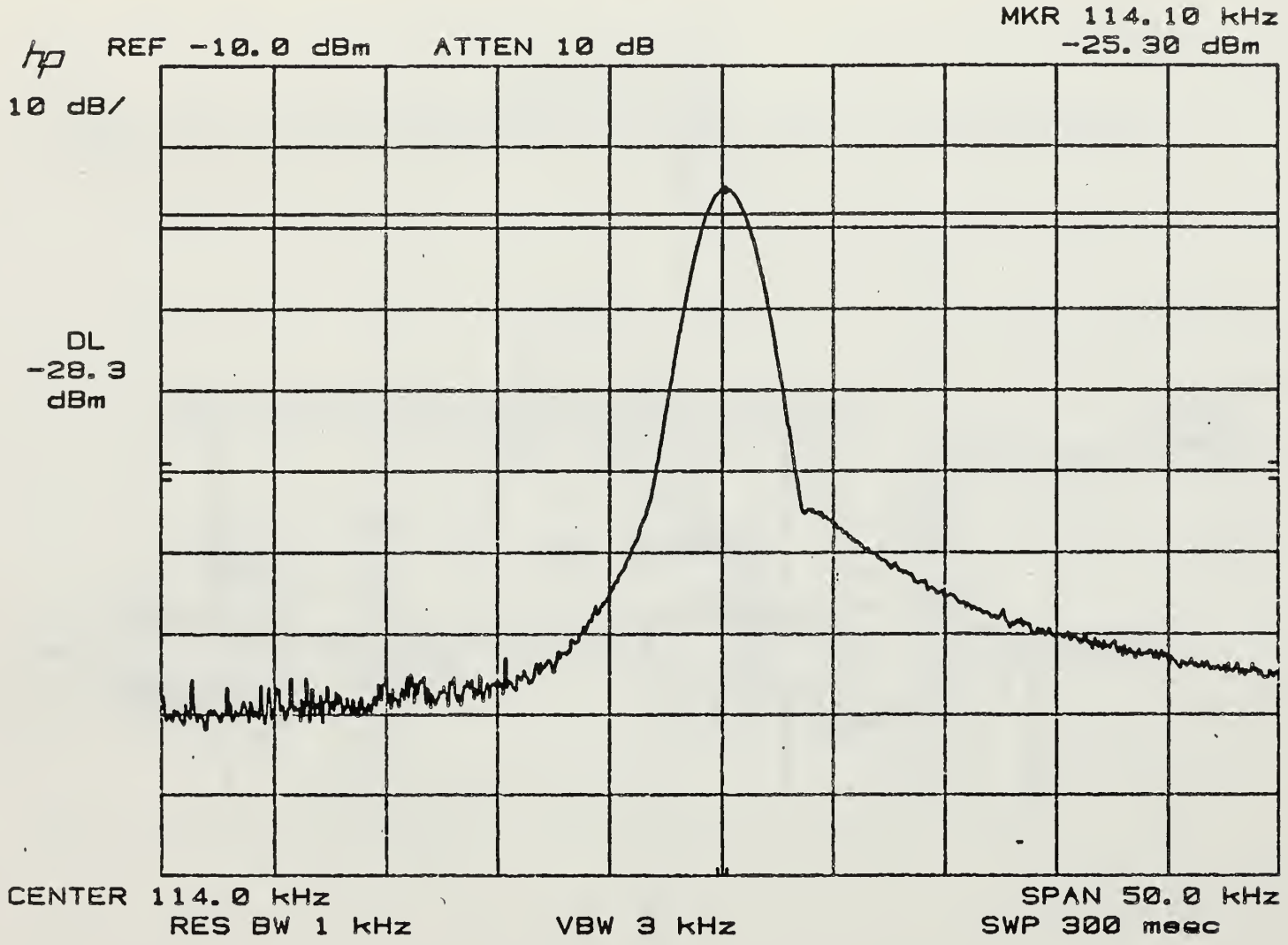


Figure A.6 Narrow Bandpass Filter Frequency Response, 50 kHz Span

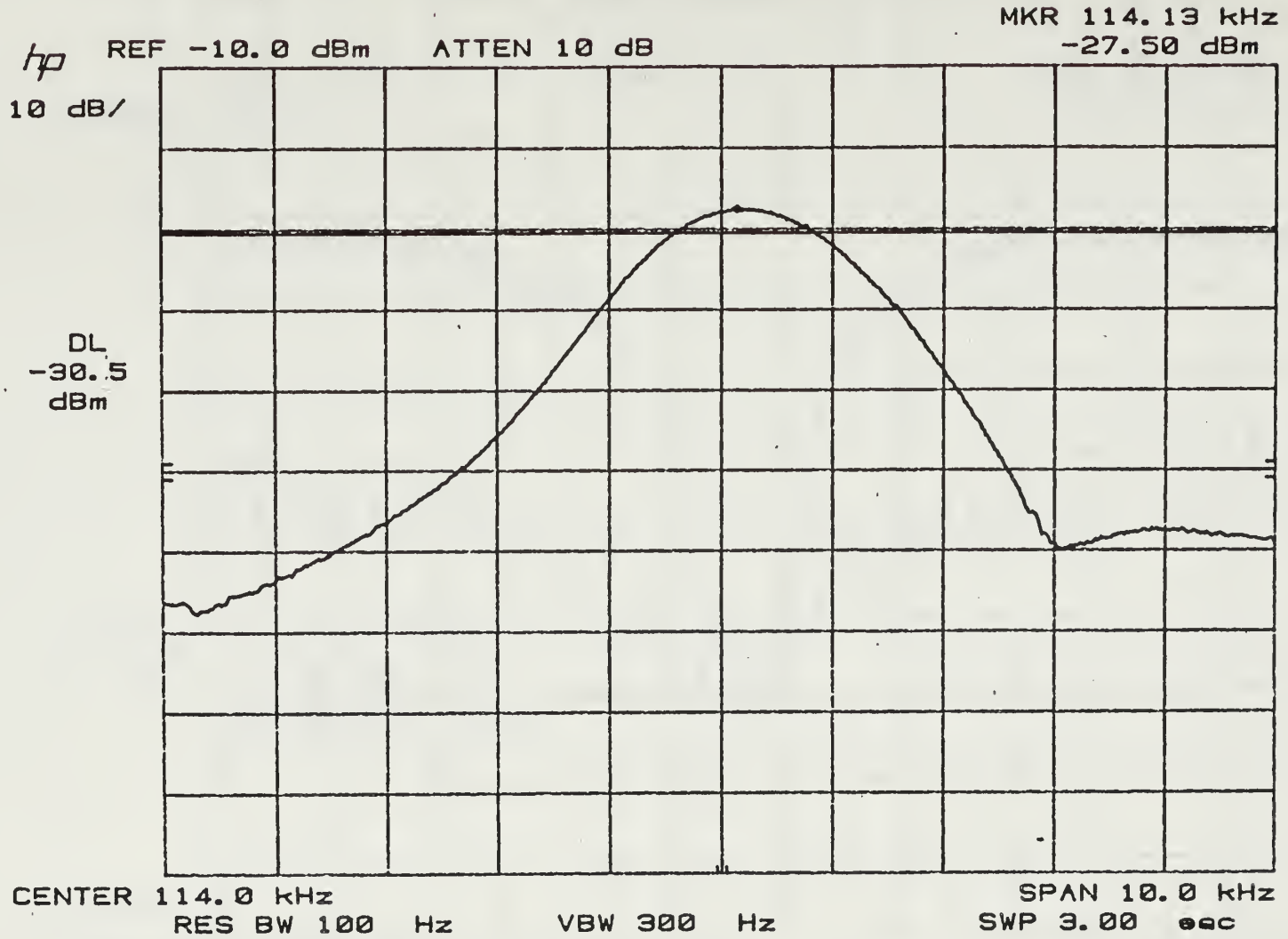


Figure A.7 Narrow Bandpass Filter Frequency Response, 10 kHz Span

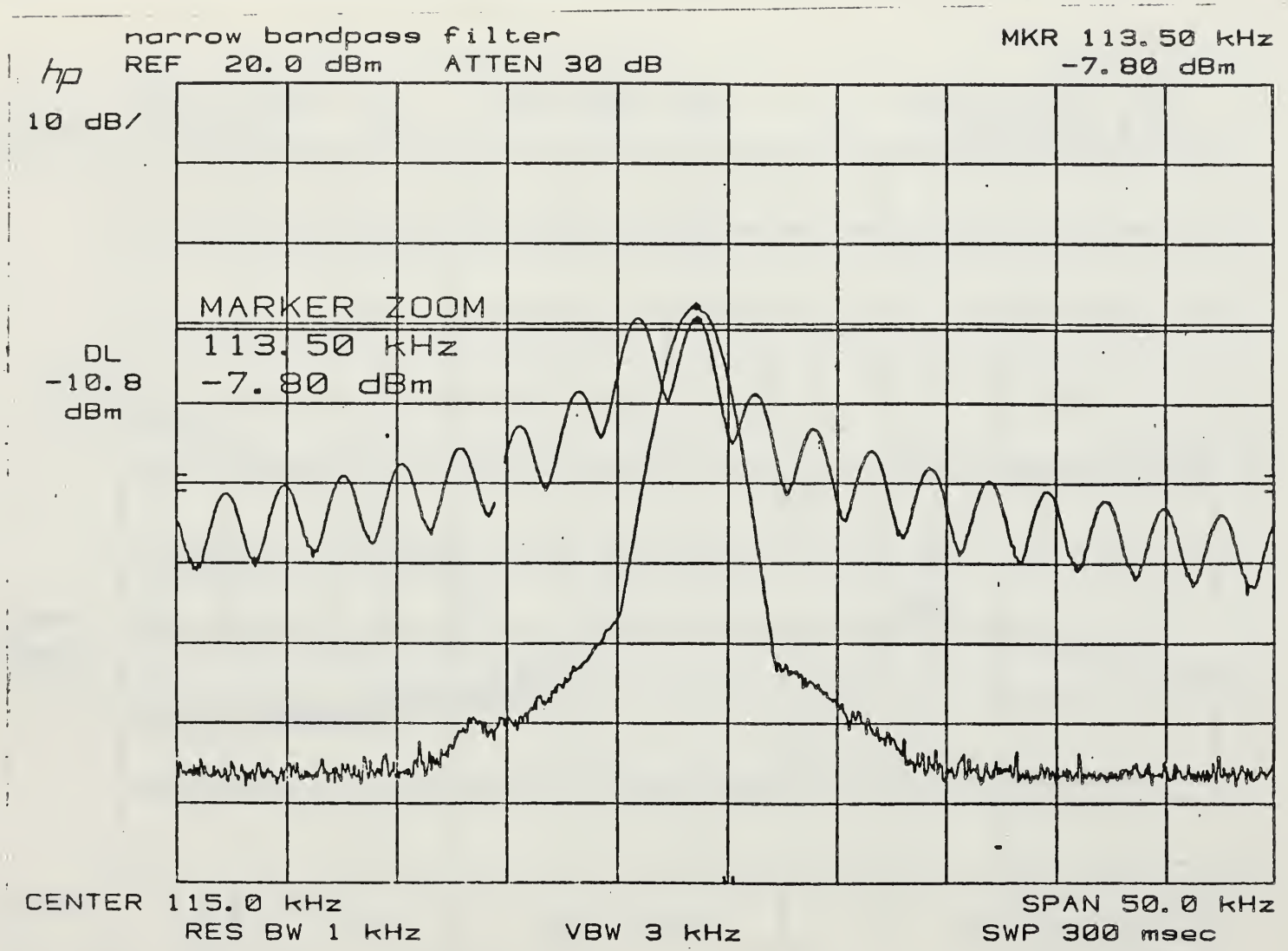


Figure A.8 Narrow Bandpass Filter Frequency Response Superimposed Over Mixer Output

1.8 kΩ, R5 = 1.8 kΩ and C = 0.005 μF. The filter response of this filter design is shown in Figures A.9.

Figure A.10 is the wiring diagram for the analog voltage multiplier (AVM). The AVM is a monolithic laser trimmed voltages multiplier. The schematic shown is the basic multiplier connection [Ref. 4].

Figure A.11 is a circuit diagram of the phase shifter. The LM710 hard limiter receives a sinusoid and converts it to a bipolar square wave. The bipolar square wave is converted to a TTL compatible unipolar square wave in the MC1489 monolithic quad line receiver. An inverter phase shifts the "phase" of a square wave by 180 degrees. In turn, the original and inverted square waves are fed into separate leading-edge-triggered flip flops, producing a 90 degree phase shift difference. The timing of the phase shift is also shown in Figure A.7.

The unity gain inverter which produces the remaining carriers after bandpass filtering is shown in Figure A.12.

The schematic of the modulator is shown in Figure A.13. A 4051B single 8-channel analog multiplexer/ demultiplexer is used. Three binary control inputs select one of the eight carriers to transmit data. Switching occurs at the rate $r_b/3$ Hz.

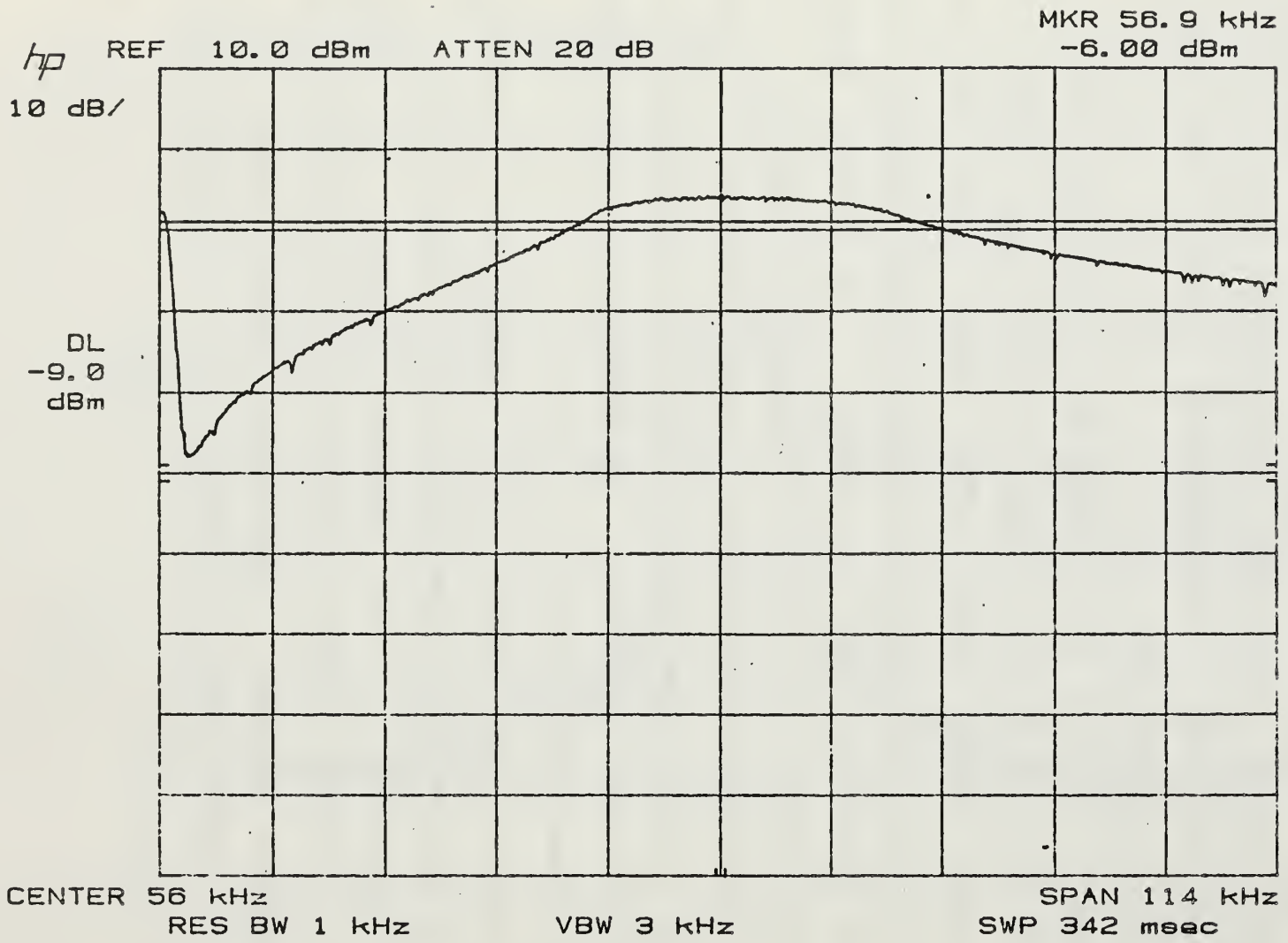


Figure A.9 Bandpass Filter Frequency Response

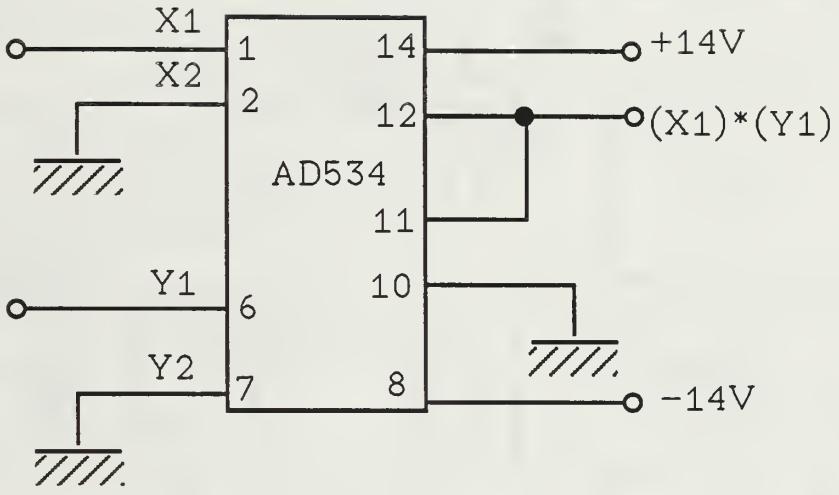


Figure A.10 Circuit Diagram of the Analog Voltage Multiplier

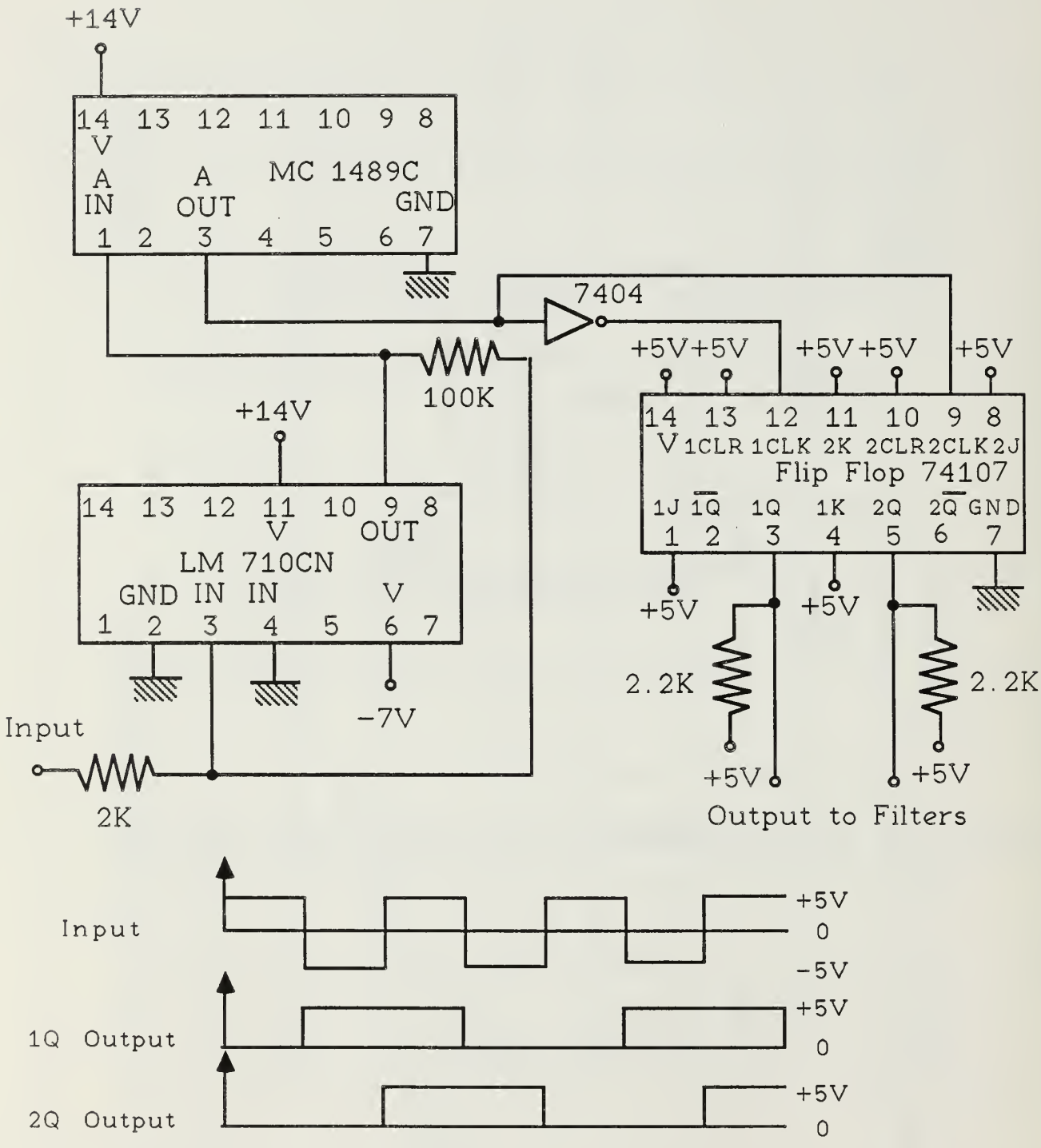


Figure A.11 Circuit Diagram and Timing of the Phase Shifter

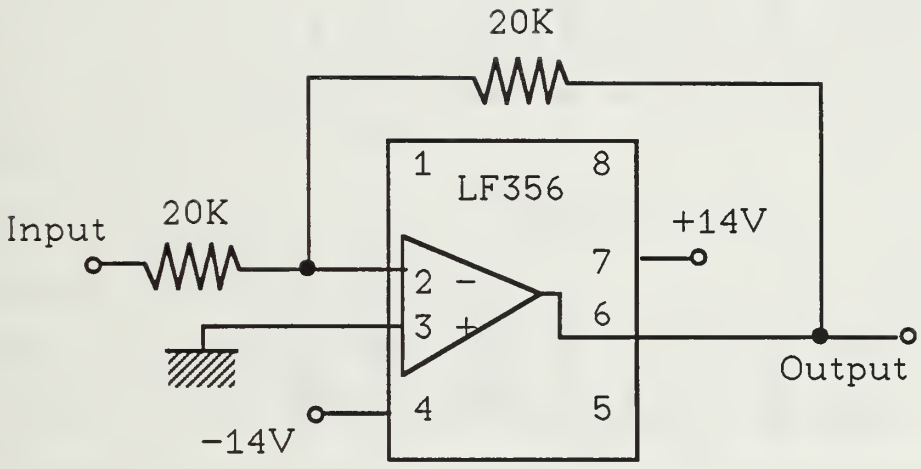


Figure A.12 Circuit Diagram of the Analog Inverter

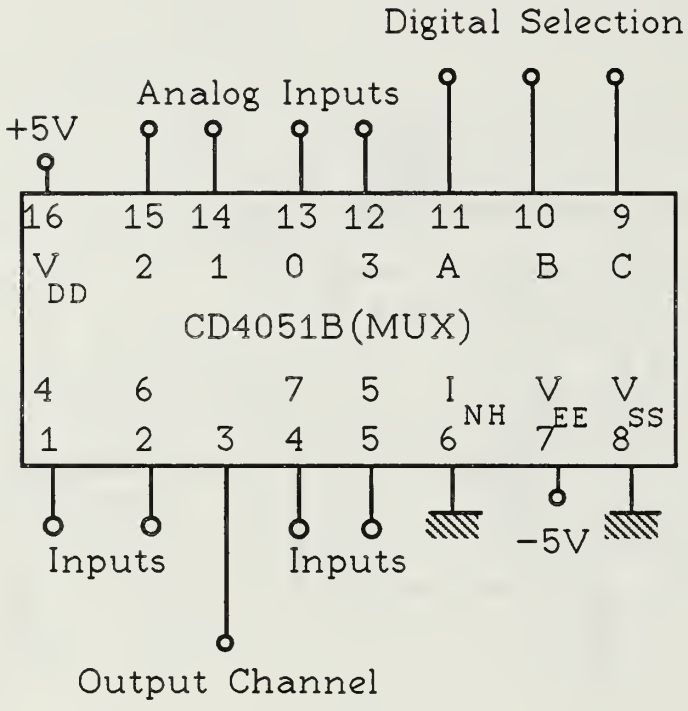


Figure A.13 Circuit Diagram of the Multiplexer

B. CHANNEL

The channel consists of a summer, bandpass filter and amplifier. The amplifier is similar to the analog inverter shown in Figure A.8 with the exception of the feedback resistor which is varied to produce a larger or smaller gain. The bandpass filter is two stages of the biquadratic bandpass filter shown in Figure A.5. where R = 277 Ω, R_5 = 7.9 kΩ and C = 0.01 μF. The 3 dB bandwidth of this filter is 2 kHz. The frequency response of this filter is shown in Figure A.14.

A two-input summer shown in Figure A.15 injects Gaussian noise into the system. A switch enables and disables the noise source. Two LF356 op-amps configured as voltage followers are buffers for impedance matching. R_1, R_2 and R_f are precision resistors matched for unity gain.

C. RECEIVER

The receiver consists of mixers, integrate and dump circuits, sample and dump pulse generators, a decoding subsystem and an error detection subsystem.

The AVM shown in Figure A.16 mixes the received signal with a local oscillator. This configuration is identical to the AVM shown in Figure A.10 except that Figure A.16 is followed by a passive lowpass filter. The lowpass filter

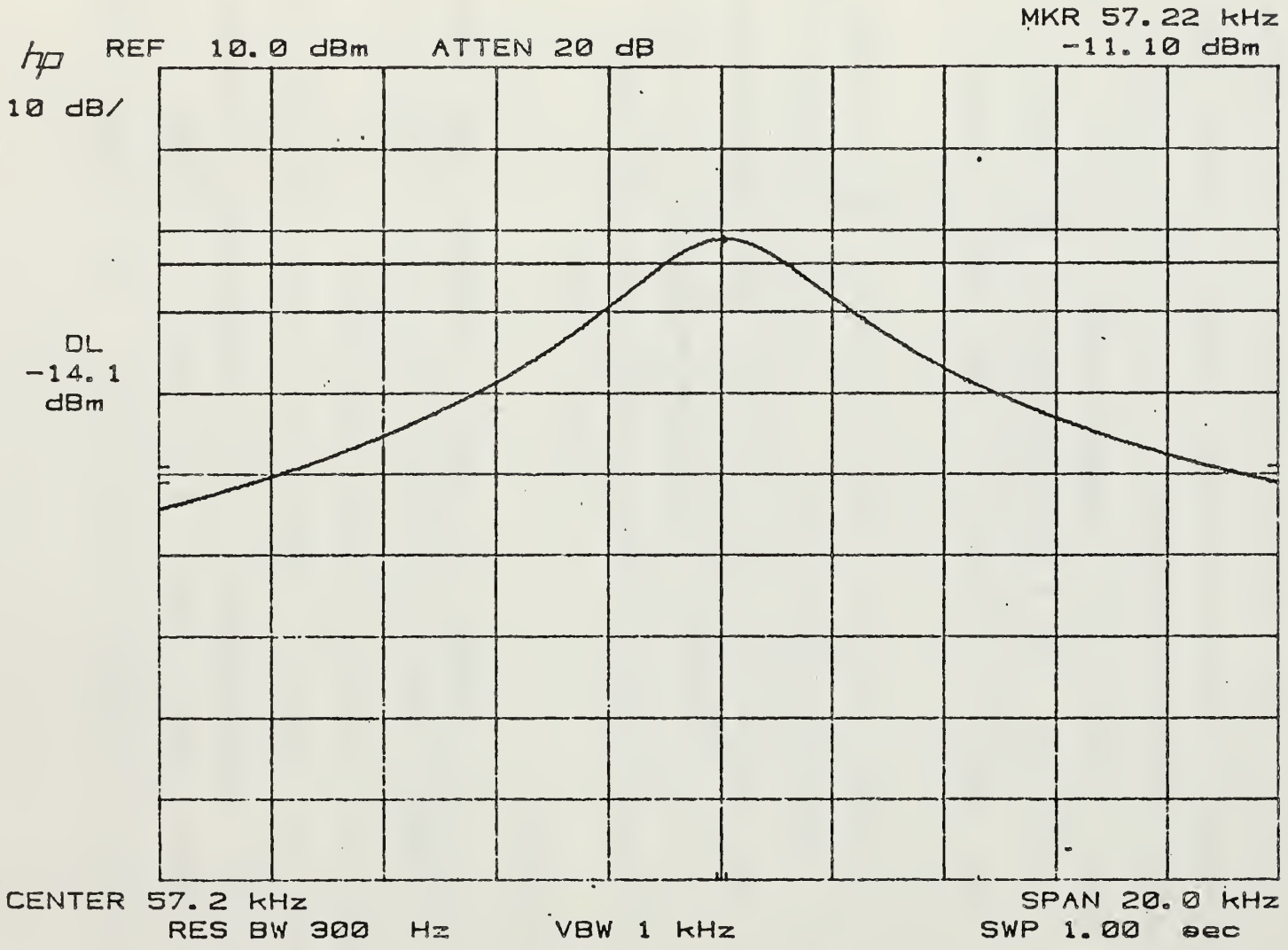


Figure A.14 Noise Limiting Bandpass Filter Frequency Response

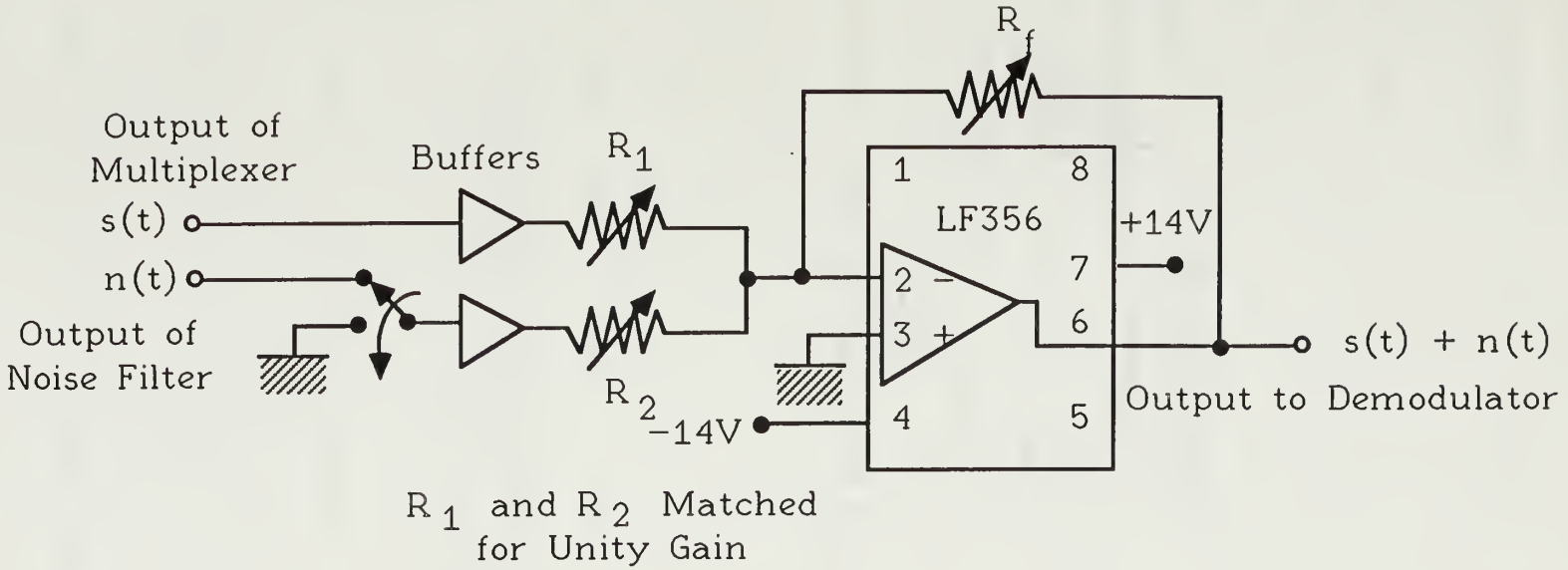


Figure A.15 Circuit Diagram of the Two-Input Inverting Summer

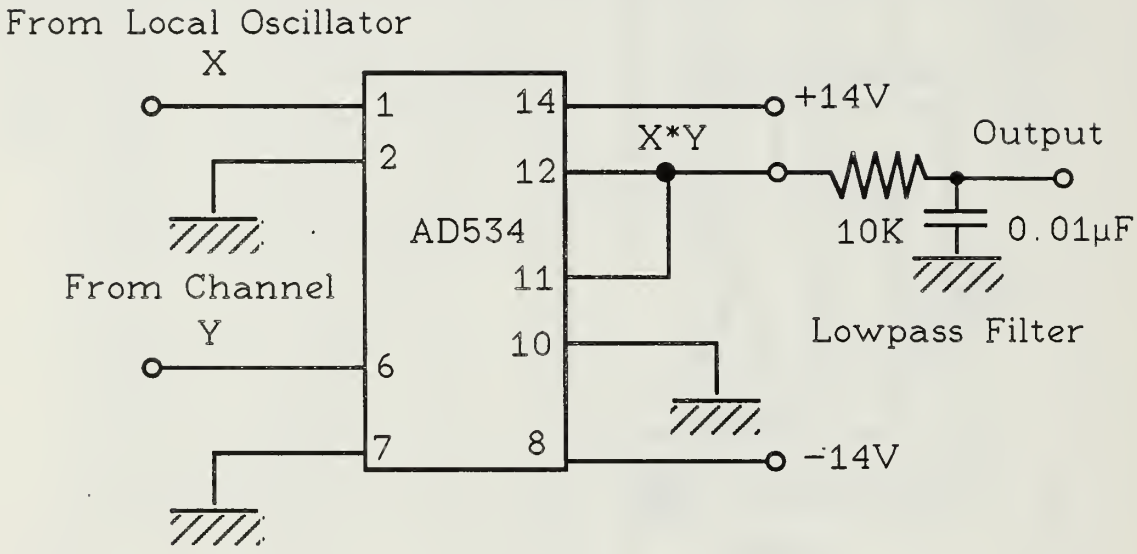


Figure A.16 Circuit Diagram of the Analog Voltage Multiplier and the Lowpass Filter

eliminates high frequency terms. Filter characteristics are R = 10 kΩ and C = 1.0 μF.

A schematic of the integrate and dump circuitry is illustrated in Figure A.17. A multiplexer and dump pulse represent an analog switch which resets the integrator after each symbol interval. The inverse of the integrator output is made available through the use of an analog inverter. Both polarities are necessary in the decoding scheme.

Figure A.18 shows the circuit diagram of the sample and dump pulse generator. Both pulses are produced by a 74221 dual one-shot. The dump pulse is made dependent upon the sample pulse so that sampling at a maximum voltage occurs prior to dumping the integrator. The sample pulse is triggered by the leading edge of the clock at a frequency of $r_b/3$ Hz. In turn, the trailing edge of the sample pulse triggers the dump pulse. Pulse width of the sample and dump pulses is much shorter than the clock pulse width and can be adjusted with the 20 kΩ variable resistors.

As shown in Figure A.19, the decoding circuitry consists of a four-input summer, a sample and hold circuit and a comparator. The four-input summer is an extended design of the summer in the channel circuitry. Precision resistors R_1, R_2, R_3 and R_4 are identical. R_f is adjusted to produce unity gain. The LF398N sample and hold circuit is clocked

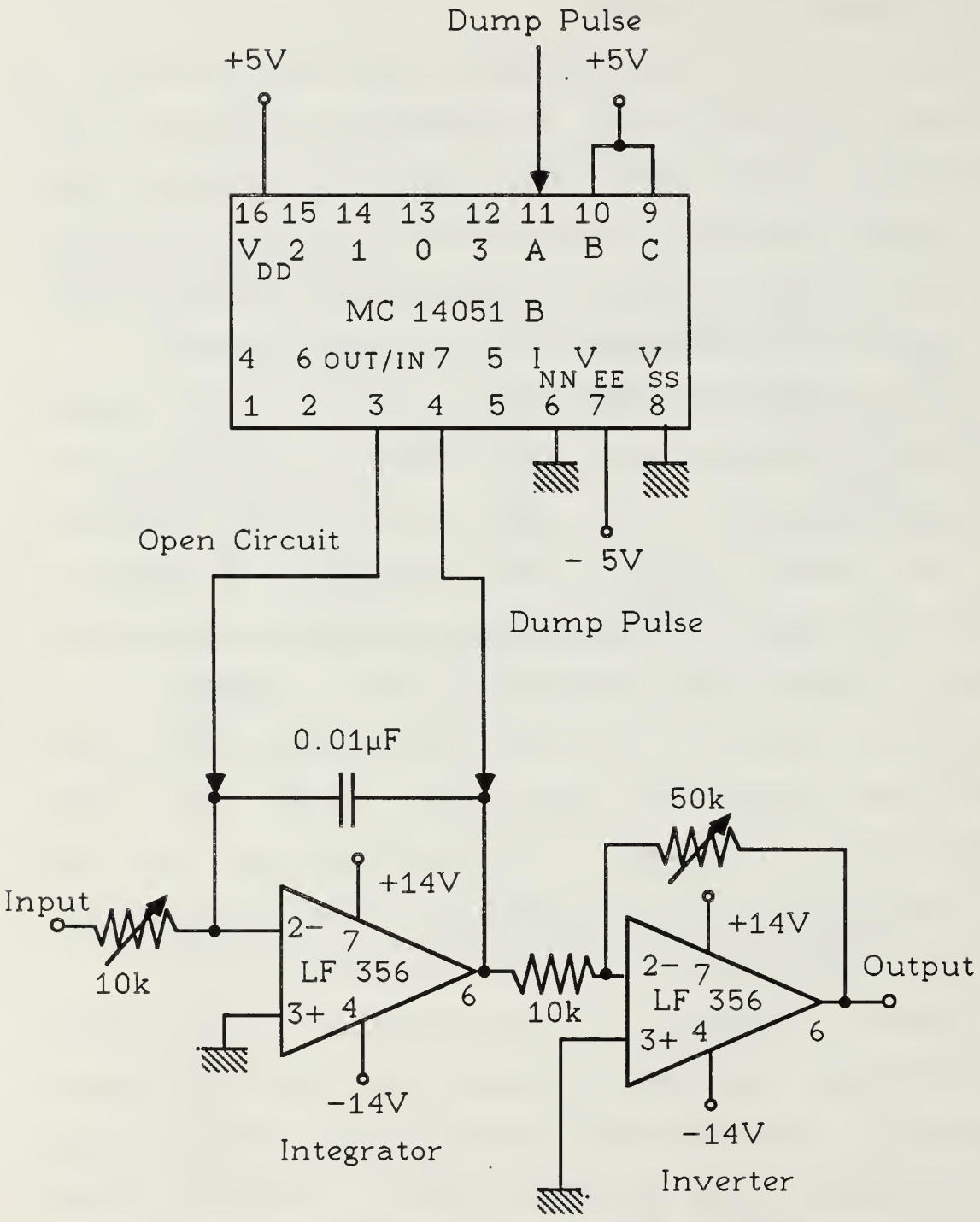


Figure A.17 Circuit Diagram of the Integrate and Dump

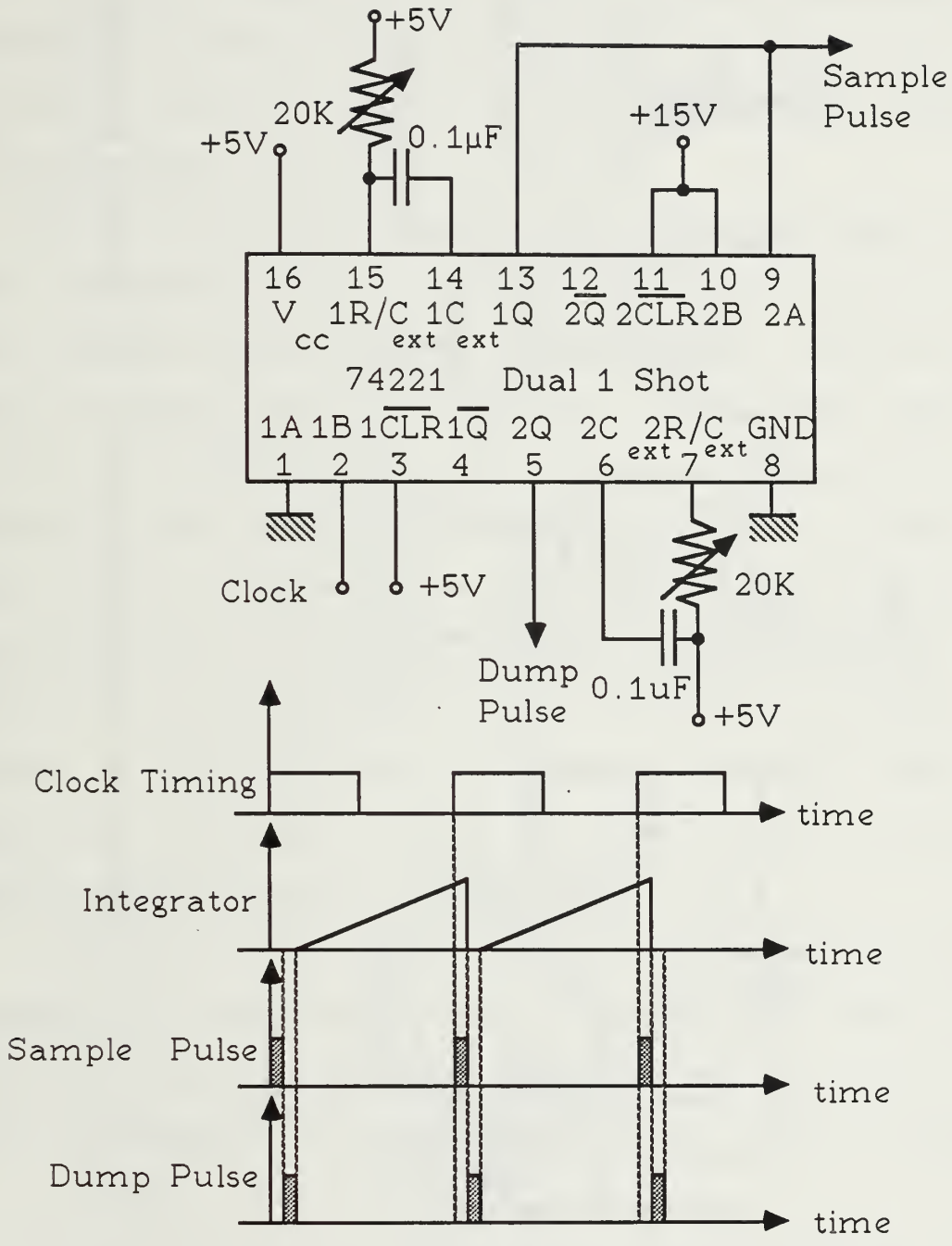


Figure A.18 Circuit Diagram of the Sample/Dump Pulse Generator

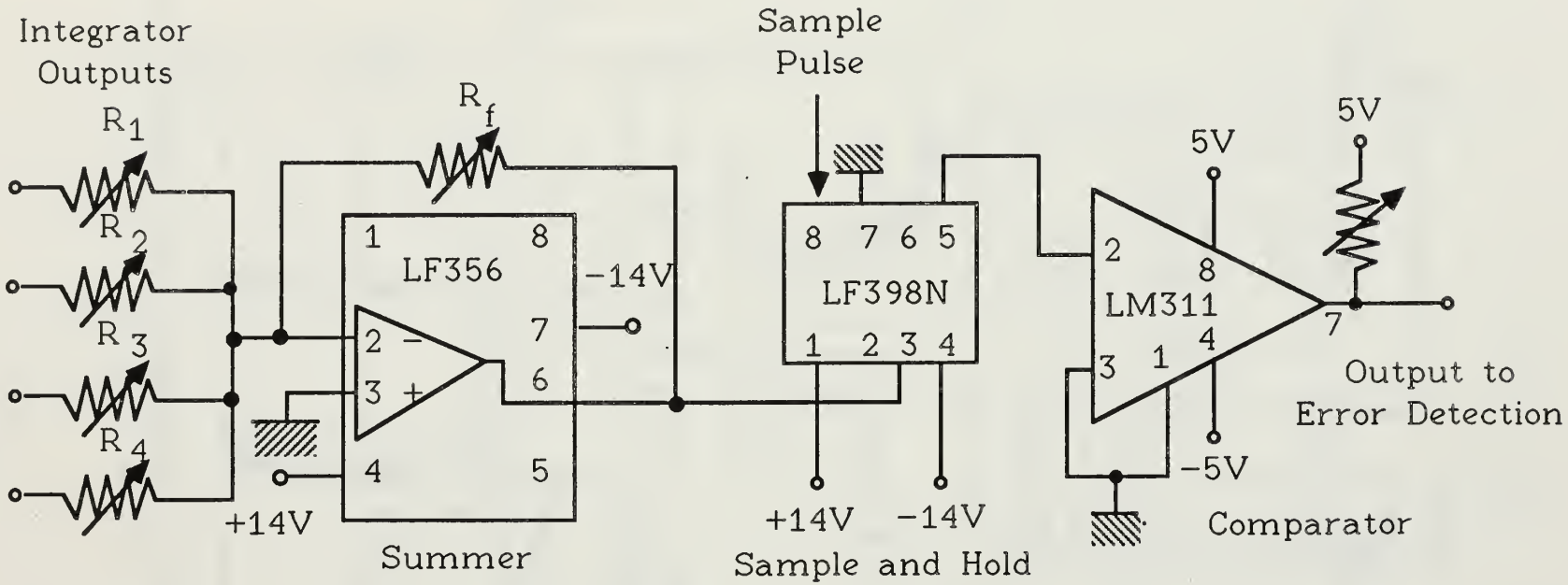


Figure A.19 Circuit Diagram of a Single Channel of the Decoding Circuitry

by the sample pulse shown in Figure A.18 at a rate of $r_b/3$ Hz. The LM311 voltage comparator is the decision circuit of the system. Based upon a zero voltage threshold, the comparator decides a negative voltage is a binary zero and a positive voltage is a binary one. The output voltage of the comparator is +5 Volts or 0 Volts.

The bit error detection circuit is shown in Figure A.20. The transmitted data is compared with the recovered data on a bit by bit basis using an XOR gate. If the data bits are the same, the XOR stays low. Both data pulses are strobed using AND gates. The strobe is produced by a dual one-shot which uses 20 kΩ variable resistors to position the data strobe at the center of each data pulse where the first pulse determines the time delay of the sample pulse. This eliminates errors due to the edges (switching times) of the pulse. If the bits differ, an error is counted. The error detection circuit is stopped and started by an external switch and another set of AND gates.

Figure A.21 is a shift register circuit which delays the transmitted data before it is compared with the received data in the error detection circuit. The transmitted data must be delayed to compensate for delays in the receiver.

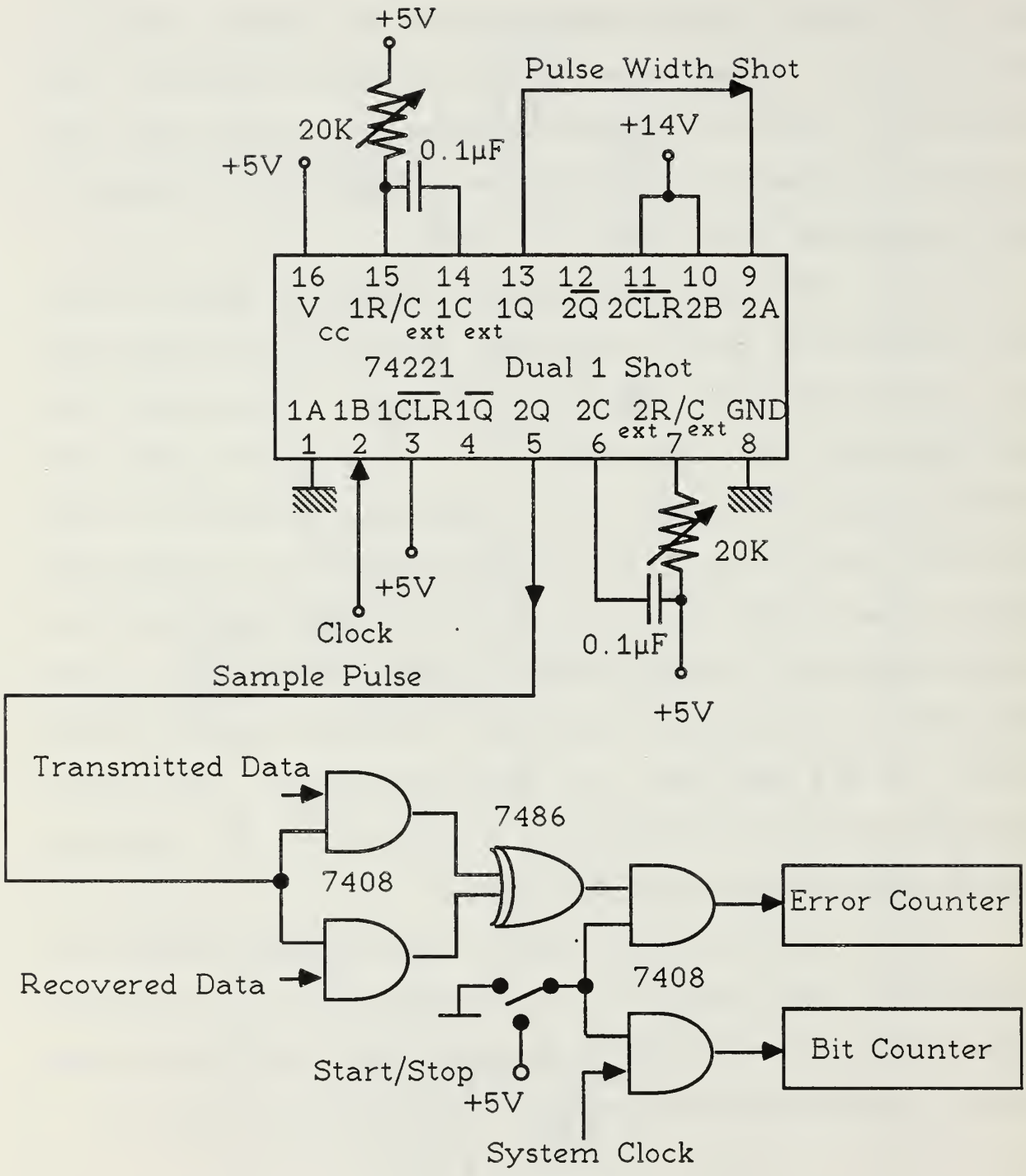


Figure A.20 Circuit Diagram of the Error Detection Subsystem

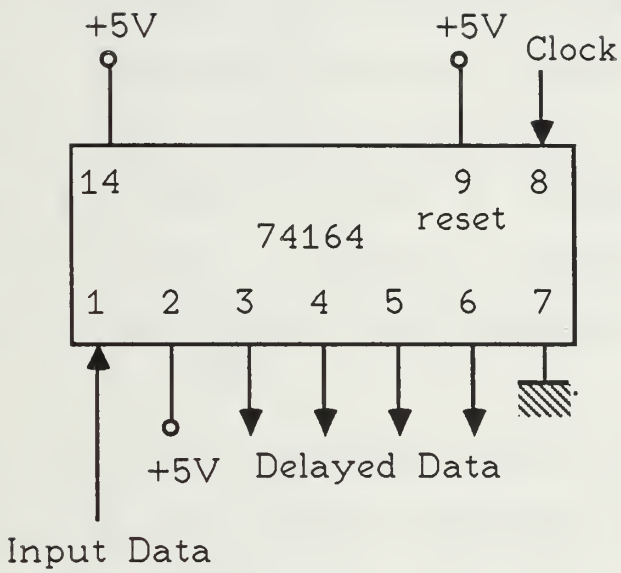


Figure A. 21 Circuit Diagram of the Shift Register

APPENDIX B

DERIVATION OF THE 2 FSK/QPSK PROBABILITY OF BIT ERROR EQUATION

The receiver decision process is based on the voltage value of $v_s(t)$ shown in Figure B.1. Samples are taken at the end of each symbol interval of duration T_s seconds. If $v_s(T_s)$ is greater than zero at the sample time, then a binary one is decided. If $v_s(T_s)$ is less than zero, then a binary zero is decided. Therefore, decisions are based on summer output voltage levels at the end of each symbol interval.

To determine that probability of bit error, the probability density functions (pdf's) of $v_s(T_s)$ given a one sent and given a zero sent are required.. Figure B.2 is an example of these two pdf's having mean values of +V volts and −V volts and variance of σ^2 watts.

The receiver model of a typical receiver channel (one of four used) is shown in Figure B.1. The following analysis uses the noise model of Rice [Ref. 6]. Assume

$$v_i(t) = A\cos\omega_1 t + n(t) \qquad (B.1)$$

and

$$v_r(t) = \cos\omega_1 t \ , \qquad (B.2)$$

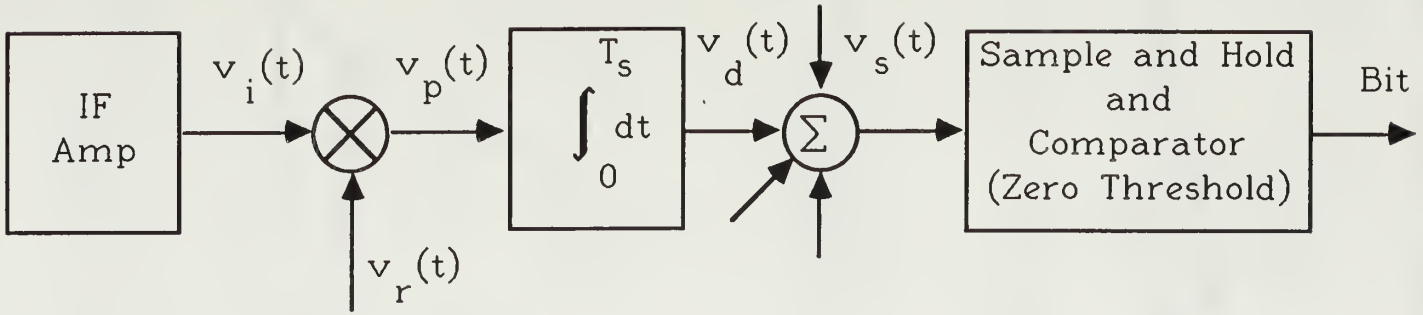


Figure B.1 Block Diagram of a Typical Receiver Channel

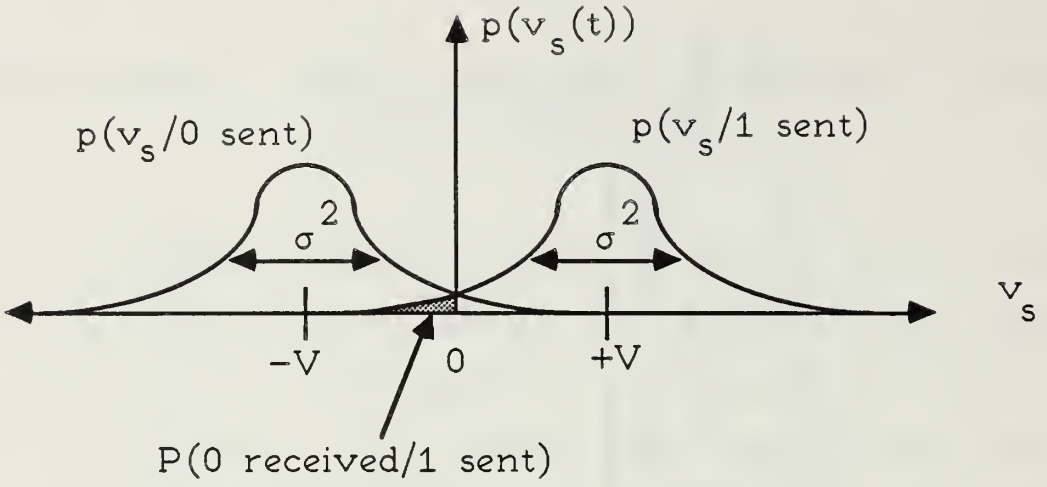


Figure B.2 Probability Density Function of the Summer Output

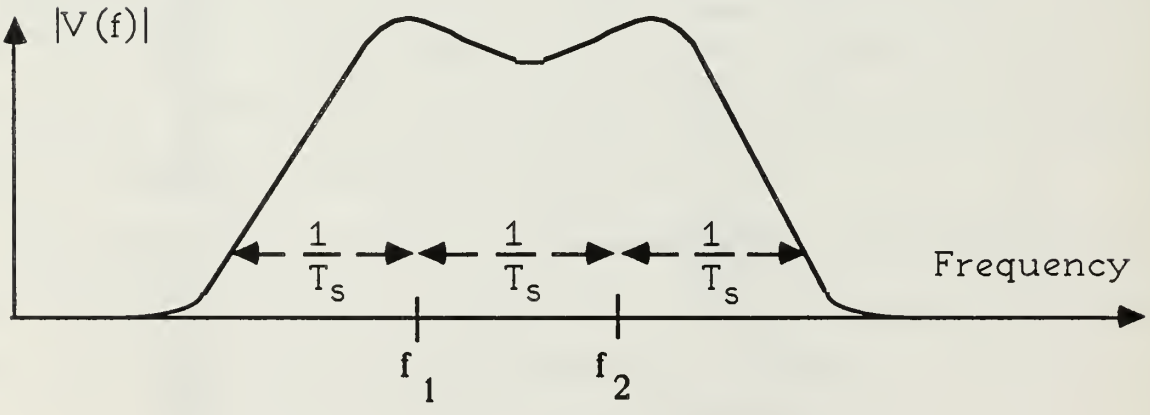


Figure B.3 Output of the Intermediate Frequency (IF) Amplifier

where $n(t)$ is bandpass Gaussian noise which can be written in terms of lowpass Gaussian noise voltage $x(t)$ and $y(t)$.

$$n(t) = x(t)\cos\omega_1 t - y(t)\sin\omega_1 t \qquad \text{(B.3)}$$

and $$\sigma_n^2 = \sigma_x^2 = \sigma_y^2 = N = \text{input noise power.} \qquad \text{(B.4)}$$

Since $v_p(t) = v_i(t)v_r(t)$, then using Equations B.1, B.2 and B.3,

$$v_p(t) = \frac{A}{2} + \frac{A}{2}\cos 2\omega_1 t + \frac{x(t)}{2} + \frac{x(t)}{2}\cos 2\omega_1 t - \frac{y(t)}{2}\sin 2\omega_1 t \qquad \text{(B.5)}$$

So,
$$v_d(t) = \int_0^{T_s} \frac{A}{2}dt + \int_0^{T_s} \frac{x(t)}{2}dt \qquad \text{(B.6)}$$

$$= \frac{AT_s}{2} + \int_0^{T_s} \frac{x(t)}{2}dt \qquad \text{(B.7)}$$

$$v_d(t) = V + \int_0^{T_s} \frac{x(t)}{2}dt \; . \qquad \text{(B.8)}$$

Since $x(t)$ is assumed to be Gaussian, then from Equation B.8, $v_d(t)$ is $N(V,\sigma^2)$. In the antipodal case, $v_d(t)$ is $N(-V,\sigma^2)$. For the other six symbols, $v_d(t)$ is $N(0,\sigma^2)$. Now, σ^2 is the AC power of $v_d(t)$ which becomes

$$\sigma^2 = E\{\int_0^{T_s}\frac{x(t)}{2}dt \int_0^{T_s}\frac{x(\tau)}{2}d\tau\} \quad . \tag{B.9}$$

Interchanging the order of integration and expectation results in

$$\sigma^2 = \int_0^{T_s}\int_0^{T_s}\frac{E\{x(t)\cdot x(\tau)\}}{4}\,dtd\tau \tag{B.10}$$

$$= \frac{1}{4}\int_0^{T_s}\int_0^{T_s}(R_{xx}(t-\tau))dtd\tau \quad . \tag{B.11}$$

For white noise,

$$R_{xx}(t-\tau) = \frac{N_o}{2}\ \delta(t-\tau) \quad . \tag{B.12}$$

where $N_o/2$ is the two-sided noise power spectral density function. Therefore,

$$\sigma^2 = \frac{N_o T_s}{8} \quad . \qquad \text{(B.13)}$$

Since all four inputs to the summer are Gaussian with variance σ^2 and since these four voltages are independent because of different frequencies or orthogonal phases, the input noise powers add. Therefore, $v_s(t)$ is $N(\frac{\pm AT_s}{2}, \frac{N_o T_s}{2})$.

To determine the error ratio (BER), the probability of receiving a zero when a one was sent must be calculated. This probability represents the shaded area in Figure B.2 which, for the Gaussian case, appears in equation form as

$$P_e = \int_{-\infty}^{0} \frac{1}{\sqrt{2\pi}\sigma} \exp\left(\frac{-(x-a)^2}{2\sigma^2}\right) dx \qquad \text{(B.14)}$$

where $a = \frac{AT_s}{2}$ and $\sigma^2 = \frac{N_o T_s}{2}$.

This reduces to

$$P_e = \frac{1}{2} \operatorname{erfc}\left(\frac{a}{\sqrt{2}\,\sigma}\right) \qquad \text{(B.15)}$$

$$= \frac{1}{2} \operatorname{erfc}\left(\frac{AT_s/2}{\sqrt{N_o T_s}}\right) \qquad \text{(B.16)}$$

$$= \frac{1}{2} \operatorname{erfc}\left(\frac{A\sqrt{T_s}}{2\sqrt{N_o}}\right) \quad . \qquad \text{(B.17)}$$

where $\text{erfc}(x) = \int_x^\infty e^{-\lambda^2}\, d\lambda$. Now, energy E_b per bit is

$$E_b = \frac{1}{3} E_s = \frac{1}{3}\left(\frac{A^2 T_s}{2}\right) = \frac{A^2 T_s}{6}, \qquad (B.18)$$

where E_s is energy per symbol. It follows that

$$A\sqrt{T_s} = \sqrt{6E_b}. \qquad (B.19)$$

Substituting Equation B.19 into B.17 results in

$$P_e = \frac{1}{2}\,\text{erfc}\left(\sqrt{\frac{3E_b}{2N_o}}\right). \qquad (B.20)$$

Signal power S is given by

$$S = \frac{A^2}{2}. \qquad (B.21)$$

Noise power is measured at the output of the IF amplifier. If the amplifier output has the spectrum shown in Figure B.3. The carriers having frequencies f_1 and f_2 are separated from each other by $1/T_s$. Each carrier is switched at a rate of $1/T_s$ Hz. Therefore the carrier having frequency f_1 has a sideband of width $1/T_s$ Hz and the carrier having frequency f_2 has a sideband width of $1/T_s$ Hz. Hence the total bandwidth is $3/T_s$ and noise power N is given by

$$N \approx \frac{N_o}{2}(2 \text{ sides})\left(\frac{3}{T_s}\right) = \frac{3N_o}{T_s} \quad . \qquad \text{(B.22)}$$

Using

$$N_o = \frac{NT_s}{3} \quad , \qquad \text{(B.23)}$$

and using Equations B.18 and B.21,

$$E_b = \frac{A^2}{2}\left(\frac{T_s}{3}\right) = S\,\frac{T_s}{3} \, , \qquad \text{(B.24)}$$

we can rewrite Equation B.20 as

$$P_e = \frac{1}{2}\,\text{erfc}\left(\sqrt{\frac{3}{2}\text{SNR}}\right). \qquad \text{(B.25)}$$

which is plotted in Figure 3.17.

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