FEASIBILITY STUDY OF $Pb_{1-x}Sn_xTe$ CHARGE COUPLED DEVICES FOR INFRARED IMAGING APPLICATIONS

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THESIS

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ABSTRACT

The purpose of this thesis is to examine the feasibility of narrow-gap semiconductor charged coupled devices for infrared imaging applications. The semiconductors considered are PbTe for a three to five micron imager and $Pb_{.76}Sn_{.24}Te$ for an eight to 12 micron imager, both operated at a temperature of 85°K. Theoretical calculations of signal current and storage time are made based on the metal-insulator-semiconductor theory developed for silicon M-I-S devices. For a 0.1°K temperature resolution of a 300°K scene, signal currents are 4.8×10^{-6} A/cm^2 for PbTe and 3.2×10^{-2} A/cm^2 for $Pb_{.76}Sn_{.24}Te$ at a clocking frequency of 1 MHz. Storage times of 5.7×10^{-5} seconds for PbTe and 1.27×10^{-6} seconds for $Pb_{.76}Sn_{.24}Te$ are calculated using a minority lifetime of 10^{-7} seconds. Therefore, clocking frequencies higher than 1 MHz are recommended. Experimental studies of $Pb_{1-x}Sn_xTe$ M-I-S were made which demonstrated that accumulation, depletion, and inversion layers can be controlled by gate voltage, following the general behavior of silicon M-I-S devices. A PbTe CCD infrared imager seems feasible. Feasibility of $Pb_{.76}Sn_{.24}Te$ CCD's will require significant improvements in material and fabrication technology to increase storage time and reduce dark current.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

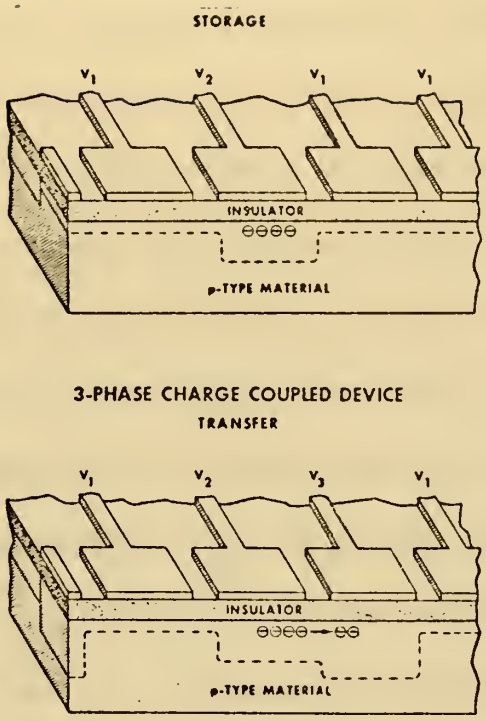
I. INTRODUCTION

A. THE CHARGE COUPLED DEVICE PRINCIPLE

The basic CCD concept consists of storing electrons (or holes) in potential wells created at the surface of a semiconductor and moving these charges as a unit across the surface by varying the depth of the potential well. This is accomplished by first applying a voltage to metal electrodes on an insulated surface of the semiconductor (a metal-insulator-semiconductor or M-I-S structure) to deplete the semiconductor surface of majority carriers. Then charges, representing a signal, can be introduced either electrically or optically into the depletion region under one of the electrodes. If a second electrode is sufficiently close, the charges may be transferred by applying a larger voltage to the second electrode, thus creating a deeper potential well. A simple three-level pulse sequence applied to the electrodes can be used to move a train of charge packets along the device in either direction [17].

B. PARAMETERS AFFECTING CCD OPERATION

For the CCD concept to be realized, several factors of the materials involved must be considered. The depletion region formed in the semiconductor must be deep enough to be able to store a useful amount of signal charge. This is related to the deep-depletion capacitance and inversion capacitance of the semiconductor, which in turn are determined



A 3-phase CCD

Figure 1

by the doping concentration, the dielectric constants of both the insulator and semiconductor, insulator thickness, and the temperature of operation.

After a charge is introduced into the depletion region under an electrode, the charge must remain there a sufficient time for the transfer to be accomplished. The length of time required for a transfer is the period of the clocking signal. The dark currents of the M-I-S structure determines the charge storage time in the depletion region. Thus the storage time must be long enough to allow the use of a reasonable clocking frequency.

Another key feature that determines the usefulness of a charge transfer device is whether the complete signal charge packet is transferred

along the device. Interface states at the semiconductor-insulator interface is the prime factor governing the amount of charge transferred. As each charge packet passes along the device, it fills the interface states almost instantaneously and then when it moves on, the states empty much more slowly. Some of the charges emitted from the interface states return to the correct packet but others empty into succeeding packets. This gives rise to a blurring effect in the signal, thus reducing its quality. The primary effect of interface states can be overcome by passing a background charge along the device. This is the so called "fat zero" operation. The background charges should completely fill the exposed interface states so that additional signal charge will not appreciably change the situation. However, this background charge takes up a portion of the storage capabilities of the device, reducing the amount of signal that can be transferred.

Factors relating to the use of a CCD in a production-type system can also be considered. The doping concentration of the semiconductor must be one that is realistically attainable. The thickness of the insulating material must be large enough to permit ease of manufacture with a relatively high yield. The amplitudes of the pulse sequence for transferring the signal must be low enough to prevent device breakdown, yet be effective in manipulating the depth of the depletion region. The temperature of operation should be in the range that does not require undully expensive and heavy cryogenic equipment.

C. THE INFRARED CCD

CCD structures have been extensively studied using silicon. These devices have many applications, including digital and analog memory and visible imaging. However, little work has been done to extend the CCD principle to infrared imaging. For use at infrared, the semiconductor in the CCD must be sensitive to infrared energy. That is, the band gap of the semiconductor must be narrow enough for the lower energy infrared photons to excite electrons from the valence band to the conduction band. The energy of a photon is related to its wavelength by

$$E(eV) = \frac{1.24}{\lambda} \qquad (1)$$

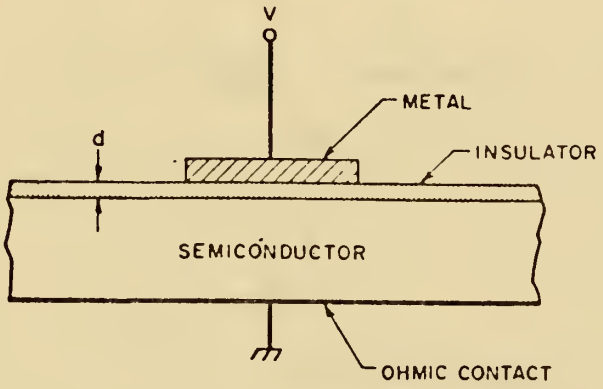
where λ is the wavelength in microns. Two very useful infrared radiation spectra are in the three to five micron and eight to 14 micron ranges. These are two of the so-called atmospheric "windows" where the radiation is not severely attenuated by the earth's atmosphere. Thus the energy gap of an infrared-sensitive semiconductor must be less than 0.24eV for three to five micron use and less than 0.09eV for eight to 14 micron use. The compound PbTe has an energy gap of .219eV at 85°K making it suitable for three to five micron infrared applications, while the alloy $Pb_{.76}Sn_{.24}Te$ has an energy gap of .102eV at 85°K, making it useful in the eight to 12 micron range.

II. METAL-INSULATOR-SEMICONDUCTOR THEORY

The building block for a CCD is the metal gate on the insulated surface of a semiconductor. This is an M-I-S structure. Therefore, it is appropriate to study the characteristics of a single M-I-S device to determine its feasibility for use in an infrared CCD.

A. THE IDEAL M-I-S STRUCTURE

The M-I-S structure is formed by depositing an insulator on the surface of a semiconductor, then a metal pad or gate is deposited on to the insulator.



The M-I-S Structure

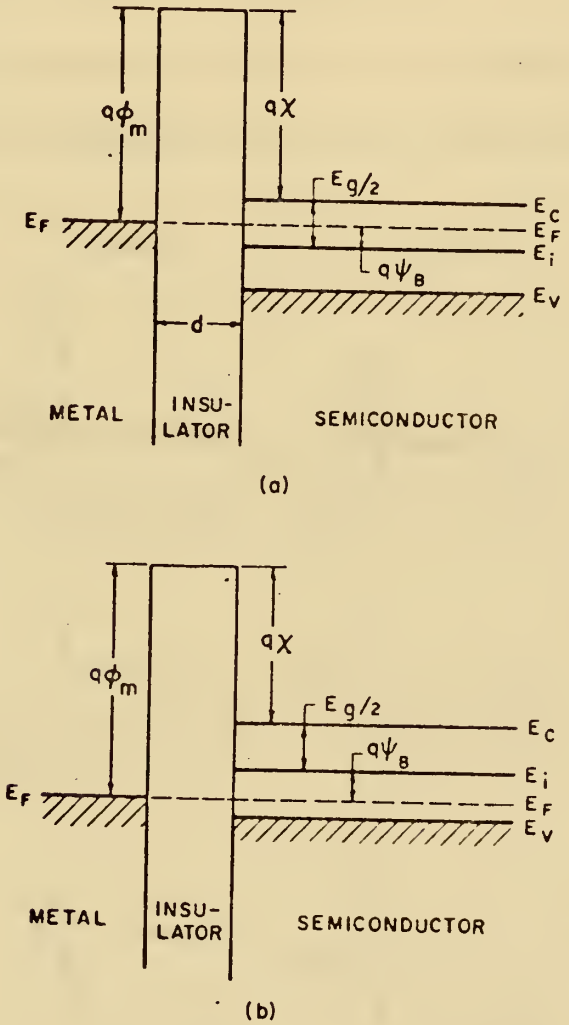
Figure 2

An ideal M-I-S structure, whose energy-band diagram at zero applied voltage is shown in Fig. 3, is defined as follows. First, there is no energy difference between the metal work function and the semiconductor work function, or

$$\Phi_{ms} = \Phi_m - (\chi + E_g/2_q - \Psi_B) = 0 \text{ for n-type} \qquad (2)$$

$$\Phi_{ms} = \Phi_m - (\chi + E_g/2_q + \Psi_B) = 0 \text{ for p-type} \qquad (3)$$

where Φ_m is the metal work function, χ is the semiconductor electron affinity, E_c is the energy of the lower edge of the conduction band, E_v is the energy of the upper edge of the valence band, E_g is the band gap, q is the charge of an electron, and Ψ_B is the potential difference between the Fermi level E_F and the intrinsic Fermi level E_i. In other

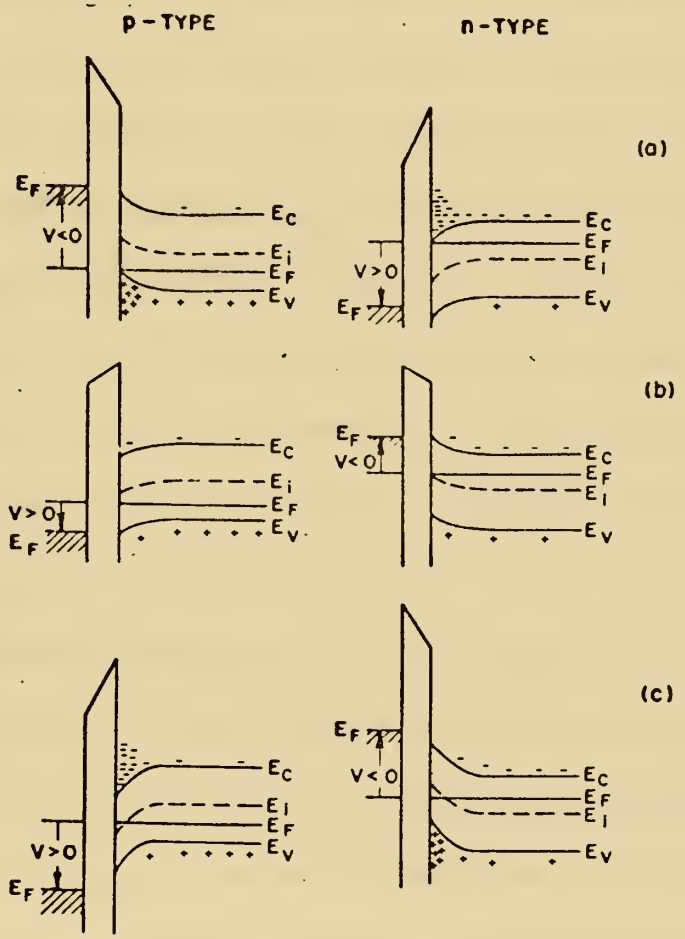


An Ideal M-I-S Band Diagram at Zero Bias

Figure·3

words, the bands are flat when there is no applied voltage. Secondly, the only charges that can exist in the structure under any biasing conditions are those in the semiconductor and those with equal but opposite sign on the metal surface adjacent to the insulator. Finally, there is no carrier transport through the insulator under dc biasing conditions, or the resistivity of the insulator is infinite [20].

When an ideal M-I-S device is biased with positive or negative voltages, there are basically three cases which may exist at the



Band Diagrams at (a) accumulation (b) depletion (c) inversion

Figure 4

semiconductor surface. These cases are illustrated in Fig. 4. First consider the p-type semiconductor. When a negative voltage is applied to the metal gate, the top of the valence band bends upward and is closer to the Fermi level. For an ideal M-I-S device there is no current flow in the structure, so the Fermi level remains constant in the semiconductor. Since the carrier density depends exponentially on the energy difference (E_F-E_v), this band bending causes an accumulation of majority carriers (holes) near the semiconductor surface. This is the "accumulation" case. When a small positive voltage is applied, the bands bend downward, and the majority carriers are depleted. This is the "depletion" case. When a larger positive voltage is applied, the bands bend even more downward such that the intrinsic level E_i at the surface crosses over the Fermi level E_F. Beyond this point the number of electrons (minority carriers) at the surface is larger than the number of holes, the surface is thus inverted and this is the case of "inversion." Similar results can be obtained for the n-type semiconductor, however, the polarity of the voltages should be reversed [15].

This voltage dependence of the M-I-S device can be characterized by the capacitance vs. bias voltage relationships in the structure. For charge neutrality in the system to be maintained, the charge per unit area on the metal Q_M must equal the total charges per unit area in the semiconductor Q_s for all bias voltages. The applied voltage will appear partly across the insulator and partly across the semiconductor. Then the potential across the insulator is given by

$$V_i = \frac{Q_M d}{\epsilon_i} = \frac{Q_M}{C_i} \qquad (4)$$

where C_i is the capacitance per unit area due to the insulator. The capacitance due to the semiconductor C_s is voltage dependent, determined by the charge distribution in the semiconductor. Thus the M-I-S device can be modeled as two capacitances in series, one constant and one voltage dependent.

A qualitative description of the ideal M-I-S capacitance-voltage curve is now possible. Again consider a p-type semiconductor. In the accumulation region (negative voltage), there is an accumulation of holes at the semiconductor-insulator interface and therefore a large capacitance. Thus the total capacitance is approximately equal to the insulator capacitance. Reduction of the negative bias leads to a reduced hole density

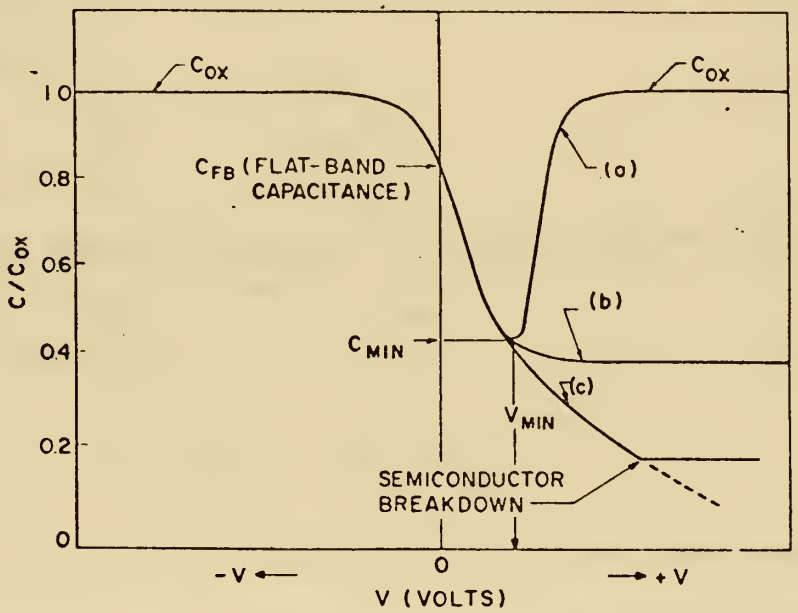


Figure 5. Ideal M-I-S Capacitance-voltage Curves
(a) low frequency
(b) high frequency
(c) deep depletion

and finally to the formation of a depletion layer. The depleted surface region contains practically no carriers and acts as a dielectric in series with the insulator. Thus the total capacity drops. The curve then goes thru a minimum and increases again as an inversion layer of electrons (minority carriers) forms at the surface. This increase is dependent upon the ability of the electron concentration to follow the applied signal. If the signal frequency is high, the electrons cannot follow the variations and the electrons will not appear at the surface, thus the capacitance remains low. In the positive voltage region under non-equilibrium conditions the capacitance continues to decrease [20]. This case of deep depletion will be discussed in greater detail below.

To obtain a more quantitative view of the ideal M-I-S C-V curve, the equations describing the capacitance must be developed. A differential capacitance associated with the semiconductor space charge region is defined by

$$C_s \equiv \frac{\partial Q_s}{\partial V_s} \tag{5}$$

The total charge per unit area in the semiconductor is given by

$$Q_s = \int_0^\infty \rho\,(x)dx \tag{6}$$

where

$$\rho = q(p - n + N_D - N_A) \tag{7}$$

and the point $x = 0$ corresponds to the insulator-semiconductor interface. The quantity $(N_D - N_A)$ is the doping level within the semiconductor. The free carrier concentrations are given by

$$p = n_i \, \mathrm{EXP}\,(U_F - U) \tag{8}$$

$$n = n_i \, \mathrm{EXP}\,(U - U_F) \tag{9}$$

where $U = \frac{q\phi}{kT}$ is the normalized electrostatic potential measured from the intrinsic Fermi level. $N_D - N_A$ may be calculated to yield

$$N_D - N_A = 2\, n_i \, \mathrm{SINH}\, |U_F| \tag{10}$$

The charge in the depletion layer and in the inversion layer as a function of surface potential requires the integration of the one-dimensional Poisson equation giving

$$Q_s = -2 \frac{U_s}{|U_s|} q\, n_i\, L_D \left\{ 2 \left[\mathrm{COSH}(U_s - U_F) - \mathrm{COSH}\, U_F + U_s \, \mathrm{SINH}\, U_F \right] \right\}^{1/2} \tag{11}$$

where

$$L_D = \left[\frac{kT\epsilon_s}{2q^2 n_i} \right]^{1/2} \tag{12}$$

is the intrinsic Debye length and the factor $\frac{U_s}{|U_s|}$ insures a physically meaningful sign. Now the part of Q_s which is due to the electrons within the inversion region can be calculated by a second integration of Poisson's equation giving

$$Q_n = - \frac{U_s}{|U_s|} q\, n_i\, L_D \int_{U_F}^{U_s} \frac{\mathrm{EXP}(U-U_F)\, du}{\left\{ 2 \left[\mathrm{COSH}(U-U_F) - \mathrm{COSH}\, U_F + U \, \mathrm{SINH}\, U_F \right] \right\}^{1/2}} \tag{13}$$

Now Q_s can be written in terms of Q_n and an effective depletion width X_d as

$$Q_s = Q_n + q(N_D - N_A) X_d \tag{14}$$

Returning to the definition of the semiconductor space-charge capacitance, the total system capacitance can now be obtained, but three cases must be considered.

At low enough measurement frequencies the minority carriers as well as the majority carriers will be able to reach equilibrium and follow the variation of the measurement signal. In this case the semiconductor capacitance can be calculated on the basis of equilibrium theory by differentiating equation (11) with respect to the surface potential yielding

$$C_s = \epsilon_s \frac{q(p - n + N_D - N_A)}{Q_s} \tag{15}$$

When the signal frequency is higher than the minority carrier generation rate, only the majority carriers will be able to follow the variations of the measurement signal and therefore the equilibrium theory cannot be applied. Instead, the space charge capacitance is obtained by differentiating equation (14), keeping the charge of the electrons in the inversion region constant or $\frac{\partial Q_n}{\partial \phi_s} = 0$. This yields

$$C_s = \frac{\epsilon_s}{X_d} \tag{16}$$

Note, however, that this is valid only in depletion and inversion regions. In the accumulation region, the same equation as developed for the low frequency case is applied.

Recall that the total capacitance of the M-I-S device is modelled as the series combination of the insulator capacitance and the semiconductor capacitance as

$$C = \frac{C_i C_s}{C_i + C_s} \tag{17}$$

This equation is usually normalized to the insulator capacitance to yield

$$\frac{C}{C_i} = \frac{1}{C_i/C_s + 1} \tag{18}$$

If the capacitance is measured under such conditions that minority carriers cannot accumulate near the surface in the inversion case, the capacitance-voltage relationship will be much like that of a reverse biased p-n junction. This situation is encountered if the dc bias is switched rapidly from accumulation to inversion and the capacitance is measured before minority carriers can accumulate near the surface. Thus, this analysis corresponds to the transient case. The capacitance will again be given by equation (16), but since $Q_n = 0$, the depletion width relationship is derived from

$$Q_s = q(N_D - N_A) X_d \tag{19}$$

Integrating Poisson's equation twice and substituting into equation (18), the normalized capacitance is given by

$$\frac{C}{C_i} = \frac{1}{\left[1 + \frac{2K_i^2 \epsilon_o}{q(N_D - N_A) K_s X_o^2} V_A\right]^{1/2}} \tag{20}$$

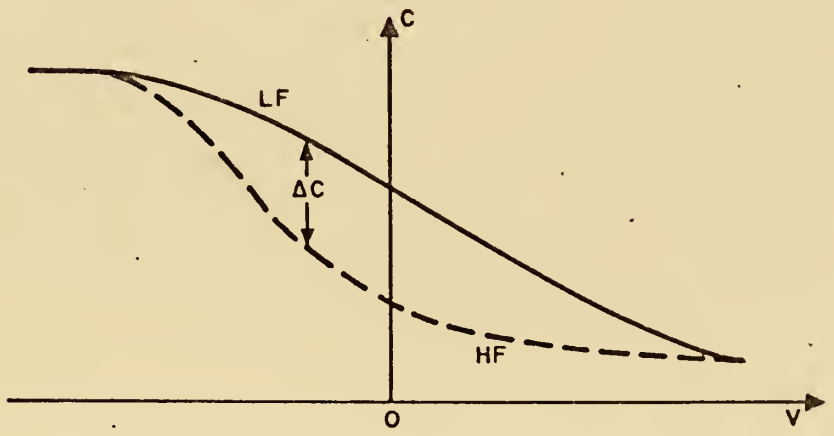
In this case, the overall capacitance keeps decreasing with increasing bias due to the unlimited increase in the depletion width which takes place if minority carriers cannot accumulate near the surface [5].

B. THE NON-IDEAL M-I-S STRUCTURE

The fabrication of M-I-S devices and the physical parameters of the materials involved introduce factors that cause deviations from the ideal behavior. To compare experimental and ideal results requires a knowledge of these factors and their influences. The most common of these are discussed below.

1. Interface States

An interface state is defined as an allowed energy level within the forbidden gap at the surface. There are two types of interface states, namely donor states and acceptor states. A donor state can have



Variation in C-V Curve due to Interface States

Figure 6

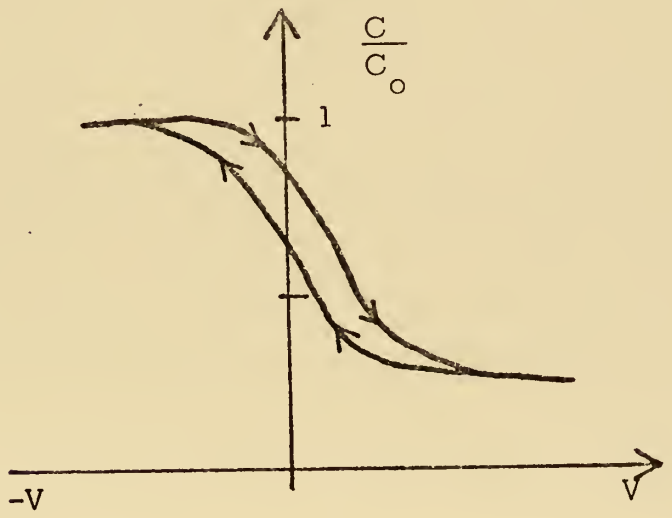
two states of charge. It can be neutral, or it can become positive by giving up an electron. Its state of charge is controlled by the Fermi level. It is always in its more positive state when it is above the Fermi level. An acceptor state, which follows the same rule, changes its charge from neutral to negative. When there is band bending in an M-I-S due to the external bias, the surface state levels will move with the valence and conduction bands, while the Fermi level remains fixed. A change of charge in the interface state occurs when it crosses the Fermi level. This change of charge contributes to the M-I-S capacitance and can alter the ideal curve. This change, pictured in Fig. 6, shows a threefold effect. The interface states give an additional capacitance, they cause a frequency dispersion, and they change the voltage axis by changing the dependence of the surface potential on the applied bias [20].

2. Metal Work Function

For an ideal M-I-S structure it was assumed that the metal-semiconductor work function difference was zero. If the value of ϕ_{ms} is not zero, the experimental capacitance-voltage curve will be displaced from the ideal theoretical curve by an amount equal to ϕ_{ms}. This deviation is not a serious drawback because the displacement can be calculated easily and it does not deform the shape of the curve.

3. Charges in the Insulator

There are basically two types of charges found in the insulator, namely fixed charges and mobile ions. Both types are introduced during the fabrication of the M-I-S device. The fixed charge is located near or at the semiconductor surface and is immobile under an applied electric



Hysterisis Effect

Figure 7

field. Thus a portion of the bias voltage will be required to neutralize the effect of the fixed charge, causing a parallel voltage shift in the CV curve. However, no distortion of the curve is introduced. The mobile ions will tend to follow the variation of the applied bias, but more slowly than the carriers. This will give a hysterisis effect to the curve (as shown in Fig. 7). That is, a curve generated by a negative to positive sweep of the bias will be shifted from one generated with a positive to negative sweep.

III. ANALYSIS OF THE IDEAL M-I-S STRUCTURE

A group at Westinghouse [14] developed a computer program to generate ideal high frequency and low frequency capacitance-voltage data for the Al-SiO_2-Si M-I-S structure. This program was generalized to make it suitable for the analysis of all M-I-S systems, especially those for infrared applications. The program was also modified to compute the deep-depletion capacitance data and several other quantities related to CCD studies. A graphical output routine was added to allow quicker interpretation of and comparison with experimental curves. With the aid of this program and data obtained from other research efforts, an attempt was made to determine the optimum material parameters for the feasibility study of an infrared CCD.

A. CAPACITANCE-VOLTAGE VARIATION WITH MATERIAL PARAMETERS

To obtain the optimum combination of material parameters, the semiconductor doping density, the insulator thickness, and the temperature are varied independently. Comparison of their results will provide a qualitative estimate of each parameter that is best suited for CCD use. Then choosing exact values on the basis of manufacturing feasibility, quantitative information is obtained for the "best case." The criteria for comparison is the amount of charge storage at the same bias voltage. This data is obtained from the computer output by the method explained

in paragraph (B) of this section. Many cases were considered but only two representative cases of each parameter are presented for brevity.

1. Semiconductor Doping

Figures 8 and 9 show the ideal capacitance-voltage curves for p-type $Pb_{.76}Sn_{.24}Te$ with the semiconductor doping $N_A = 1.0x10^{16}$ cm^{-3} and $N_A = 1.0x10^{17}$ cm^{-3} respectively. The temperature is 85°K and a 100Å thick Al_2O_3 insulator is used in each case. Comparison (see pages 67-74 for computer output) of $Q_{storage}$ at an applied bias of .57V reveals that the lower doping density creates a storage capability approximately 10 times greater than the higher doping density. This indicates that a low doping density is more attractive to CCD applications.

2. Insulator Thickness

Figures 10 and 11 present the CV curves for a p-type $Pb_{.76}Sn_{.24}Te$ with a 100Å and 300Å thick Al_2O_3 insulator respectively. Doping density $N_A = 1.0x10^{16}$ cm^{-3} and the temperature is 85°K in each case. Comparison of the storage capacity at a bias of .23V reveals that the thinner insulator has a storage capacity approximately 30 times larger. The indication is that a thin insulator is more appropriate for infrared CCD's.

3. Temperature

Figures 12 and 13 give the capacitance-voltage curves for p-type $Pb_{.76}Sn_{.24}Te$ at temperatures of 85°K and 150°K respectively. The doping concentration N_A is $1.0x10^{16}$ cm^{-3} and the Al_2O_3 insulator thickness is 100Å in each case. At a bias voltage of .46V, the charge

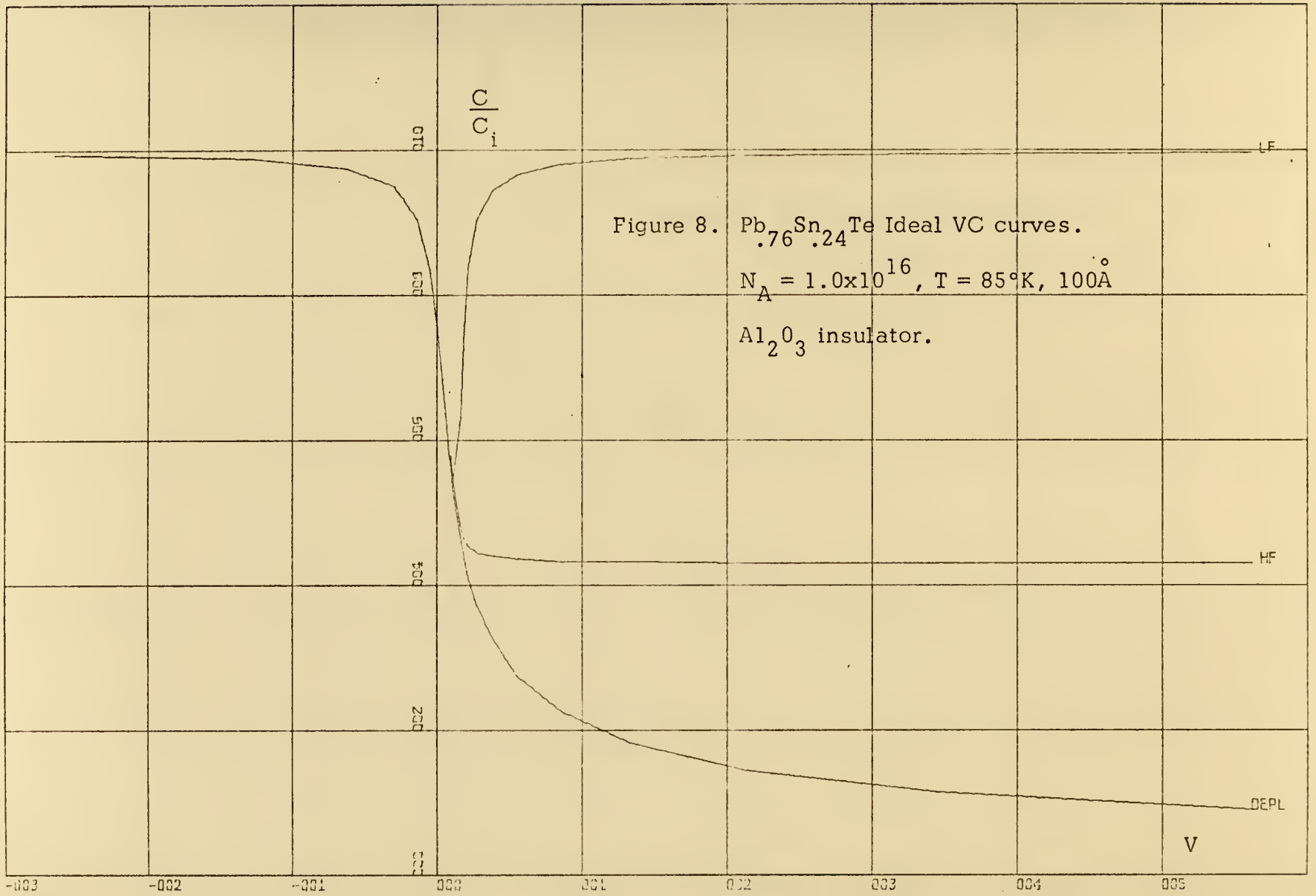


Figure 8. $Pb_{.76}Sn_{.24}Te$ Ideal VC curves.

$N_A = 1.0 \times 10^{16}$, T = 85°K, 100Å

Al_2O_3 insulator.

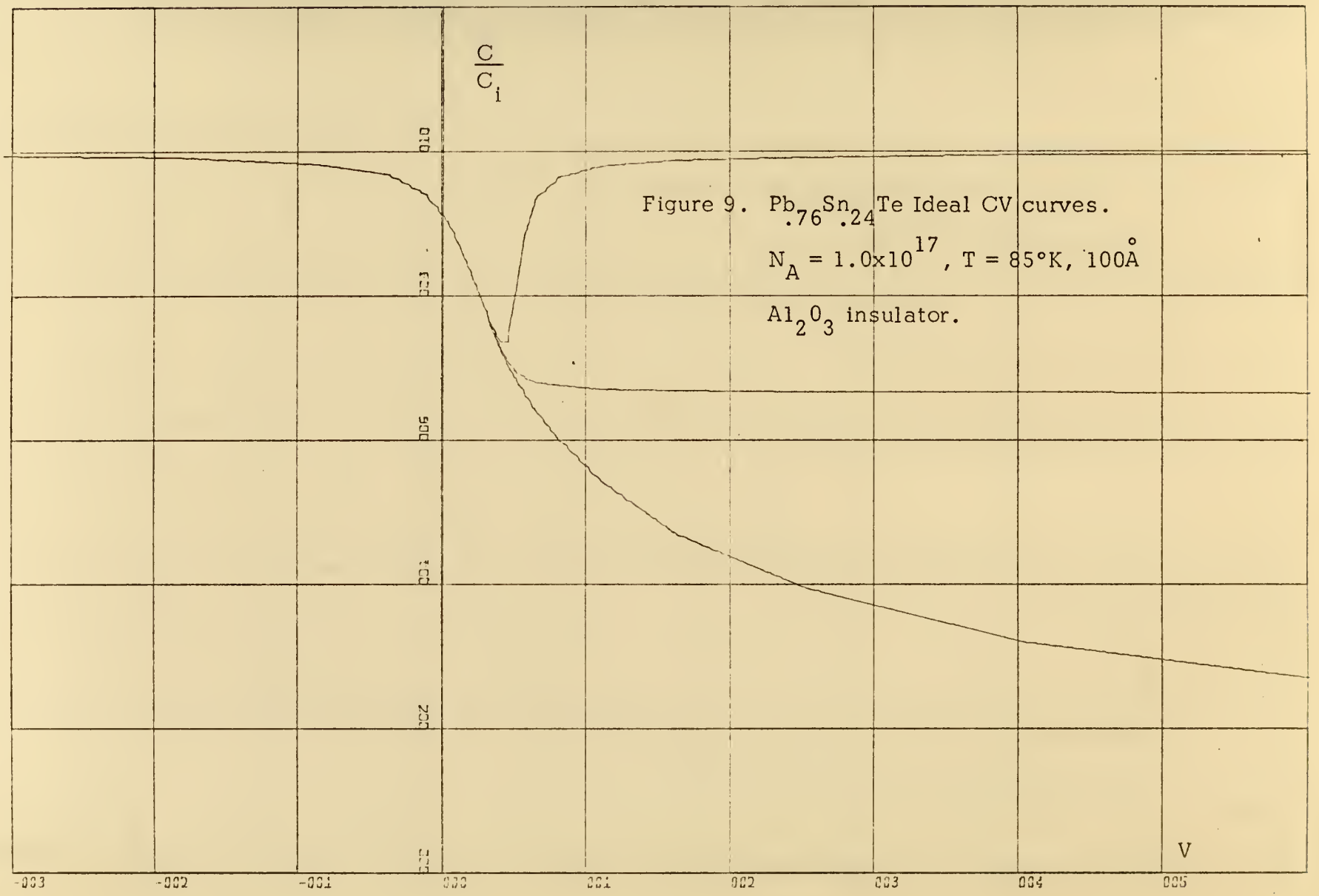


Figure 9. $Pb_{.76}Sn_{.24}Te$ Ideal CV curves.
$N_A = 1.0 \times 10^{17}$, T = 85°K, 100Å
Al_2O_3 insulator.

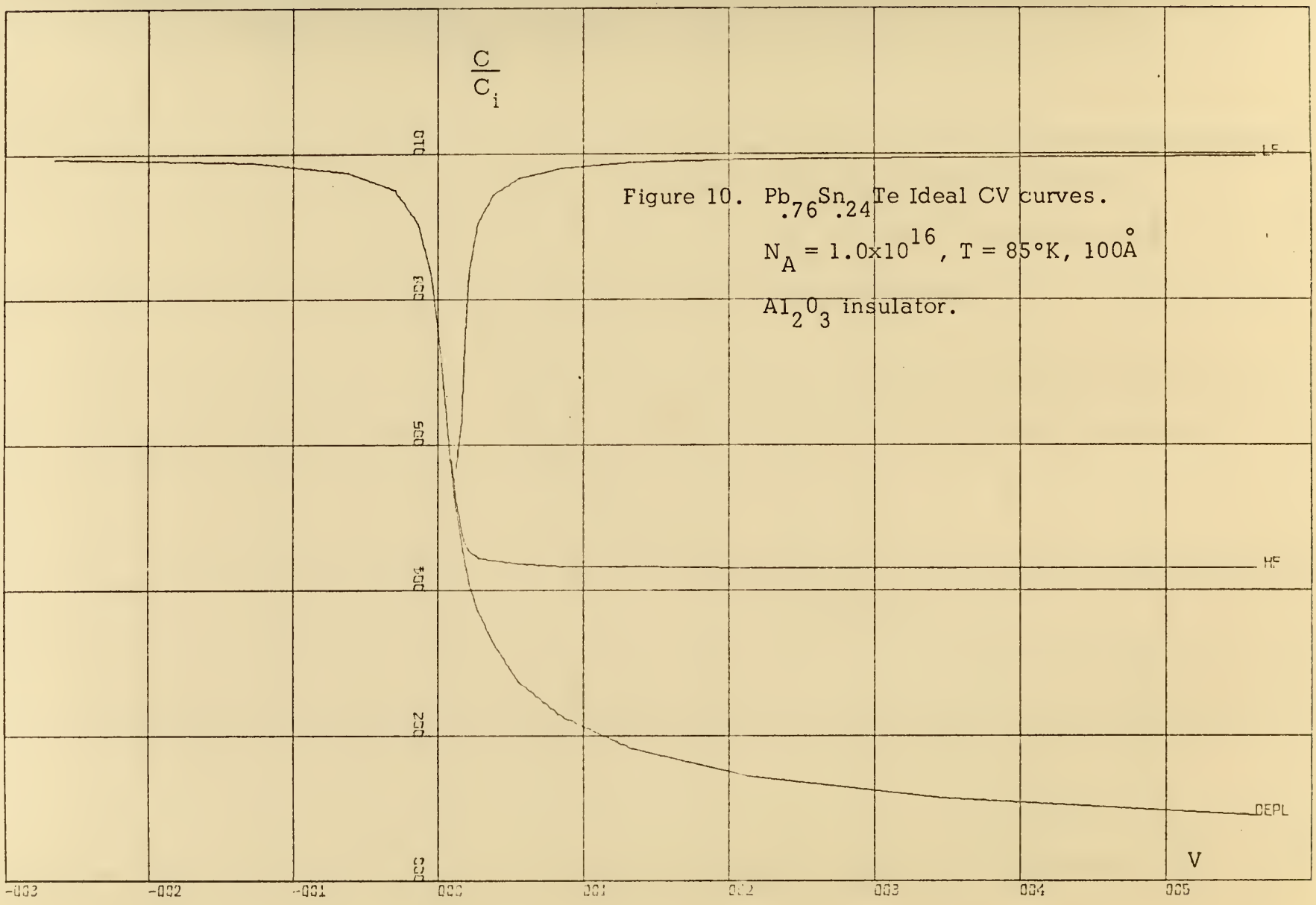


Figure 10. $Pb_{.76}Sn_{.24}Te$ Ideal CV curves.
$N_A = 1.0 \times 10^{16}$, T = 85°K, 100Å
Al_2O_3 insulator.

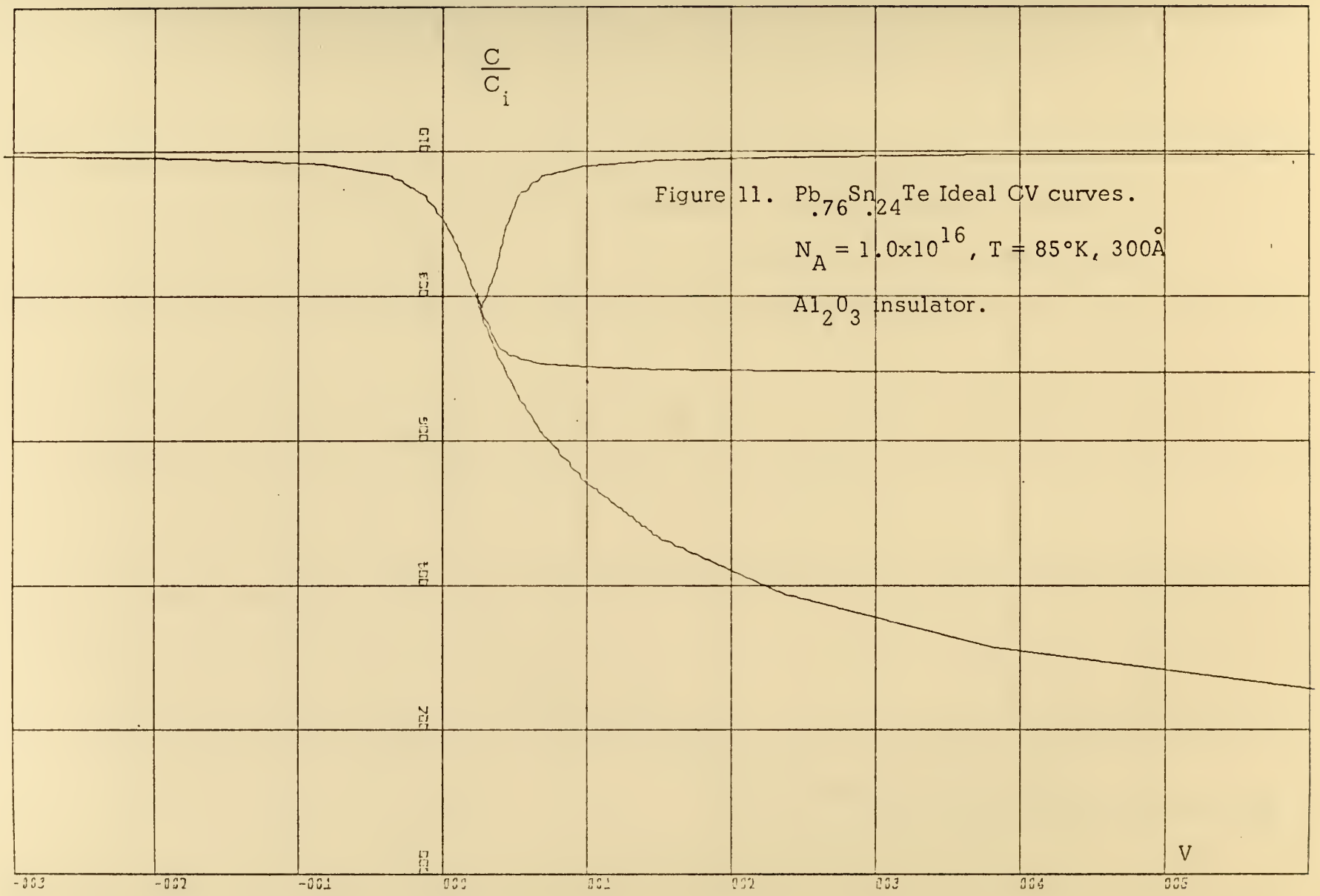


Figure 11. $Pb_{.76}Sn_{.24}Te$ Ideal CV curves.
$N_A = 1.0 \times 10^{16}$, T = 85°K, 300Å
Al_2O_3 insulator.

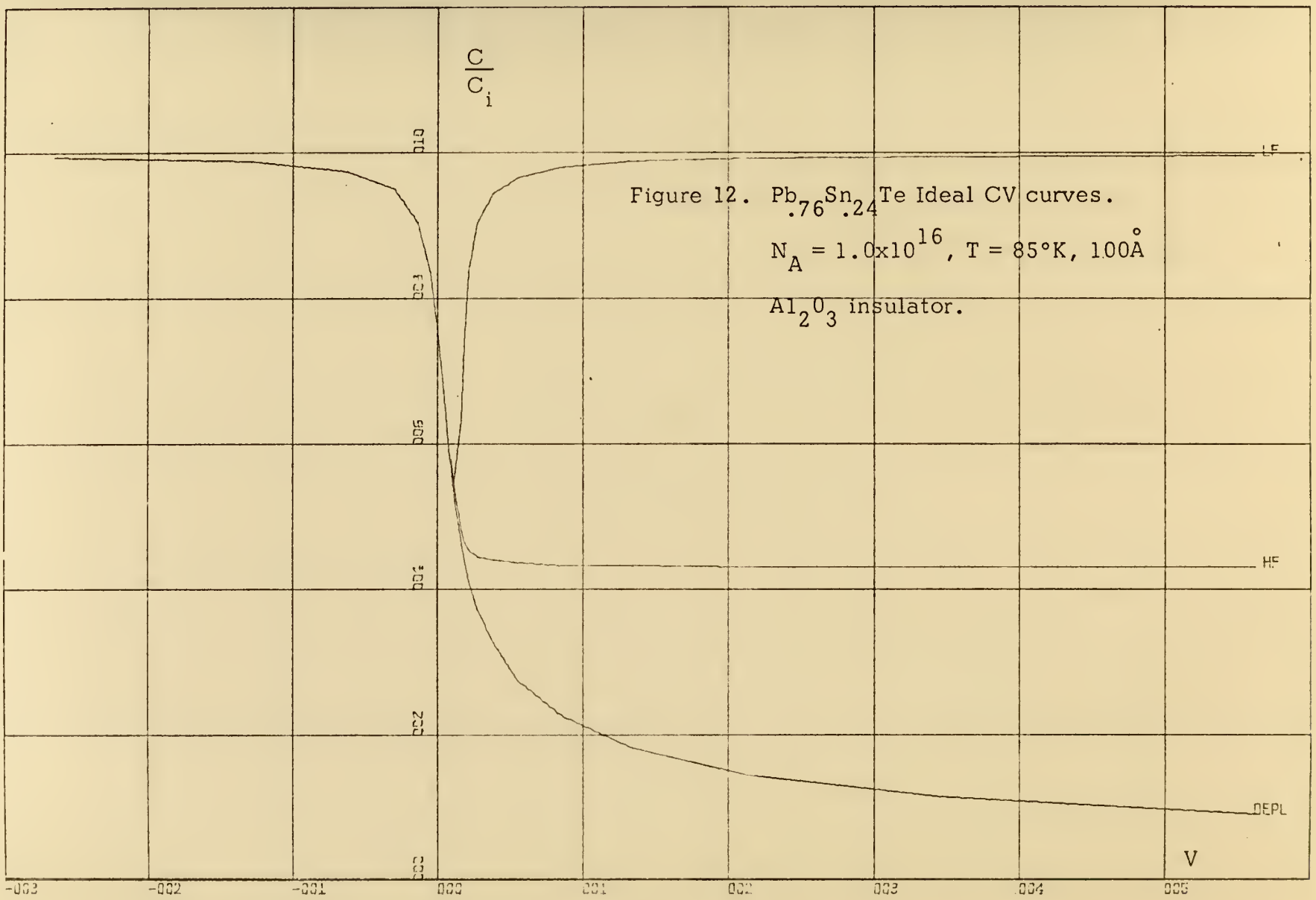


Figure 12. $Pb_{.76}Sn_{.24}Te$ Ideal CV curves.
$N_A = 1.0 \times 10^{16}$, T = 85°K, 100Å
Al_2O_3 insulator.

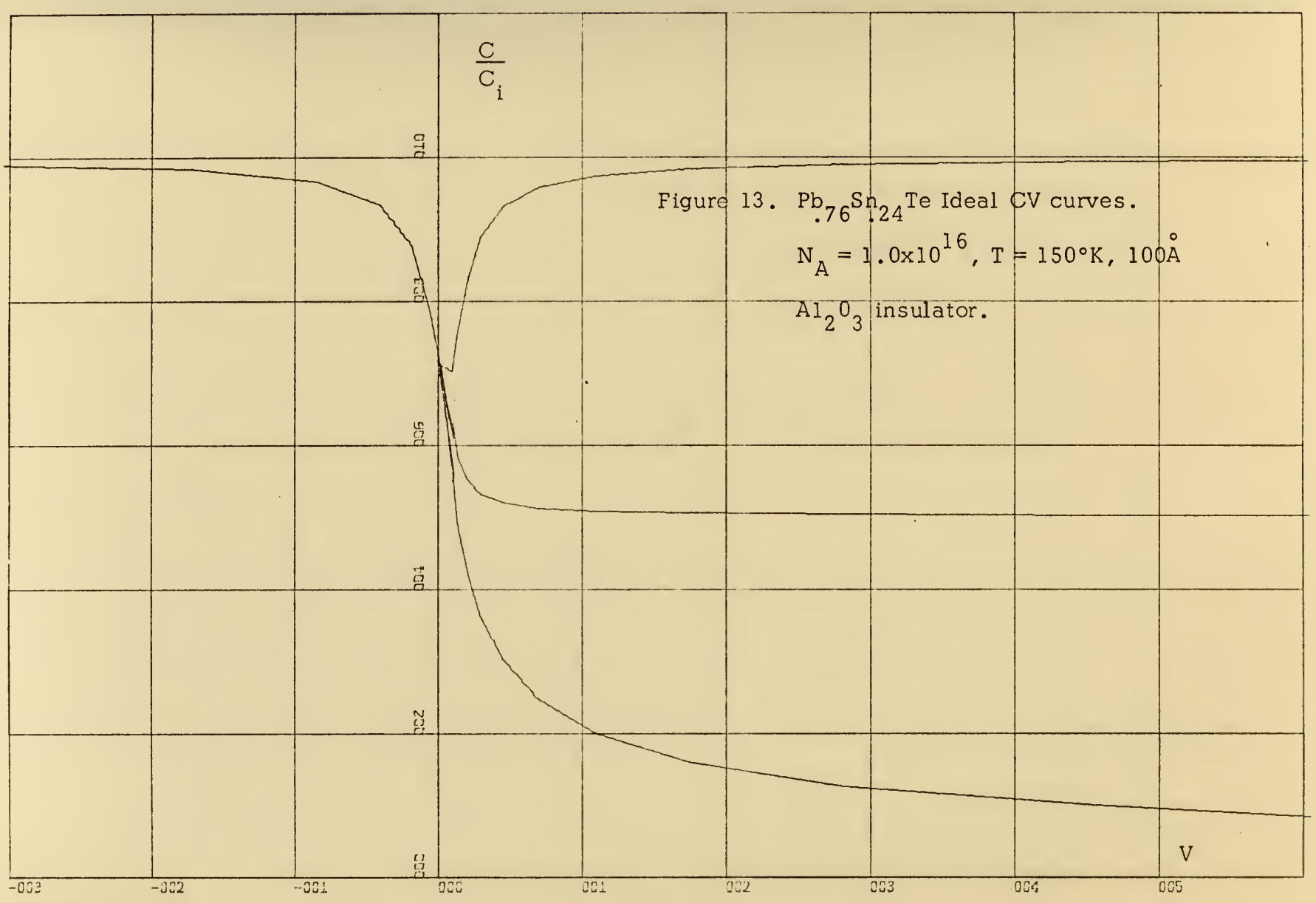


Figure 13. $Pb_{.76}Sn_{.24}Te$ Ideal CV curves.
$N_A = 1.0 \times 10^{16}$, T = 150°K, 100Å
Al_2O_3 insulator.

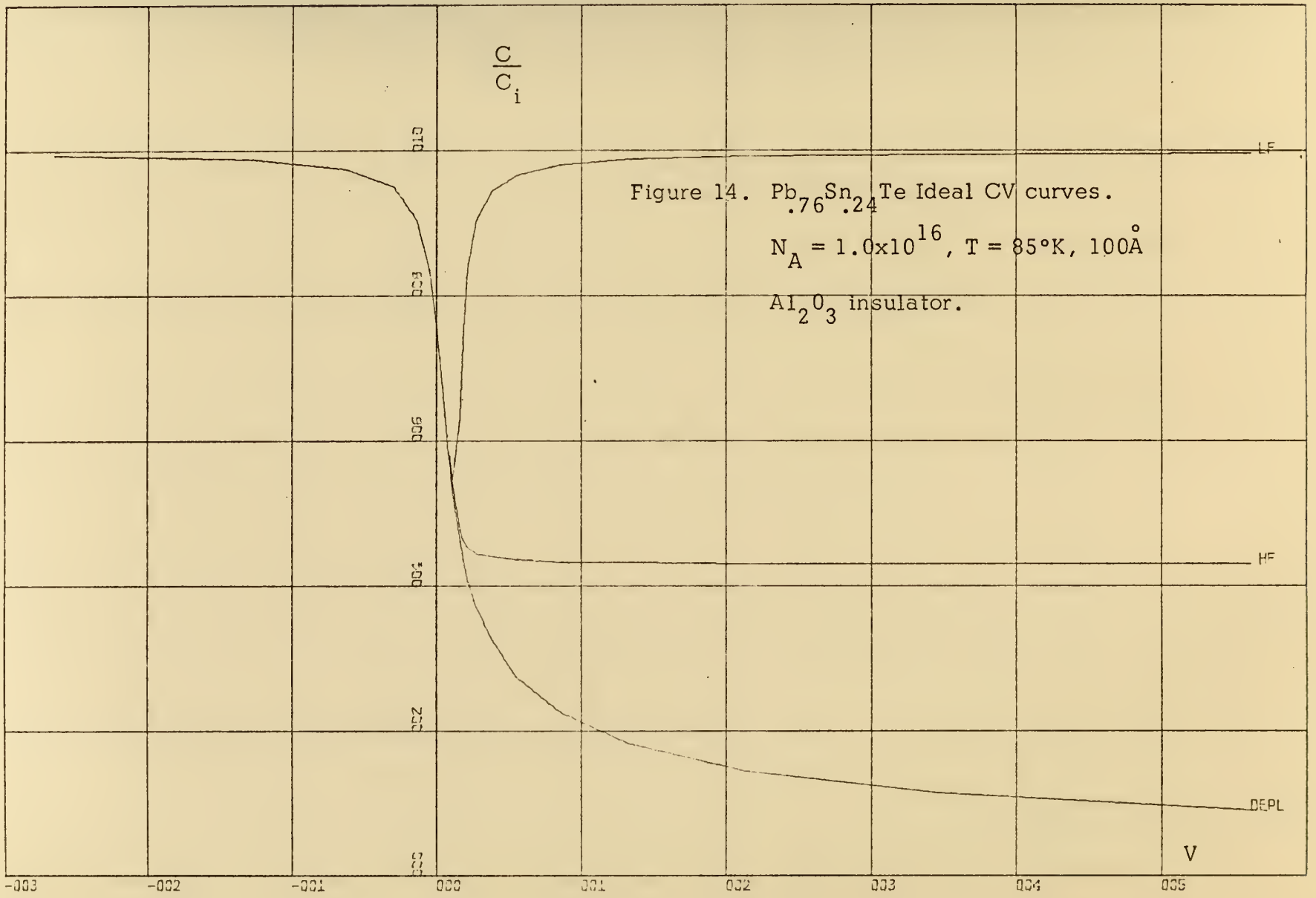


Figure 14. $Pb_{.76}Sn_{.24}Te$ Ideal CV curves.
$N_A = 1.0 \times 10^{16}$, T = 85°K, 100Å
Al_2O_3 insulator.

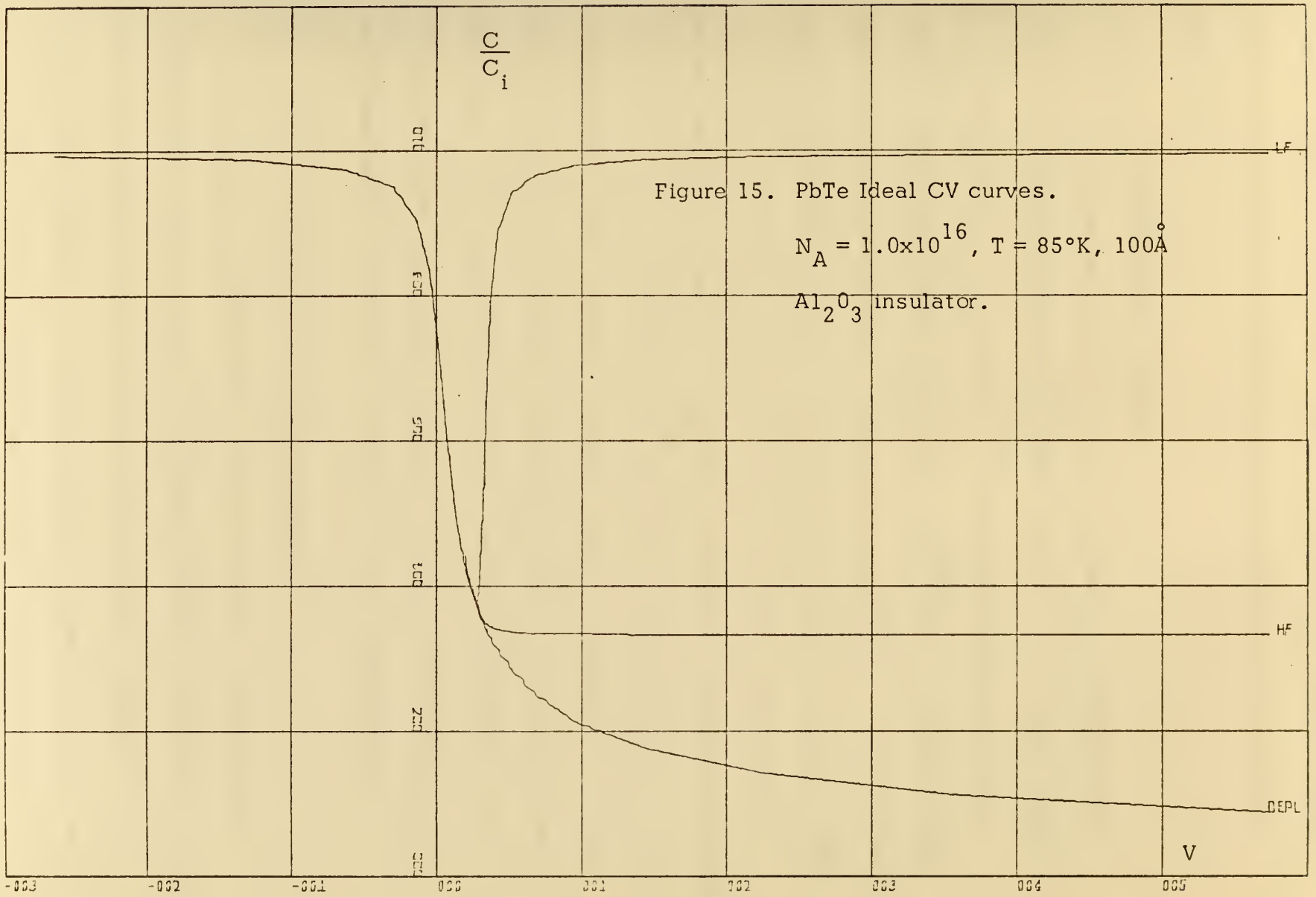


Figure 15. PbTe Ideal CV curves.

$N_A = 1.0 \times 10^{16}$, T = 85°K, 100Å

Al_2O_3 insulator.

storage available for the 150°K case is approximately 50 times greater than for the 85°K case. Higher temperature operation is desirable for CCD use.

4. The "Best Case" Values

The present state of the art in narrow gap semiconductor fabrication yields doping densities in the mid 10^{16} cm^{-3} range at best. In the near future an N_A of $1x10^{16}$ cm^{-3} will likely become realistic. For this reason a best case value of $N_A = 1x10^{16}$ cm^{-3} is chosen. Easy fabrication with relatively high yield requires insulators with a thickness on the order of 500Å or greater. For laboratory research, however, 100Å is feasible. To achieve comparable values of storage capacity with larger insulator thickness, other materials with higher dielectric constants (e.g., TiO_2, $K_{ins} \approx 100$) might be considered. Using Al_2O_3 ($K_{ins} = 8.8$) a thickness of 100Å is used as the best case. The temperature of operation is chosen as 85°K so that energy gaps of PbTe and $Pb_{.76}Sn_{.24}Te$ will have values that respond to the infrared energy in consideration. The "best case" ideal capacitance-voltage curves for a p-type $Pb_{.76}Sn_{.24}Te$ and p-type PbTe are presented in Figures 14 and 15 respectively.

B. CHARGE STORAGE AND SIGNAL CURRENT

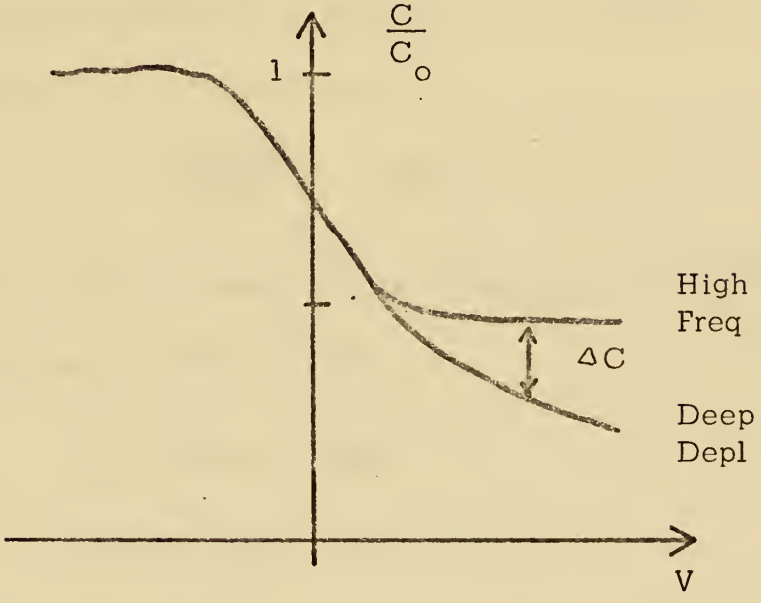
In a charge coupled device, the semiconductor is depleted by a voltage pulse, then the signal is injected as minority carriers and moved before the background minority carriers appear at the surface. Thus it is possible to estimate the maximum amount of signal charge that can be accommodated by noting the difference between the high frequency

capacitance and the depletion capacitance at a particular bias voltage, as shown in Fig. 16. Since charge is given by

$$Q \equiv C V \tag{21}$$

the charge that can be stored is

$$Q_{storage} = \Delta C V_{bias} \tag{22}$$



Estimation of $Q_{storage}$

Figure 16

in units of coulombs per square centimeter. The storage capacity in units of charges per square centimeter, is obtained by dividing by the electronic charge. The computer program calculates this $Q_{storage}$ for

several values of bias voltage. From the "best case" curve for p-type $Pb_{.76}Sn_{.24}Te$ $Q_{storage} = 5.32 \times 10^{12}$ charges/cm^2 for a bias of 3.46V. For p-type PbTe, the "best case" value of $Q_{storage}$ is 3.79×10^{12} charges/cm^2 at a bias of 3.57V. These bias voltages were chosen because they are the largest values before the breakdown field strength of 100Å thick insulator is reached.

In use as an infrared imager, a device must be able to differentiate a signal that is near the temperature of the earth background. First it is necessary to determine the amount of photons emitted by the earth background up to the semiconductor cut-off wavelength λ_c. The cut-off wavelength in microns is given by

$$\lambda_c = \frac{1.24}{E(eV)} \tag{23}$$

For PbTe at 85°K the energy gap is .219eV and for $Pb_{.76}Sn_{.24}Te$ at 85°K the energy gap is .102eV. Thus

$$\lambda_c \text{ (PbTe)} = 5.66\mu \tag{24}$$

$$\lambda_c \text{ } (Pb_{.76}Sn_{.24}Te) = 12.16\mu \tag{25}$$

The number of background photons is calculated from

$$N_{o-\lambda} = \left[\frac{N_{0-\lambda}}{N_{0-\infty}} \right] N_{o-\infty} \tag{26}$$

where $\frac{N_{0-\lambda}}{N_{0-\infty}}$ is obtained from a table [10] and $N_{0-\infty}$ is calculated from

$$N_{0-\infty} = 15.1 \frac{C}{(C_2)^3} T^3 \tag{27}$$

where C_2 = 1.43879 cm °K and C is the speed of light. Assuming that the earth's ambient temperature is 300°K, it is found that the number of background photons is

$$N_{0 - 5.66\mu} = 3.3\text{x}10^{16} \text{ PH/cm}^2\text{sec} \tag{28}$$

$$N_{0 - 12.16\mu} = 8.52\text{x}10^{17} \text{ PH/cm}^2\text{sec} \tag{29}$$

If each of these photons creates a hole-electron pair in the semiconductor it is seen that the earth background radiation will overwhelm the charge storage capabilities for both the case of PbTe and the case of $Pb_{.76}Sn_{.24}Te$. However, this assumes the semiconductor is exposed to the background radiation for a full second. If some sort of shutter were used to block the radiation except for a short period of time, fewer background photons would be able to reach the semiconductor. Consider the case if the scene was viewed for 10^{-6} seconds. Then

$$N_{0 - 5.66\mu} = 3.3\text{x}10^{10} \text{ PH/cm}^2 \tag{30}$$

$$N_{0 - 12.16\mu} = 8.5\text{x}10^{11} \text{ PH/cm}^2 \tag{31}$$

The difference in the storage capacities and these background charges gives the amount of useful signal charge that can be accommodated.

$$Q_{\text{signal}}\,(\text{PbTe}) = 3.76\text{x}10^{12} \text{ CH/cm}^2 \tag{32}$$

$$Q_{\text{signal}}\,(Pb_{.76}Sn_{.24}Te) = 4.468\text{x}10^{12} \text{ CH/cm}^2 \tag{33}$$

If these charges are moved out of the CCD at a clocking rate of 1MHz (which is often used in silicon CCD's), the signal current is

$$I_{sig}\ (PbTe) = .602\ A/cm^2 \tag{34}$$

$$I_{sig}\ (Pb_{.76}Sn_{.24}Te) = .716\ A/cm^2 \tag{35}$$

However, this assumes that all of the charge storage available is filled by signal photons. This will not be the case if the target is viewed for only 10^{-6} seconds.

Consider the case where the target is .5°K warmer than the earth background. Using equation (26) the following values are obtained

$$N_{0 - 5.66\mu} = 3.34x10^{16}\ PH/cm^2sec \tag{36}$$

$$N_{0 - 12.16\mu} = 8.6x10^{17}\ PH/cm^2sec \tag{37}$$

The difference between this number of photons and 300°K earth background photons is the number of signal photons ΔN

$$\Delta N\ (PbTe) = 4.3x10^{14}\ PH/cm^2sec \tag{38}$$

$$\Delta N\ (Pb_{.76}Sn_{.24}Te) = 8.0x10^{15}\ PH/cm^2sec \tag{39}$$

Again using a shutter to expose the semiconductor to the scene for 10^{-6} seconds, and assuming each photon creates one hole-electron pair then

$$Q_{sig}\ (PbTe) = 4.3x10^{8}\ CH/cm^2 \tag{40}$$

$$Q_{sig}\ (Pb_{.76}Sn_{.24}Te) = 8.0x10^{9}\ CH/cm^2 \tag{41}$$

If the signal packet is moved along the CCD with a clocking frequency of 1MHz, the signal current is

$$I_{sig}\ (PbTe) = 69\mu A/cm^2 \tag{42}$$

$$I_{sig}\ (Pb_{.76}Sn_{.24}Te) = 1.28mA/cm^2 \tag{43}$$

Tables I and II show the values of signal current for various temperature resolutions for PbTe and $Pb_{.76}Sn_{.24}Te$ respectively.

$\Delta T(°K)$	.1	.5	1.0	5.0
I_{sig} (A/cm^2)	4.8×10^{-6}	6.88×10^{-5}	1.62×10^{-4}	9.11×10^{-4}

TABLE I

$\Delta T(°K)$	.1	.5	1.0	5.0
I_{sig} (A/cm^2)	3.2×10^{-4}	1.28×10^{-3}	2.56×10^{-3}	1.28×10^{-2}

TABLE II

Though it was assumed that these temperature differentials are warmer than the background, cooler temperatures of the same magnitude will give the same values. The overall signal will be in the form of a dc current proportional to the background, with variations (either plus or minus) corresponding to target photons.

Note that the signal currents given in Tables I and II are in units of Amperes per square centimeter. Thus to obtain the actual signal current it is necessary to multiply by the gate area of the CCD. These

areas are usually on the order of 10^{-6} cm^2 for silicon devices. This would give signal currents in the 10^{-9} Ampere range.

It is worthwhile to summarize the assumptions used to arrive at these signal current values for later reference. First the earth background was assumed to be a uniform 300°K. Then it was assumed that a shutter mechanism would limit the exposure time to 10^{-6} seconds. Each photon was assumed to create one hole-electron pair. Finally, it was assumed that the clocking frequency of the CCD would be 1MHz.

C. STORAGE TIME

When signal charge is introduced into the depletion region of a CCD, a non-equilibrium condition exists. With increasing time, however, the system will move toward equilibrium by means of the thermal generation of minority carriers. This is called dark current. Thus it is possible to estimate the storage time T_S of the CCD by

$$T_S = \frac{Q_{storage}}{I_D} \tag{44}$$

where $Q_{storage}$ is the storage capacity of the device and I_D is the dark current.

There are four principle dark current components that must be considered. One is the current arising from minority carriers generated in the depletion region given by

$$I_D = \frac{1}{2} \frac{q\, n_i W}{\tau} \tag{45}$$

where W is the depletion layer width and τ is the minority carrier lifetime. A second component of dark current is due to generation of minority carriers in the semiconductor bulk. It is given by

$$I_b = \frac{q\, n_i^2}{N_I \tau} \quad L \tag{46}$$

where L is the diffusion length

$$L = \left[\frac{kT}{q}\, \mu \tau\right]^{1/2} \tag{47}$$

and μ is the mobility. A third component of the dark current arises from surface generation by those surface states within a few kT of midband [1]. However, this current is assumed small compared to the others since the success of making Schottky-barrier lasers using $Pb_{1-x}Sn_xTe$ indicate a small capture cross-section for these surface states. The fourth component of dark current is tunneling between the valence and conduction bands at very high bias voltage. This tunneling current is also quite small compared with the other mechanisms of dark current unless the depletion layer width is on the order of few hundred angstroms [12]. Thus the total dark current is

$$I_D \approx I_b + I_d \tag{48}$$

Numerical values of I_b and I_d for PbTe and $Pb_{.76}Sn_{.24}Te$ were obtained by use of the best case data from the computer program and information from other research [11]. The data used for these calculations is shown in Table III. From this data and equation (45), (46), and (47) it is found for PbTe that

$$I_b = 1.28\times10^{-6}\ A/cm^2 \tag{49}$$

$$I_d = 1.06\times10^{-2}\ A/cm^2 \tag{50}$$

and for $Pb_{.76}Sn_{.24}Te$ that

$$I_b = 1.16\times10^{-2}\ A/cm^2 \tag{51}$$

$$I_d = 6.6\times10^{-1}\ A/cm^2 \tag{52}$$

	PbTe	$Pb_{.76}Sn_{.24}Te$
τ (sec)	10-7	10-7
$n_i(cm^{-3})$	1.447×10^{12}	1.375×10^{14}
w(cm)	9.13×10^{-3}	5.99×10^{-3}
$Q_{storage}$ (CH/cm^2)	3.8×10^{12}	5.32×10^{12}
μ $(cm^2/V\ sec)$	2×10^{4}	2×10^{4}
$N_A(cm^{-3})$	1×10^{16}	1×10^{16}

TABLE III

Note that in both cases the dark current component of depletion layer generation is the dominant factor. Application of equation (48) yields

$$I_D\ (PbTe) = 1.02\times10^{-2}\ A/cm^2 \tag{53}$$

$$I_D\ (Pb_{.76}Sn_{.24}Te) = 6.72\times10^{-1}\ A/cm^2 \tag{54}$$

Then from equation (44)

$$T_S \text{ (PbTe)} = 5.7\text{x}10^{-5} \text{ sec} \tag{55}$$

$$T_S \text{ } (Pb_{.76}Sn_{.24}Te) = 1.27\text{x}10^{-6} \text{ sec} \tag{56}$$

When these values are compared with the period of the 1MHz clocking signal that was used in the preceding section, it is seen that difficulties arise for $Pb_{.76}Sn_{.24}Te$. For PbTe, the ratio of storage time to the period of the clocking signal is approximately 60, which is acceptable in that it allows a margin for variation introduced in fabrication. However, the ratio for $Pb_{.76}Sn_{.24}Te$ is approximately unity. This indicates borderline performance at best, with no margin for error. Thus for a CCD to be feasible, methods for improving this ratio must be considered.

Examination of the equation for depletion-layer generation reveals that the only parameters that could be improved with a significant effect on T_S are intrinsic carrier concentration and minority carrier lifetime. The intrinsic concentration is determined by the temperature, which is approximately 85°K for infrared imaging. The minority carrier lifetime could be increased by improving the quality of semiconductor, but a theoretical limit of radiative recombination lifetime of approximately 10^{-6} seconds exists [11]. This yields a one order of magnitude improvement in the storage time over the value obtained using presently available materials. This is still borderline performance. Consideration of equation (44) indicates a decrease in the capacitance due to the insulator will increase storage time. However, this would also result in a decrease in the amount of charge storage. An increase in the clocking frequency,

though it will not effect the storage time, can be used to improve the ratio of storage time to clocking signal period. A 5MHz clocking frequency combined with a minority carrier lifetime of 10^{-6} seconds yields a storage time to clocking period ratio on the order of 75 for $Pb_{.76}Sn_{.24}Te$. This indicates that the feasibility of narrow gap semiconductor CCD requires advances in the fabrication of narrow gap semiconductors.

IV. EXPERIMENTAL METHODS

The analysis presented in the preceding section was based upon idealized theory developed by the silicon device industry. To verify that it is applicable to the narrow-gap semiconductor in this study, experimental data must be obtained. The test configurations for obtaining capacitance-voltage curves at high frequency and capacitance-time curves are presented in this section.

A. HIGH FREQUENCY CAPACITANCE-VOLTAGE CURVES

The Boonton Model 72A Capacitance Meter was the basic element for the high frequency CV measurement. It provides a direct capacitance reading by generating a 1MHz signal and measuring its phase variations due to the capacitance of the device under test. The Boonton Model 72A also has provisions for external dc bias and an output to drive an X-Y recorder.

The M-I-S device was mounted in an insulated container to allow immersion in liquid nitrogen for obtaining low temperature data. A mechanical probe was situated on the outside of the insulated container to make electrical contact at various points on the M-I-S structure.

A Wavetek Model 142 Function Generator was used in the sawtooth mode to provide the varying dc bias. A Hewlett-Packard Model 7004B X-Y Recorder completed the instrumentation. It gave the capacitance-

voltage curve for the M-I-S under study in a form suitable for comparison to the computer-generated ideal curve. The schematic for the test set up is pictured in Fig. 17.

B. CAPACITANCE-TIME CURVES

The capacitance-time data required to verify the ideal storage time calculations was obtained from an experimental setup similar to that used for the capacitance-voltage measurements. Again the Booton 72A Capacitance Meter was employed. Since the M-I-S must be switched rapidly from accumulation to deep depletion, the Wavetek Function Generator was used in the square wave mode for the C-t measurement. The expected storage time was on the order of microseconds, so a Tektronics Type 422 Oscilloscope was used to observe the response instead of an X-Y recorder. The experimental schematic is pictured in Fig. 18.

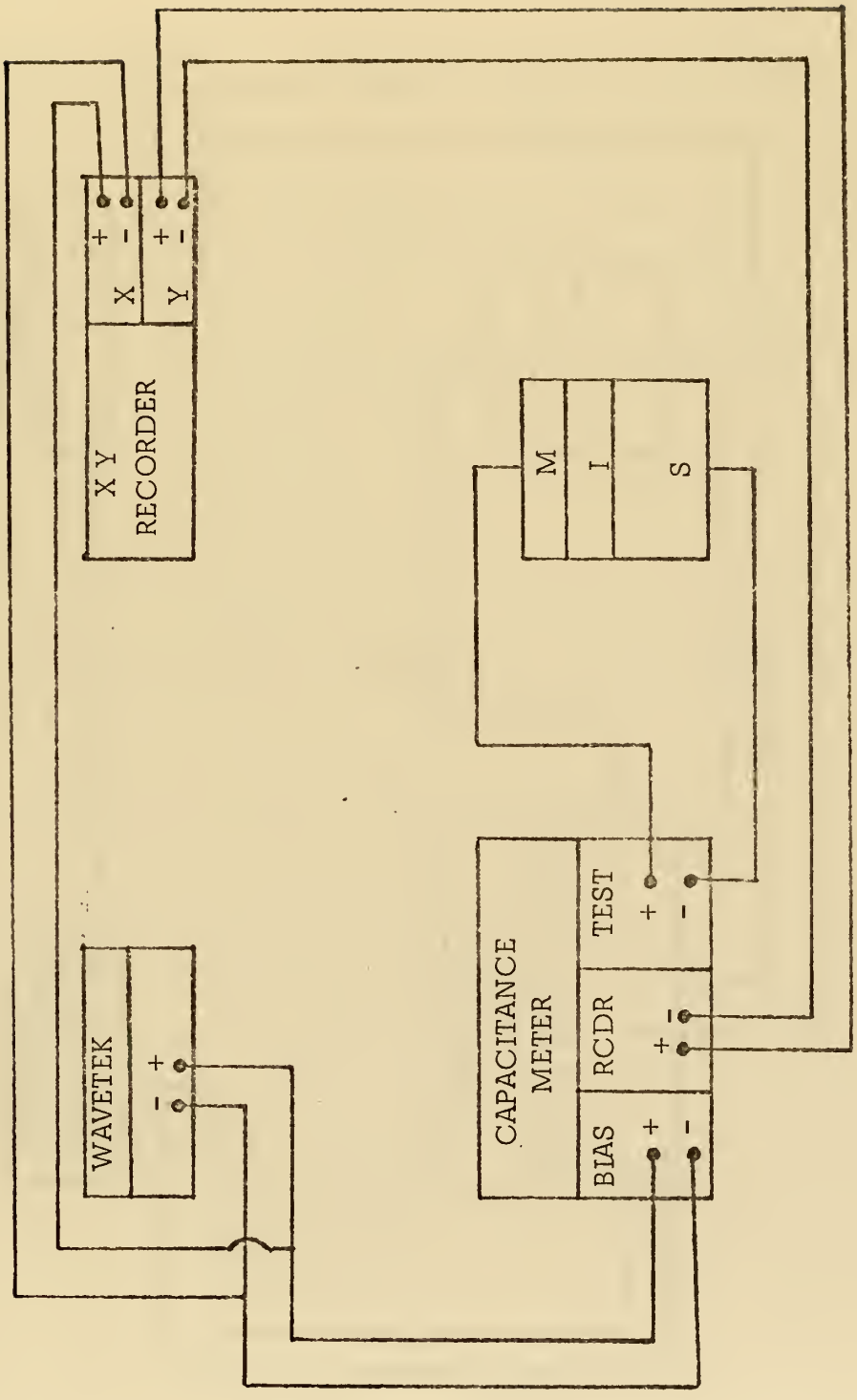


Figure 17. C-V Test Circuit

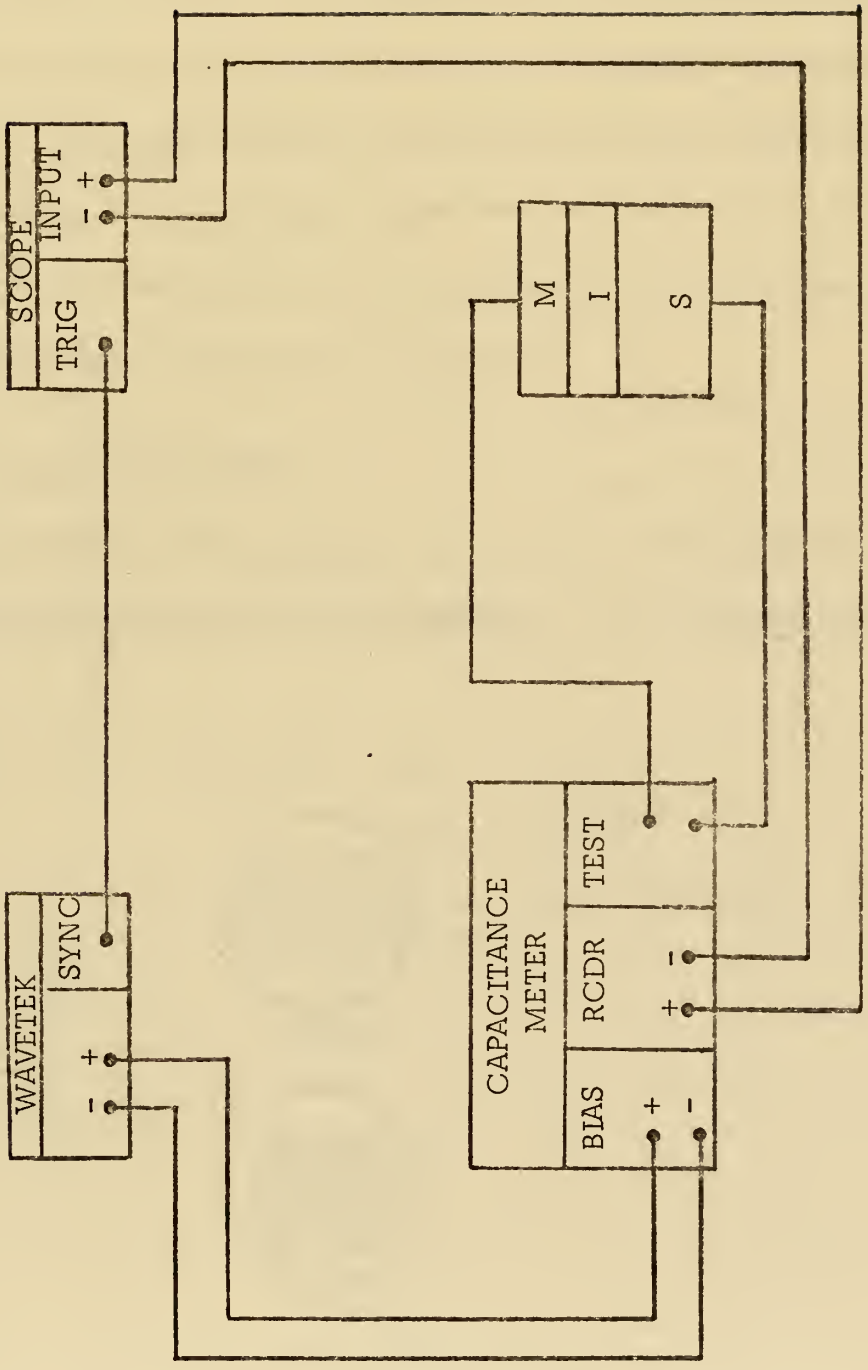


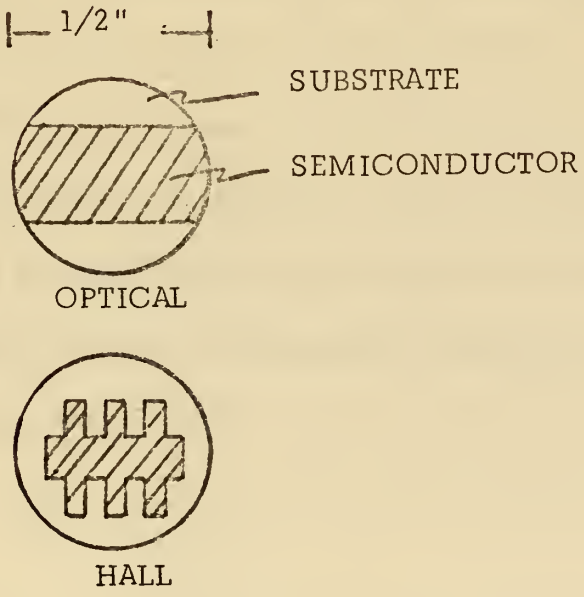
Figure 18. C-t Test Circuit

V. METAL-INSULATOR-SEMICONDUCTOR FABRICATION

A brief summary of the fabrication processes and materials of the M-I-S devices used in the experimental investigation is presented in this section. The semiconductors were deposited in the Naval Postgraduate School Solid State Laboratory under the direction of Dr. T. F. Tao. The insulators and metal gates were deposited by Dr. N. Bottka at the Naval Weapons Center, China Lake, California.

A. SEMICONDUCTORS

Thin films of $Pb_{1-x}Sn_xTe$ semiconductor were evaporated onto half-inch diameter substrates of CaF_2 and BaF_2. The compositions (x values)



Semiconductor Samples

Figure 19

of zero, .2, and .24 were used. Two types of masks were used, Hall and optical, so that the samples could be utilized for other research projects. The thickness of the semiconductor material ranged from two microns to 10 microns. Evaluations using the Hall technique showed carrier concentrations ranging from low 10^{17} cm^{-13} to low 10^{19} cm^{-3}. X-ray Laue photographs indicated that both single crystal and poly-crystalline samples were obtained.

B. INSULATOR

The semiconductor samples were cleaned with trichloroethylene, then methanol, and finally with de-ionized water. They were then masked and mounted in a vacuum station. The system was pumped down to approximately $3x10^{-17}$ Torr. The deposition was then performed using the electron-beam method. The thickness of the insulator deposition was monitored with a Sloan Model DTM-4 Thickness Monitor.

The Model DTM-4 gives a frequency reading that is proportional to the thickness of the deposit by beating a stable oscillator frequency with the frequency of a crystal that is proportional to its mass. As the deposit builds up on the crystal, its frequency changes proportionally. The thickness is then obtained from

$$\Delta f = \frac{DT}{2} \tag{57}$$

where D is the density of the material deposited in gm/cm^3 and T is the thickness in Angstroms. Two Al_2O_3 ($D = 4$ gm/cm^3) and one SiO_2

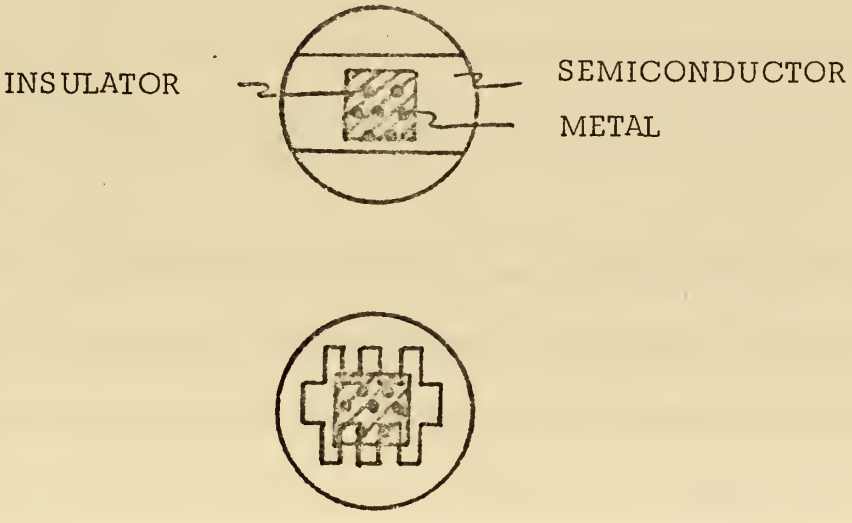
($D = 2.5\ gm/cm^3$) deposits were made. The insulator thickness obtained are given in Table IV.

INSULATOR	THICKNESS (Å)
Al_2O_3	~100
Al_2O_3	~300
SiO_2	~450

TABLE IV

C. METAL

The insulator-semiconductor samples were masked to expose various sized circular areas, then Ni was deposited on them by the resistive-heating method. The two types of completed M-I-S devices are pictured in Fig. 20.



M-I-S Samples

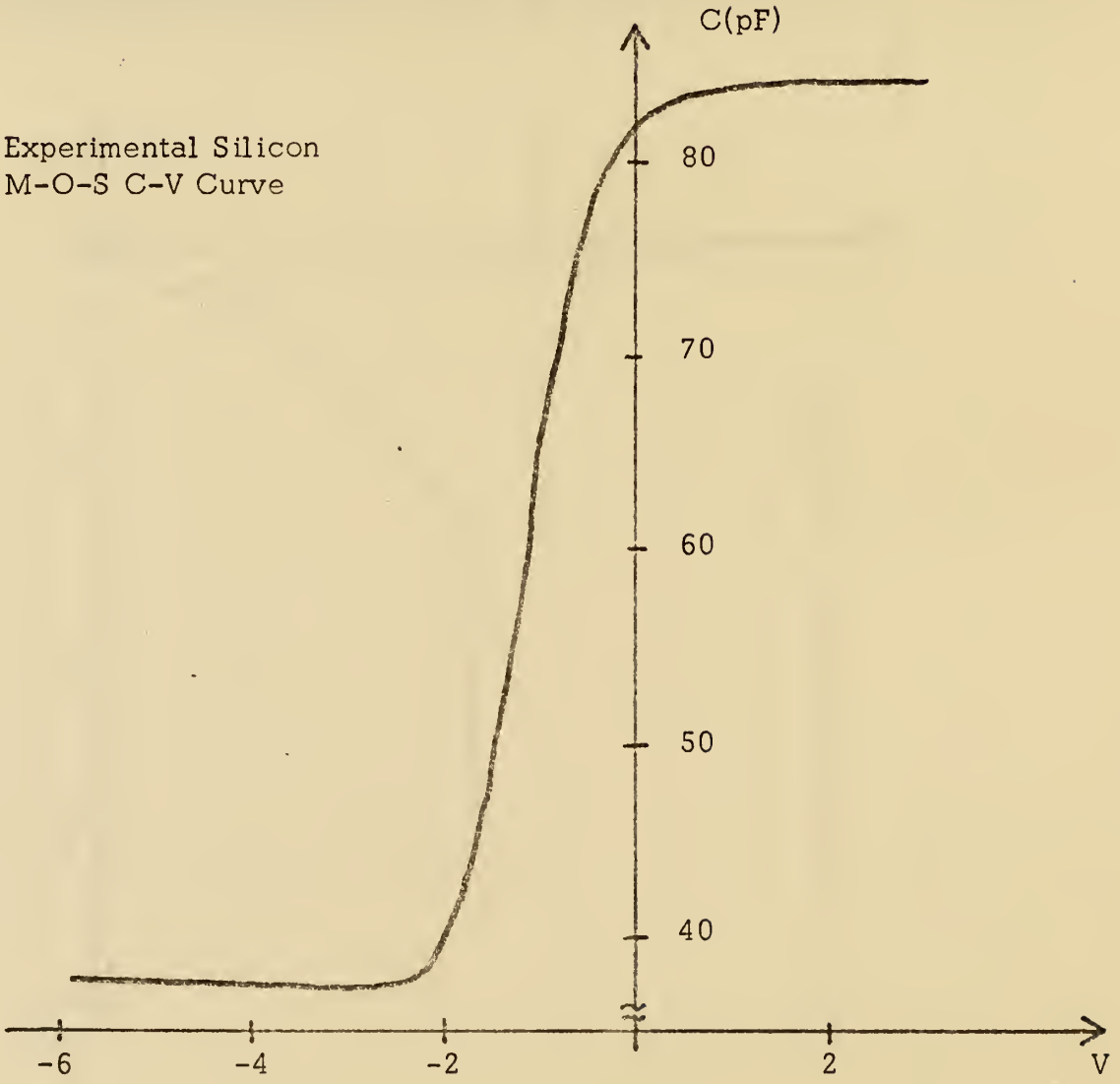
Figure 20

VI. EXPERIMENTAL RESULTS

The first step in the experimental investigation of the M-I-S devices was to verify that the test circuits of Section IV were functioning properly. For this purpose, an Al-SiO_2-Si M-I-S device with a known high frequency capacitance-voltage curve was obtained from Stanford University, Stanford, California. The capacitance-voltage results are shown in Fig. 21. The close agreement of this curve and the one obtained at Stanford indicated that the CV test procedures would yield reliable results. A capacitance-time measurement was also made on the Al-SiO_2-Si sample. These results are shown in Fig. 22. Though there was no standard with which to compare this curve, it followed that the general shape of curves presented in other papers [8]. Therefore, the C-t test circuit was assumed to be functional. With the test circuits functioning properly, the next task was to obtain high frequency capacitance-voltage curves from the $Pb_{1-x}Sn_xTe$ M-I-S devices, and examine if the theory developed for silicon M-I-S devices apply equally well for these narrow gap semiconductors.

Measurements made with the probe touching various Ni gates on several of the samples yielded either no capacitance variation or an unusual reaction from the Boonton Capacitance Meter. For example, the Boonton would give a full-scale deflection on the 300pF scale, but would read zero on the 1000pF scale-setting. Using standard capacitors, the

Figure 21. Experimental Silicon M-O-S C-V Curve



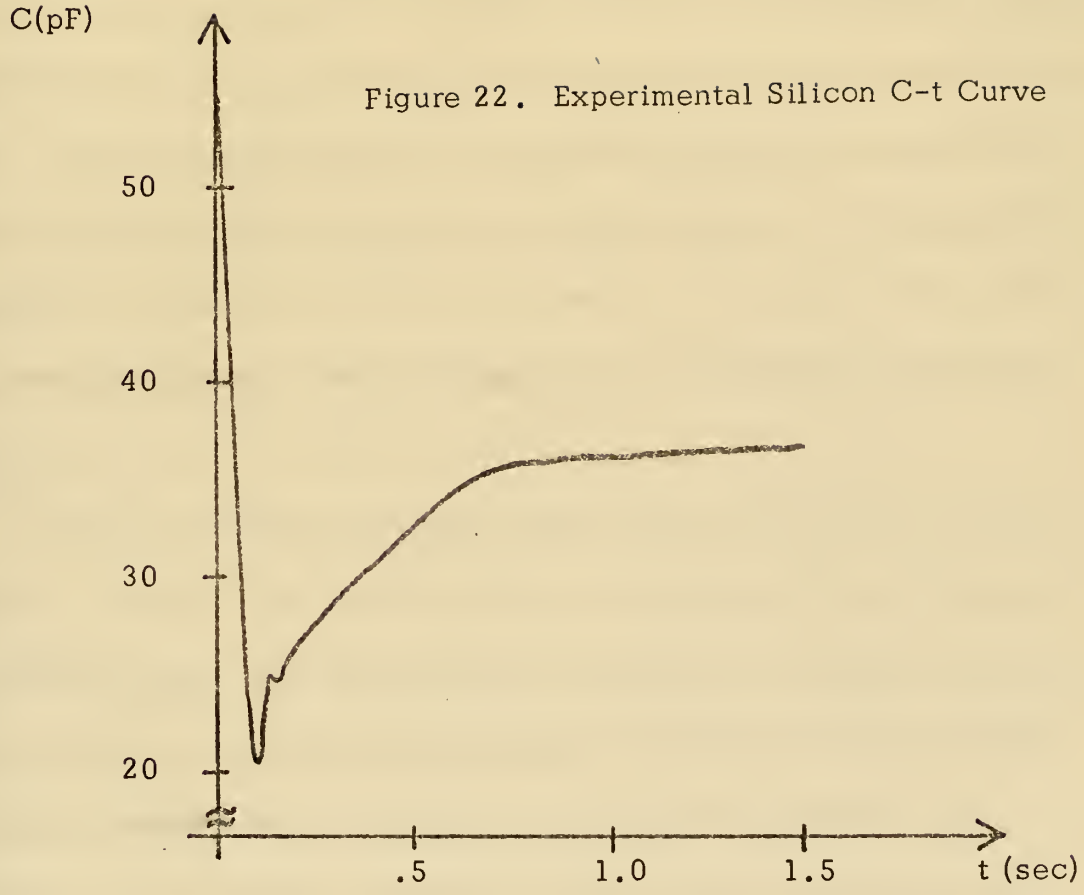


Figure 22. Experimental Silicon C-t Curve

Boonton was checked and found to be operating properly. This indicated that the devices were the source of the erroneous readings. The conclusion was that due to its very thin the insulator contained many pin holes, thus the metal gate was making direct contact to the semiconductor. To decrease the probability of finding a pin hole under the gate, it was decided to reduce the gate area. This was accomplished by using the tip of the probe as the gate, touching it directly to the insulator. Results obtained in this fashion, however, were little better than those described above. The cause was thought to be that the pressure of the probe was great enough to break through the thin insulator layer. To alleviate this possibility, a small amount of Hg was placed on the metal probe which was lowered to the point where the mercury just made contact with the insulator.

Using this method the results shown in Fig. 23 thru Fig. 27 were obtained. However, the results were not consistent. The resistance of the insulating layer was measured and it varied from 50 ohms to approximately 2 K ohms. To determine the effect of leakage on the C-V result, the silicon sample, with a variable shunt resistor connected, was measured. For a leakage resistance of 100 K ohms, the silicon M-I-S CV curve showed some noticeable distortion. For a leakage of 5 K ohms, there was no capacitance variation at all. By comparing the value of leakage at which distortion of the CV curve was first observed to the ac impedence given by

$$|Z| = \frac{1}{\omega C} \tag{58}$$

where C is the maximum capacitance of the M-I-S and W is 2 π times the measurement frequency, it was determined that for reliable C-V results the insulator resistance must be at least 250 times greater than the ac impedence of the M-I-S.

This indicated that the results obtained were distorted by the leakage of the M-I-S device. This precluded the use of these curves for accurate numerical analysis to determine the surface state density, carrier concentration, or insulator charge. However, the general shape of the curves can be used to substantiate that the $Pb_{1-x}Sn_xTe$ M-I-S devices follow qualitatively the capacitance-voltage variations of silicon M-I-S devices.

Attempts to make CV measurements with the M-I-S device immersed in liquid nitrogen gave inconclusive results. The expected result was a sharper curve, that is the transition from accumulation to inversion would take place over a smaller voltage range. Also expected was that the percentage change from accumulation capacitance to inversion capacitance would be greater than at room temperature. In the few measurement attempts which yielded C-V data (one is shown in Fig. 27) the capacitance variation did occur over a smaller voltage range, however, the percentage of change in capacitance was smaller than in the room temperature case. It was also noted that the actual capacitance values were much lower at reduced temperatures. This could be caused by the fact that the Hg probe solidified at liquid nitrogen temperature ($\sim$ 77°K), resulting in a smaller gate area. Another problem encountered in low temperature measurements

was the presence of jitter in the CV curve. The source of the jitter was thought to be the boiling of the liquid nitrogen which shook the probe during measurement. Another inconsistency was the variation of the accumulation capacitance with temperature. In some samples the accumulation capacitance decreased with decreasing temperature while in other cases the reverse was true. Theoretically accumulation capacitance should remain constant (approximately equal to insulator capacitance) for all temperatures.

In an effort to determine the effect of illumination of the capacitance-voltage curves, measurements were made under various lighting conditions. The expected result was a higher value of capacitance in the inversion region for higher light intensities, due to the added number of minority carriers produced by the light photons. However, no noticeable effect was observed in the C-V curves. Some low frequency C-V measurements were attempted using a Princeton Applied Research Model 124 Lock-in Amplifier (LIA), though few useful results were obtained due to the LIA's sensitivity to leakage resistance. Also due to this leakage problem, capacitance-time measurements did not yield any conclusive results on charge storage time.

In general, the percentage of capacitance variation was much greater in experimental data than in theoretical calculations. In many cases, hysterisis and/or drift were observed. This was expected since insulators usually contain mobile charges. The voltage range over which the capacitance variation took place was considerably larger than in

theoretical calculations. In many cases, especially at low temperature, there were some unexpected capacitance variations: the change from accumulation capacitance to inversion capacitance was not smooth (see Fig. 26 and Fig. 27).

To summarize, mainly due to the leakage in the insulator layer the C-V results were distorted. Thus they were not suitable for quantitative analysis. However, the general shape of the curves can be used to infer the general behavior of narrow-gap semiconductor M-I-S devices and the feasibility of their applications as infrared CCD's.

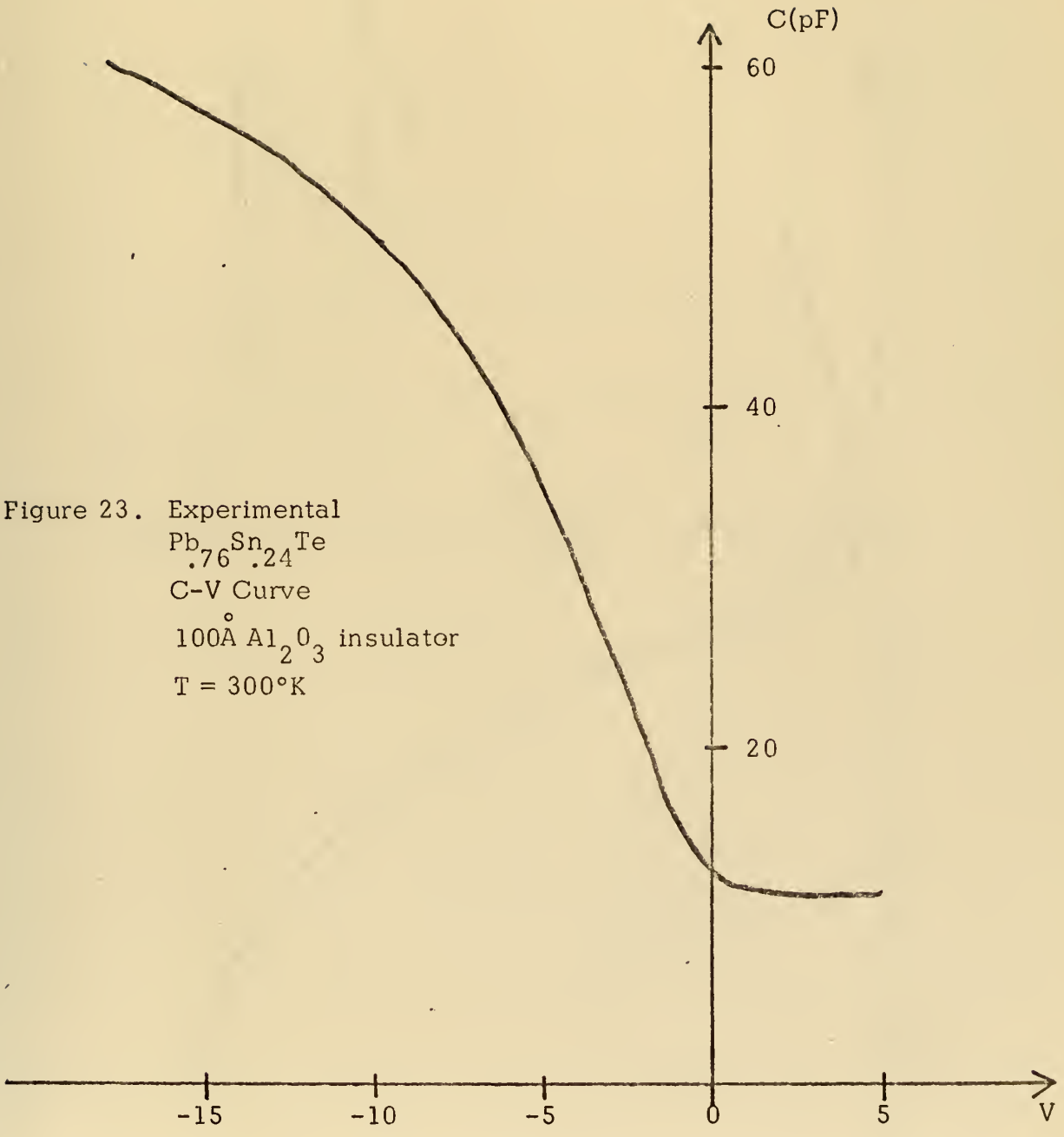


Figure 23. Experimental
$Pb_{.76}Sn_{.24}Te$
C-V Curve
100Å Al_2O_3 insulator
T = 300°K

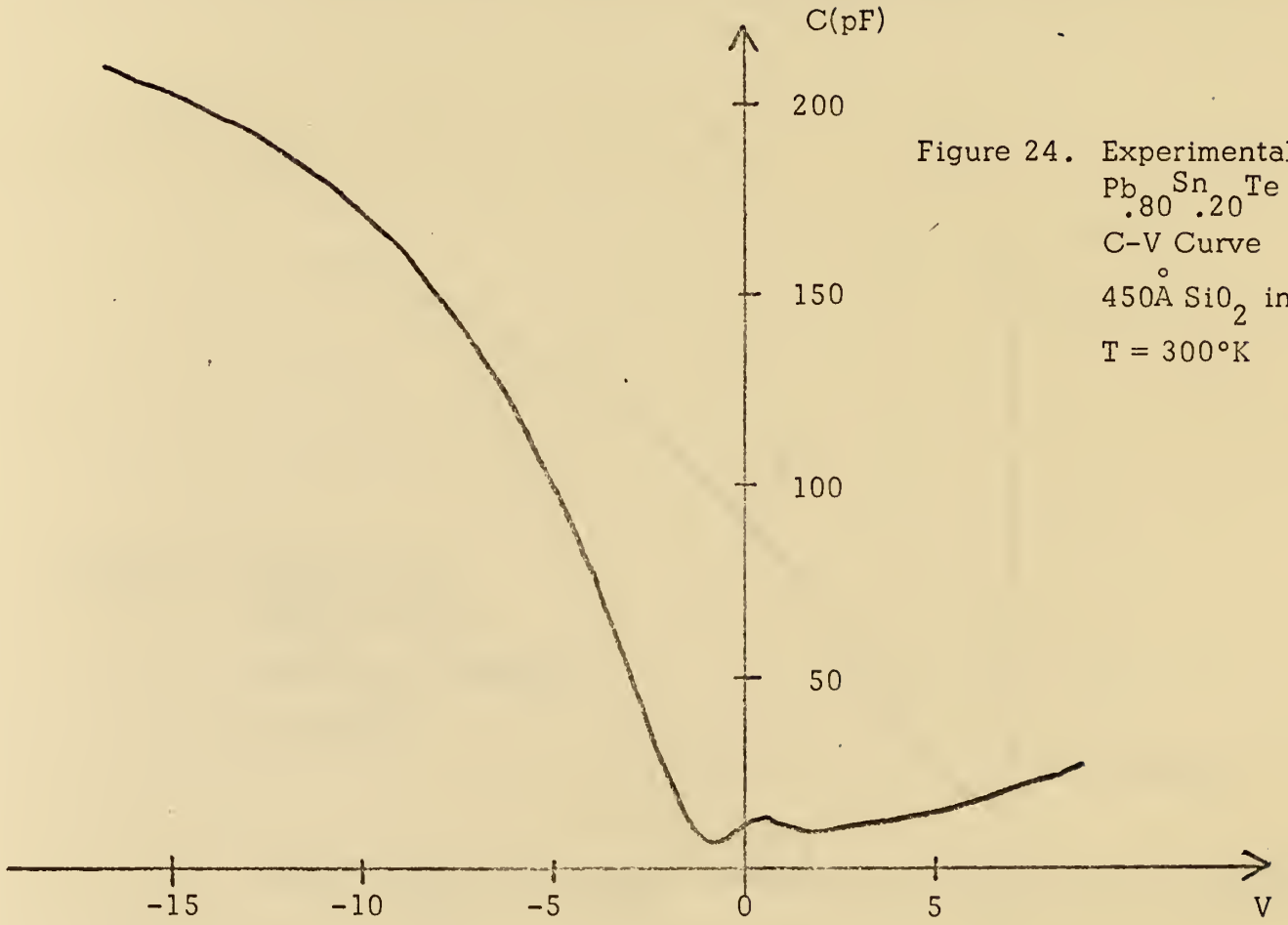


Figure 24. Experimental $Pb_{.80}Sn_{.20}Te$ C-V Curve 450Å SiO_2 insulator T = 300°K

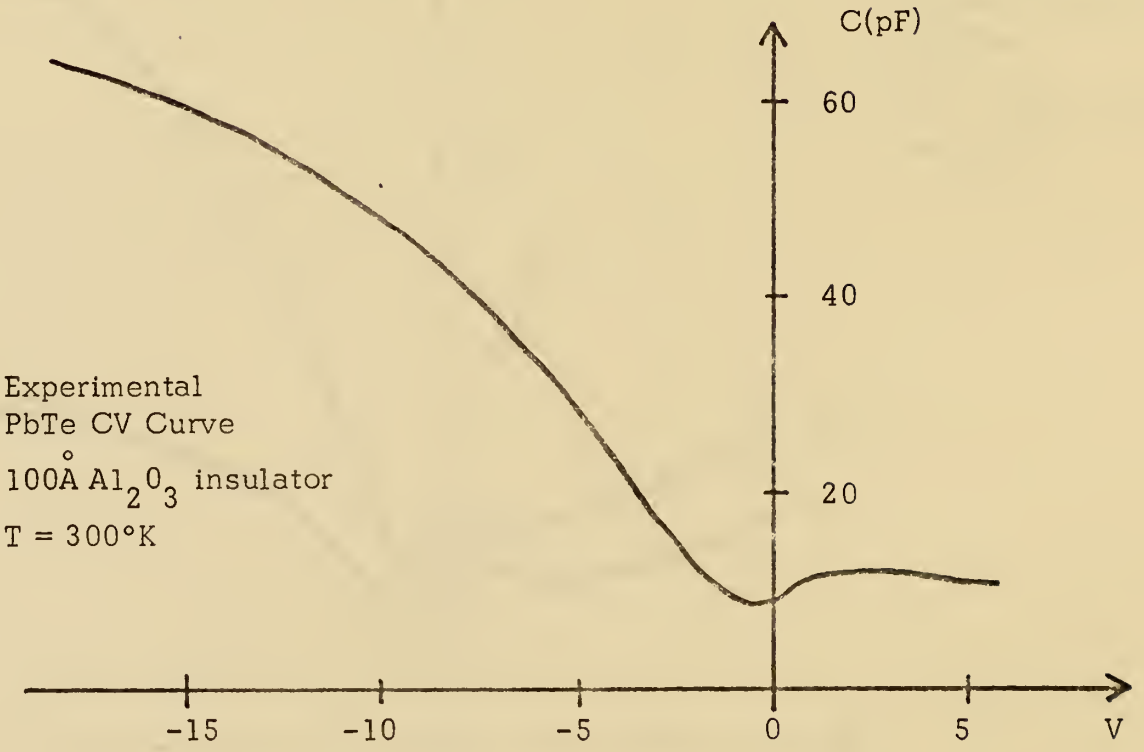


Figure 25. Experimental
PbTe CV Curve
100Å Al_2O_3 insulator
T = 300°K

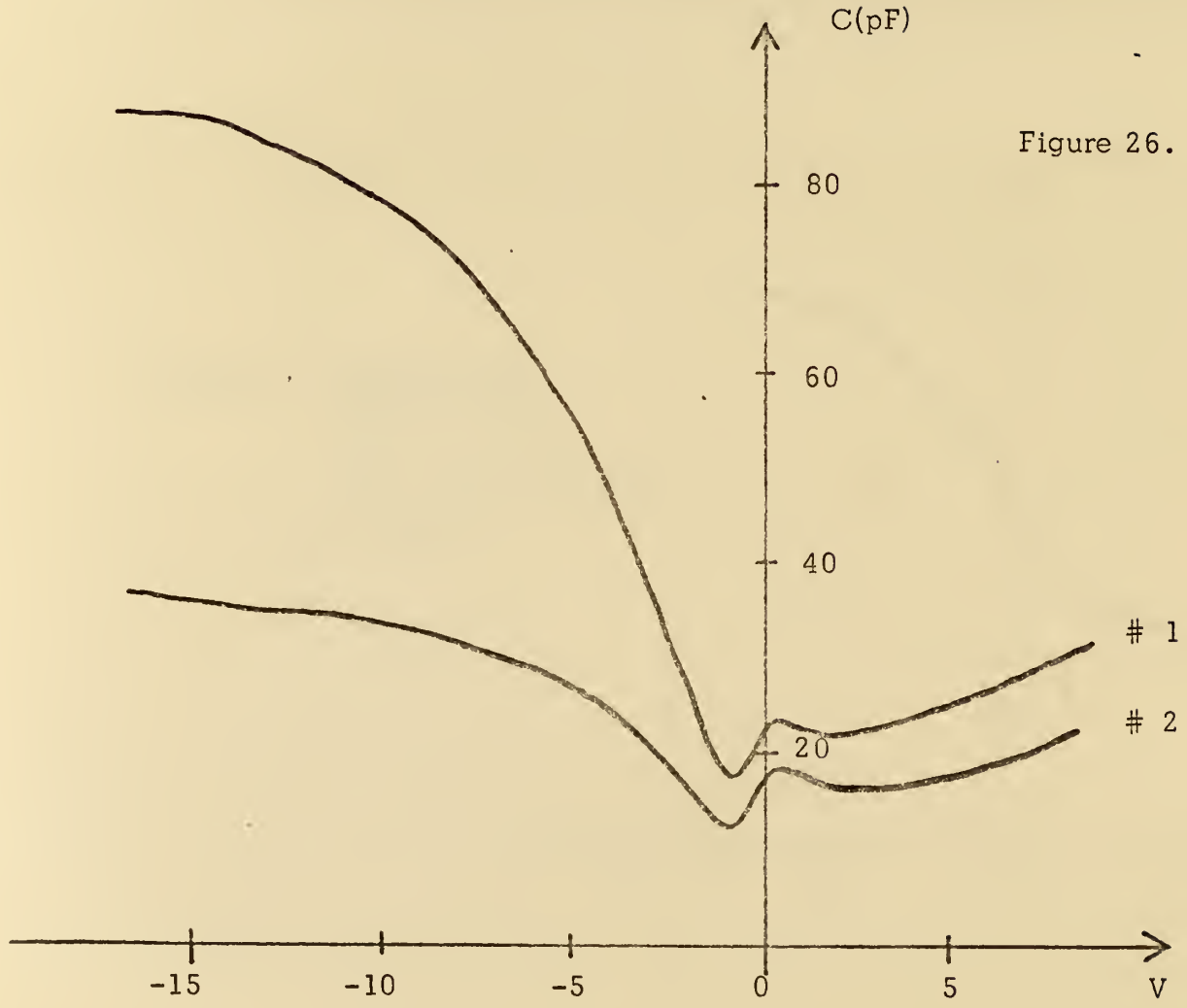


Figure 26. Experimental $Pb_{.80}Sn_{.20}Te$ CV Curves at two probe locations.
300Å Al_2O_3 insulator
T = 300°K

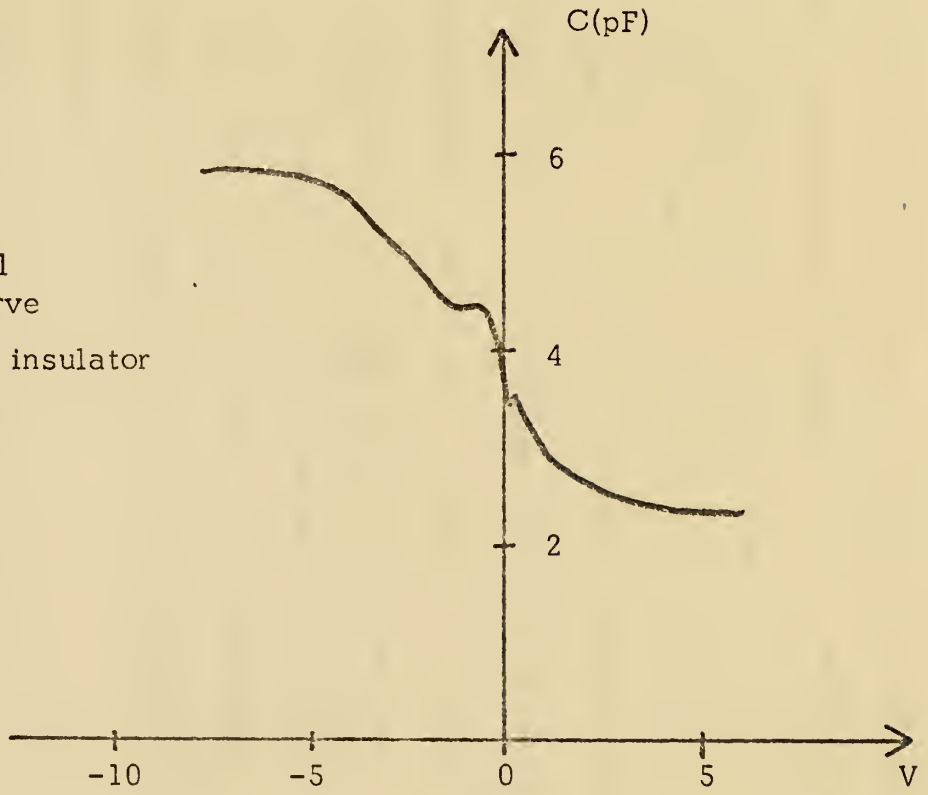


Figure 27. Experimental
PbTe CV Curve
100Å Al_2O_3 insulator
T = 80°K

VII. CONCLUSIONS

The theoretical analysis of $Pb_{1-x}Sn_xTe$ M-I-S devices indicated that signal currents comparable to those obtained in silicon CCD's are realizable. With a temperature differential of 0.1°K, which is desirable for high resolution infrared imaging, signal currents of 4.8×10^{-6} A/cm^2 for PbTe and 3.2×10^{-4} A/cm^2 for $Pb_{.76}Sn_{.24}Te$ were calculated. These values were obtained by assuming that the device viewed the scene for only 10^{-6} seconds. This poses a limitation since present mechanical choppers and shutters that operate with this speed are not available. Other methods of reducing background photons, such as spectral filters, would reduce the requirements placed on the mechanical shutter speed. Further study on the effect of spectral filters in limiting background photons is suggested as an alternative to the high frequency choppers presently considered.

Another limitation to the signal current which has not been considered in detail in this thesis is the effect of noise current, which should be studied. This would allow a prediction of the signal to noise ratio for comparison to that obtained in other infrared imagers.

Charge storage times obtained from the theoretical analysis are significantly shorter than those in silicon charge coupled devices. For PbTe $T_S = 5.7 \times 10^{-5}$ seconds was obtained, and for $Pb_{.76}Sn_{.24}Te$ $T_S = 1.27 \times 10^{-6}$ seconds. The storage time for PbTe compared to the

period of a 1MHz clocking signal indicates that the length of storage time is satisfactory for CCD applications. However, this is not true for $Pb_{.76}Sn_{.24}Te$. Methods of increasing the storage time are required before a CCD will be feasible using this material at the 1MHz clocking frequency. Increased clocking frequencies could be a possible improvement without increasing storage time, but a limit exists on the clocking frequency. This limit is imposed by the requirement of interface with available display systems. Methods of limiting dark current by varying material parameters such as doping concentration also require further study.

All of the theoretical analysis of $Pb_{1-x}Sn_xTe$ devices was based on the assumption that the theory developed for silicon M-I-S was applicable. Preliminary experimental investigation has been carried out to examine this assumption. After initial instrumentation problems were overcome, the C-V data obtained showed qualitatively the typical behaviors of accumulation, depletion, and inversion in an M-I-S. Capacitance-voltage curves showed a definite transition from accumulation capacitance to inversion capacitance, but there were two basic deviations from theoretical calculations. First the percentage change in capacitance from the accumulation region to the inversion region was greater than that in theoretical calculations. One possible explanation of this is that the value of the relative dielectric constant for $Pb_{1-x}Sn_xTe$ used in theoretical calculation ($K_S = 400$) is too high. Accurate data for the dielectric constant is not available at present, thus more extensive

experimentation using CV method of $Pb_{1-x}Sn_xTe$ M-I-S could provide an alternate means of measuring the dielectric constant. Another deviation from the theoretical curves noted in the experimental investigation was that the transition from accumulation to inversion was not smooth. This was possibly due to interface states in the M-I-S structure.

In general, all of the experimental data suffered from the leakage through the insulator. Experiments on silicon and germainium devices with a simulated leakage indicated that the C-V variations were distorted. Experimentation using better insulators is necessary for quantitative analysis of $Pb_{1-x}Sn_xTe$ M-I-S. It is suggested that other insulators, especially those with higher dielectric constants, such as TiO_2, be considered to meet the production requirement for thicker insulating layers. With better fabricated devices, storage times can be accurately determined also.

The conclusions of this thesis can be summarized as follows. First, $Pb_{1-x}Sn_xTe$ M-I-S devices do show controllable depletion and inversion behaviors qualitatively similar to the Si M-O-S theory. From the storage time and storage capacity points of view, charge coupled device infrared imagers using PbTe are feasible without extensive improvements of material and fabrication technology. Devices using $Pb_{.76}Sn_{.24}Te$ will require more extensive material advances to increase the storage time. Finally it is suggested that more experimental investigation be carried out for quantitative study of the $Pb_{1-x}Sn_xTe$ M-I-S.

NA-ND = 0.100E 17
OXIDE THICKNESS(MICRONS) = 0.0100
FLATBAND CAPACITANCE = .78129
COI(F PER SQ CM) =0.7792E-06
CINT =0.1375E 15
TEMP = 85.000
EG(EV) = 0.102

GATE VOLTAGE	LOW FREQ. CAP.	HIGH FREQ. CAP.	DEPL. LAYER WIDTH(METERS)	SURFACE POTENTIAL		DEPL. CAP.	Q STORAGE
-2.65	0.99439			-0.062			
-1.27	0.98822			-0.051			
-0.61	0.97554			-0.040			
-0.29	0.95055			-0.029			
-0.13	0.90554			-0.018			
-0.04	0.83664			-0.007			
0.02	0.75282			0.004			
0.05	0.67234			0.015			
0.08	0.60754			0.026			
0.10	0.58115	0.58179	0.3267E-06	0.031		0.56683	.71815E 10
0.12	0.54832	0.53606	0.3934E-06	0.042		0.52344	.76051E 10
0.17	0.63306	0.47997	0.4925E-06	0.063	T	0.46321	.13948E 11
0.19	0.73651	0.46580	0.5213E-06	0.070		0.44025	.24160E 11
0.23	0.83728	0.45444	0.5457E-06	0.077		0.41112	.48414E 11
0.29	0.90583	0.44594	0.5648E-06	0.085		0.37278	.10305E 12
0.39	0.94525	0.44008	0.5783E-06	0.092		0.32601	.21306E 12
0.57	0.96748	0.43629	0.5873E-06	0.099		0.27556	.44471E 12
0.86	0.98040	0.43394	0.5929E-06	0.107		0.22676	.86889E 12
1.35	0.98812	0.43250	0.5964E-06	0.114		0.18311	.16344E 13
2.15	0.99279	0.43162	0.5986E-06	0.121		0.14598	.29825E 13
3.46	0.99562	0.43109	0.5999E-06	0.129		0.11541	.53167E 13
5.63	0.99734	0.43077	0.6006E-06	0.136		0.09075	.93100E 13

NA-ND = 0.100E 18
OXIDE THICKNESS(MICRONS) = 0.0100
FLATBAND CAPACITANCE = .91868
COIF PER SQ CM) =0.7792E-06
CINT =0.1375E 15
TEMP = 85.000
EG(EV) = 0.102

GATE VOLTAGE	LOW FREQ. CAP.	HIGH FREQ. CAP.	DEPL. LAYER WIDTH(METERS)	SURFACE POTENTIAL		DEPL. CAP.	Q STORAGE
-8.26	0.99822			-0.062			
-3.91	0.99624			-0.051			
-1.85	0.99213			-0.040			
-0.85	0.98382			-0.029			
-0.36	0.96807			-0.018			
-0.11	0.94184			-0.007			
0.04	0.90592			0.004			
0.14	0.86635			0.015			
0.21	0.82965			0.026			
0.27	0.79858			0.037			
0.32	0.77295			0.048			
0.32	0.77158	0.77162	0.1345E-06	0.048		0.76806	.56284E 10
0.37	0.75101	0.75091	0.1515E-06	0.059		0.74671	.59682E 10
0.41	0.73658	0.73162	0.1667E-06	0.070		0.72836	.65625E 10
0.46	0.73746	0.71557	0.1807E-06	0.081		0.71181	.83184E 10
0.52	0.81484	0.69536	0.1982E-06	0.097	T	0.68759	.22222E 11
0.57	0.88165	0.68844	0.2057E-06	0.104		0.67114	.48004E 11
0.65	0.93519	0.68157	0.2124E-06	0.111		0.64546	.11495E 12
0.81	0.96594	0.67601	0.2178E-06	0.118		0.60413	.28432E 12
1.11	0.98141	0.67194	0.2219E-06	0.126		0.54434	.68397E 12
1.64	0.98933	0.66920	0.2247E-06	0.133		0.47110	.15759E 13
2.54	0.99368	0.66746	0.2265E-06	0.140		0.39405	.33815E 13
4.06	0.99621	0.66638	0.2276E-06	0.148		0.32146	.68047E 13
6.56	0.99771	0.66573	0.2282E-06	0.155		0.25782	.13024E 14
10.71	0.99861	0.66533	0.2286E-06	0.162		0.20451	.24001E 14
17.54	0.99916	0.66509	0.2289E-06	0.170		0.16110	.43004E 14

NA-ND = 0.100E 17
OXIDE THICKNESS(MICRONS) = 0.0100
FLATBAND CAPACITANCE = .78129
COX(F PER SQ CM) =0.7792E-06
CINT =0.1375E 15
TEMP = 85.000
FG(EV) = -0.102

GATE VOLTAGE	LOW FREQ. CAP.	HIGH FREQ. CAP.	DEPL. LAYER WIDTH(METERS)	SURFACE POTENTIAL	DEPL. CAP.	Q STORAGE
-2.65	0.99439			-0.062		
-1.27	0.98822			-0.051		
-0.61	0.97554			-0.040		
-0.29	0.95055			-0.029		
-0.13	0.90554			-0.018		
-0.04	0.83664			-0.007		
0.02	0.75282			0.004		
0.05	0.67234			0.015		
0.08	0.60754			0.026		
0.10	0.58115	0.58179	0.3267E-06	0.031	0.56683	.71815E 10
0.12	0.54832	0.53606	0.3934E-06	0.042	0.52344	.76051E 10
0.17	0.63306	0.47997	0.4925E-06	0.063	0.46321	.13948E 11
0.19	0.73651	0.46580	0.5213E-06	0.070	0.44025	.24160E 11
0.23	0.83728	0.45444	0.5457E-06	0.077	0.41112	.48414E 11
0.29	0.90583	0.44594	0.5648E-06	0.085	0.37278	.10305E 12
0.39	0.94525	0.44008	0.5783E-06	0.092	0.32601	.21806E 12
0.57	0.96748	0.43529	0.5873E-06	0.099	0.27556	.44471E 12
0.86	0.98040	0.43394	0.5929E-06	0.107	0.22676	.86889E 12
1.35	0.98812	0.43250	0.5964E-06	0.114	0.18311	.16344E 13
2.15	0.99279	0.43162	0.5986E-06	0.121	0.14598	.29825E 13
3.46	0.99562	0.43109	0.5999E-06	0.129	0.11541	.53167E 13
5.63	0.99734	0.43077	0.6006E-06	0.136	0.09075	.93100E 13

NA-ND = 0.100E 17
OXIDE THICKNESS(MICRONS) = 0.0300
FLATBAND CAPACITANCE = .91465
COX(F PER SQ CM) =0.2597E-06
CINT =0.1375E 15
TEMP = 85.000
EG(EV) = 0.102

GATE VOLTAGE	LOW FREQ. CAP.	HIGH FREQ. CAP.	DEPL. LAYER WIDTH(METERS)	SURFACE POTENTIAL	DEPL. CAP.	Q STORAGE
-7.84	0.99812			-0.062		
-3.71	0.99604			-0.051		
-1.75	0.99171			-0.040		
-0.81	0.98296			-0.029		
-0.35	0.96640			-0.018		
-0.10	0.93889			-0.007		
0.04	0.90135			0.004		
0.13	0.86025			0.015		
0.20	0.82282			0.026		
0.23	0.80630	0.80670	0.3267E-06	0.031	0.80196	.17949E 10
0.29	0.78457	0.77610	0.3934E-06	0.042	0.77110	.23252E 10
0.39	0.33808	0.73467	0.4925E-06	0.063	0.72137	.33640E 10
0.44	0.89345	0.72344	0.5213E-06	0.070	0.69789	.18352E 11
0.53	0.93916	0.71420	0.5457E-06	0.077	0.66363	.43027E 11
0.70	0.96651	0.70714	0.5648E-06	0.085	0.61287	.10688E 12
1.00	0.98106	0.70220	0.5783E-06	0.092	0.54513	.25337E 12
1.51	0.98892	0.69896	0.5873E-06	0.099	0.46707	.56687E 12
2.37	0.99338	0.69695	0.5929E-06	0.107	0.38803	.11887E 13
3.81	0.99601	0.69571	0.5964E-06	0.114	0.31518	.23531E 13
6.20	0.99758	0.69495	0.5986E-06	0.121	0.25212	.44495E 13
10.13	0.99854	0.69450	0.5999E-06	0.129	0.19968	.81272E 13
16.62	0.99911	0.69422	0.6006E-06	0.136	0.15714	.14469E 14

NA-ND = 0.100E 17
OXIDE THICKNESS(MICRONS) = 0.0100
FLATBAND CAPACITANCE = .78129
COX(F PER SQ CM) =0.7792E-06
CINT =0.1375E 15
TEMP = 85.000
EG(EV) = 0.102

GATE VOLTAGE	LOW FREQ. CAP.	HIGH FREQ. CAP.	DEPL. LAYER WIDTH(METERS)	SURFACE POTENTIAL		DEPL. CAP.	Q STORAGE
-2.65	0.99439			-0.062			
-1.27	0.98822			-0.051			
-0.61	0.97554			-0.040			
-0.29	0.95055			-0.029			
-0.13	0.90554			-0.018			
-0.04	0.83664			-0.007			
0.02	0.75282			0.004			
0.05	0.67234			0.015			
0.08	0.60754			0.026			
0.10	0.58115	0.58179	0.3267E-06	0.031		0.56683	.71815E 10
0.12	0.54832	0.53606	0.3934E-06	0.042		0.52344	.76051E 10
0.17	0.63306	0.47997	0.4925E-06	0.063	T	0.46321	.13948E 11
0.19	0.73651	0.46580	0.5213E-06	0.070		0.44025	.24160E 11
0.23	0.83728	0.45444	0.5457E-06	0.077		0.41112	.48414E 11
0.29	0.90583	0.44594	0.5648E-06	0.085		0.37278	.10305E 12
0.39	0.94525	0.44008	0.5783E-06	0.092		0.32601	.21806E 12
0.57	0.96748	0.43629	0.5873E-06	0.099		0.27556	.44471E 12
0.86	0.98040	0.43394	0.5929E-06	0.107		0.22676	.86889E 12
1.35	0.98812	0.43250	0.5964E-06	0.114		0.18311	.16344E 13
2.15	0.99279	0.43162	0.5986E-06	0.121		0.14598	.29825E 13
3.46	0.99562	0.43109	0.5999E-06	0.129		0.11541	.53167E 13
5.63	0.99734	0.43077	0.6006E-06	0.136		0.09075	.93100E 13

NA-ND = 0.100E 17
OXIDE THICKNESS(MICRONS) = 0.0100
FLATBAND CAPACITANCE = .72893
CO(F PER SQ CM) =0.7792E-06
CINT =0.3098E 16
TEMP = 150.000
EG(EV) = 0.131

GATE VOLTAGE	LOW FREQ. CAP.	HIGH FREQ. CAP.	DEPL. LAYER WIDTH(METERS)	SURFACE POTENTIAL		DEPL. CAP.	Q STORAGE
-3.55	0.99256			-0.110			
-1.71	0.98441			-0.090			
-0.83	0.96775			-0.071			
-0.40	0.93529			-0.052			
-0.18	0.87820			-0.032			
-0.06	0.79578			-0.013			
0.02	0.71374			0.006			
0.05	0.69245	0.74542	0.1552E-06	0.015		0.68571	.15297E 11
0.10	0.70256	0.63549	0.2607E-06	0.030	T	0.56092	.36934E 11
0.15	0.75920	0.58385	0.3240E-06	0.043		0.48800	.69714E 11
0.21	0.83114	0.55204	0.3688E-06	0.056		0.42392	.13295E 12
0.31	0.89101	0.53248	0.3991E-06	0.069		0.36250	.25543E 12
0.46	0.93203	0.52051	0.4187E-06	0.082		0.30363	.48553E 12
0.70	0.95813	0.51323	0.4311E-06	0.095		0.24940	.90438E 12
1.10	0.97434	0.50885	0.4387E-06	0.108		0.20164	.16480E 13
1.75	0.98433	0.50621	0.4434E-06	0.121		0.16112	.29438E 13
2.82	0.99045	0.50462	0.4462E-06	0.134		0.12767	.51719E 13
4.57	0.99419	0.50366	0.4479E-06	0.147		0.10058	.89664E 13
7.46	0.99647	0.50303	0.4490E-06	0.160		0.07893	.15381E 14

GRAPH TITLED
PB(.76) SN(.24) TE NA=1.0E16 T=150 X=100A
DOSHIER
HAS BEEN PLOTTED.

NA-ND = 0.100E 17
OXIDE THICKNESS(MICRONS) = 0.0100
FLATBAND CAPACITANCE = .78129
COX(PER SQ CM) =0.7792E-06
CINT =0.1447E 12
TEMP = 85.000
EG(EV) = 0.219

GATE VOLTAGE	LOW FREQ. CAP.	HIGH FREQ. CAP.	DEPL. LAYER WIDTH(METERS)	SURFACE POTENTIAL	DEPL. CAP.	Q STORAGE
-2.65	0.99439			-0.062		
-1.27	0.98822			-0.051		
-0.61	0.97554			-0.040		
-0.29	0.95055			-0.029		
-0.13	0.90554			-0.018		
-0.04	0.83664			-0.007		
0.02	0.75279			0.004		
0.05	0.67211			0.015		
0.08	0.60631			0.026		
0.11	0.55623			0.037		
0.13	0.51815			0.048		
0.16	0.48833			0.059		
0.18	0.46419			0.070		
0.20	0.44407			0.081		
0.20	0.44231	0.44232	0.5731E-06	0.082	0.43574	.63865E 10
0.22	0.42539	0.42538	0.6140E-06	0.093	0.41952	.62385E 10
0.24	0.41071	0.41064	0.6524E-06	0.104	0.40537	.60999E 10
0.26	0.39793	0.39763	0.6886E-06	0.115	0.39283	.59755E 10
0.27	0.38735	0.38501	0.7230E-06	0.126	0.38161	.58716E 10
0.29	0.38144	0.37554	0.7558E-06	0.137	0.37143	.58342E 10
0.31	0.39138	0.36604	0.7873E-06	0.148	0.36203	.60459E 10
0.34	0.51694	0.35393	0.8297E-06	0.163	0.34861	.87453E 10
0.36	0.65257	0.34889	0.8483E-06	0.171	0.34087	.13869E 11
0.38	0.79279	0.34434	0.8655E-06	0.178	0.32988	.26918E 11
0.43	0.88884	0.34048	0.8805E-06	0.185	0.31258	.58575E 11
0.52	0.94017	0.33750	0.8923E-06	0.193	0.28638	.13009E 12
0.69	0.96616	0.33541	0.9007E-06	0.200	0.25208	.27920E 12
0.98	0.98009	0.33405	0.9062E-06	0.207	0.21389	.56988E 12
1.46	0.98805	0.33321	0.9096E-06	0.214	0.17640	.11100E 13
2.25	0.99277	0.33269	0.9117E-06	0.222	0.14260	.20819E 13
3.57	0.99561	0.33238	0.9130E-06	0.229	0.11375	.37919E 13
5.73	0.99734	0.33219	0.9138E-06	0.236	0.08994	.67531E 13

NA-ND = 0.100E 17
OXIDE THICKNESS(MICRONS) = 0.0100
FLATBAND CAPACITANCE = .78129
COX(F PER SQ CM) =0.7792E-06
CINT =0.1375E 15
TEMP = 85.000
EG(EV) = 0.102

GATE VOLTAGE	LOW FREQ. CAP.	HIGH FREQ. CAP.	DEPL. LAYER WIDTH(METERS)	SURFACE POTENTIAL	DEPL. CAP.	Q STORAGE
-2.65	0.99439			-0.062		
-1.27	0.98822			-0.051		
-0.61	0.97554			-0.040		
-0.29	0.95055			-0.029		
-0.13	0.90554			-0.018		
-0.04	0.83664			-0.007		
0.02	0.75282			0.004		
0.05	0.67234			0.015		
0.08	0.60754			0.026		
0.10	0.58115	0.58179	0.3267E-06	0.031	0.56683	.71815E 10
0.12	0.54832	0.53606	0.3934E-06	0.042	0.52344	.76051E 10
0.17	0.63306	0.47997	0.4925E-06	0.063 T	0.46321	.13948E 11
0.19	0.73651	0.46580	0.5213E-06	0.070	0.44025	.24160E 11
0.23	0.83728	0.45444	0.5457E-06	0.077	0.41112	.48414E 11
0.29	0.90583	0.44594	0.5648E-06	0.085	0.37278	.10305E 12
0.39	0.94525	0.44008	0.5783E-06	0.092	0.32601	.21806E 12
0.57	0.96748	0.43629	0.5873E-06	0.099	0.27556	.44471E 12
0.86	0.98040	0.43394	0.5929E-06	0.107	0.22676	.86889E 12
1.35	0.98812	0.43250	0.5964E-06	0.114	0.18311	.16344E 13
2.15	0.99279	0.43162	0.5986E-06	0.121	0.14598	.29825E 13
3.46	0.99562	0.43109	0.5999E-06	0.129	0.11541	.53167E 13
5.63	0.99734	0.43077	0.6006E-06	0.136	0.09075	.93100E 13

COMPUTER PROGRAM FOR CALCULATION OF IDEAL CAPACITANCE-VOLTAGE CURVES

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THE FOLLOWING COMMENT CARDS DEFINE THE VARIABLES USED IN THE IDEAL CV
CURVE CALCULATIONS
K=1 FOR N TYPE SEMICONDUCTOR
K=2 FOR P TYPE SEMICONDUCTOR
BKC=BACKGROUND CONCENTRATION IN CM**3
DD=INSULATOR THICKNESS IN MICRONS
TEMP=TEMPERTURE IN DEGREES KELVIN
CINT=INTRINSIC CARRIER CONC. IN CM**3
KS=REL. DIELECTRIC CONSTANT OF SEMICONDUCTOR
KINS=REL. DIELECTRIC CONSTANT OF INSULATOR
CO=CAPACITANCE DUE TO THE INSULATOR
EG=ENERGY GAP IN EV
VT=Q/KT
CFB=FLATBAND CAPACITANCE
VG=APPLIED BIAS VOLTAGE
LD=DEBYE LENGTH
UF=FERMI LEVEL INQ/KT UNITS
US=SURFACE POTENTIAL IN Q/KT UNITS
MM=NUMBER OF SETS OF DATA USED IN THIS RUN
T(X)=ROOTS OF EQUATIONS FOR INTEGRATION BY GAUSSIAN QUADRATURE TECHNIQUE
USING 40 ROOTS
A(X)=WEIGHTING FACTORS FOR GAUSSIAN QUADRATURE INTEGRATION

      DIMENSION B(40),R(40),G(40),C(40),D(40),F(40),XD(40),A(40),T(40)
      DIMENSION X1(100),X2(100),Y1(100),Y2(100)
      DIMENSION RANGE(4)
      DIMENSION Y3(100)
      REAL LD,KS,KINS
      REAL LABL1/' LF '/
      REAL LABL2/' HF '/
      REAL LABL3/'DEPL'/
      REAL*8 TITLE(12)
      MM=2
      DO 100 L=1,MM
      READ(5,555) TITLE
  555 FORMAT(6A8)
      READ(5,22) BKC
   22 FORMAT(E8.3)
      READ(5,33) DD
   33 FORMAT(E8.3)
```

```
      READ(5,44) TEMP
   44 FORMAT(E8.3)
      K=2
      KINS=8.8
      KS=400.
NOTE THAT THE EQUATIONS FOR EG AND CINT MUST BE ALTERED FOR DIFFERENT
SEMICONDUCTOR MATERIALS
      EG=6.37E-2+4.52E-4*TEMP
      CINT1=4.82E15*(TEMP**1.5)
      AAA=-5.8E3*EG/TEMP
      CINT2=2.7183**AAA
      CINT3=(EG*1.12)**1.5
      CINT=CINT1*CINT2*CINT3
      N=40
      T(1)=-.99823772
      T(2)=-.99072625
      T(3)=-.97725996
      T(4)=-.95791683
      T(5)=-.93281282
      T(6)=-.90209882
      T(7)=-.86595952
      T(8)=-.82461224
      T(9)=-.77830566
      T(10)=-.72731826
      T(11)=-.67195670
      T(12)=-.61255389
      T(13)=-.54946713
      T(14)=-.48307581
      T(15)=-.41377921
      T(16)=-.34199410
      T(17)=-.26815218
      T(18)=-.19269758
      T(19)=-.11608407
      T(20)=-.03877242
      T(21)=-T(20)
      T(22)=-T(19)
      T(23)=-T(18)
      T(24)=-T(17)
      T(25)=-T(16)
      T(26)=-T(15)
      T(27)=-T(14)
      T(28)=-T(13)
      T(29)=-T(12)
      T(30)=-T(11)
      T(31)=-T(10)
      T(32)=-T(9)
      T(33)=-T(8)
      T(34)=-T(7)
```

```
T(35)=-T(6)
T(36)=-T(5)
T(37)=-T(4)
T(38)=-T(3)
T(39)=-T(2)
T(40)=-T(1)
A(1)=.00452099
A(2)=.01049824
A(3)=.01642096
A(4)=.02224580
A(5)=.02793700
A(6)=.03346017
A(7)=.03878215
A(8)=.04387093
A(9)=.04869579
A(10)=.05322785
A(11)=.05743978
A(12)=.06130627
A(13)=.06480403
A(14)=.06791206
A(15)=.07061167
A(16)=.07288660
A(17)=.07472319
A(18)=.07611039
A(19)=.07703985
A(20)=.07750598
A(21)=A(20)
A(22)=A(19)
A(23)=A(18)
A(24)=A(17)
A(25)=A(16)
A(26)=A(15)
A(27)=A(14)
A(28)=A(13)
A(29)=A(12)
A(30)=A(11)
A(31)=A(10)
A(32)=A(9)
A(33)=A(8)
A(34)=A(7)
A(35)=A(6)
A(36)=A(5)
A(37)=A(4)
A(38)=A(3)
A(39)=A(2)
A(40)=A(1)
LD=4.879525E-2*SQRT(TEMP*KS/CINT)
CO=8.85415E-6*KINS/DD
```

```
      VT=1.16057E4/TEMP
      CD=8.85415E-12*KS/LD
      UF=((-1.)**K)*ALOG(BKC/CINT)
      CFF=1./SQRT(2.)*EXP(ABS(UF/2.))*CD
      CFB=1./(1.+CO/CFF)
      WRITE(6,997)
  997 FORMAT('1')
      IF(K-2)1,2,12
    1 WRITE(6,4) BKC
    4 FORMAT(//9H ND-NA = ,E9.3)
      GO TO 11
    2 WRITE(6,5) BKC
    5 FORMAT(//9H NA-ND = ,E9.3)
   11 WRITE(6,6) DD
    6 FORMAT(28H OXIDE THICKNESS(MICRONS) = ,F6.4)
      WRITE(6,49) CFB
   49 FORMAT(24H FLATBAND CAPACITANCE = ,F6.5)
      COO=CO*1.0E-4
      WRITE(6,99) COO
   99 FORMAT(18H GO(F PER SQ CM) =,E10.4)
      WRITE(6,88)CINT
   88 FORMAT(7H CINT =,E10.4)
      WRITE(6,77) TEMP
   77 FORMAT(7H TEMP =,F10.3)
      WRITE(6,66) EG
   66 FORMAT(9H EG(EV) =,F10.3)
      WRITE(6,200)
  200 FORMAT(66X,11HDEPL. LAYER8X,7HSURFACE)
      WRITE(6,7)
    7 FORMAT(6X,12HGATE VOLTAGE6X,14HLOW FREQ. CAP.6X,15HHIGH FREQ. CAP.
     16X,13HWIDTH(METERS)6X,9HPOTENTIAL6X,10HDEPL. CAP.9X,9HQ STORAGE)
      US=((-1.)**(K+1))*10
      DELUS=((-1.)**K)*1.5
      KK=(UF-US)/DELUS
CALCULATION OF LOW FREQUENCY CV CURVE ONLY
      DO 30 M=1,KK
      INDX1=M
      US=US+DELUS
      Z=US/ABS(US)
      CC=Z*(SINH(US-UF)+SINH(UF))*CD
      CCC=SQRT(2.*(COSH(US-UF)+US*SINH(UF)-COSH(UF)))
      CS=CC/CCC
      CLF=1./(1.+CO/CS)
      QS1=-2.*7.62913E-16*Z*KS*TEMP/LD
      QS2=SQRT(.5*(COSH(US-UF)+US*SINH(UF)-COSH(UF)))
      QS=QS1*QS2
      PHIS=US/VT
      VG=PHIS-(QS/CO)
```

```
      WRITE(6,35) VG,CLF,PHIS
   35 FORMAT(9X,F6.2,9X,F10.5,50X,F6.3)
      X1(INDX1)=VG
      Y1(INDX1)=CLF
   30 CONTINUE
      US=UF-DELUS
      AA=0.
CALCULATION OF LOW AND HIGH FREQUENCY CV CURVES TOGETHER
      LL=UF/DELUS
      DO 10 J=1,LL
      INDX1=KK+J
      INDX2=J
      XDX=0.0
   18 US=US+DELUS
      B(J)=US
CALCULATION OF EFFECTIVE DEPLETION LAYER WIDTH BY GAUSSIAN QUADRATURE
INTEGRATION
      DO 45 I=1,N
      R(I)=.5*(B(J)-AA)*T(I)+.5*(B(J)+AA)
      IF(K-2) 21,24,24
   21 G(I)=EXP(R(I))-1.
      GO TO 25
   24 G(I)=1.-EXP(-R(I))
   25 C(I)=COSH(R(I)-UF)
      D(I)=R(I)*SINH(UF)-COSH(UF)
      F(I)=G(I)/SQRT(2.*(C(I)+D(I)))
      XD(J)=A(I)*F(I)+XDX
      XDX=XD(J)
   45 CONTINUE
      XD(J)=(B(J)-AA)*LD*XDX/2.
      XDY=XD(J)
      CSC=8.85415E-12*KS/XDY
      CHF=1./(1.+CO/CSC)
      CC=Z*(SINH(US-UF)+SINH(UF))*CD
      CCC=SQRT(2.*(COSH(US-UF)+US*SINH(UF)-COSH(UF)))
      CS=CC/CCC
      CLF=1./(1.+CO/CS)
      QS1=-2.*7.62913E-16*Z*KS*TEMP/LD
      QS2=SQRT(.5*(COSH(US-UF)+US*SINH(UF)-COSH(UF)))
      QS=QS1*QS2
      PHIS=US/VT
      VG=PHIS-(QS/CO)
      DC=1./(SQRT(1.+1.105E14*ABS(VG)*KINS**2/(BKC*KS*DD**2)))
      STORE=ABS(VG)*CO*(CHF-DC)/1.602E-15
      WRITE(6,80)VG,CLF,CHF,XDY,PHIS,DC,STORE
   80 FORMAT(9X,F6.2,9X,F10.5,10X,F10.5,11X,E10.4,9X,F6.3,10X,F10.5,9X,E
     110.5)
      X1(INDX1)=VG
```

```
      Y1(INDX1)=CLF
      X2(INDX2)=VG
      Y2(INDX2)=CHF
      Y3(INDX2)=DC
   10 CONTINUE
      DELUS=((-1.)**K)*1.0
      US=2.*UF-DELUS
      DO 60 M=1,11
      INDX1=KK+LL+M
      INDX2=LL+M
      XDX=0.0
      US=US+DELUS
      B(M)=US
C CALCULATION OF EFFECTIVE DEPLETION LAYER WIDTH BY GAUSSIAN QUADRATURE
C INTEGRATION
      DO 50 I=1,N
      R(I)=.5*(B(M)-AA)*T(I)+.5*(B(M)+AA)
      IF(K-2)26,27,27
   26 G(I)=EXP(R(I))-1.
      GO TO 28
   27 G(I)=1.-EXP(-R(I))
   28 C(I)=COSH(R(I)-UF)
      D(I)=R(I)*SINH(UF)-COSH(UF)
      F(I)=G(I)/SQRT(2.*(C(I)+D(I)))
      XD(M)=A(I)*F(I)+XDX
      XDX=XD(M)
   50 CONTINUE
      XD(M)=(B(M)-AA)*LD*XDX/2.
      XDY=XD(M)
      CSC=8.85415E-12*KS/XDY
      CHF=1./(1.+CO/CSC)
      CC=Z*(SINH(US-UF)+SINH(UF))*CD
      CCC=SQRT(2.*(COSH(US-UF)+US*SINH(UF)-COSH(UF)))
      CS=CC/CCC
      CLF=1./(1.+CO/CS)
      QS1=-2.*7.62913E-16*Z*KS*TEMP/LD
      QS2=SQRT(.5*(COSH(US-UF)+US*SINH(UF)-COSH(UF)))
      QS=QS1*QS2
      PHIS=US/VT
      VG=PHIS-(QS/CO)
      DC=1./(SQRT(1.+1.105E14*ABS(VG)*KINS**2/(BKC*KS*DD**2)))
      STORE=ABS(VG)*CO*(CHF-DC)/1.602E-15
      X1(INDX1)=VG
      Y1(INDX1)=CLF
      X2(INDX2)=VG
      Y2(INDX2)=CHF
      Y3(INDX2)=DC
      IF(M-1) 57,58,57
```

```
 57 WRITE(6,42)VG,CLF,CHF,XDY,PHIS,DC,STORE
 42 FORMAT(9X,F6.2,9X,F10.5,10X,F10.5,11X,E10.4,9X,F6.3,10X,F10.5,9X,E
   110.5)
    GO TO 60
 58 WRITE(6,41)VG,CLF,CHF,XDY,PHIS,DC,STORE
 41 FORMAT(9X,F6.2,9X,F10.5,10X,F10.5,11X,E10.4,9X,F6.3,1X,1HT8X,F10.5
   1,9X,E10.5)
 60 CONTINUE
    CALL DRAW(INDX1,X1,Y1,1,0,LABL1,TITLE,1.0,0.0,0,3,0,2,9,6,1,LAST)
    CALL DRAW(INDX2,X2,Y2,2,0,LABL2,TITLE,1.0,0.0,0,3,0,2,9,6,1,LAST)
    CALL DRAW(INDX2,X2,Y3,3,0,LABL3,TITLE,1.0,0.0,0,3,0,2,9,6,1,LAST)
 12 CONTINUE
100 CONTINUE
    END
```

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13. ABSTRACT

The purpose of this thesis is to examine the feasibility of narrow-gap semiconductor charged coupled devices for infrared imaging applications. The semiconductors considered are PbTe for a three to five micron imager and $Pb_{.76}Sn_{.24}Te$ for an eight to 12 micron imager, both operated at a temperature of 85°K. Theoretical calculations of signal current and storage time are made based on the metal-insulator-semiconductor theory developed for silicon M-I-S devices. For a 0.1°K temperature resolution of a 300°K scene, signal currents are 4.8×10^{-6} A/cm^2 for PbTe and 3.2×10^{-2} A/cm^2 for $Pb_{.76}Sn_{.24}Te$ at a clocking frequency of 1 MHz. Storage times of 5.7×10^{-5} seconds for PbTe and 1.27×10^{-6} seconds for $Pb_{.76}Sn_{.24}Te$ are calculated using a minority lifetime of 10^{-7} seconds. Therefore, clocking frequencies higher than 1 MHz are recommended. Experimental studies of $Pb_{1-x}Sn_xTe$ M-I-S were made which demonstrated that accumulation, depletion, and inversion layers can be controlled by gate voltage, following the general behavior of silicon M-I-S devices. A PbTe CCD infrared imager seems feasible. Feasibility of $Pb_{.76}Sn_{.24}Te$ CCD's will require significant improvement in material and fabrication technology to increase storage time and reduce dark current.

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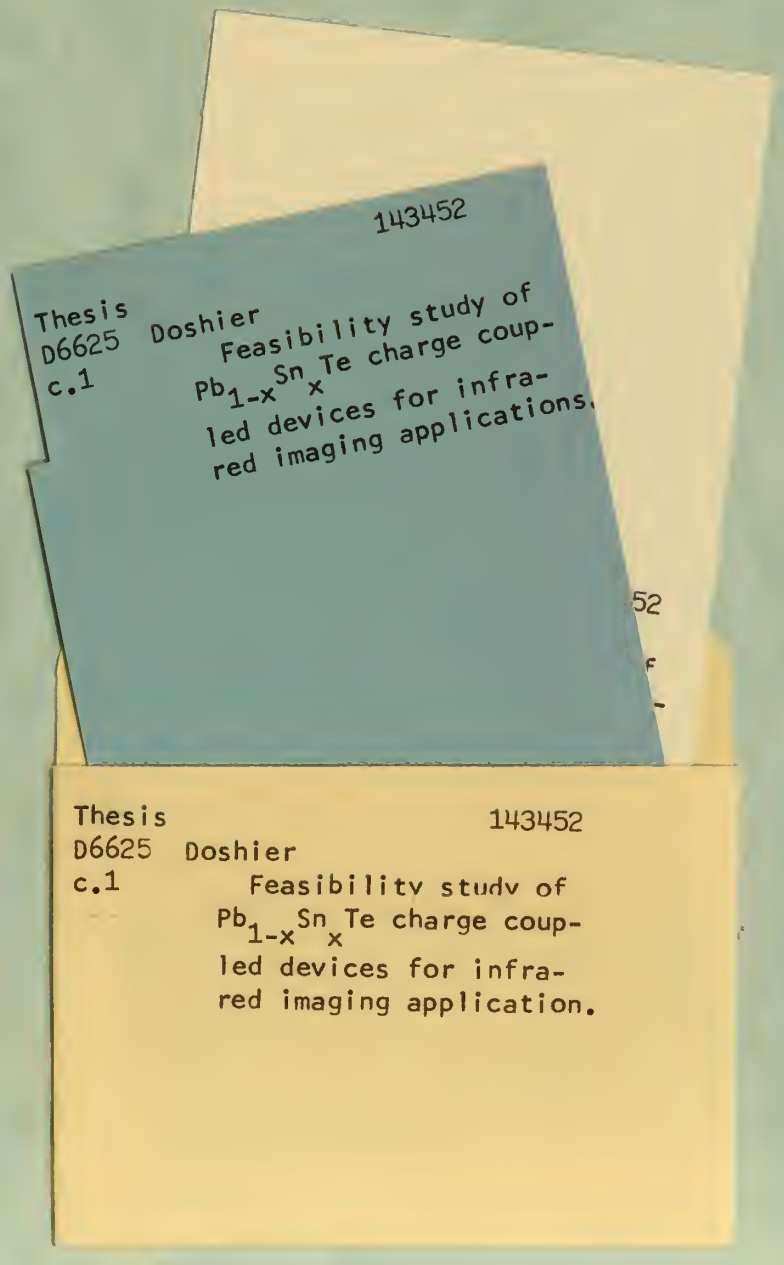
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