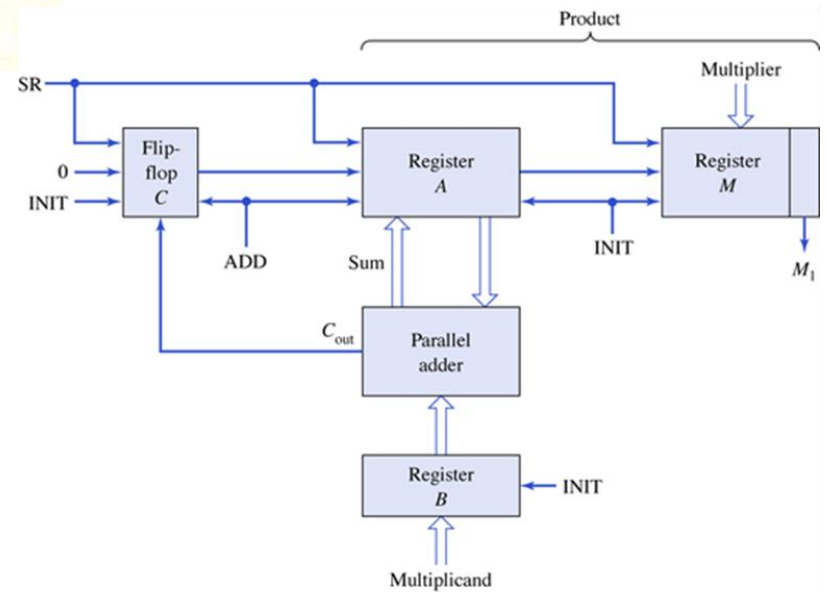
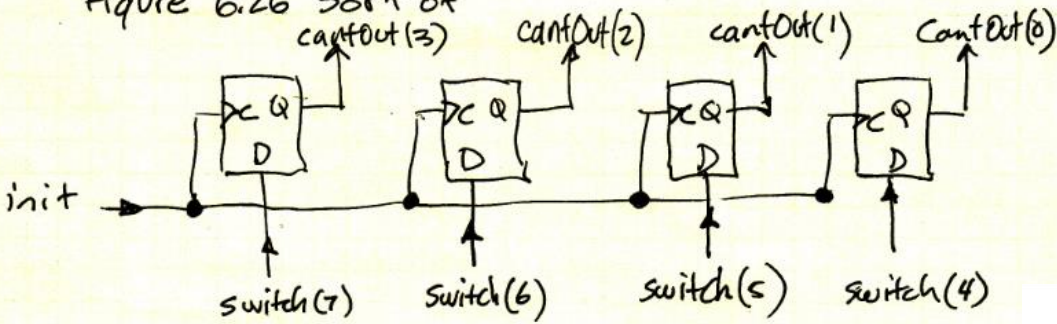


Figure 6.26 sort of



Parallel Adder

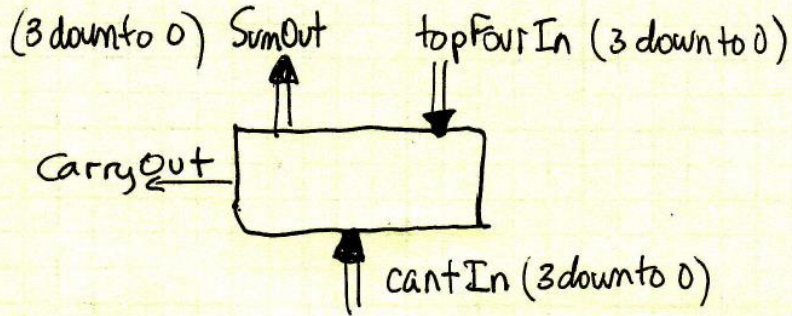
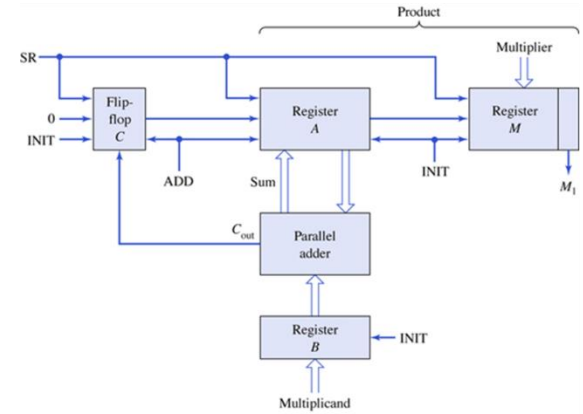
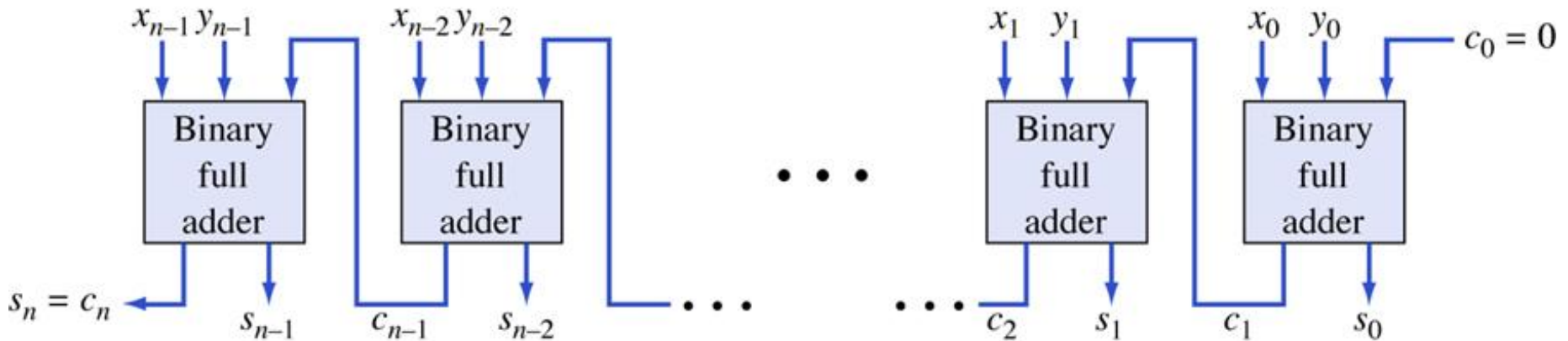
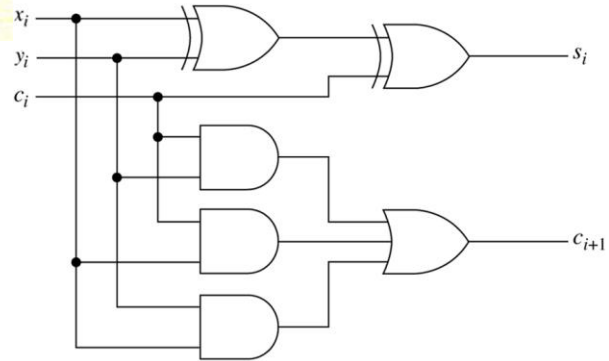


Fig. 5.2 & 5.4 from text
Need 4 individual adders
Then build parallel adder.

		$y_i c_i$			
s_i		00	01	11	10
0	x_i	0	1		1
1		1	0	1	0

		$y_i c_i$			
c_{i+1}		00	01	11	10
0	x_i	0	0	1	0
1		0	1	1	1



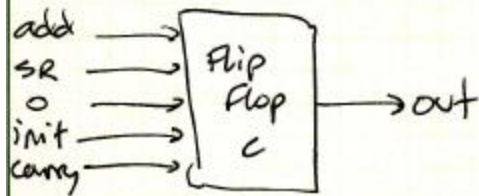
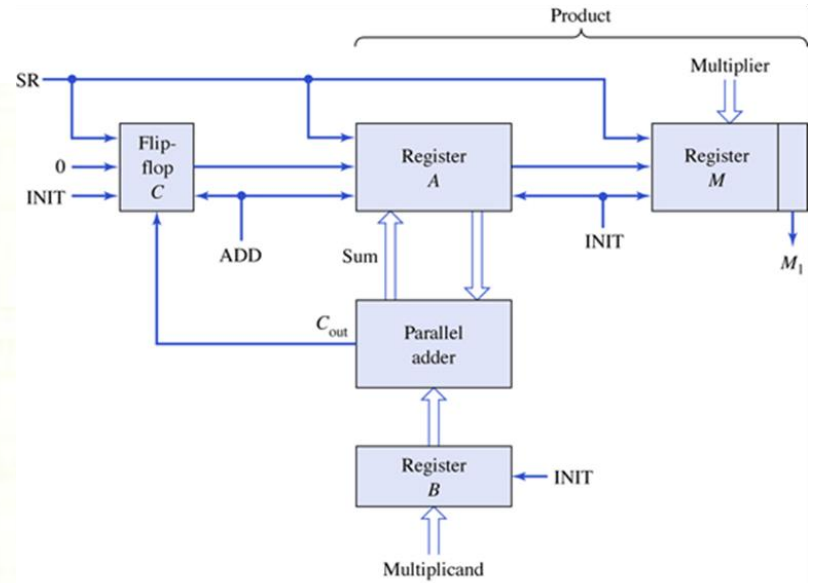
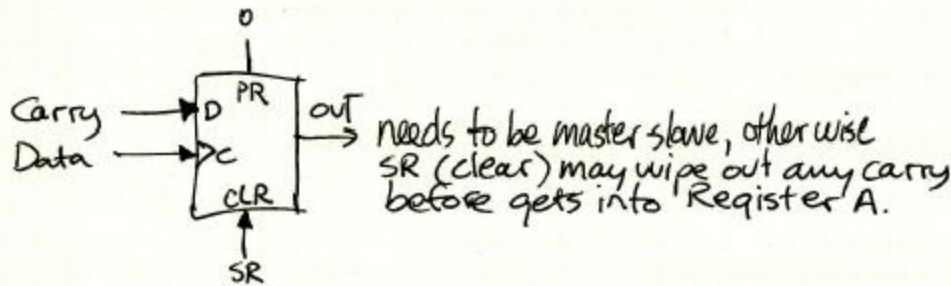


Fig 6.21 tie \overline{PR} to a 1 then what's left is:

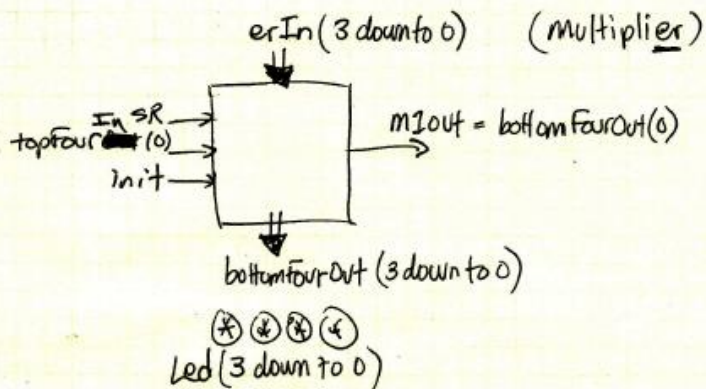
\overline{CLR}	D	C	Q	
0	X	X	0	no matter what, make Q = 0
1	0	↑	0	follow 0 (clock) going up.
1	X	↑	1	follow D (clock going up.)
1	X	0	Q	} hold Q value if clock not changing
1	X	1	Q	

So if Clock = Data, then ~~the~~ carry will appear at output
 if D = carry, then rising edge will capture carry in flip flop, and present it on Q.

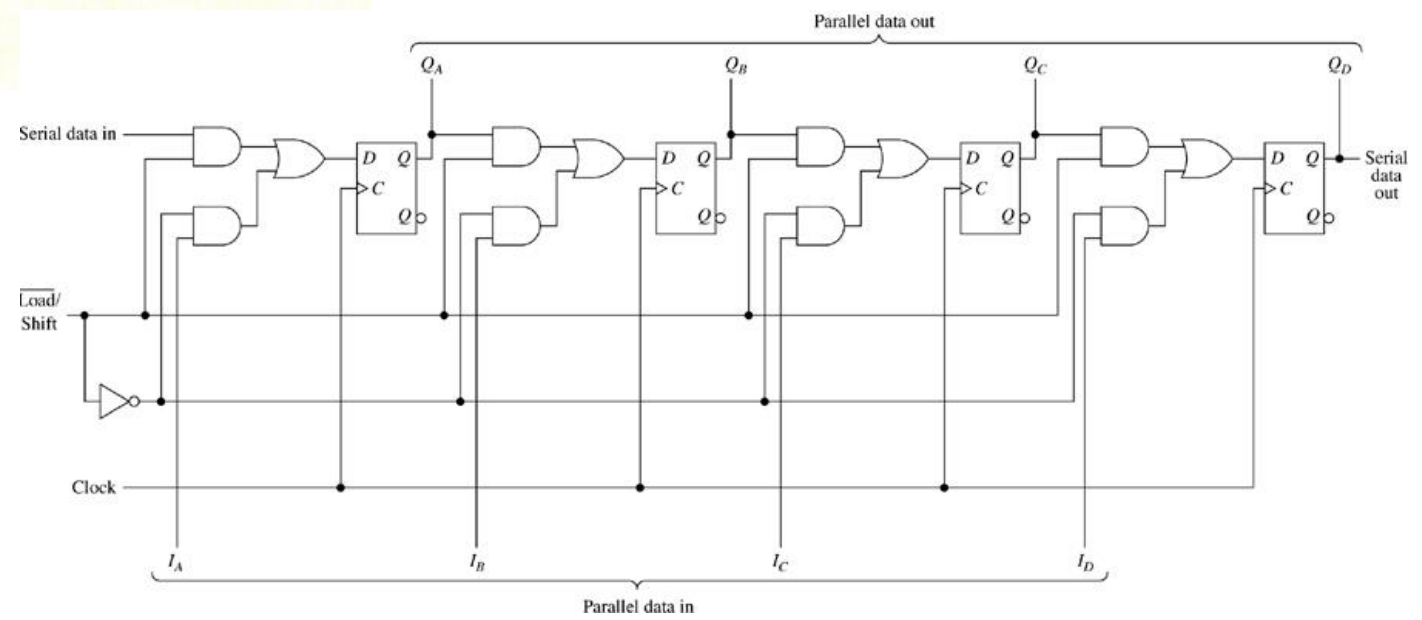
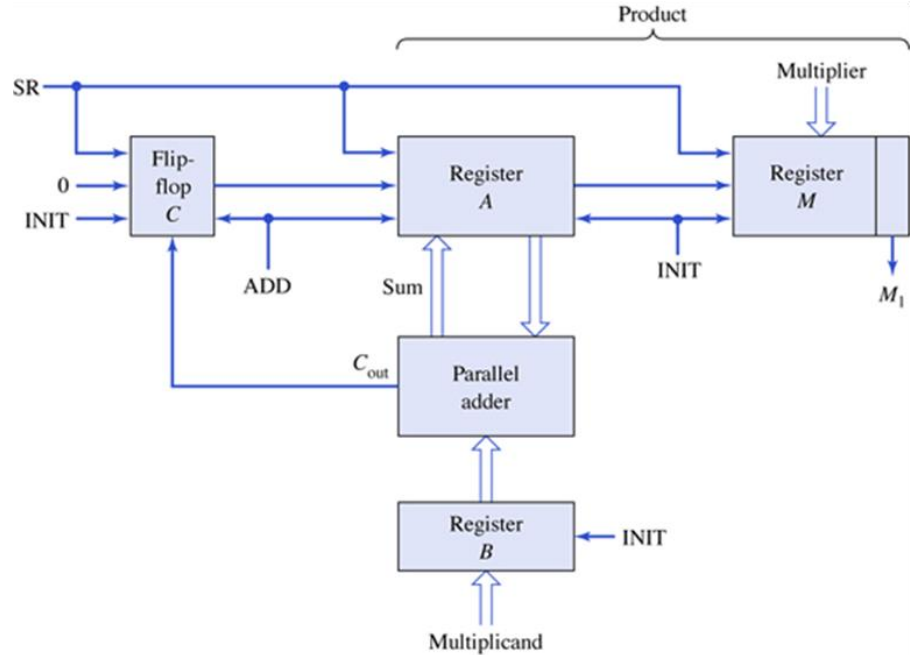
So would look like this:

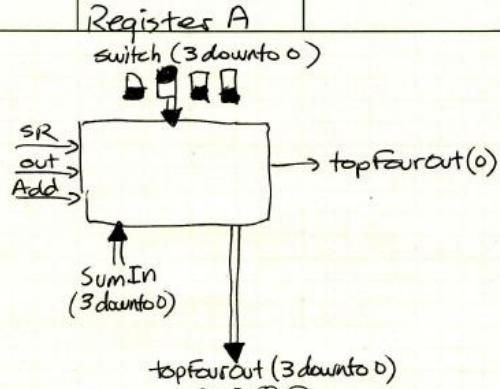


Register M.



Looks like Figure 6.28 in text:
 Serial Data In = topfourIn(0)
 Serial Data Out (not connected).
 Parallel Data In ($I_A I_B I_C I_D$) = erIn(3 down to 0).
 Shift = ~~SR~~ init
 Clock = SR.





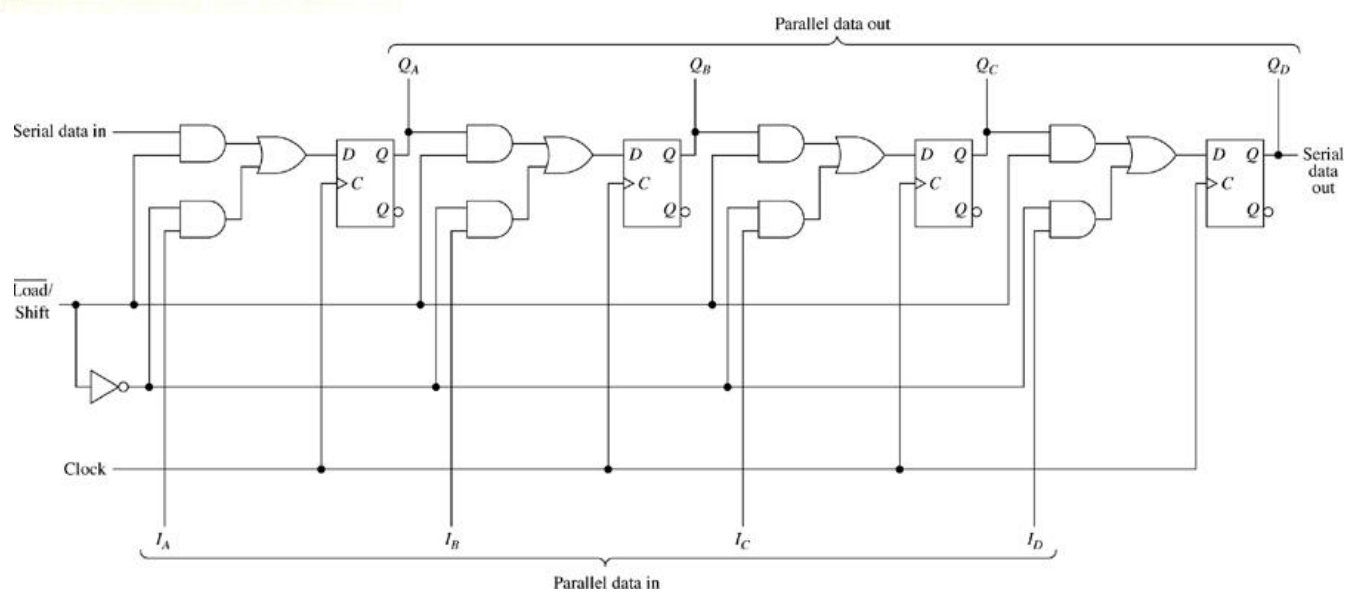
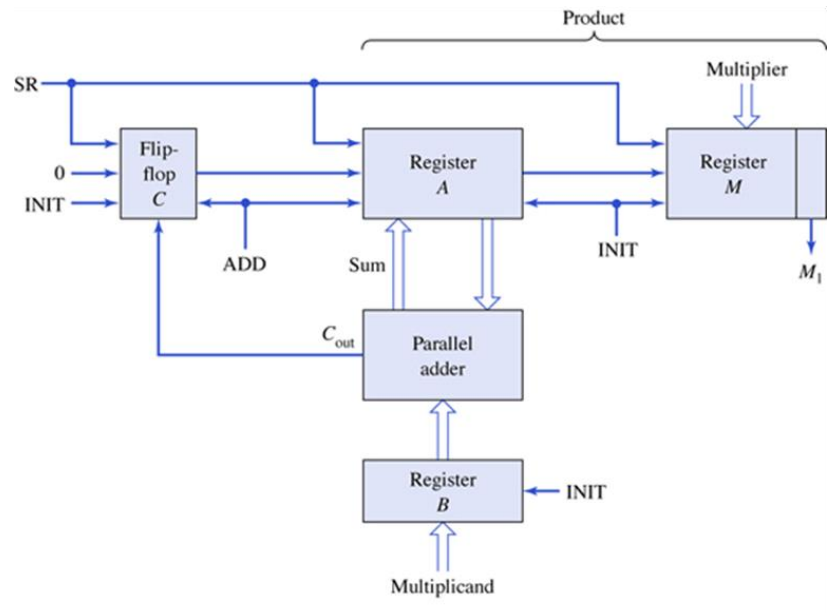
6.28

Fig. ~~6.28~~ in text

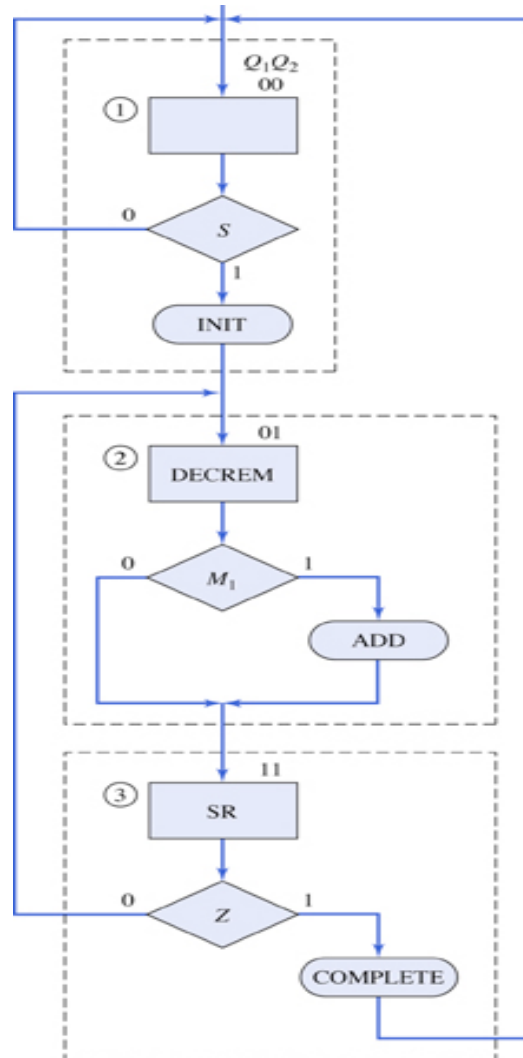
Serial Data In = out (out from flip flop)
 Clock = SR (shift right)

$\overline{\text{LOAD}}/\text{shift} = \text{DATA}$
 when DATA = 0 then want to open possibility of serial in.
 when DATA = 1 then want to load SUM In.

$I_A - I_D = \text{Sum In}$
 $Q_A - Q_D = \text{top Four Rout (3 down to 0)}$
 Serial out = topFourOut(0)



ASM CHART



Plan

- 3-state ASM
 - Initialize
 - Add or not
 - Shift + Zero Detector
- Modules
 - parallel adder
 - Shift Registers or Latches