CMOS Transistor Switching

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10/31/13

Please send corrections (or suggestions) to youngwlim@hotmail.com.

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Simple Transistor Model

Cutoff, subthreshold, or weak-inversion mode

When $V_{GS} < V_t$:

$$I_d = 0$$

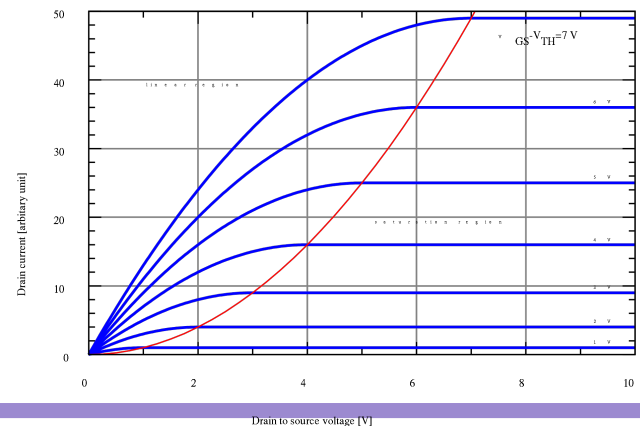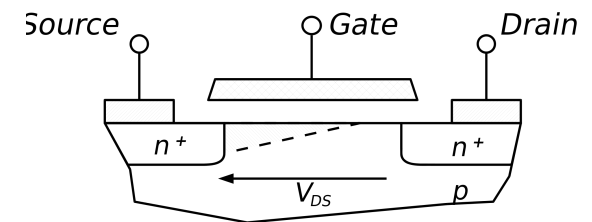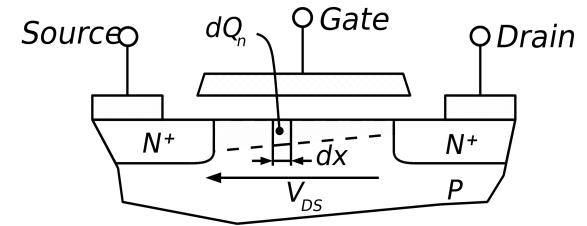**Triode mode or linear region (the ohmic mode)**

When $V_{GS} > V_t$ and $V_{DS} < (V_{GS} - V_t)$

$$I_d = k' \frac{W}{L} \left[(v_{gs} - v_t) v_{ds} - \frac{1}{2} v_{ds}^2 \right]$$
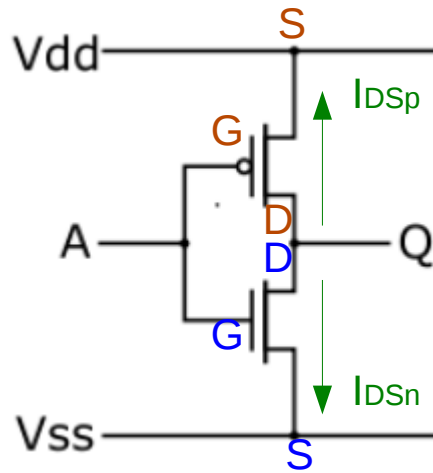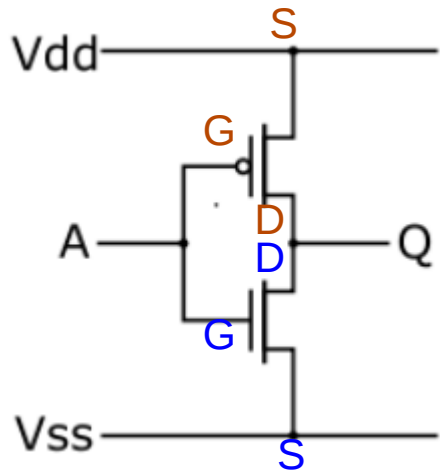
Saturation or active mode

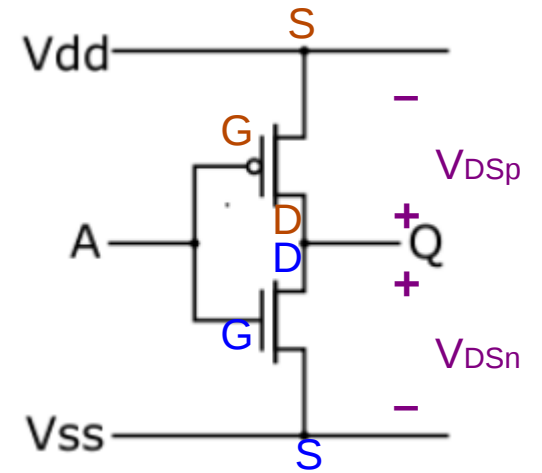When $V_{GS} > V_t$ and $V_{DS} \geq (V_{GS} - V_t)$

$$I_d = \frac{1}{2} k' \frac{W}{L} (v_{gs} - v_t)^2$$

Notation

Current
Notation

Voltage
Notation

Input Voltage
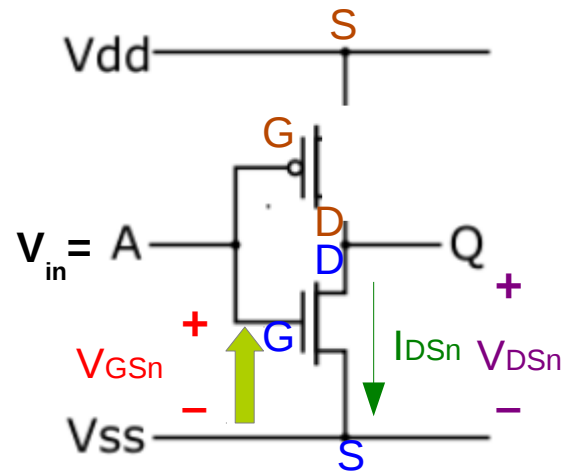
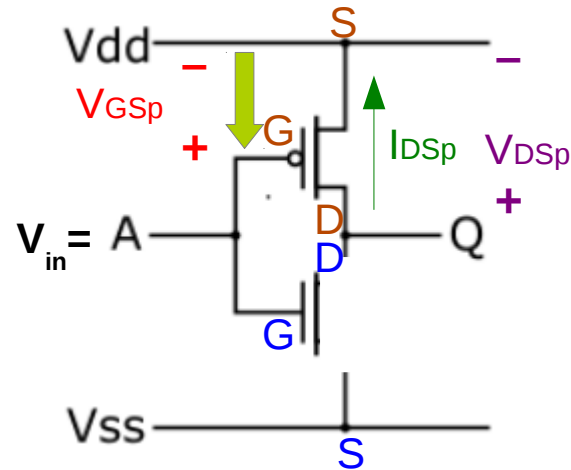$$V_{GSp} = V_{Gp} - V_{Sp}$$

$$= V_{in} - V_{dd}$$

$$V_{SGp} = V_{Sp} - V_{Gp}$$
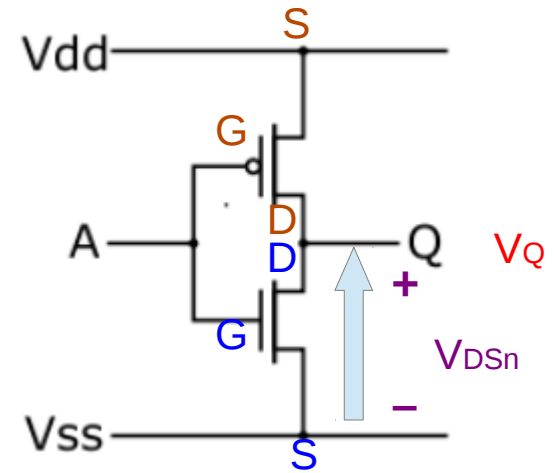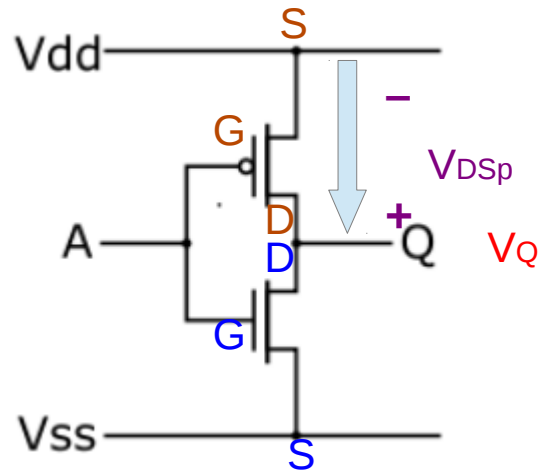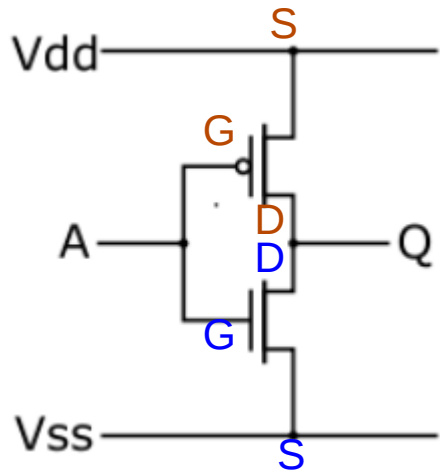
$$= V_{dd} - V_{in}$$

$$V_{in} = V_{GSp} + V_{dd}$$

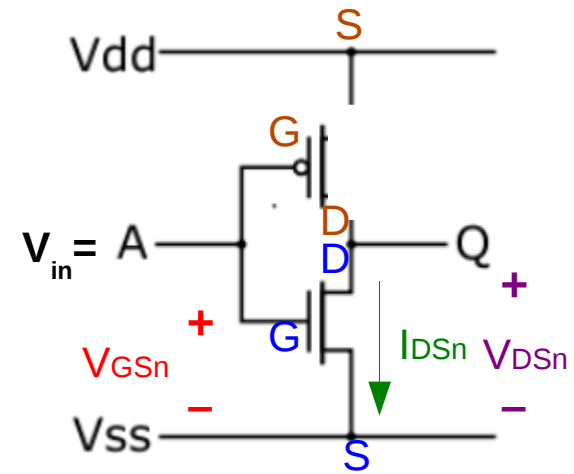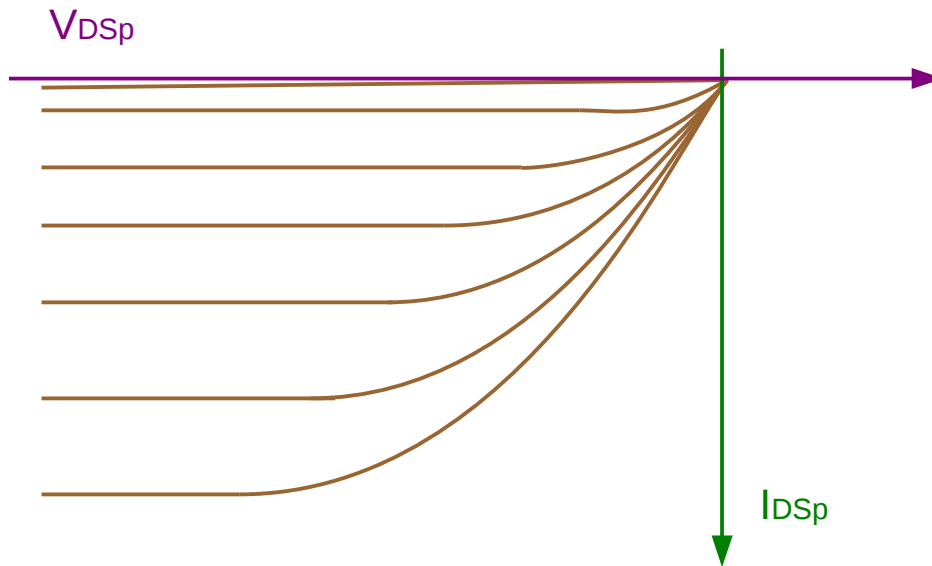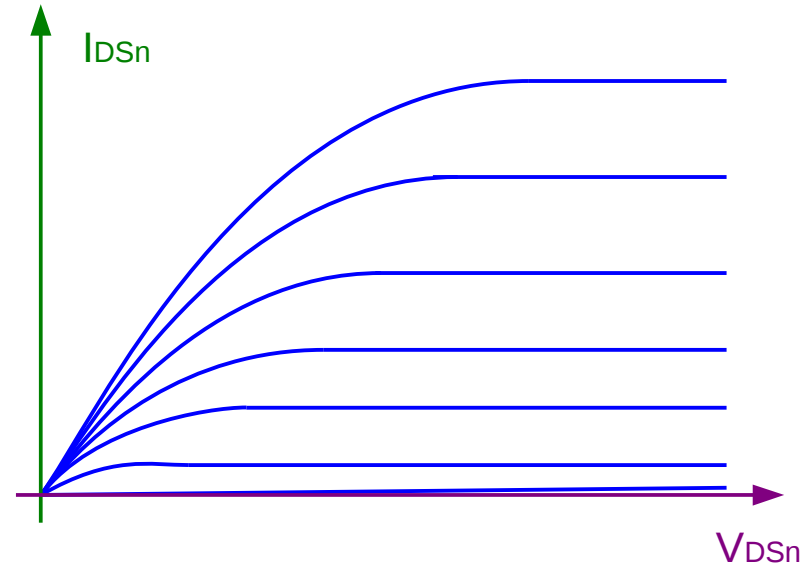$$= V_{GSn}$$

$$V_{GSn} = V_{Gn} - V_{Sn}$$

$$= V_{in}$$

Vdd —— S

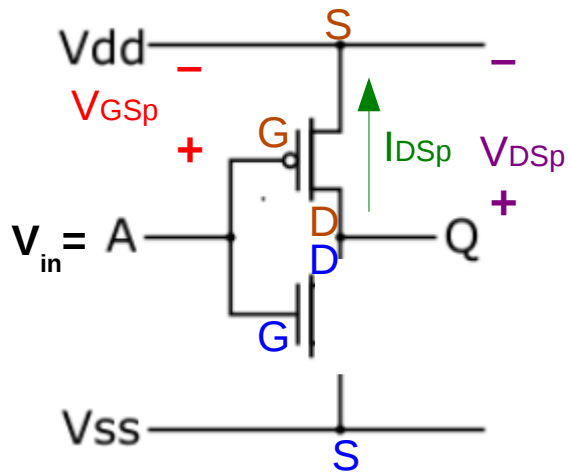V_{GSp} — + G I_{DSp} V_{DSp} +

V_{in} = A —— D Q

G

Vss —— S

Vdd —— S

G

V_{in} = A —— D Q +

+ G I_{DSn} V_{DSn}

V_{GSn} — S

Vss —— S

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Output Voltage

$$V_Q = V_{DSp} + V_{Sp}$$

$$= V_{DSp} + V_{dd}$$

$$V_Q = V_{DSn} + V_S$$

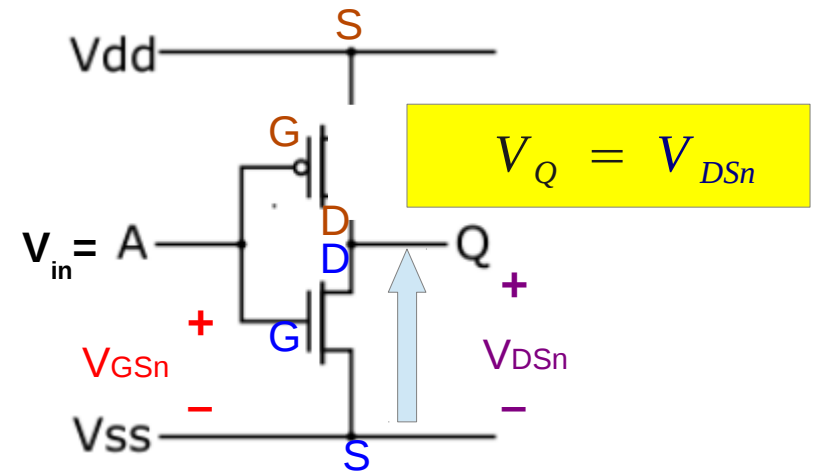$$= V_{DSn} + V_{ss}$$
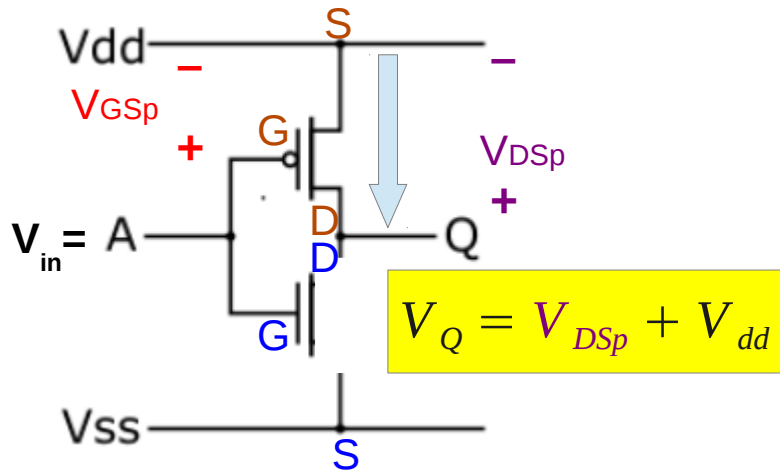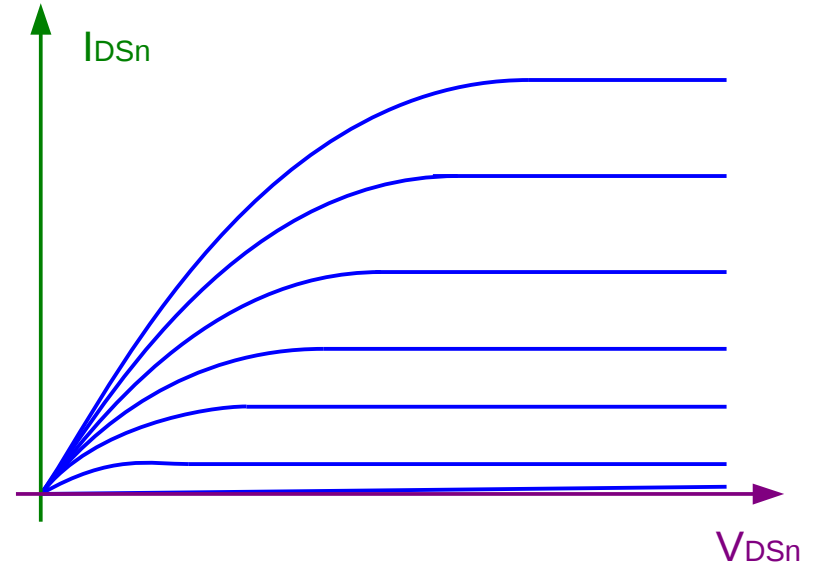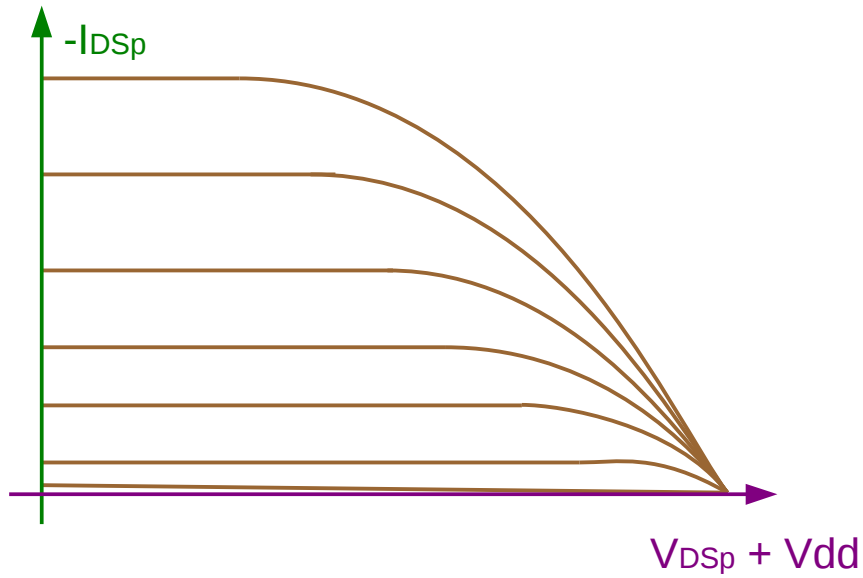
$$= V_{DSn}$$

$$V_{out} = V_{DSp} + V_{dd} = V_{DSn}$$

Characteristic Curves (1)

Characteristic Curves (2)

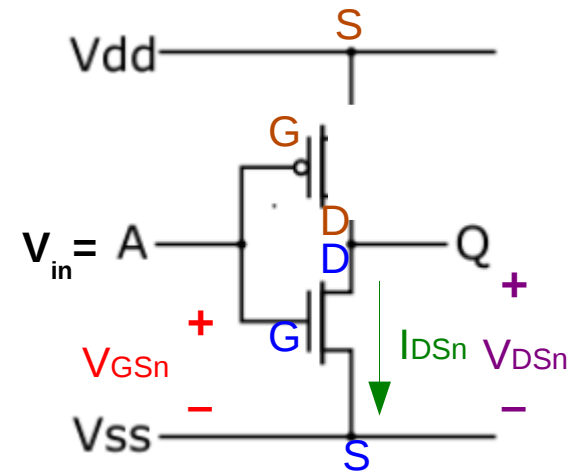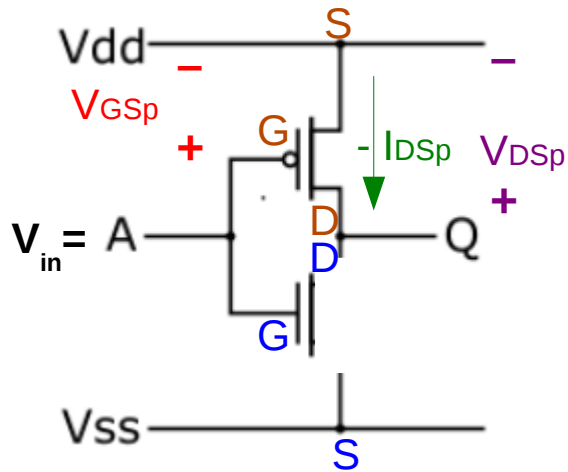8
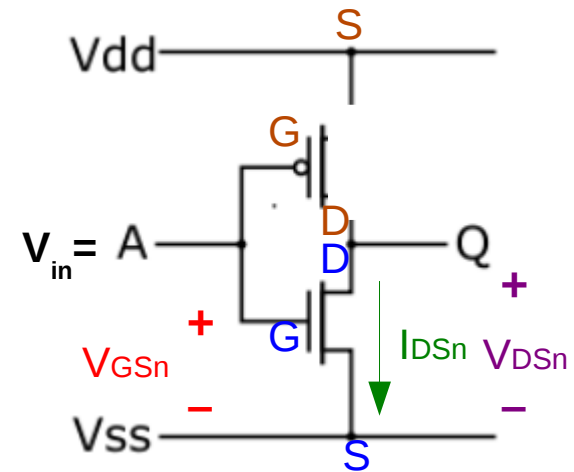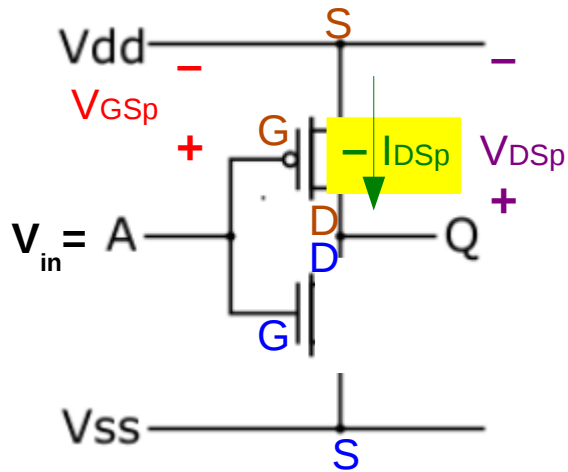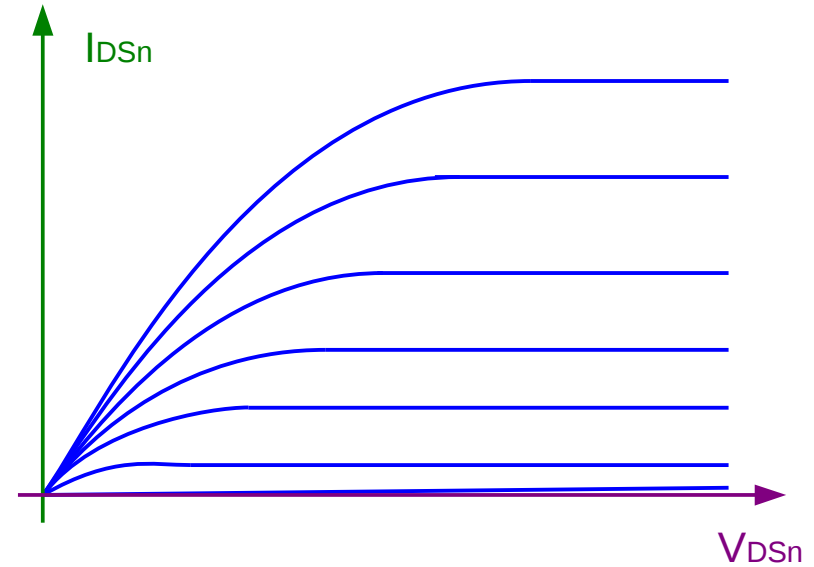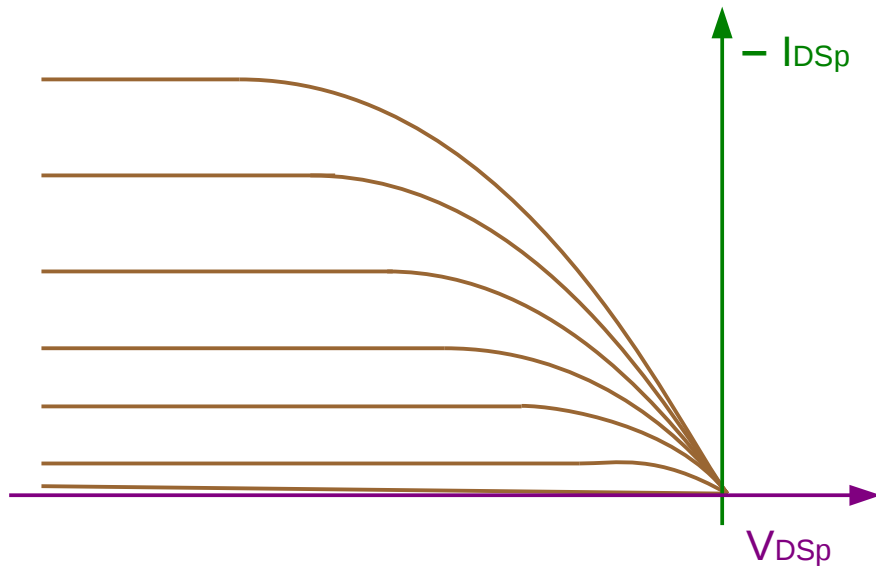
Characteristic Curves (3)

$$V_Q = V_{DSp} + V_{dd}$$

$$V_Q = V_{DSn}$$

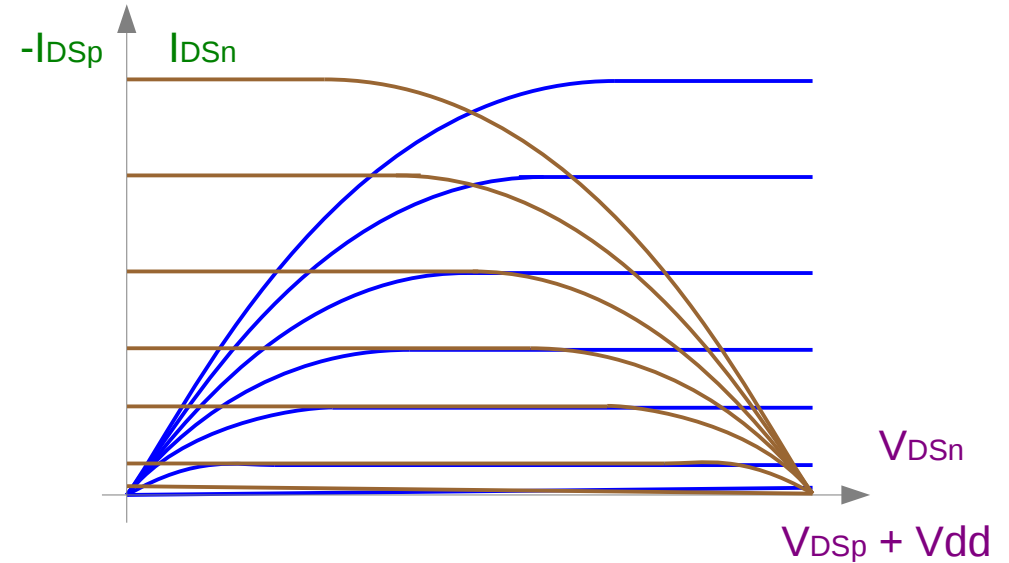# Characteristic Curves (4)

$$V_{in} = V_{GSp} + V_{dd} = V_{GSn}$$

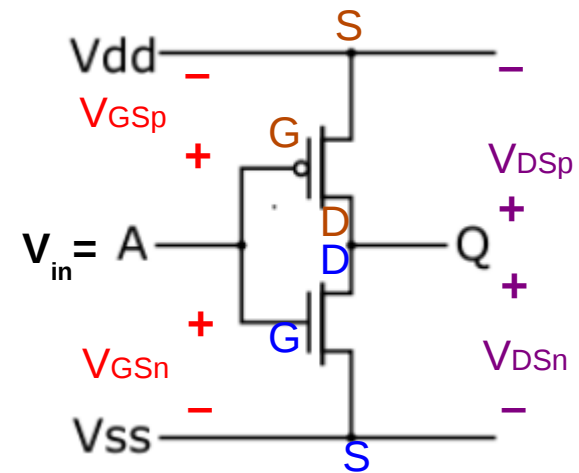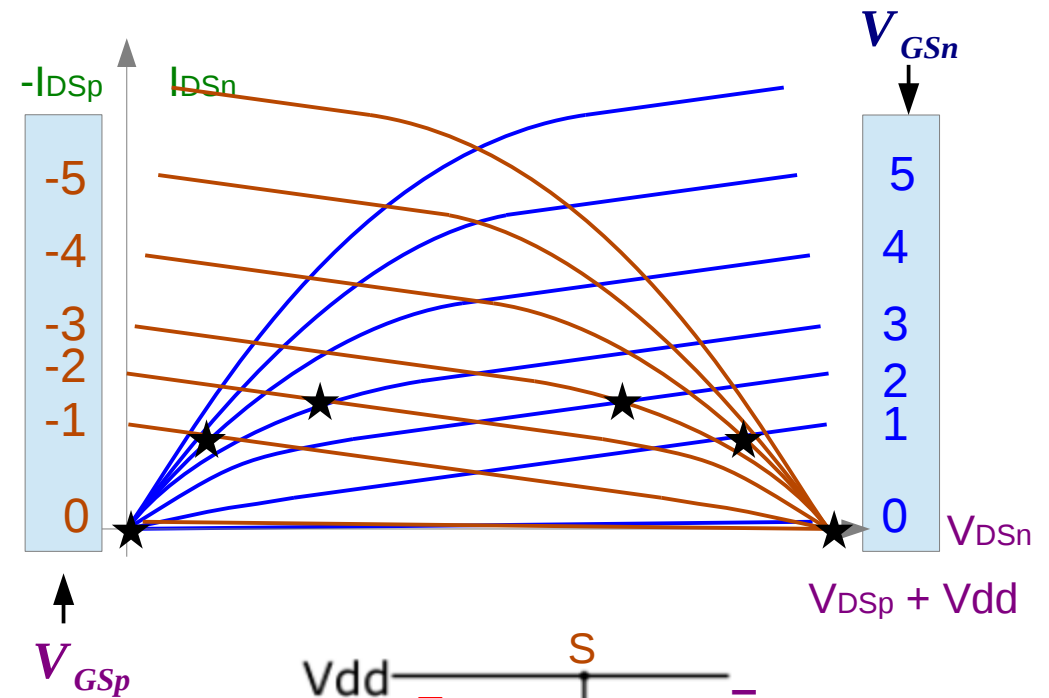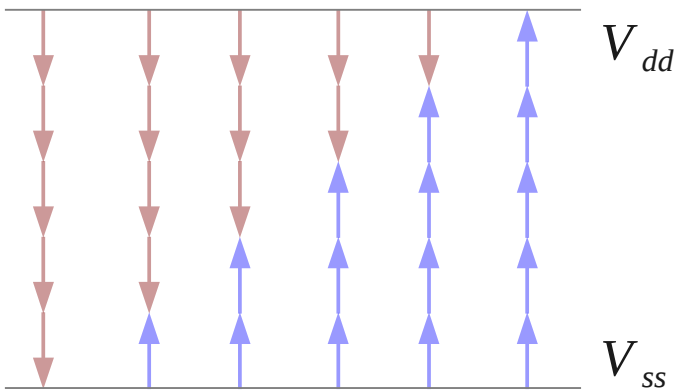$$V_{out} = V_{DSp} + V_{dd} = V_{DSn}$$

Characteristic Curves (5)

$$V_{in} = V_{GSp} + V_{dd} = V_{GSn} \quad \star$$

$$V_{out} = V_{DSp} + V_{dd} = V_{DSn}$$

V_{in}	0	1	2	3	4	5
V_{GSp}	-5	-4	-3	-2	-1	0
V_{GSn}	0	1	2	3	4	5

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Characteristic Curves (6)

V_{in}	0	1	2	3	4	5
V_{GSp}	-5	-4	-3	-2	-1	0
V_{GSn}	0	1	2	3	4	5

pLIN	pLIN	pSAT	pSAT	pSAT	pOFF
nOFF	nSAT	nSAT	nSAT	nLIN	nLIN

Voltage Transfer Curve (1)

in	nMOS	out
H	nLIN	L
↓	↓	↓
	nSAT	
	↓	
L	nOFF	H

Voltage Transfer Curve (2)

in	nMOS	out
H	nLIN	L
	nSAT	
L	nOFF	H

v_{in}: H → L (time)

v_{out}: L → H (time)

v_{out} vs v_{in}: nOFF, nSAT, nLIN
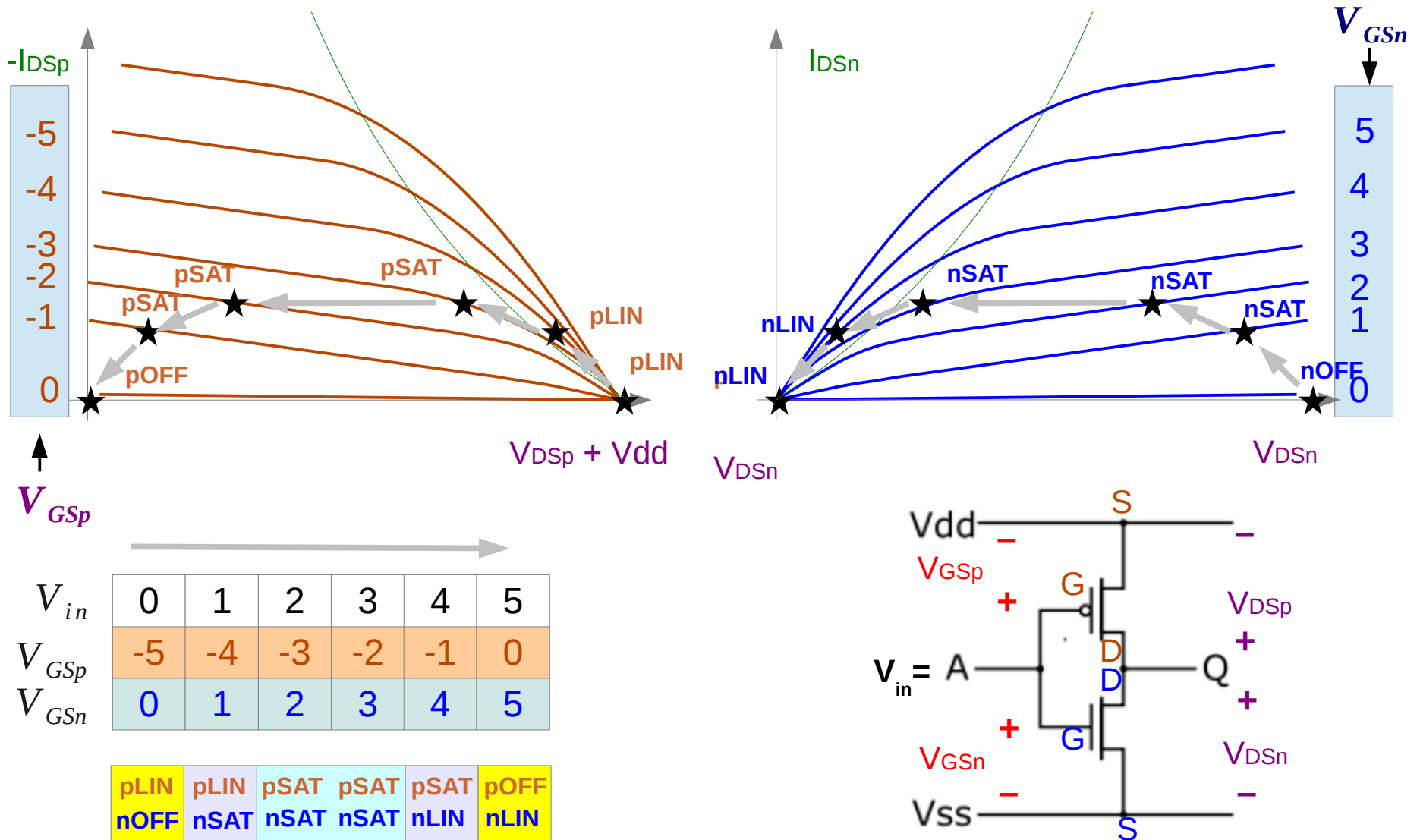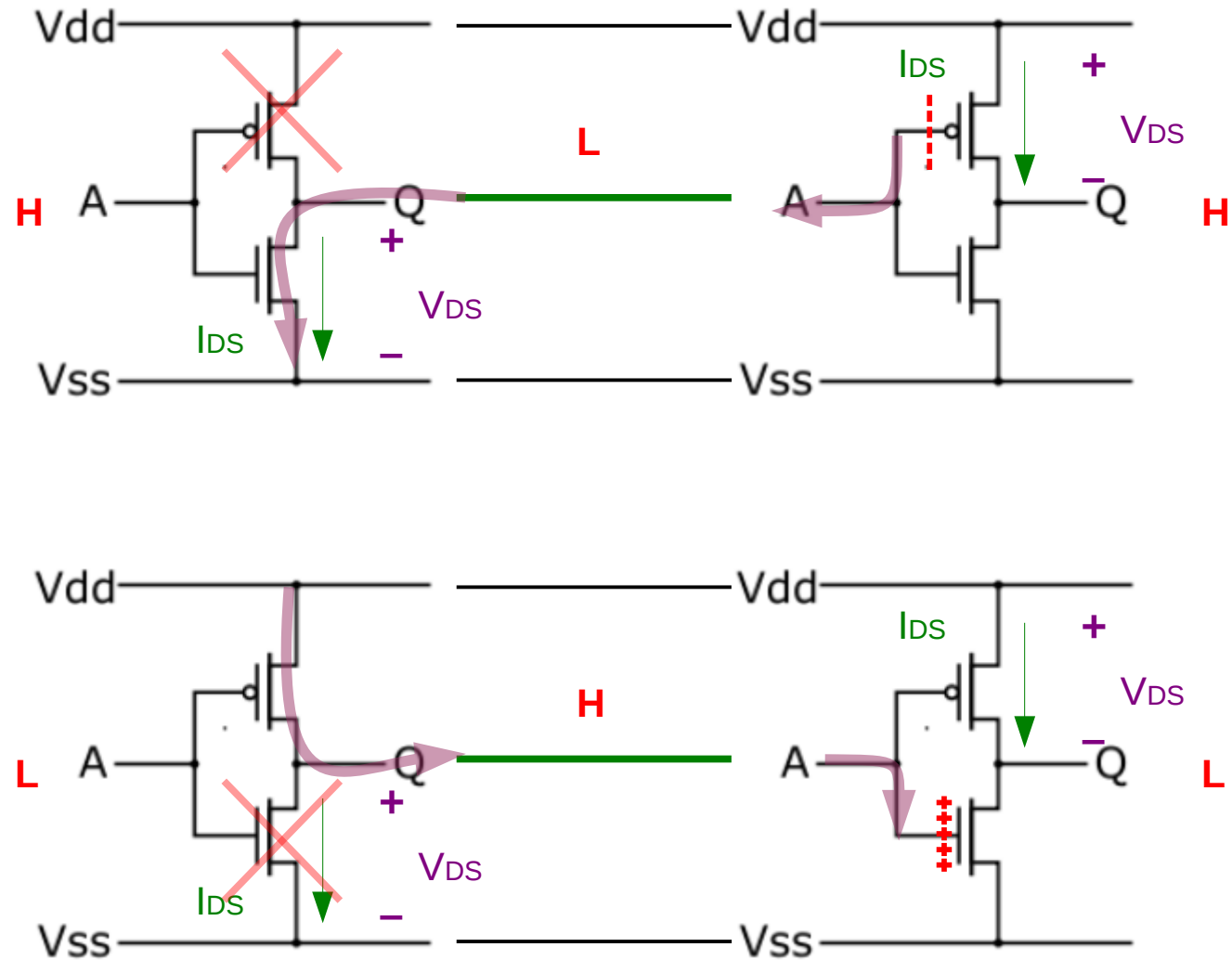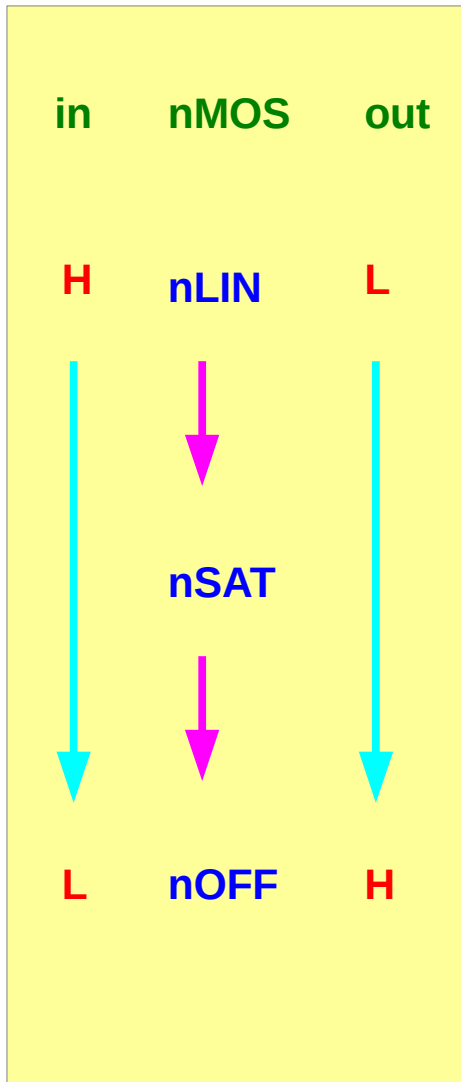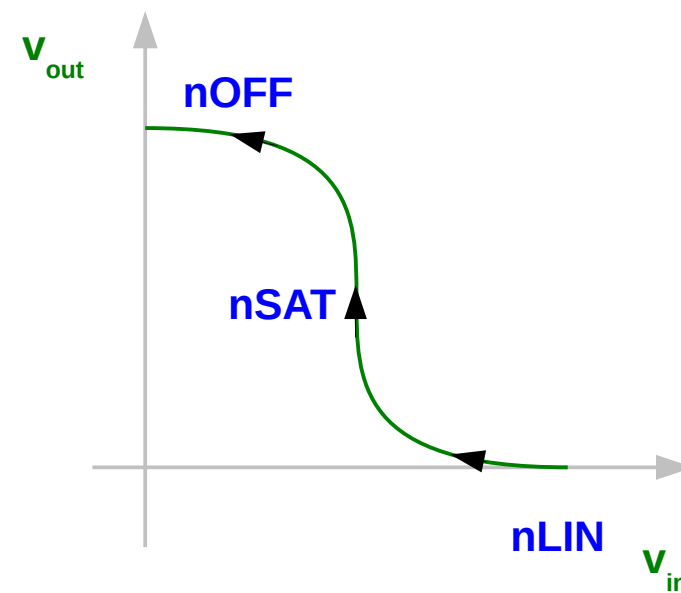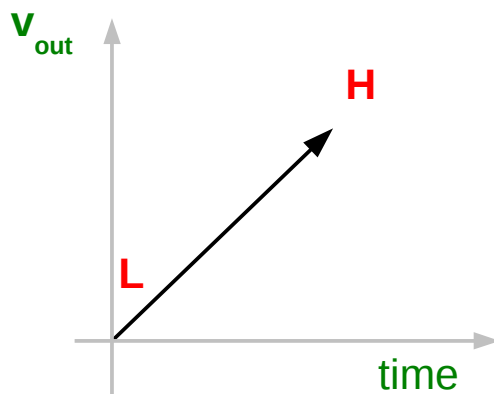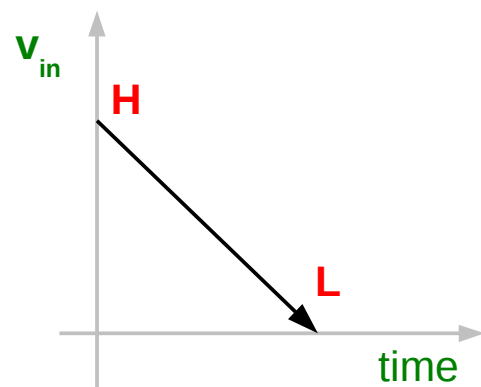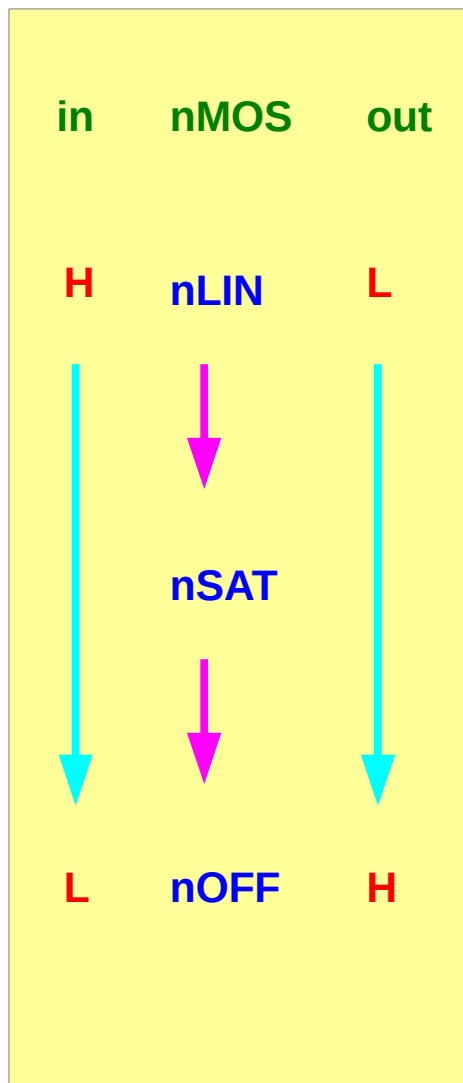
Voltage Transfer Curve (3)
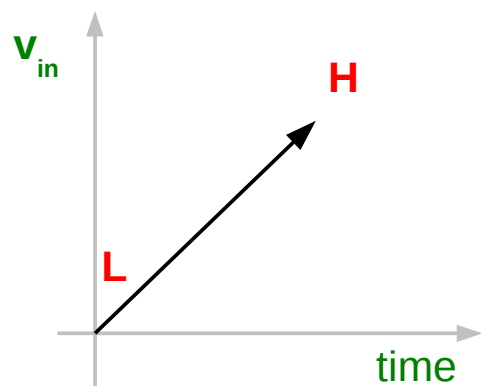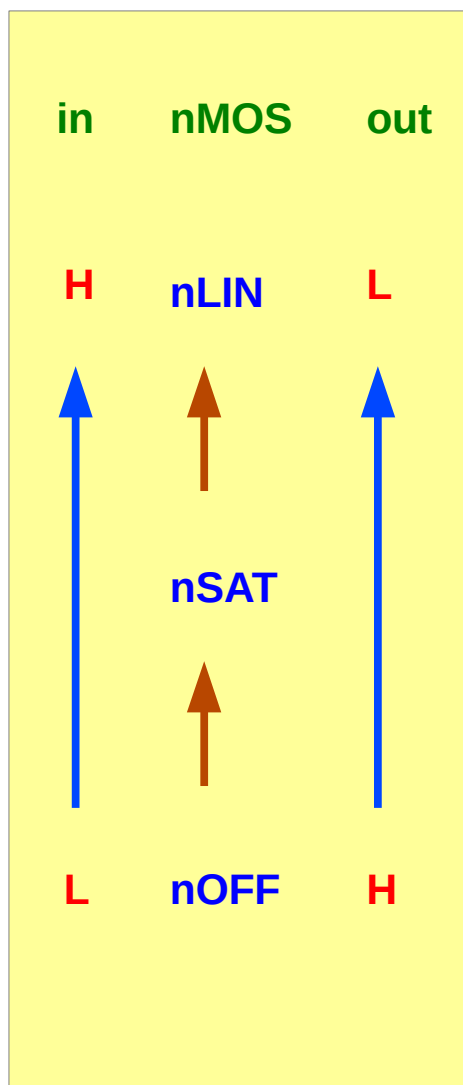
Noise Margin

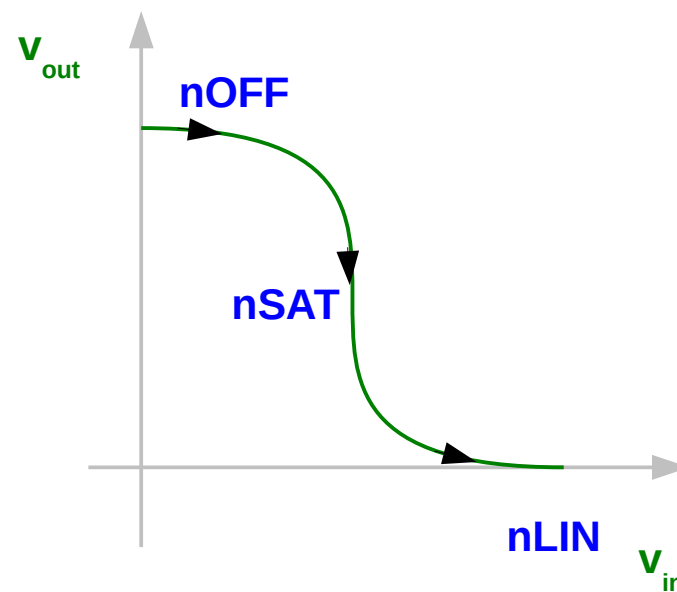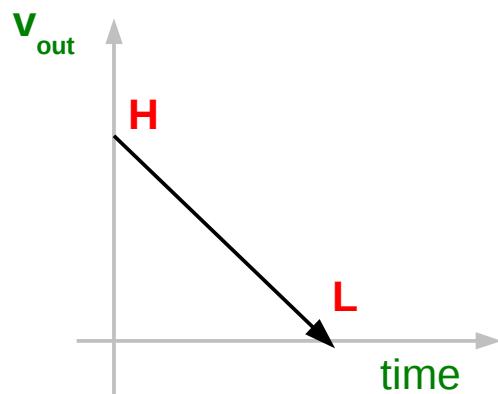# Transconductance Parameter (1)

When $V_{GS} > V_t$ and $V_{DS} < (V_{GS} - V_t)$

$$I_d = k' \frac{W}{L} \left[(v_{gs} - v_t) v_{ds} - \frac{1}{2} v_{ds}^2 \right]$$

When $V_{GS} > V_t$ and $V_{DS} \geq (V_{GS} - V_t)$

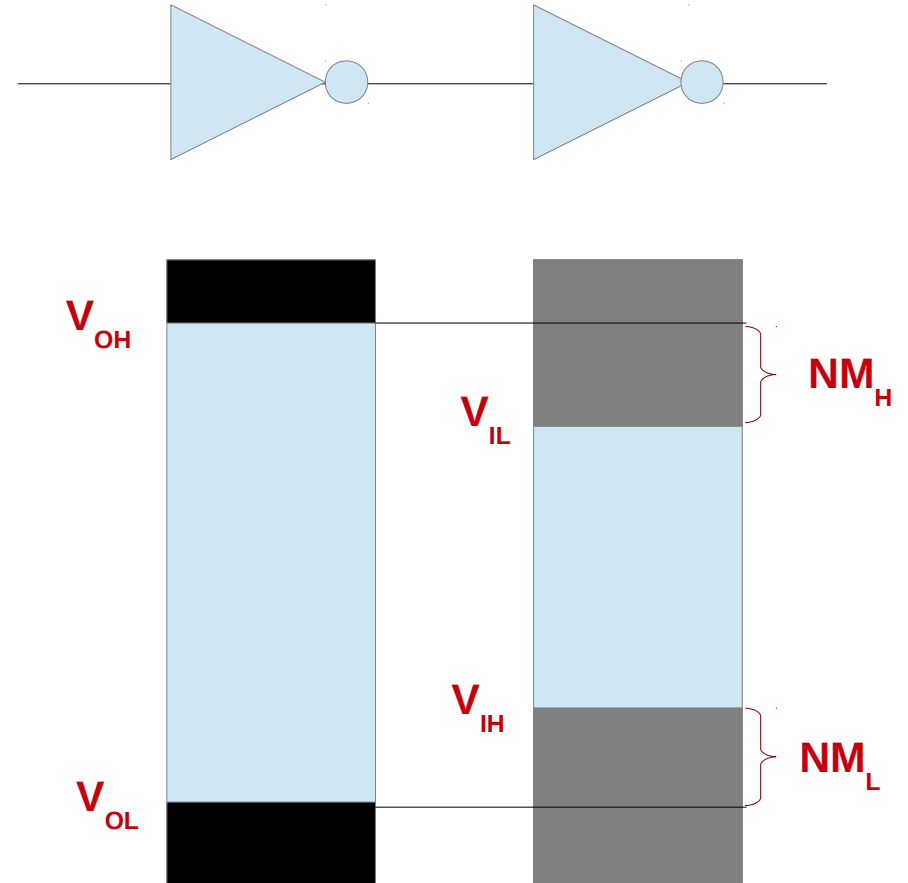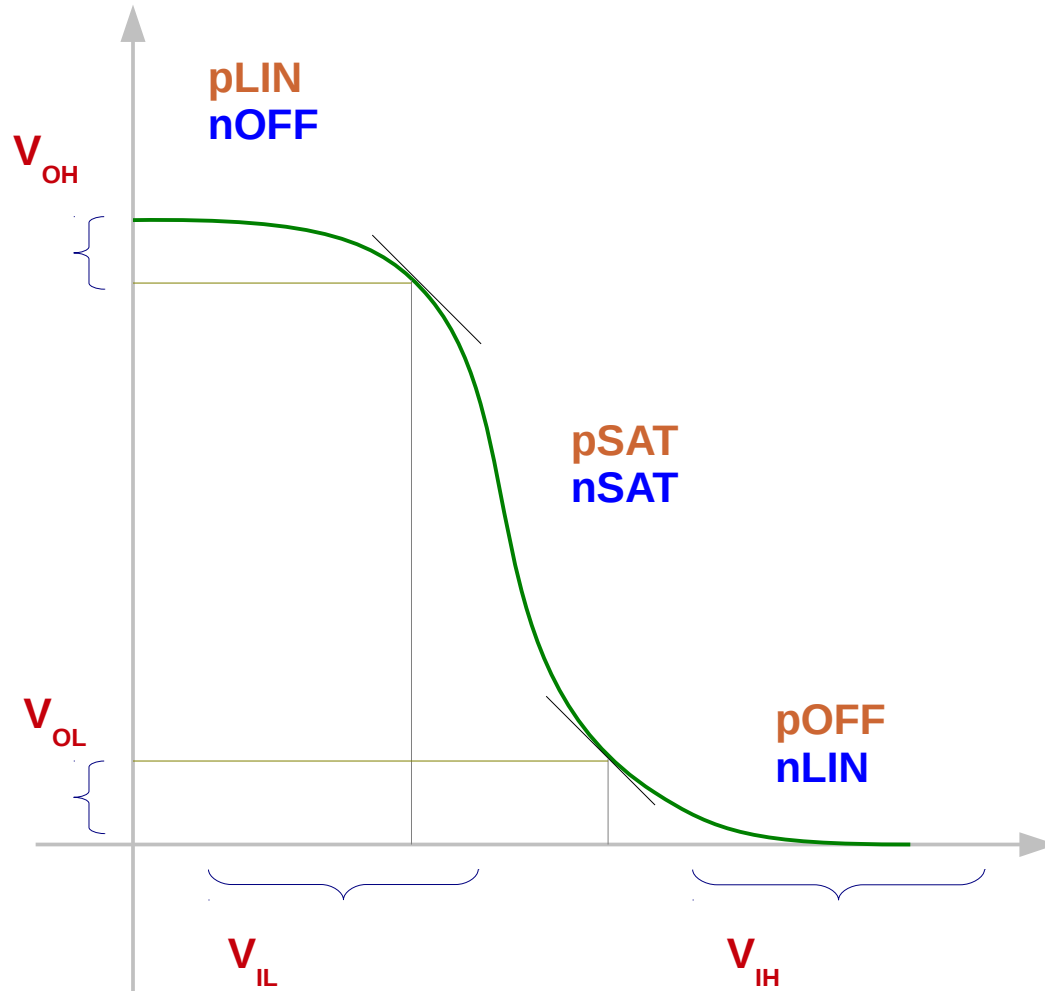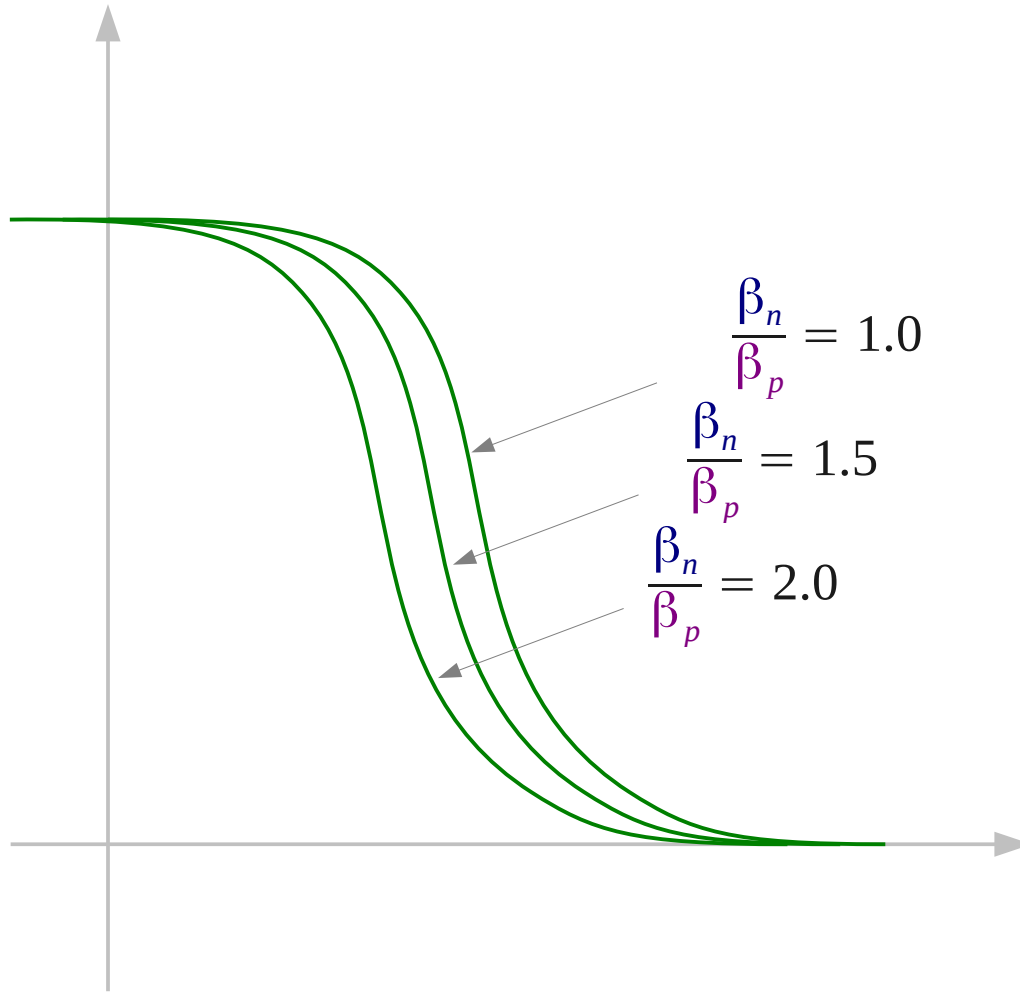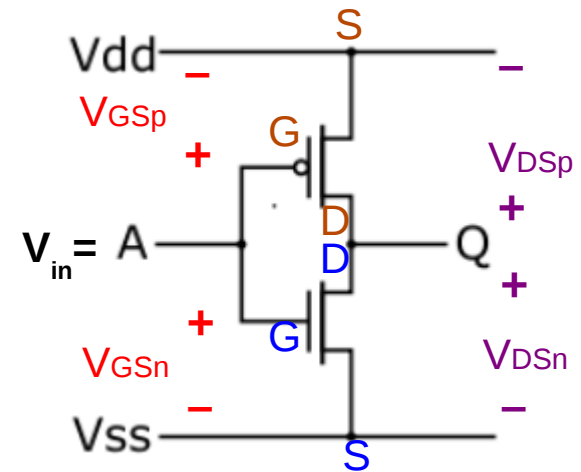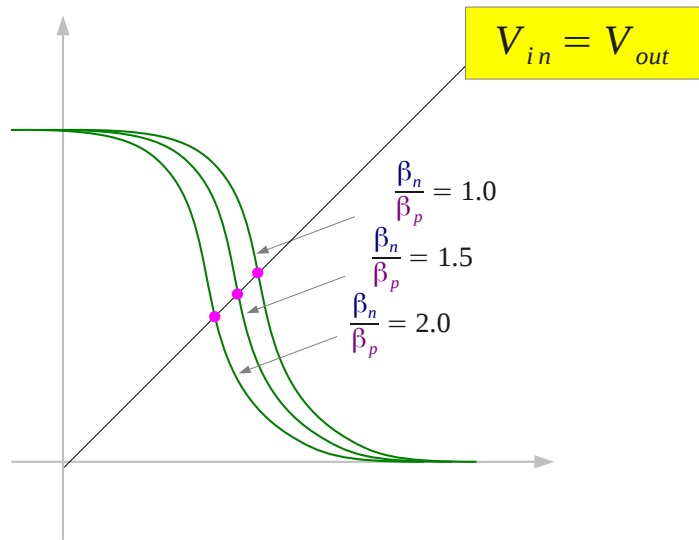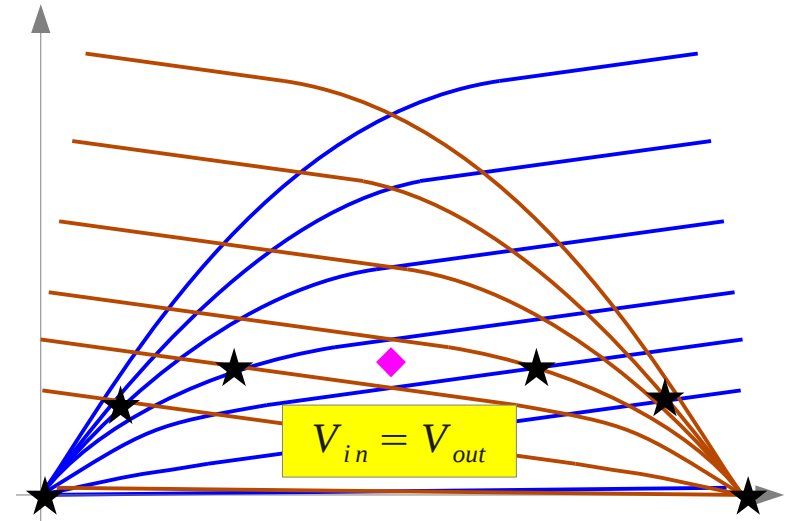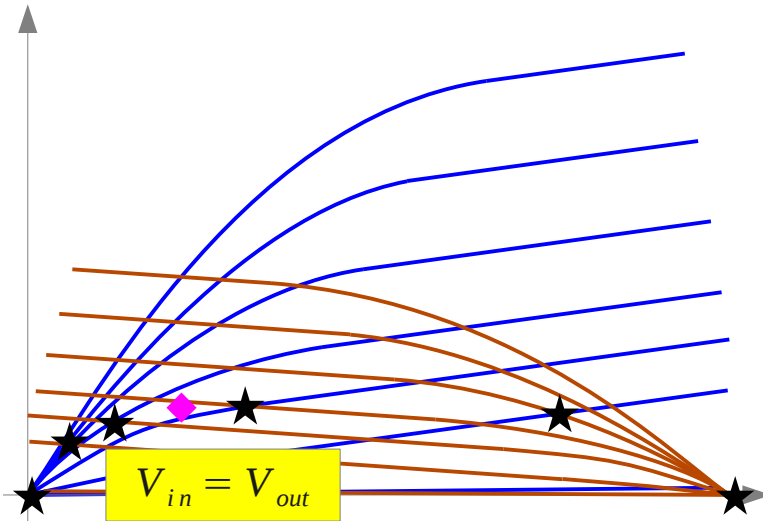$$I_d = \frac{1}{2} k' \frac{W}{L} (v_{gs} - v_t)^2$$

$$\frac{\beta_n}{\beta_p} = 1.0$$

$$\frac{\beta_n}{\beta_p} = 1.5$$

$$\frac{\beta_n}{\beta_p} = 2.0$$

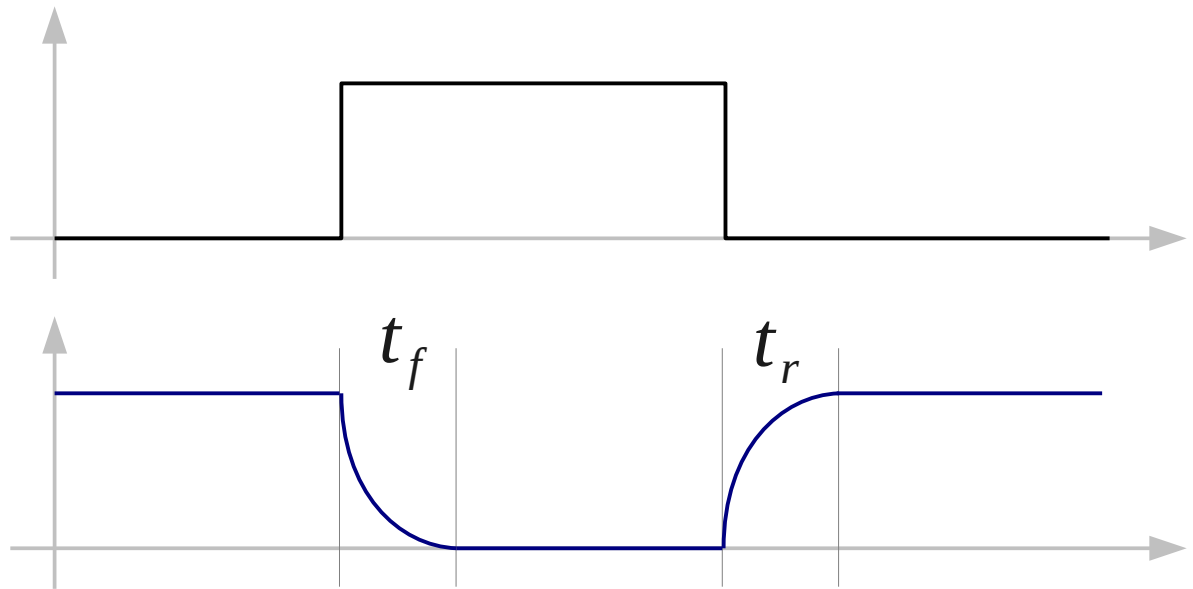$$\beta_p = k'_p \left(\frac{W}{L} \right)_p$$

$$\beta_n = k'_n \left(\frac{W}{L} \right)_n$$

Transconductance Parameter (2)

$V_{in} = V_{out}$

$V_{in} = V_{out}$

$V_{in} = V_{out}$

$\dfrac{\beta_n}{\beta_p} = 1.0$

$\dfrac{\beta_n}{\beta_p} = 1.5$

$\dfrac{\beta_n}{\beta_p} = 2.0$

Vdd

V_{GSp} — +

G

S

−

−

V_{DSp}

+

$V_{in} = $ A

D

Q

+

V_{GSn} + G

Vss

D

V_{DSn}

−

S

Rising and Falling Time

Rising and Falling Time

t_r

Rise Time

t_f

Fall Time

Vdd

L A

Q

+

V_{DS}

I_{DS}

Vss

Vdd

H A

Q

+

V_{DS}

I_{DS}

Vss
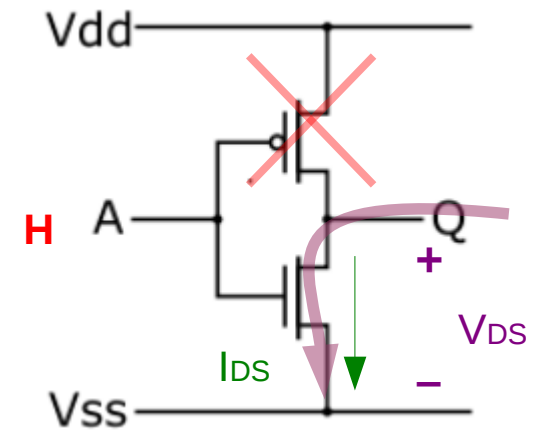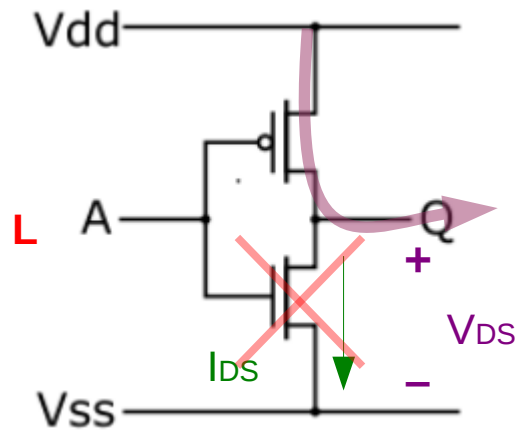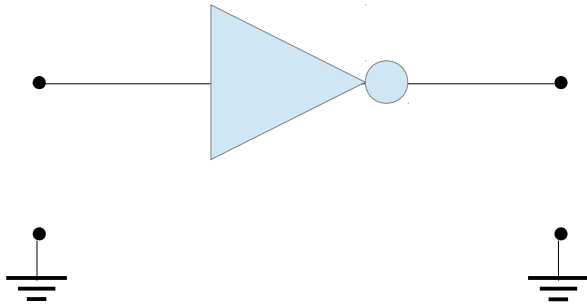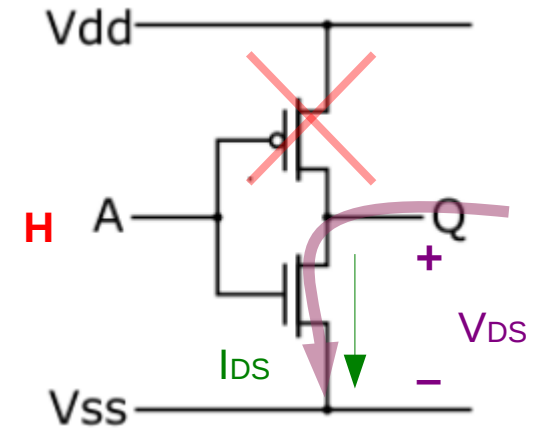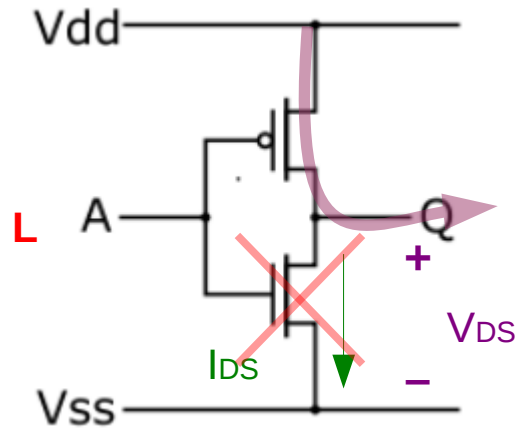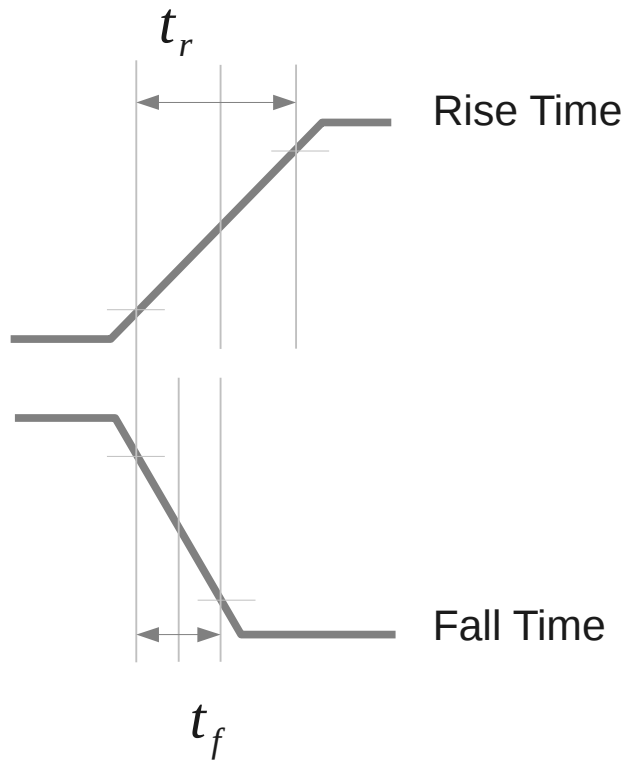
$$\frac{\beta_n}{\beta_p} > 1 \qquad \frac{R_n}{R_p} < 1$$

$$\frac{t_f}{t_r} = \frac{2.2\,\tau_n}{2.2\,\tau_p} \qquad \frac{\tau_n}{\tau_p} = \frac{R_n C_{out}}{R_p C_{out}} = \frac{R_n}{R_p} < 1$$

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Propagation Delay

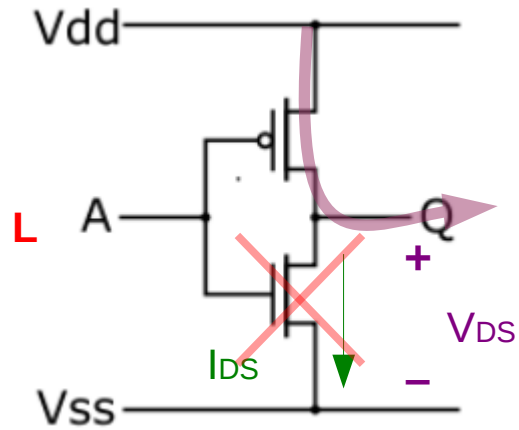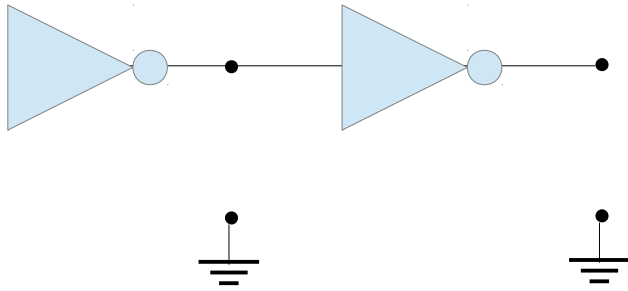t_{pdf}

t_{pdr}
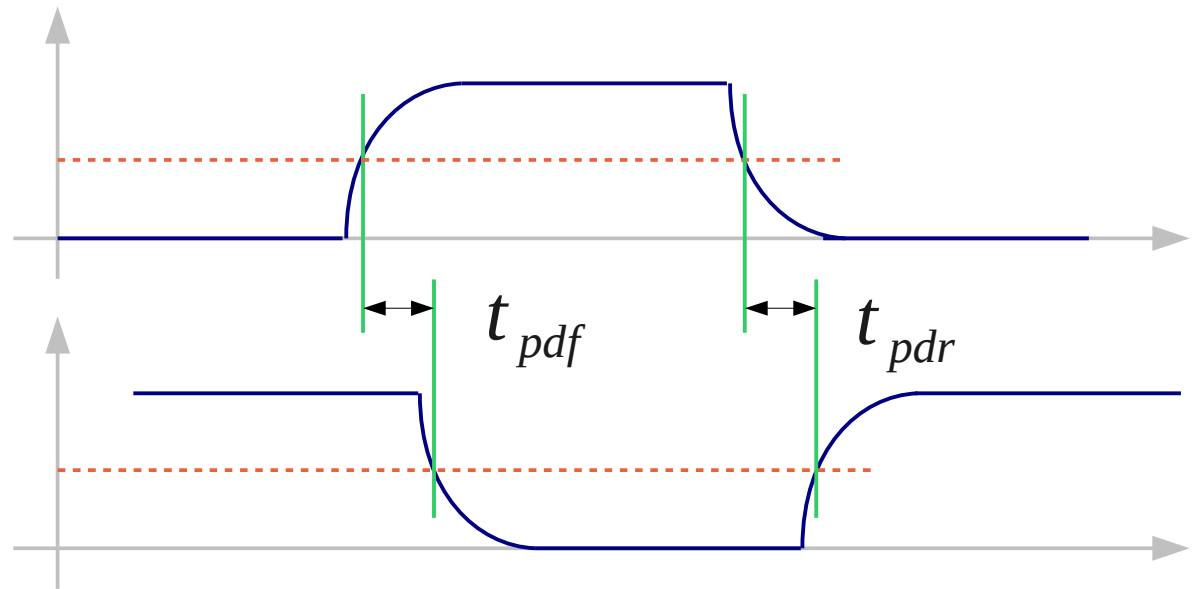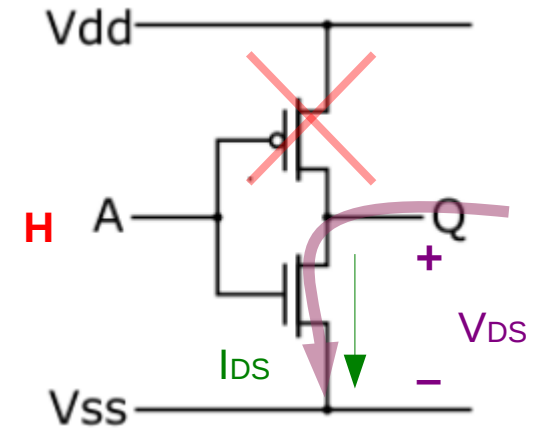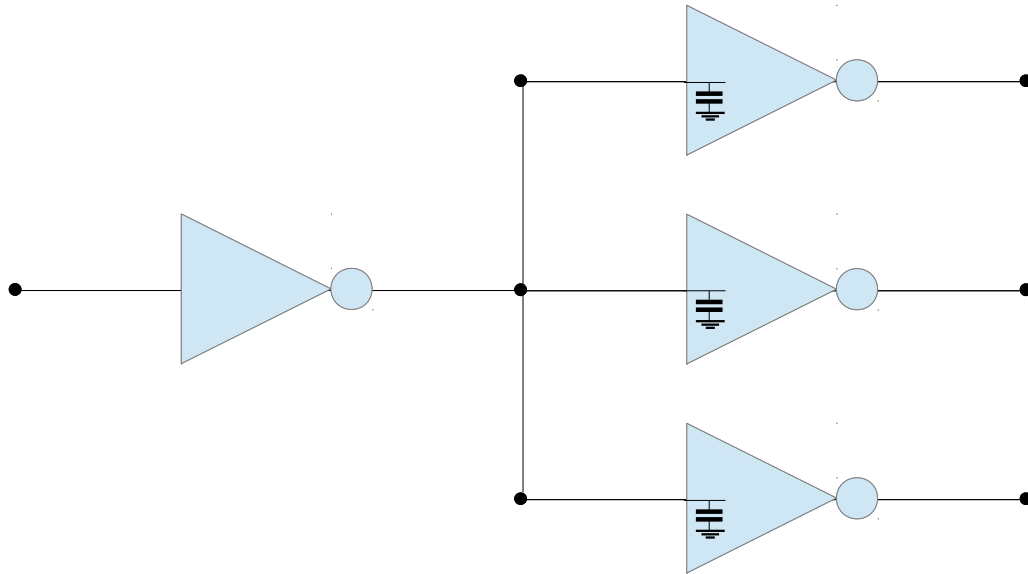
Load Capacitance

$$C_{in} = 3\,C_g$$

Big Capacitance

- A signal connected off-chip
- A signal with very long wire
- A clock signal driving many flip-flops

Characteristic Curve

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References

[1] http://en.wikipedia.org/
[2] http://www.allaboutcircuits.com/
[3] W. Wolf, "Modern VLSI Design : Systems on Silicon
[4] N. Weste, D. Harris, "CMOS VLSI Design: A Circuits and Systems Perspective"
[5] J. P. Uyemura, "Introduction to VLSI Circuits and Systems"