CMOS Transistor & Layout

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4/8/13

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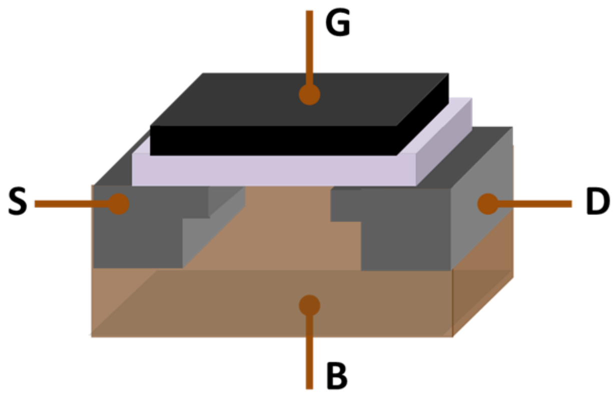
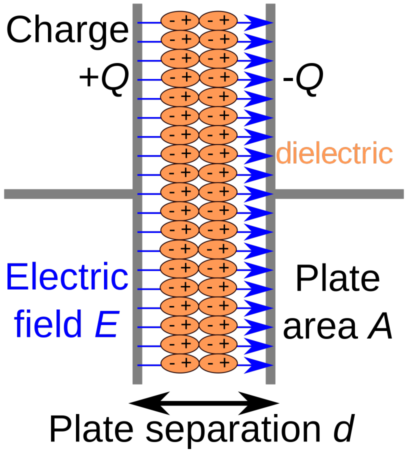
MOSFET

The metal–oxide–semiconductor field-effect transistor
a transistor used for amplifying or switching electronic signals
usually, the body (or substrate) is connected to the source

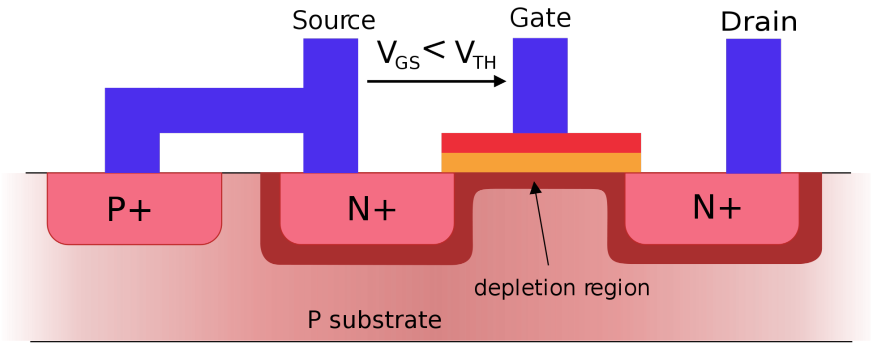


MOSFET showing gate (G), body (B), source (S) and drain (D) terminals. The gate is separated from the body by an insulating layer (white)



Charge separation in a parallel-plate capacitor causes an internal electric field. A dielectric (orange) reduces the field and increases the capacitance.

Metal & Oxide

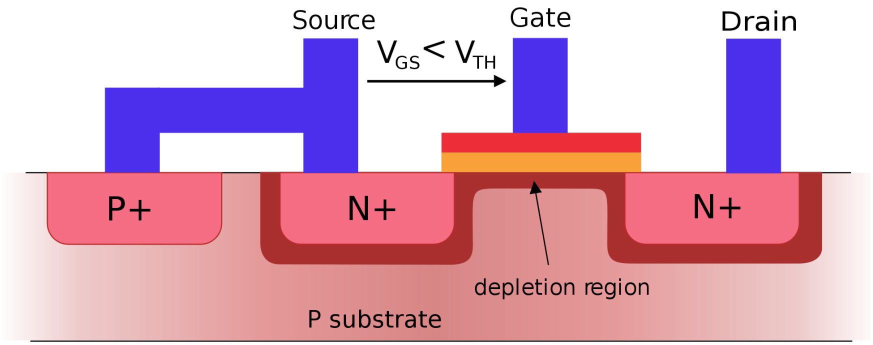


The 'metal' in the name MOSFET is now often a misnomer because the previously metal gate material is now often a layer of polysilicon (polycrystalline silicon). Aluminium had been the gate material until the mid 1970s, when polysilicon became dominant, due to its capability to form self-aligned gates. Metallic gates are regaining popularity, since it is difficult to increase the speed of operation of transistors without metal gates.

the 'oxide' in the name can be a misnomer, as different dielectric materials are used with the aim of obtaining strong channels with applied smaller voltages.

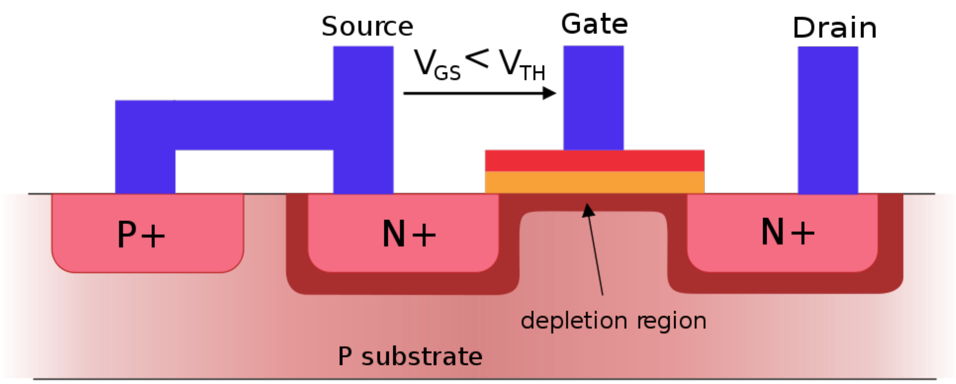
The traditional metal–oxide–semiconductor (MOS) structure is obtained by growing a layer of silicon dioxide (SiO2) on top of a silicon substrate and depositing a layer of metal or polycrystalline silicon (the latter is commonly used). As the silicon dioxide is a dielectric material, its structure is equivalent to a planar capacitor, with one of the electrodes replaced by a semiconductor. When a voltage is applied across a MOS structure, it modifies the distribution of charges in the semiconductor

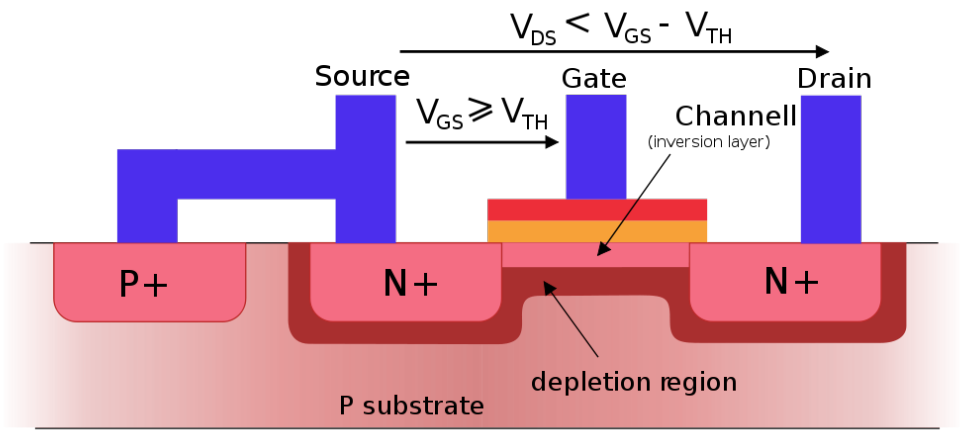
MOSFET : below threshold



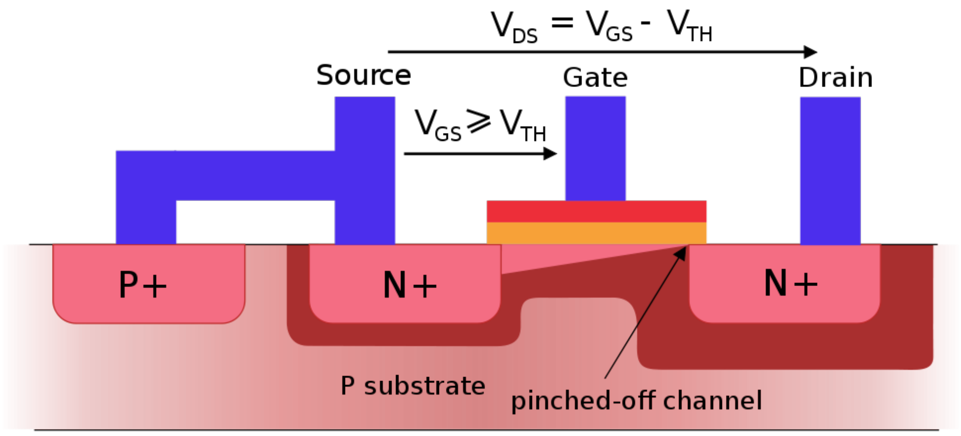
when the gate voltage VGS is below the threshold for making a conductive channel; there is little or no conduction between the terminals source and drain; the switch is off. When the gate is more positive, it attracts electrons, inducing an n-type conductive channel in the substrate below the oxide, which allows electrons to flow between the n-doped terminals; the switch is on.

MOSFET: Modes of Operation (1)

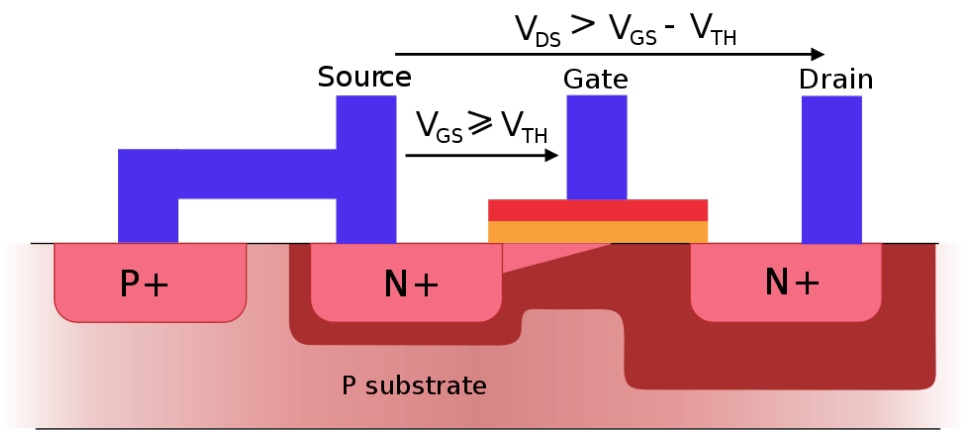




Linear operating region (ohmic mode)



Saturation mode at point of pinch-off



Saturation mode

MOSFET: Modes of Operation (2)

Cutoff, subthreshold, or weak-inversion mode

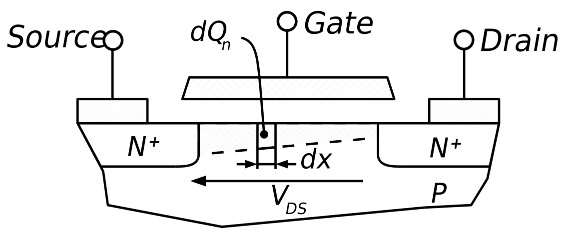
When VGS < Vth:

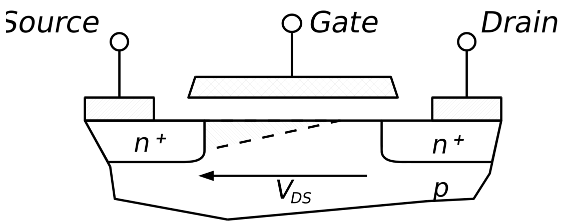
Triode mode or linear region (the ohmic mode)

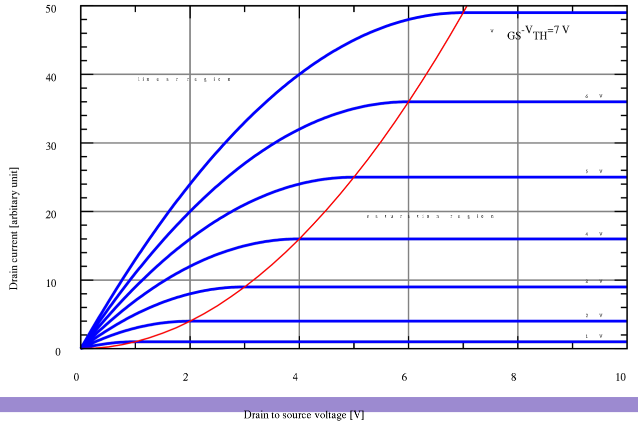
When VGS > Vth and VDS < (VGS – Vth)

Saturation or active mode

When VGS > Vth and VDS ≥ (VGS – Vth)







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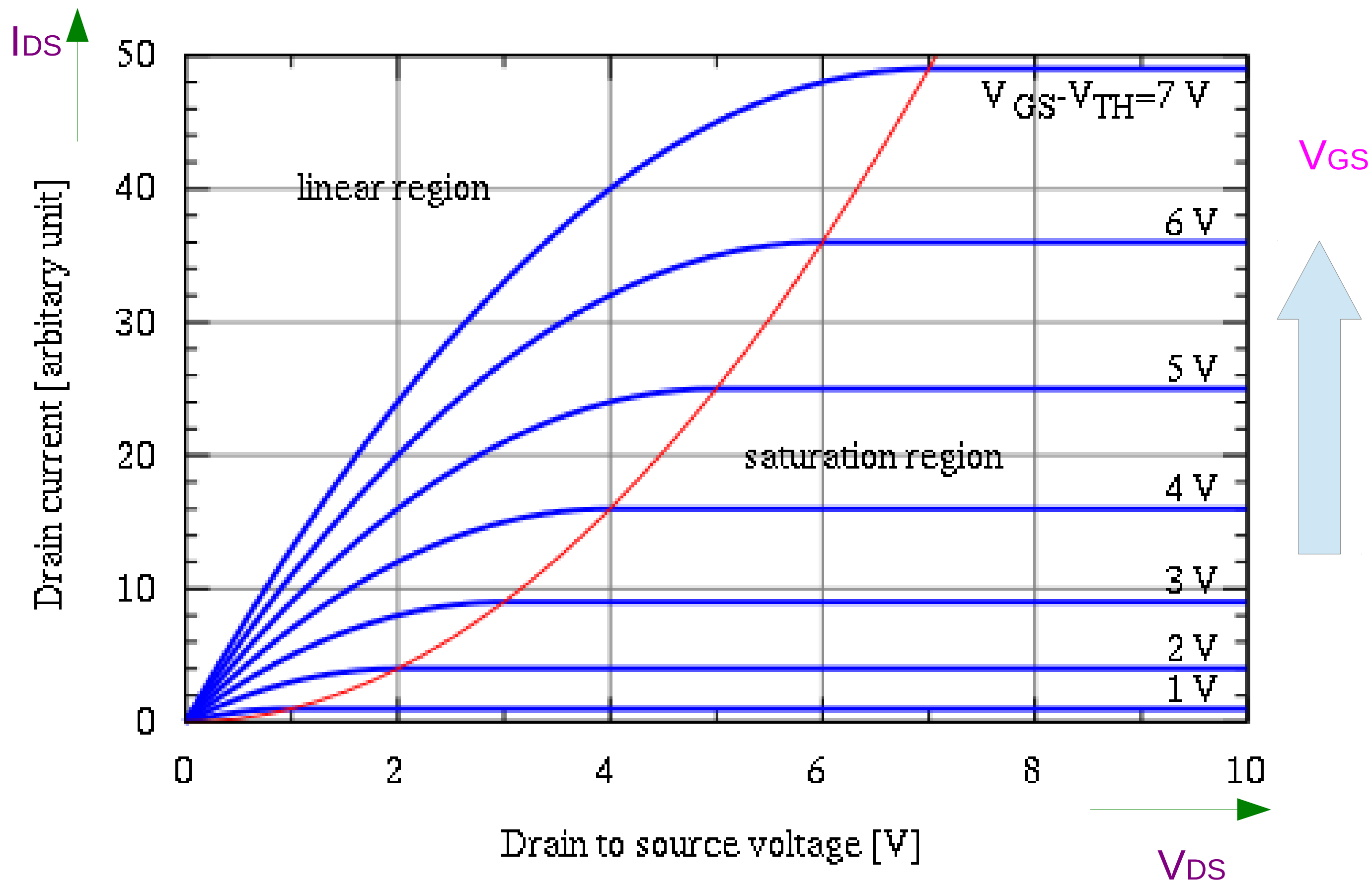
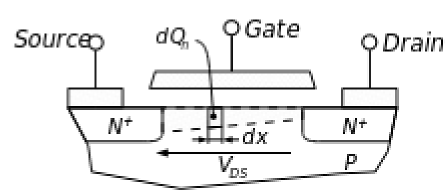
MOSFET: Modes of Operation (3)

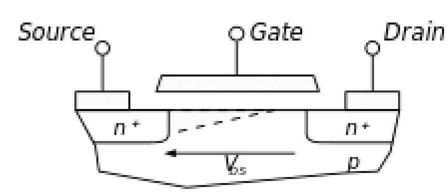
Cutoff
VGS < Vth:

Linear region
VGS > Vth and
VDS < (VGS – Vth)

Saturation
VGS > Vth and
VDS ≥ (VGS – Vth)





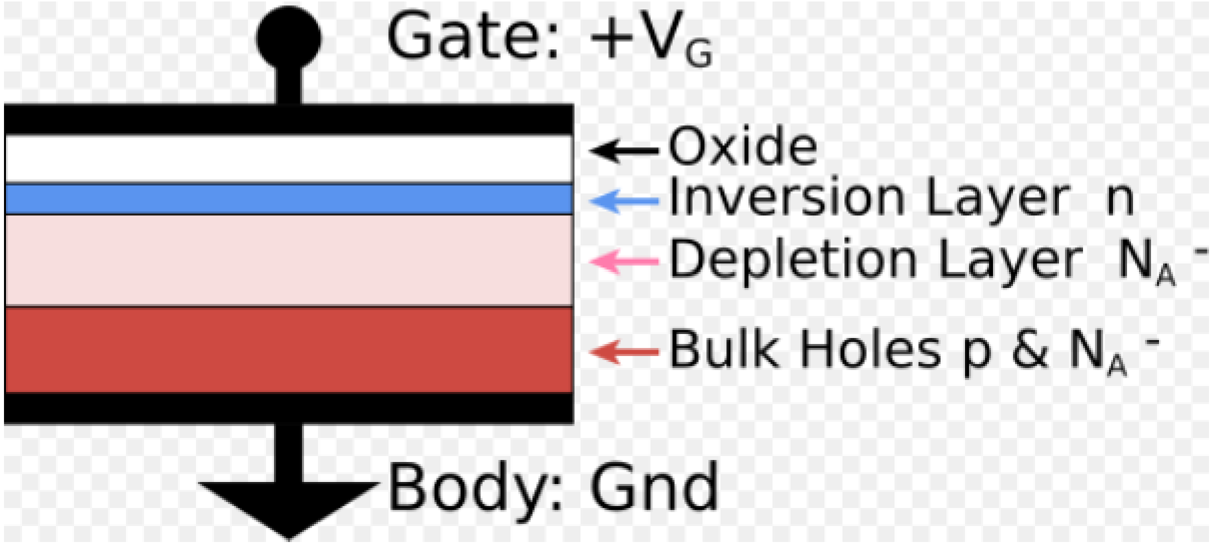


Depletion Region (1)

Suppose that the semiconductor initially is charge neutral, with the charge due to holes exactly balanced by the negative charge due to acceptor doping impurities.

If a positive voltage now is applied to the gate, which is done by introducing positive charge Q to the gate, then some positively charged holes in the semiconductor nearest the gate are repelled by the positive charge on the gate, and exit the device through the bottom contact.

They leave behind a **depleted region** that is insulating because no mobile holes remain; only the immobile, negatively charged acceptor impurities.

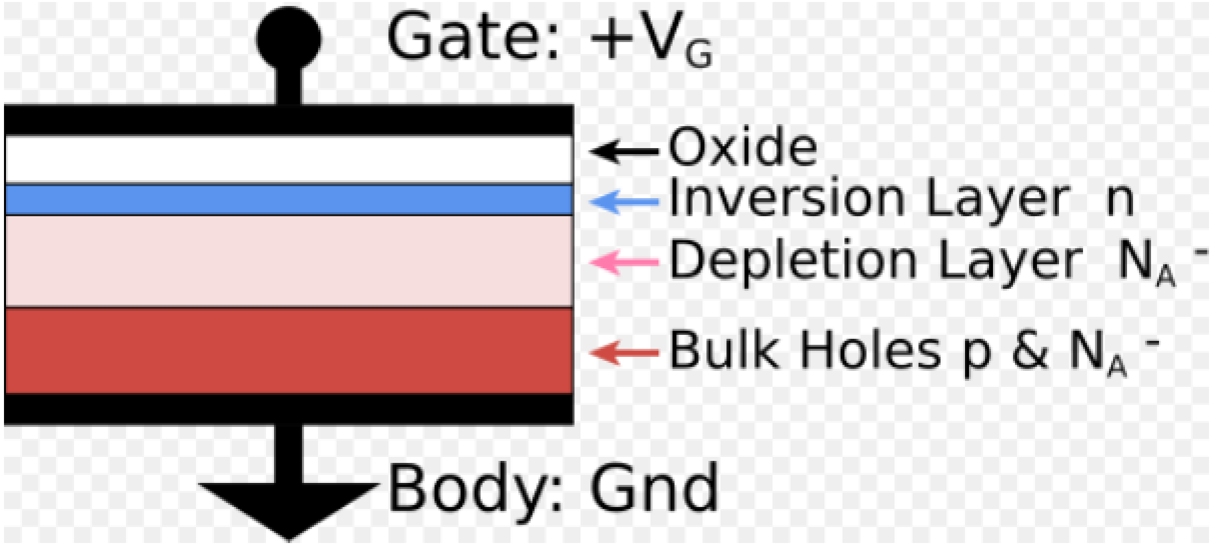


Depletion Region (2)

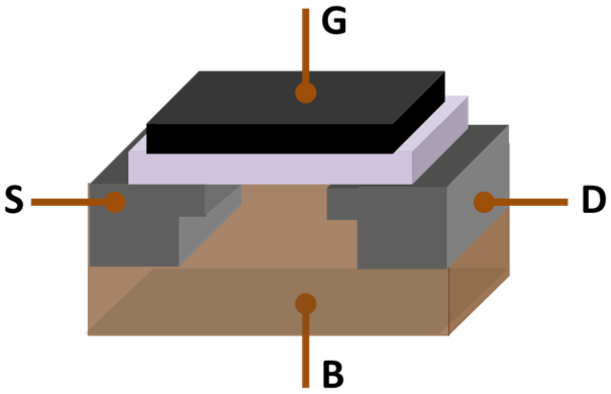
The greater the positive charge placed on the gate, the more positive the applied gate voltage, and the more holes that leave the semiconductor surface, enlarging the depletion region.

(In this device there is a limit to how wide the depletion width may become. It is set by the onset of an inversion layer of carriers in a thin layer, or channel, near the surface. The above discussion applies for positive voltages low enough that an inversion layer does not form.)

If the gate material is polysilicon of opposite type to the bulk semiconductor, then a spontaneous depletion region forms if the gate is electrically shorted to the substrate, in much the same manner as described for the p–n junction above.



Enhancement, Depletion Mode MOSFET



The metal–oxide–semiconductor field-effect transistor
a transistor used for amplifying or switching electronic signals
usually, the body (or substrate) is connected to the source

enhancement mode
a voltage drop across the oxide induces
a conducting channel (field effect)
the increase of conductivity with increase in oxide field
that accumulates carriers to the channel - the inversion layer.
nMOS : the channel of electrons (with p-type substrate)
pMOS the channel of holes (with n-type substrate)

depletion mode
the channel consists of carriers in a surface impurity layer of opposite type to the substrate
conductivity is decreased by application of a field that depletes carriers from this surface layer

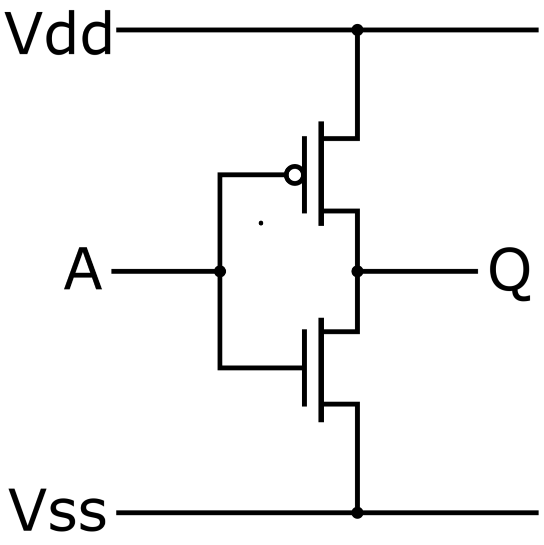
MOSFET Symbols

Enhancement pMOS

Enhancement nMOS

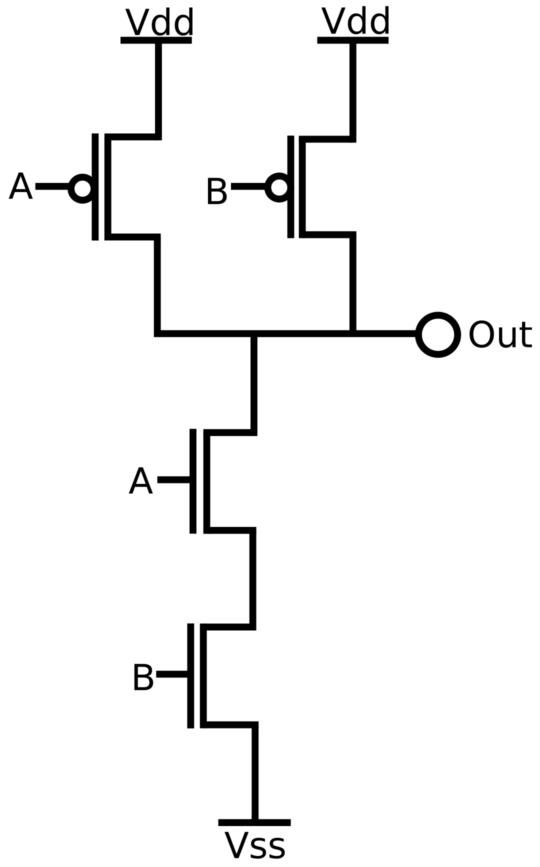
CMOS

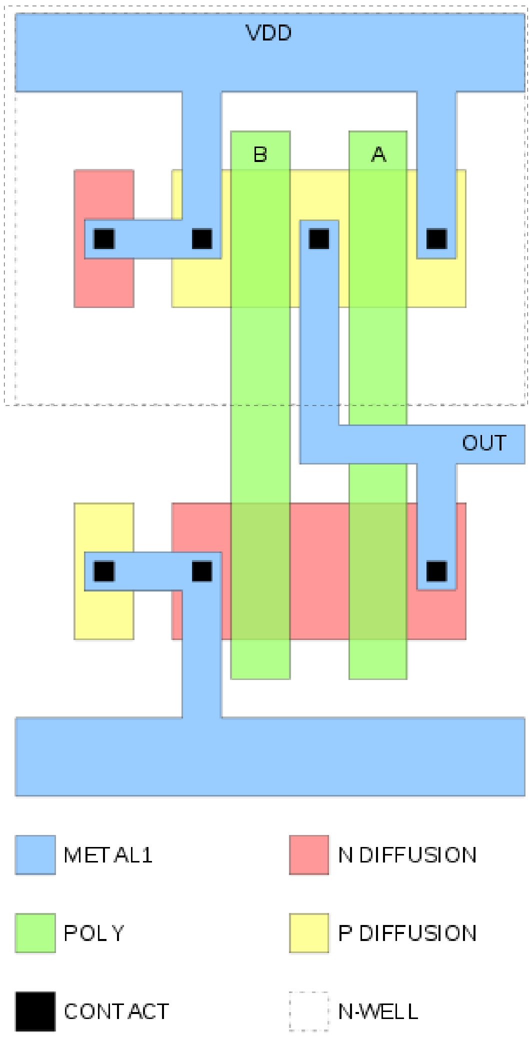
Complementary metal–oxide–semiconductor (CMOS) is a technology for constructing integrated circuits. CMOS technology is used in microprocessors, microcontrollers, static RAM, and other digital logic circuits. CMOS technology is also used for several analog circuits such as image sensors (CMOS sensor), data converters, and highly integrated transceivers for many types of communication.



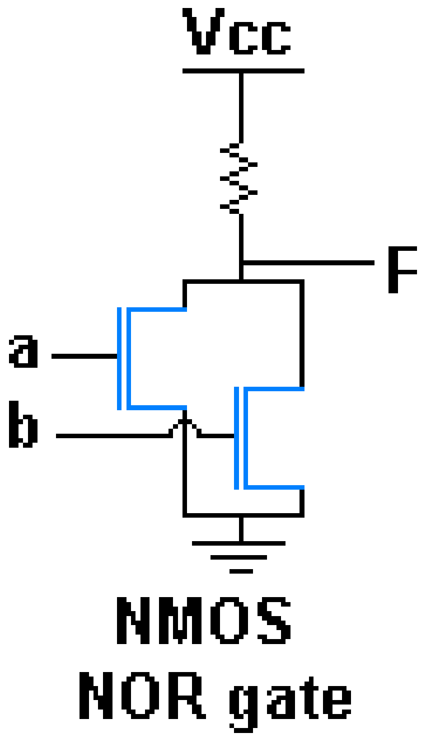
The words "complementary-symmetry" refer to the fact that the typical digital design style with CMOS uses complementary and symmetrical pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) for logic functions.

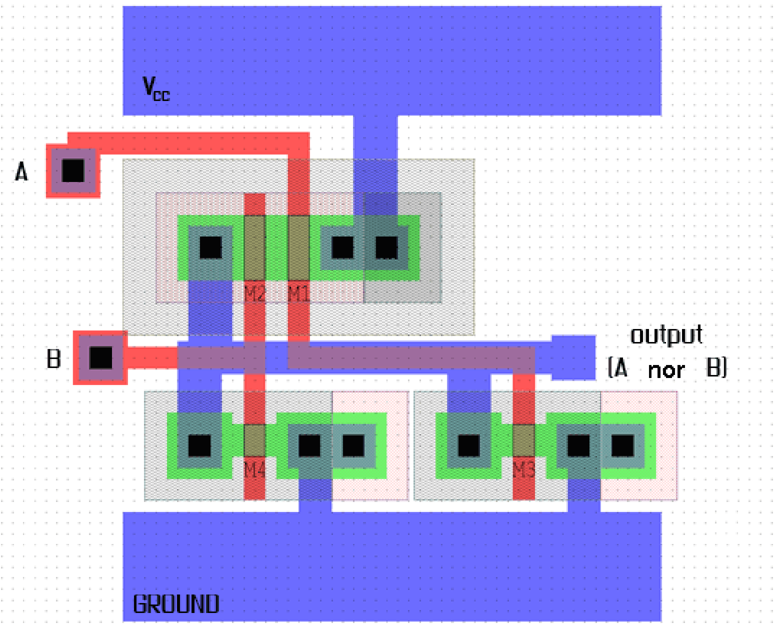
NAND Gate


Vdd
Vdd
A
B
Out
A
B
Vss


VDD
B
A
OUT
METAL1
N DIFFUSION
POLY
P DIFFUSION
CONTACT
N-WELL

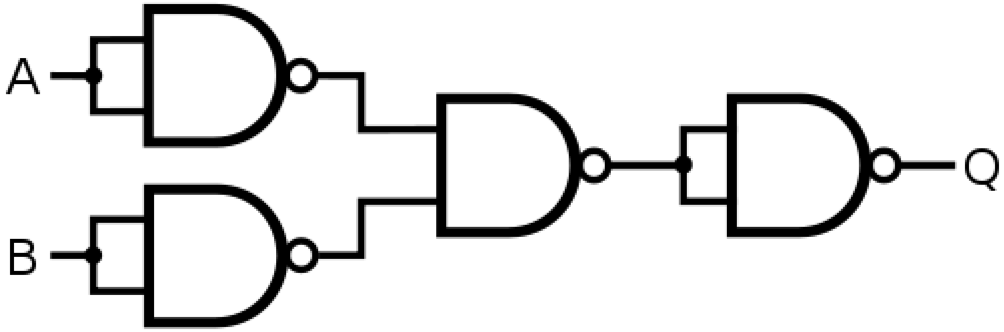
NOR Gate

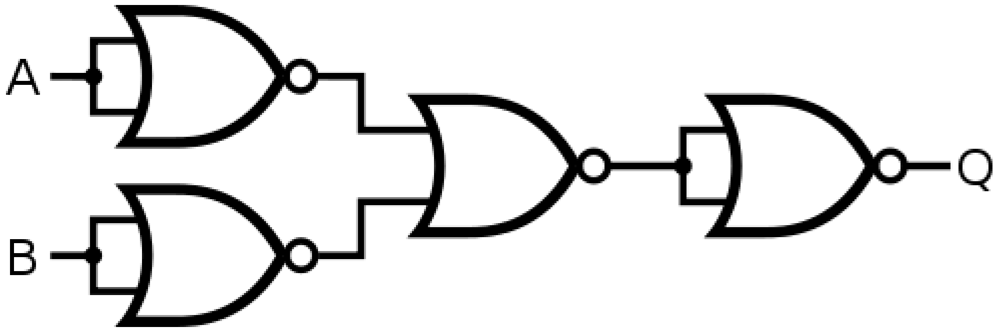




CMOS NOR ?

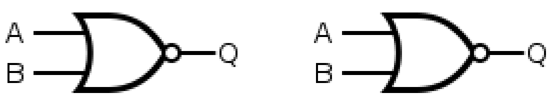
NOR and NAND Combinations



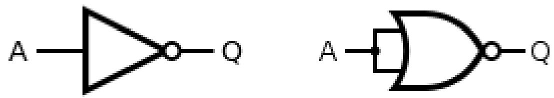


NOR Based Logic

Desired Gate **NOR Construction**



Desired Gate **NOR Construction**



Desired Gate **NOR Construction**

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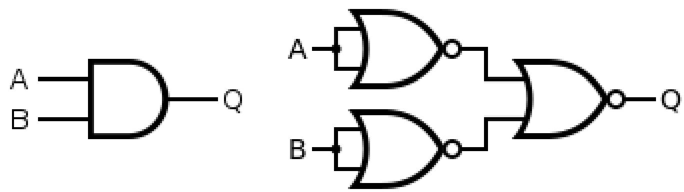
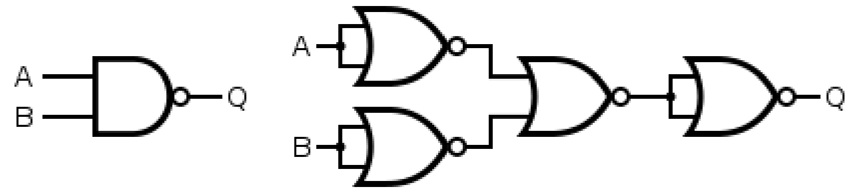


Desired Gate **NOR Construction**



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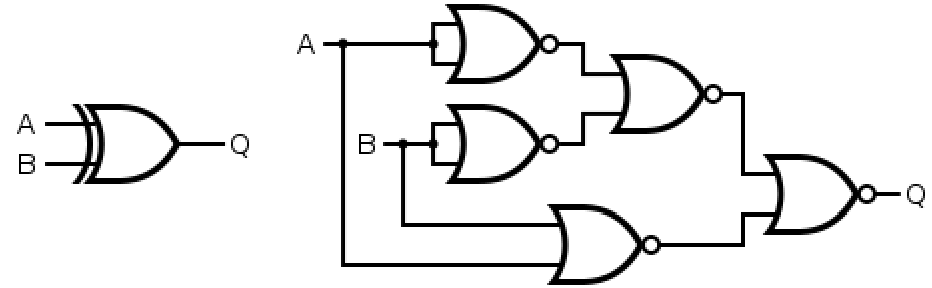
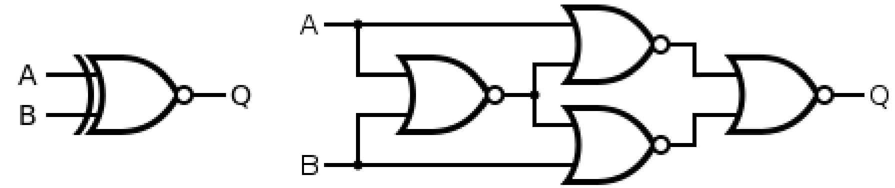


Desired Gate **NOR Construction**



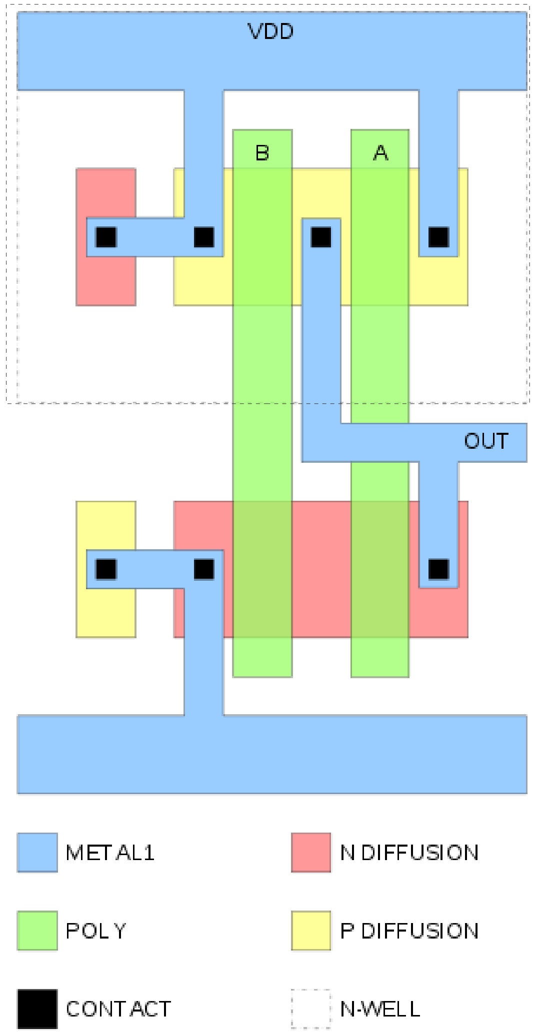
NAND Gate Layout View

a "bird's eye view" of a stack of layers.
the circuit is constructed **on** a P-type substrate
the polysilicon, diffusion, and n-well : base layers - actually inserted into trenches of the P-type substrate
the contacts penetrate an insulating layer between the base layers and the first layer of metal (metal1)

The **inputs (A, B)** to the NAND (green) are in polysilicon.
The CMOS transistors are formed
by the intersection of the polysilicon and *diffusion*
    N diffusion for the N device (salmon)
    P diffusion for the P device (yellow)

the **output (out)** is connected together in metal (cyan)

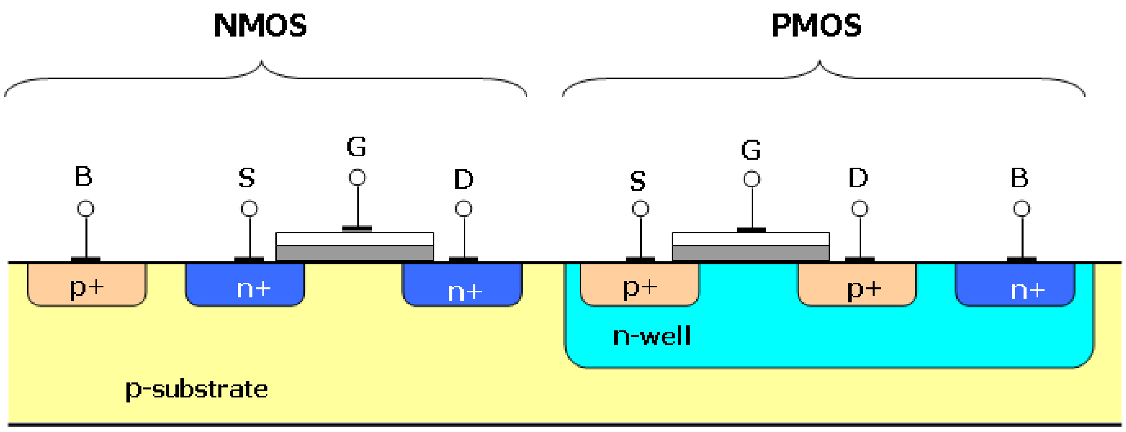
Connections between metal and polysilicon or *diffusion*
are made through **contacts** (black)

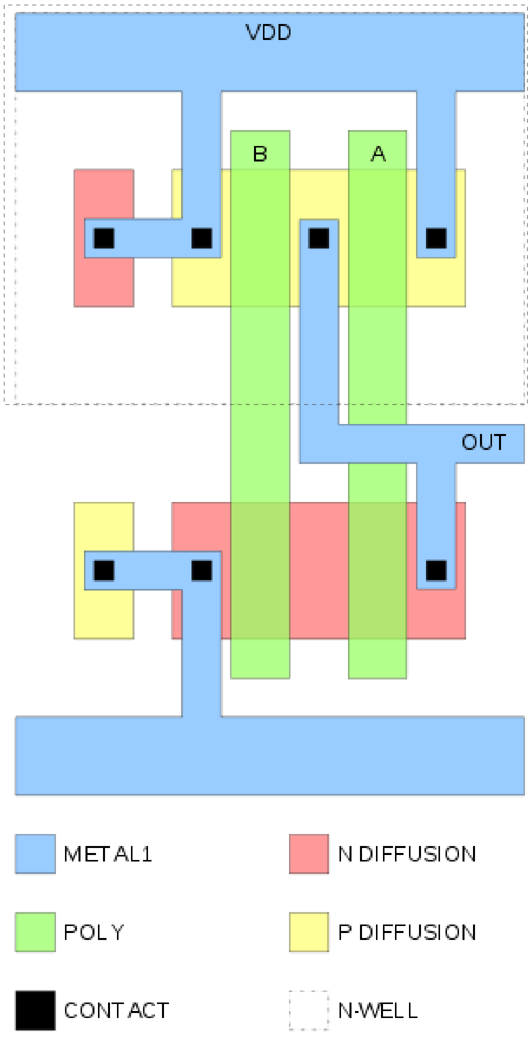


NAND Gate Cross Section View

the N device is manufactured on a P-type substrate
the P device is manufactured in an N-type well (n-well).

to prevent latchup
    a P-type substrate tap is connected to VSS
    an N-type n-well tap is connected to VDD





Dielectric

References

[1] http://en.wikipedia.org/
[2] http://planetmath.org/
[3] M.L. Boas, “Mathematical Methods in the Physical Sciences”