

CMOS Processing Technology

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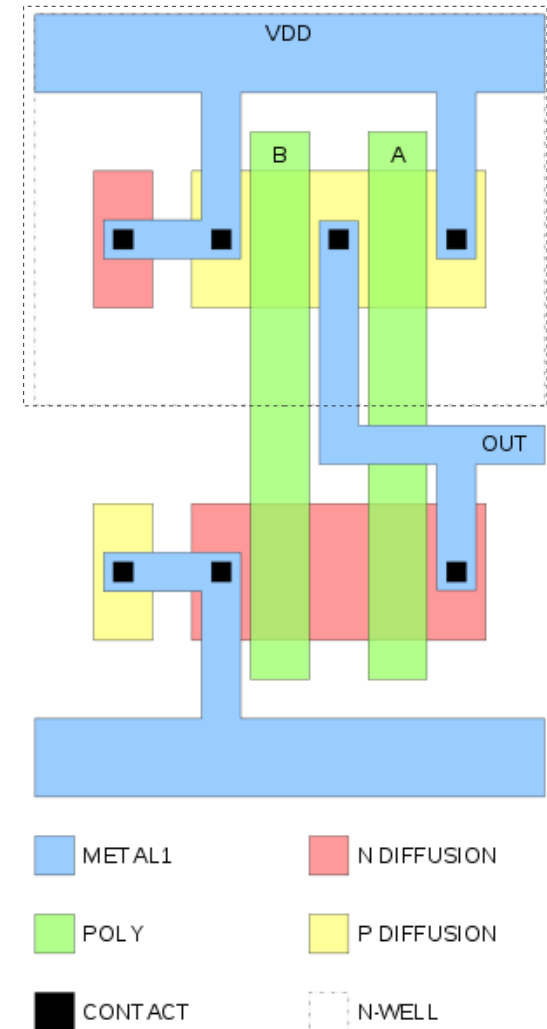
NAND Gate Layout View

a "bird's eye view" of a stack of layers.
the circuit is constructed **on a P-type substrate**
the polysilicon, diffusion, and n-well : **base layers** - actually **inserted** into trenches of the P-type substrate
the **contacts** penetrate an insulating layer between the **base layers** and the **first layer of metal** (metal1)

The **inputs (A, B)** to the NAND (green) are in **polysilicon**.
The CMOS transistors are formed
by the **intersection** of the **polysilicon** and *diffusion*
N diffusion for the N device (salmon)
P diffusion for the P device (yellow)

the **output (out)** is connected together in **metal** (cyan)

Connections between **metal** and **polysilicon** or *diffusion*
are made through **contacts** (black)

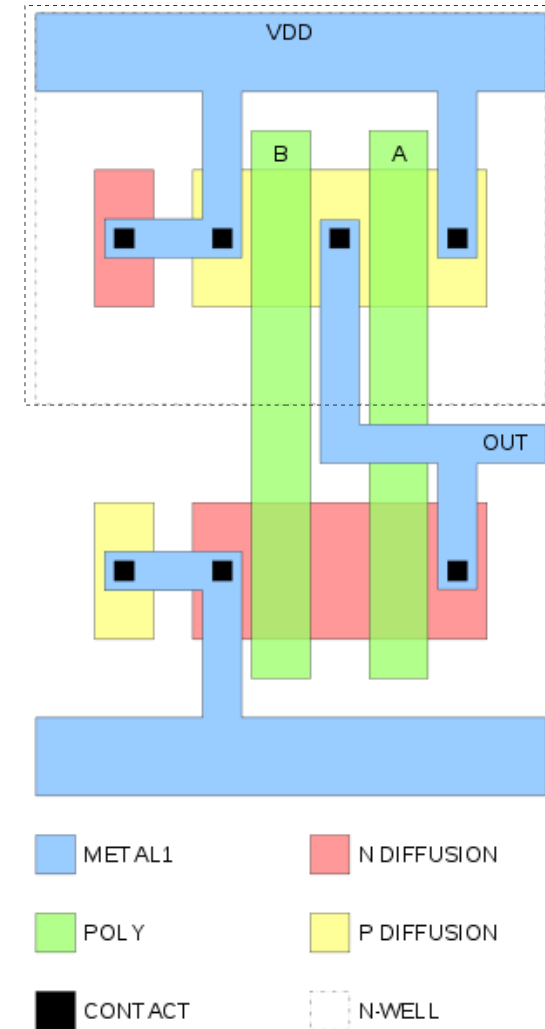
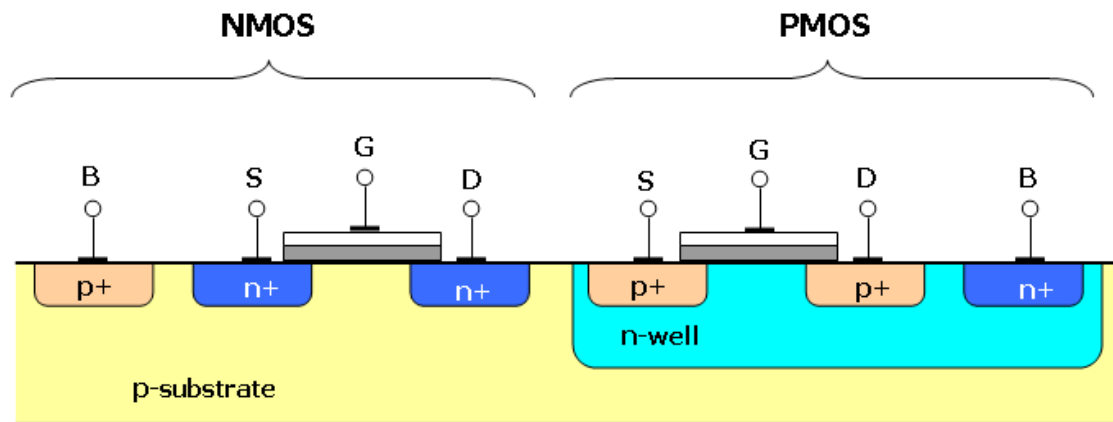


NAND Gate Cross Section View

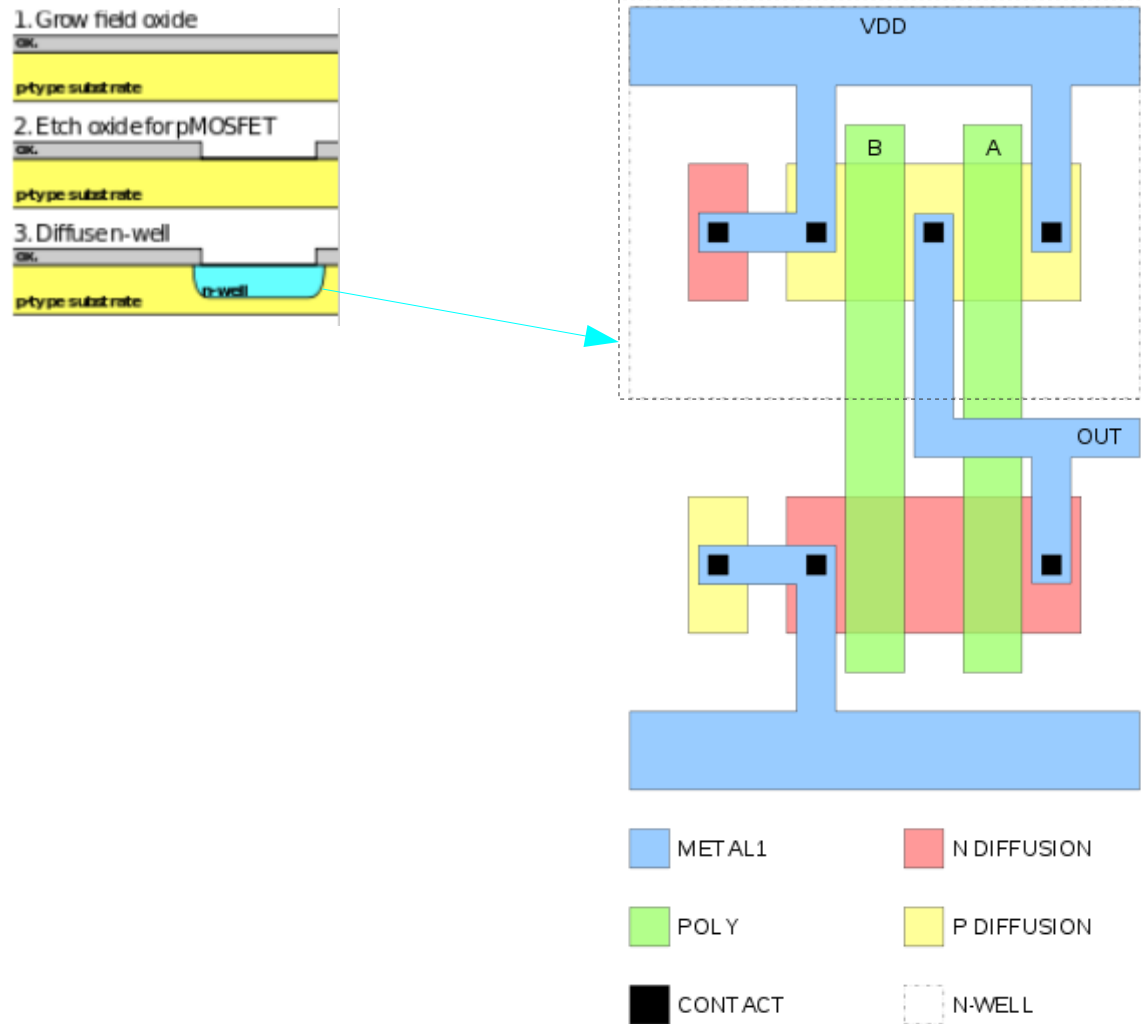
the N device is manufactured on a P-type substrate
the P device is manufactured in an N-type well (n-well).

to prevent latchup

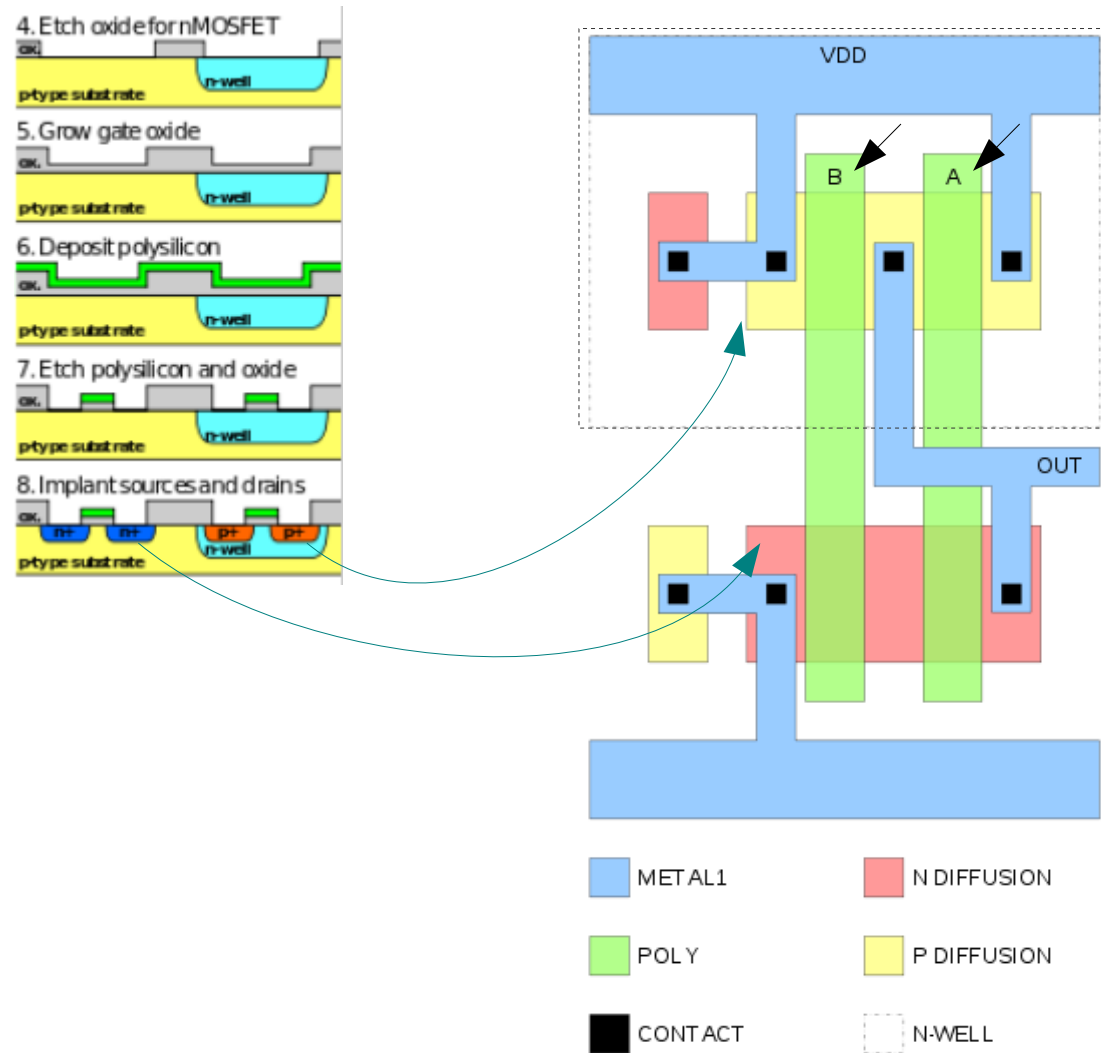
a P-type substrate tap is connected to VSS
an N-type n-well tap is connected to VDD



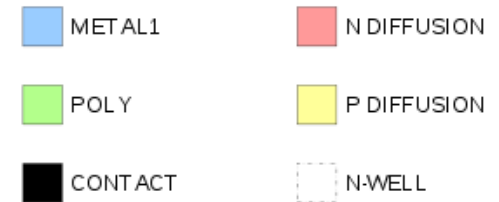
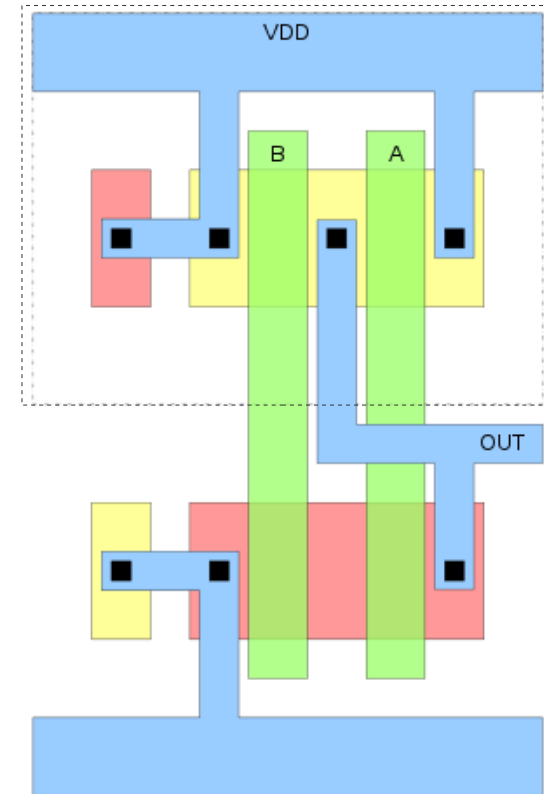
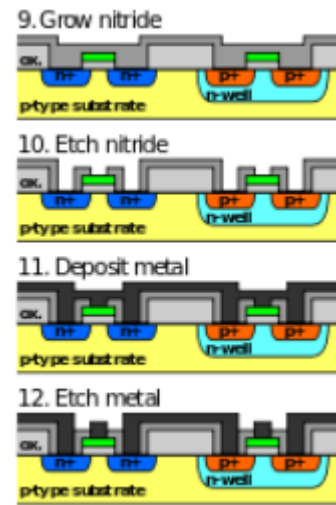
N-well



Diffusion



Metal



Dielectric

References

- [1] <http://en.wikipedia.org/>
- [2] <http://planetmath.org/>
- [3] M.L. Boas, "Mathematical Methods in the Physical Sciences"