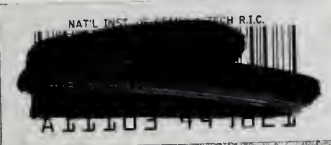Federal Standard 1007 has been redesignated
as Federal Information Processing Standards
Publication (FIPS PUB) 135. Issued by the
National Institute of Standards and Technology pursuant
to Section 111(d) of the Federal Property and Adminis-
trative Services Act of 1949 as amended by the
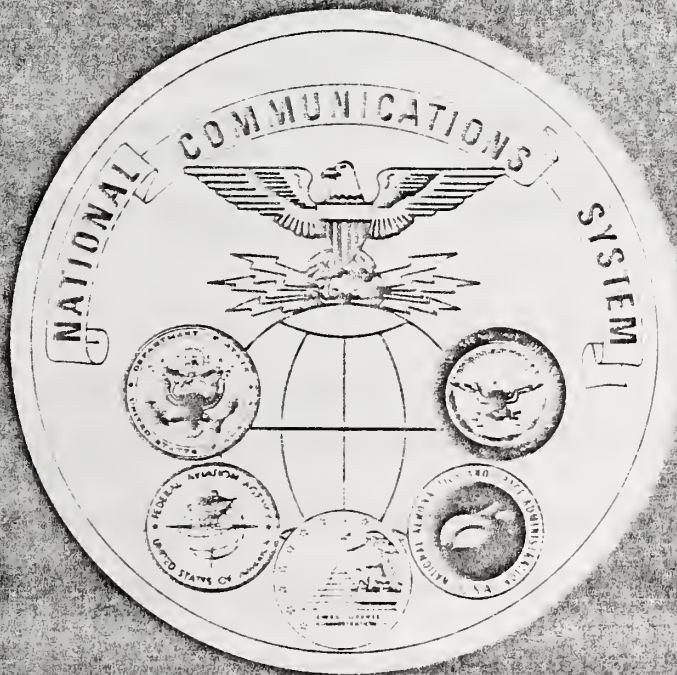Computer Security Act of 1987, Public Law 100-235.

FEDERAL STANDARD 1007

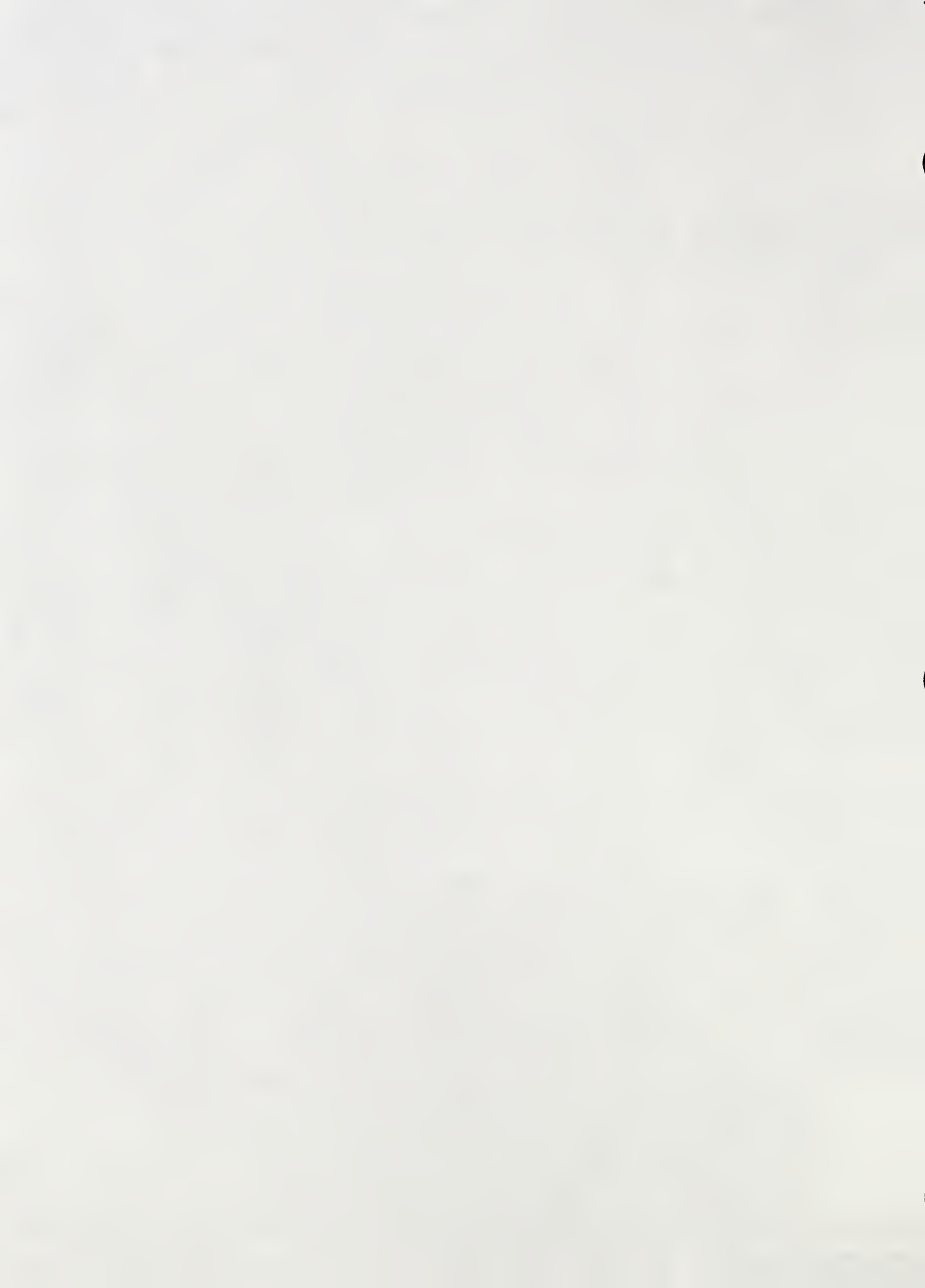# CODING AND MODULATION REQUIREMENTS FOR DUPLEX 9600 BIT/SECOND MODEMS

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MARCH 1981

FEDERAL STANDARD

TELECOMMUNICATIONS: CODING AND MODULATION
REQUIREMENTS FOR DUPLEX 9600 BIT/SECOND MODEMS

This standard is issued by the General Services Administration pursuant to
the Federal Property and Administrative Services Act of 1949, as amended.

1. SCOPE

1.1   Description. This standard establishes coding and modulation requirements for duplex 9600 bit/s modems owned or leased by the Federal Government for use over four-wire, analog transmission channels. It is based upon CCITT Recommendation V.29.

1.2   Purpose. This standard is to facilitate interoperability between telecommunication facilities and systems of the Federal Government.

1.3   Application

1.3.1   All Federal departments and agencies shall comply with this standard in the design and procurement of duplex 9600 bit/s modems (and equipment containing such modems) for use over four-wire, nominal 4 kHz analog channels. Typically, nominal 4 kHz analog channels are derived from frequency division multiplex equipment associated with microwave, coaxial cable, and satellite transmission systems.

1.3.2   For application of this standard within the Department of Defense, users should refer to the supplemental requirements contained in Military Standard 188-110.

1.3.3   Modems described by this standard may also be used on nonmultiplexed transmission systems, such as metallic cable facilities, but are not required for use with such systems.

2. REQUIREMENTS

2.1   9600 Bit/s Operation

2.1.1   Carrier Frequency. The carrier frequency shall be 1700 ± 1 Hz.

2.1.2   Spectrum. The modulator energy spectrum shall be shaped in such a way that when continuous ONE's are applied to the input of the scrambler:

(1) the resulting transmitted spectrum shall have a substantially linear phase characteristic over the range of 700 Hz to 2700 Hz and

(2) the energy density at 500 Hz and 2900 Hz shall be attenuated 4.5 ± 2.5 dB with respect to the maximum energy density between 500 Hz and 2900 Hz.

2.1.3   Data and Modulation Rate. The data rate shall be 9600 bits/s $\pm.01$ percent. The modulation (symbol) rate shall be 2400 baud $\pm.01$ percent.

2.1.4   Encoding Data Bits. The data stream to be modulated shall be divided into groups of four consecutive bits (quadbits). The first bit in time of each quadbit (Q1) shall be used to determine the signal element amplitude to be transmitted. The second (Q2), third (Q3), and fourth (Q4) bits shall be encoded as a phase change of the 1700 Hz carrier relative to the phase of the carrier during transmission of the immediately preceding signal element as indicated below.

| Q2	Q3	Q4	Phase Change
0	0	1	0^{0}
0	0	0	45^{0}
0	1	0	90^{0}
0	1	1	135^{0}
1	1	1	180^{0}
1	1	0	225^{0}
1	0	0	270^{0}
1	0	1	315^{0}

The phase change is the actual on-line phase shift in the transition region from the end of one signal element to the beginning of the following signal element.

The relative amplitude of the transmitted signal element is determined by the first bit of the quadbit (Q1) and the absolute phase of the signal element. Absolute phase reference is established during the synchronization procedure, described in section 2.4.1.2. The method of determining signal element relative amplitude is shown below.

Absolute Phase	Q1	Relative Signal Element Amplitude
0°, 90°, 180°, 270°	0	3
	1	5
45°, 135°, 225°, 315°	0	$\sqrt{2}$
	1	$3\sqrt{2}$

A signal space diagram, showing amplitude states with respect to absolute phase, is depicted below.
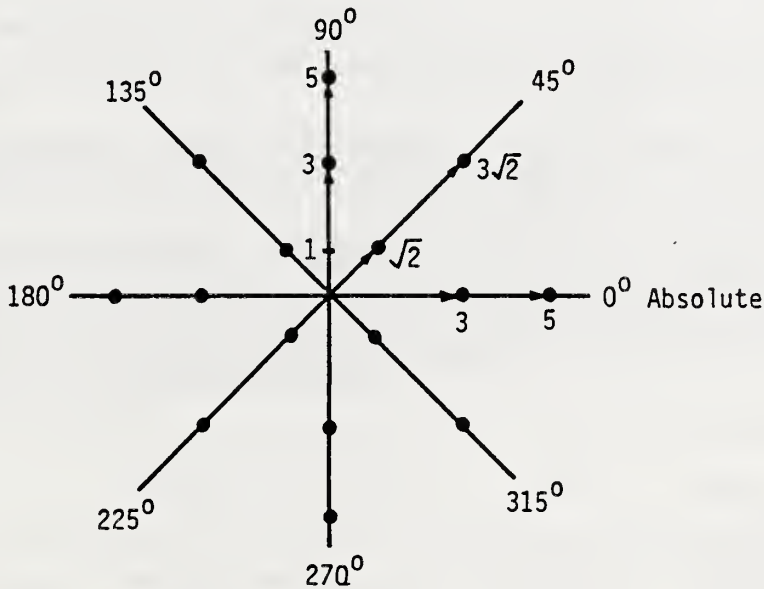
At the receiver, the quadbits are decoded and the bits are reassembled in correct order.

2.2   7200 Bit/s Operation (Optional)

2.2.1   Data and Modulation Rate. The data rate shall be 7200 bits/s $\pm$.01 percent. The modulation (symbol) rate shall be 2400 baud $\pm$.01 percent.

2.2.2   Encoding Data Bits. At the 7200 bit/s fallback rate, the data stream to be modulated shall be divided into groups of three consecutive bits. The first data bit in time determines Q2 of the modulator quadbit. The second and third data bits determine Q3 and Q4 of the modulator quadbit, respectively. Q1 of the modulator quadbit is kept as data ZERO.

2.2.3   All other characteristics shall be as in section 2.1.

2.3   4800 Bit/s Operation (Optional). 4800 bit/s operation, when utilized, shall follow one of the two options described below.

2.3.1   Option I

2.3.1.1   Data and Modulation Rate. The data rate shall be 4800 bits/s +.01 percent. The modulation (symbol) rate shall be 2400 baud +.01 percent.

2.3.1.2   Encoding Data Bits. The data stream to be modulated shall be divided into groups of two consecutive bits. The first data bit in time determines Q2 of the modulator quadbit and the second data bit determines Q3 of the modulator quadbit. Q1 of the modulator quadbit is kept as data ZERO. Q4 is determined by inverting the modulo-2 sum of Q2 and Q3. A table showing this method is given below.

Data Bits		Quadbits				Phase Change
		Q1	Q2	Q3	Q4	
0	0	0	0	0	1	0^0
0	1	0	0	1	0	90^0
1	1	0	1	1	1	180^0
1	0	0	1	0	0	270^0

2.3.1.3   All other characteristics shall be as in section 2.1.

2.3.2   Option II. Federal Standard 1006 (4800 bit/s modem) shall be followed completely for 4800 bit/s operation in lieu of this standard.

2.4   Synchronization Signals. Modems shall be capable of operation utilizing the normal synchronization signal, described in section 2.4.1. However, this does not preclude use of the long synchronization signal (section 2.4.2) or the use of shorter than normal synchronization signals in special applications.

2.4.1   Normal Synchronization Signal. Transmission of a synchronization signal may be initiated by a modem or its associated Data Terminal Equipment (DTE). When Request to Send (RS) indication is used to control modulator carrier, a synchronization signal shall be generated during the interval between Request to Send (RS) indication from the DTE and the modem responding with Clear to Send (CS) indication. Also, when a modem detects a channel condition that requires resynchronization/reequalization, or receives a synchronization signal from the distant modem, it shall withhold Clear to Send (CS) indication to its associated DTE and generate a synchronization signal. The normal synchronization signal, for all data rates, is divided into four segments as follows:

	Segment 1	Segment 2	Segment 3	Segment 4	Total of Segments 1,2,3,and 4
Type of Line Signal	No Transmitted Energy	Alternations	Equalizer Conditioning Pattern	Scrambled All Data ONEs	Total Synchronization Signal
Number of Symbol Intervals	48	128	384	48	608
Approximate Time in ms	20	53	160	20	253

2.4.1.1   Segment 1 withholds carrier for 48 symbol intervals.

2.4.1.2   Segment 2 consists of alternations between two signal elements. The first signal element (A) has a relative amplitude of 3 and defines an absolute phase of 180º. The second signal element (B) depends upon the data rate. The following chart gives the absolute phase and relative amplitude of signal element B for each data rate:

Data Rate	Absolute Phase	Relative Amplitude
9600 Bits/s	315°	$3\sqrt{2}$
7200 Bits/s	315°	$\sqrt{2}$
4800 Bits/s	270°	3

Segment 2 alternates ABAB..... for 128 symbol intervals.

2.4.1.3   Segment 3 consists of two signal elements transmitted according to an equalizer conditioning pattern. The first signal element (C) has a relative amplitude of 3 and an absolute phase of 0°. The second signal element (D) depends upon data rate as shown below.

Data Rate	Absolute Phase	Relative Amplitude
9600 Bits/s	135°	$3\sqrt{2}$
7200 Bits/s	135°	$\sqrt{2}$
4800 Bits/s	90°	3

The equalizer conditioning pattern shall be a pseudorandom sequence generated by the polynomial:

$$1 + X^{-6} + X^{-7}$$

Each time the pseudorandom sequence contains a ZERO, signal element C is transmitted. Each time the pseudorandom sequence contains a ONE, signal element D is transmitted. Segment 3 begins with the sequence CDCDCDC..... according to the pseudorandom sequence and continues for 384 symbol intervals.

A block diagram of the pseudorandom sequence generator is given below. (Logically equivalent configurations may be utilized in place of the one shown.)
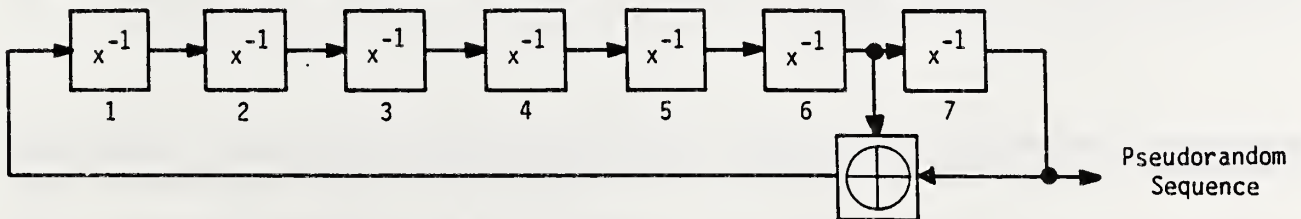
In the above diagram, the seven-bit shift register is initially set to a 0101010 state. During operation, the shift register is clocked at the symbol rate (2400 symbols/s) and bits 6 and 7 of the shift register are modulo-2 added, with the sum being applied to the shift register input (bit 0). Output of the pseudorandom sequence generator is taken from bit 7 of the shift register. For informational purposes, the first three shifts produce shift register states of 1010101, 1101010, and 1110101, respectively.

2.4.1.4   Segment 4 commences transmission with continuous ONE's applied to the input of the scrambler. Segment 4 is 48 symbol intervals in duration. At the end of segment 4, the Clear to Send (CS) circuit is turned ON and data is applied to the input of the scrambler.

2.4.2   Long Synchronization Signal (Optional). In special applications, as an additional capability, long synchronization signals may be utilized. Long synchronization signals shall be the same as normal synchronization signals except that

Segment 2 shall be extended to 180 symbol intervals and Segment 3 shall be extended to 1,920 symbol intervals.

2.5 Scrambler/Descrambler. A self-synchronizing scrambler/descrambler having the generating polynomial

$$1 + X^{-18} + X^{-23}$$

shall be utilized. The purpose of this scrambler is randomization of the data stream in order to maintain proper convergence of the automatic adaptive equalizer at the demodulator.

2.5.1 Scrambler. A block diagram of the scrambler is given below. (Logically, equivalent configurations may be utilized in place of the one shown.)
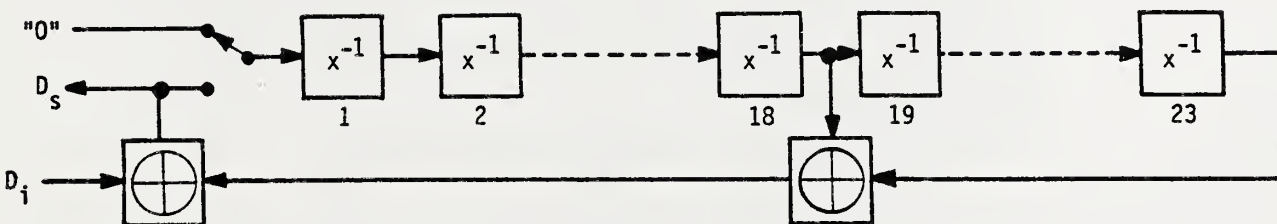
In the diagram above, Di represents input data to the scrambler and Ds represents scrambled output data. During operation, the 23-bit shift register, initially filled with all ZERO's, is clocked at the data rate. Shift register bits 18 and 23 are modulo-2 added and the resulting sum is then modulo-2 added with Di to produce Ds. Ds, the scrambler output, is then also applied to the shift register input (bit 0).

In order to ensure that the proper starting sequence is generated, the shift register input is fed all ZERO's during synchronization signal segments 1, 2, and 3. During segment 4, and normal data transmission, the shift register is fed with output Ds (input Di being all ONE's during segment 4).

2.5.2 Descrambler. The block diagram of the descrambler is given below. (Logically, equivalent configurations may be utilized in place of the one shown.)
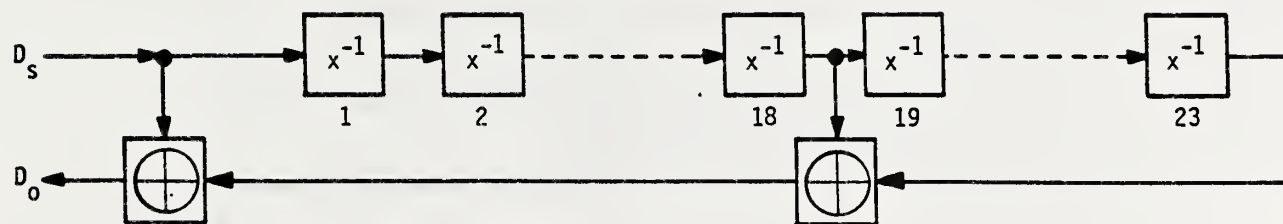
In the diagram above, Ds represents scrambled input data and Do represents descrambled output data. The operation of the descrambler is basically the same as that of the scrambler described in the previous section. At the start of operation, all shift register bits must be in a ZERO state.

2.5.3 Scrambler Bypass (Optional). In special applications, as an additional capability, data may be permitted to bypass the scrambler if the transmitted data is of a very random nature (e.g., encrypted). When operating in this mode, the scrambler still shall be utilized during segment 4 of normal and long synchronization signals.

2.6 Equalization

2.6.1 An automatic adaptive equalizer shall be provided. It shall be in the demodulator.

2.6.2 A synchronization signal is initiated when a modem detects a loss of equalization (and requires a synchronization signal) or when the Request to Send (RS) circuit is turned ON in the carrier-controlled mode. Having initiated a synchronization signal, a modem expects a synchronization signal from the distant modem. If a modem does not receive a synchronization signal from the distant modem within an expected time interval

(1.2 seconds is recommended), it transmits another synchronization signal. When a modem fails to synchronize on the received signal sequence, it can transmit another synchronization signal. If a modem receives a synchronization signal when it has not initiated a synchronization signal, and its demodulator is properly synchronized, it returns only one synchronization signal.

2.7   Multiplexing (Optional). When a modem contains a multiplexer to combine 7200 bit/s, 4800 bit/s, and 2400 bit/s subchannels into a single aggregate bit stream for transmission, the modulator quadbits shall be allocated in accordance with the following table.

AGGREGATE DATA RATE	MULTIPLEX CONFIGURATION	SUBCHANNEL DATA RATE	MULTIPLEX CHANNEL	MODULATOR QUADBITS			
				Q1	Q2	Q3	Q4
9600 BITS/S	1	9600	A	•	•	•	•
	2	7200	A	•	•	•	
		2400	B				•
	3	4800	A	•		•	
		4800	B		•		•
	4	4800	A	•		•	
		2400	B		•		
		2400	C				•
	5	2400	A	•			
		2400	B		•		
		2400	C			•	
		2400	D				•
7200 BITS/S	6	7200	A		•	•	•
	7	4800	A		•	•	
		2400	B				•
	8	2400	A	•			
		2400	B			•	
		2400	C				•
4800 BITS/S	9	4800	A		•	•	
	10	2400	A		•		
		2400	B			•	

2.8   General Characteristics

2.8.1   Impedance. The modem shall be capable of presenting an input and output impedance to the analog line of 600+60 ohms, balanced.

2.8.2   Output Level. The output level of the modulator shall be adjustable from at least -12 dBm to -3 dBm in no greater than 2 dB steps. Output level controls shall be such that they are not readily adjustable by untrained personnel.

2.8.3   Input Sensitivity. The demodulator shall have an input sensitivity adjustable to -45+4 dBm and -30+4 dBm. When the above-stated input sensitivities are used, the input level dynamic range shall be at least 30 dB above the input sensitivity.

2.8.4   Digital Interface. Digital interface characteristics for modems, when applicable, are specified in other Federal standards. These standards include Federal Standards 1020A, 1030A, and 1031.

3. CHANGES. When a Federal agency considers that this standard does not provide for its essential needs, a statement citing inadequacies shall be sent in duplicate to the General Services Administration (C), Washington, D.C. 20405, in accordance with the provisions of Federal Property Management Regulations 41 CFR 101-29.3. The General Services Administration will determine the appropriate action to be taken and will notify the agency.

Preparing Activity:

    National Communications System
      Office of Technology and Standards
    Washington, DC 20305

MILITARY INTERESTS:

Military Coordinating Activity
DCA — DC

Custodians
Army — CR
Navy — EC
Air Force — 90

Review Activities
Army — CR, SC
Navy — EC, COMNAVTELCOM, MC
Air Force — 90, 17
DCA — DC
NSA — NS
TRI-TAC — TT

User Activities
Navy — MCLB

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