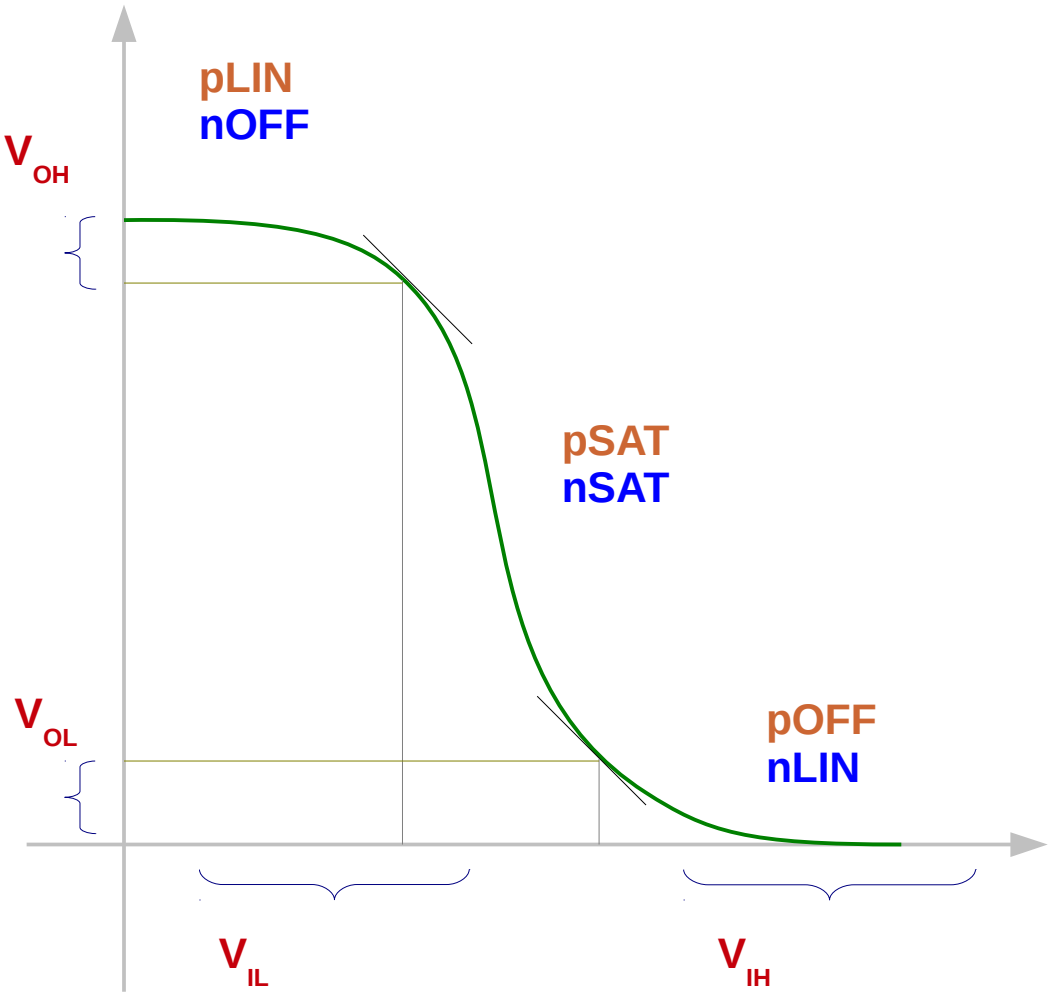
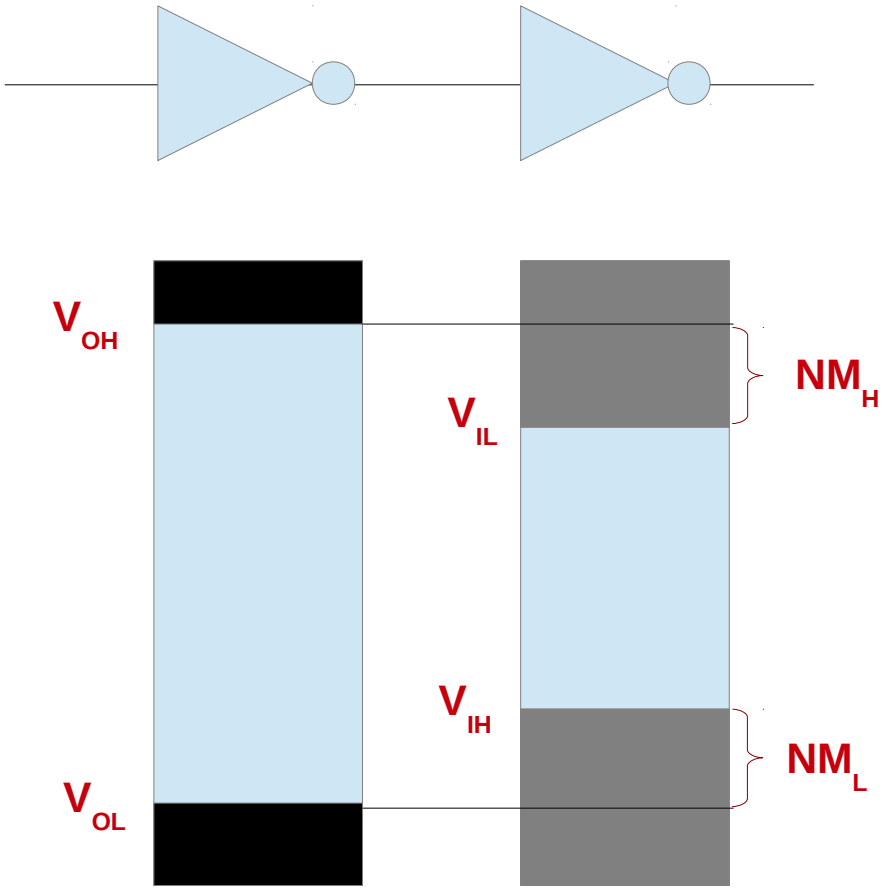
CMOS Transistor Sizing (3G)

Please send corrections (or suggestions) to youngwlim@hotmail.com.

This document was produced by using OpenOffice and Octave.

Noise Margin





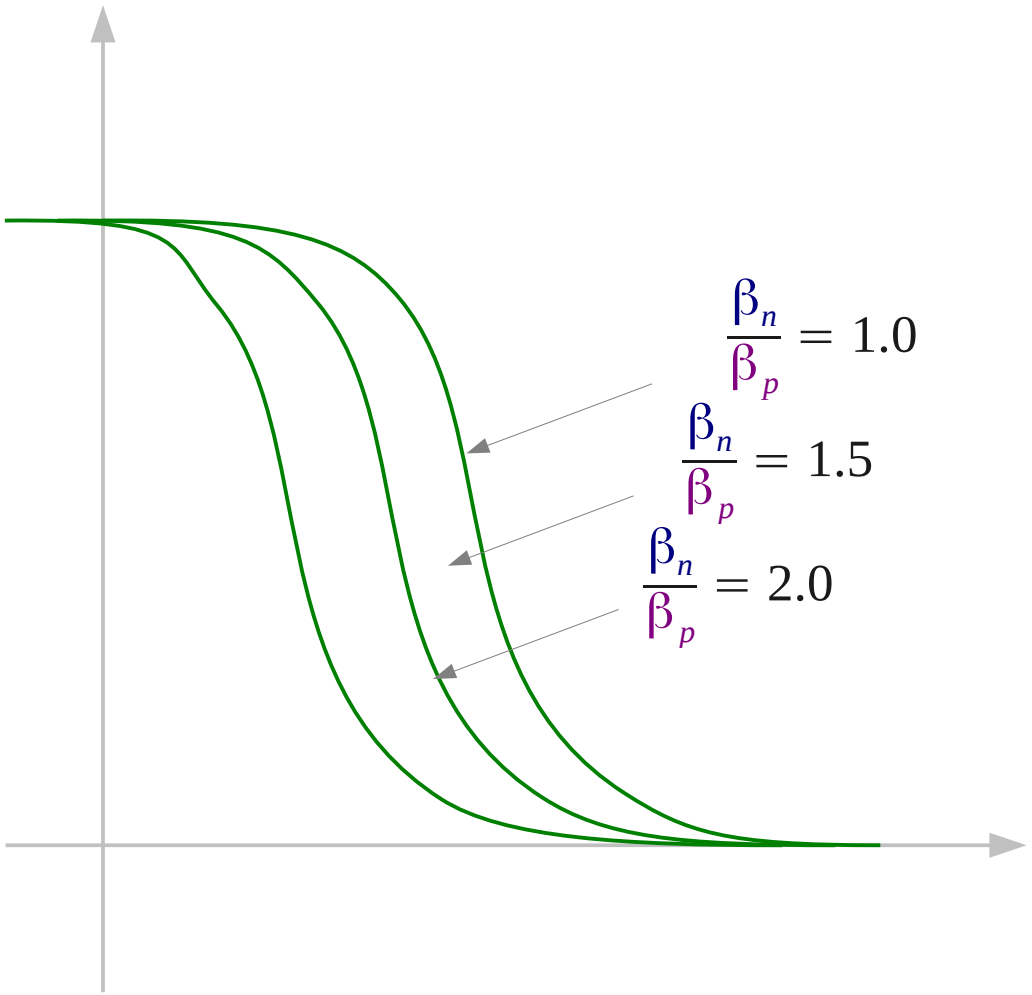
Transconductance Parameter (1)

When $V_{GS} > V_t$ and $V_{DS} < (V_{GS} - V_t)$

$$I_d = k' \frac{W}{L} \left[(v_{gs} - v_t) v_{ds} - \frac{1}{2} v_{ds}^2 \right]$$

When $V_{GS} > V_t$ and $V_{DS} \geq (V_{GS} - V_t)$

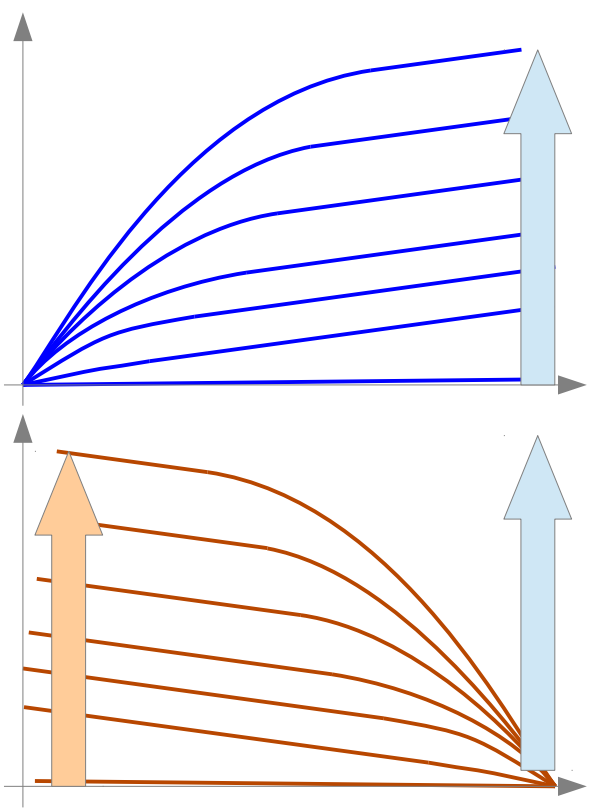
$$I_d = \frac{1}{2} k' \frac{W}{L} (v_{gs} - v_t)^2$$



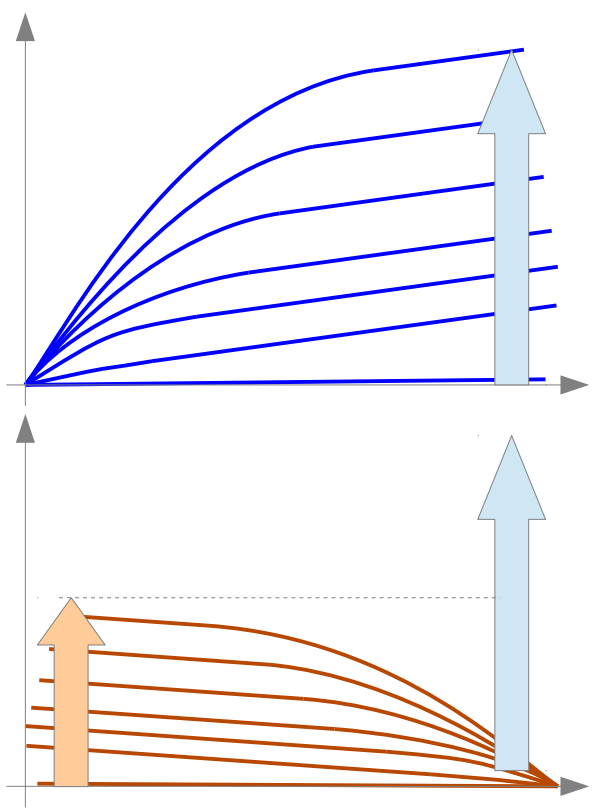
$$\beta_p = k'_p \left(\frac{W}{L} \right)_p$$

$$\beta_n = k'_n \left(\frac{W}{L} \right)_n$$

Transconductance Parameter (2)



$$\frac{\beta_n}{\beta_p} = 1.0$$



$$\frac{\beta_n}{\beta_p} = 2.0$$

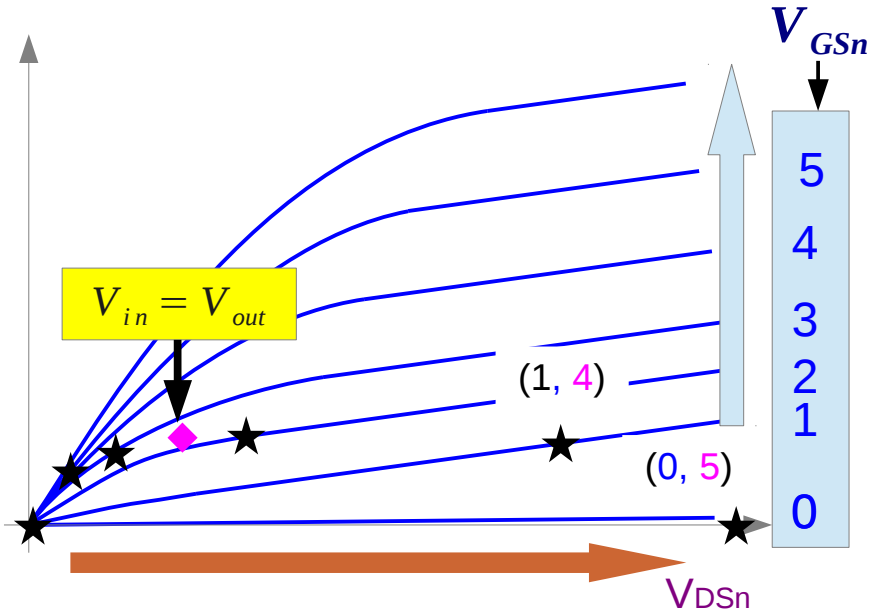
When $V_{GS} > V_t$ and $V_{DS} < (V_{GS} - V_t)$

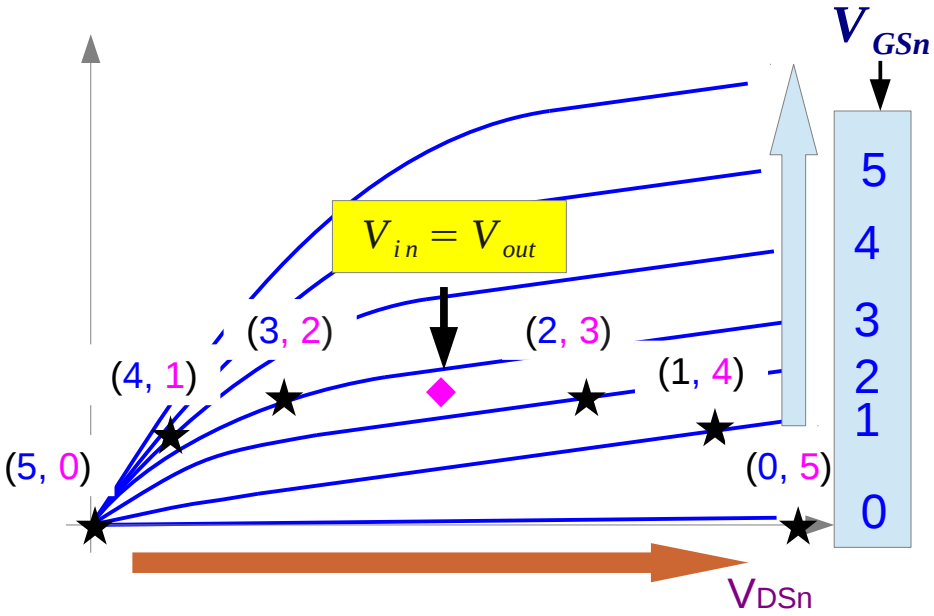
$$I_d = \beta \left[(v_{gs} - v_t) v_{ds} - \frac{1}{2} v_{ds}^2 \right]$$

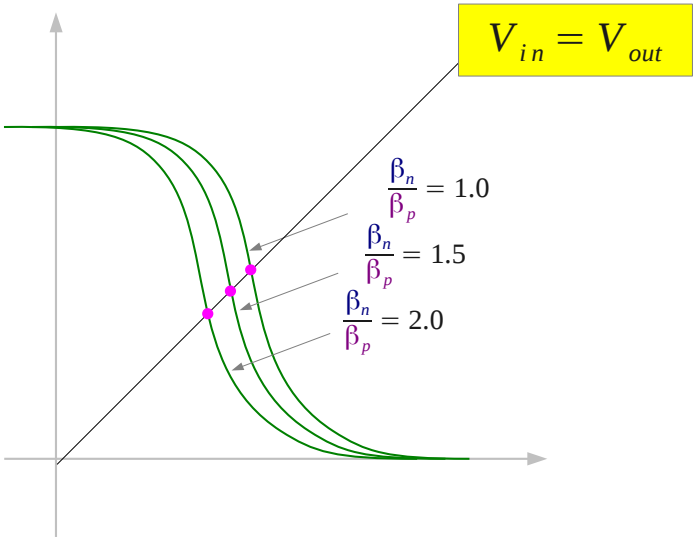
When $V_{GS} > V_t$ and $V_{DS} \geq (V_{GS} - V_t)$

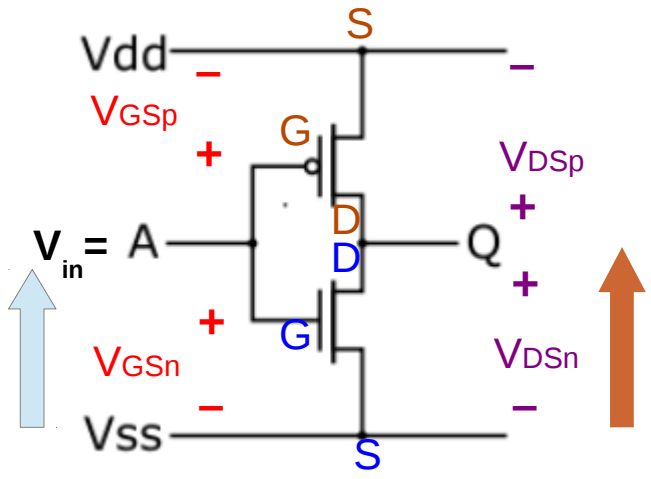
$$I_d = \frac{1}{2} \beta (v_{gs} - v_t)^2$$

Transconductance Parameter (3)

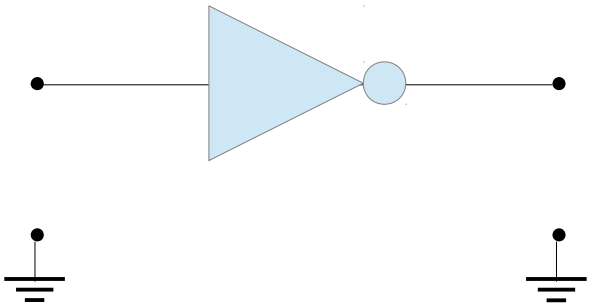


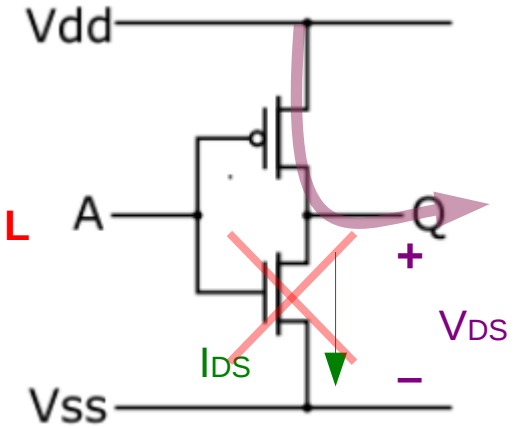


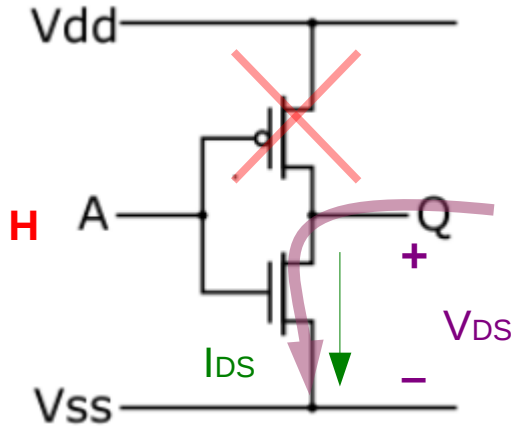


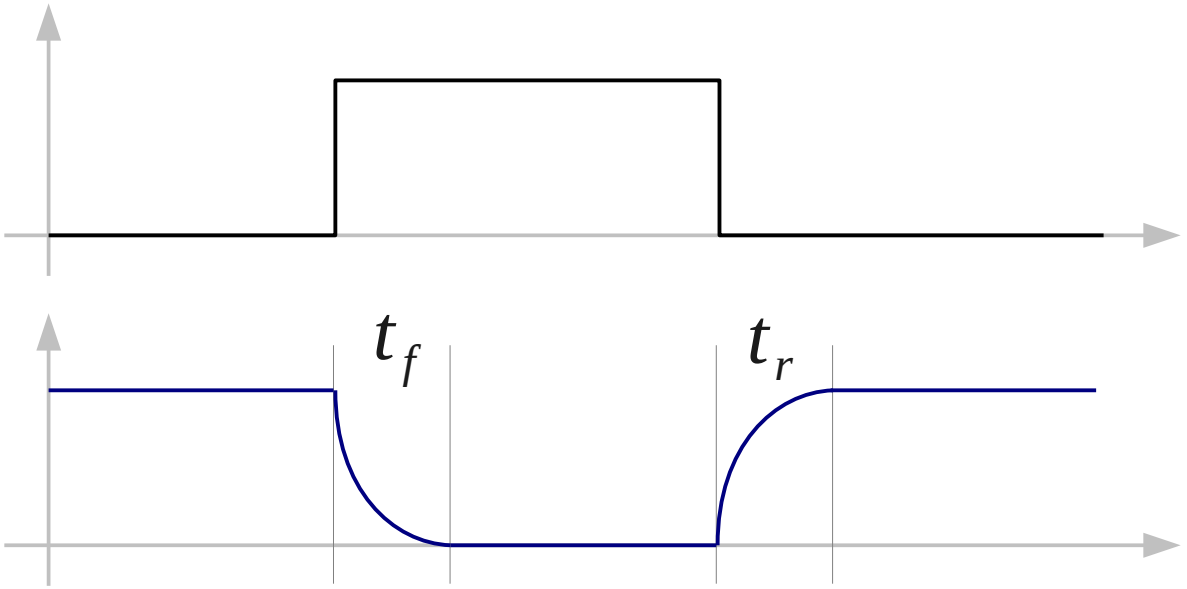


Rising and Falling Time (1)

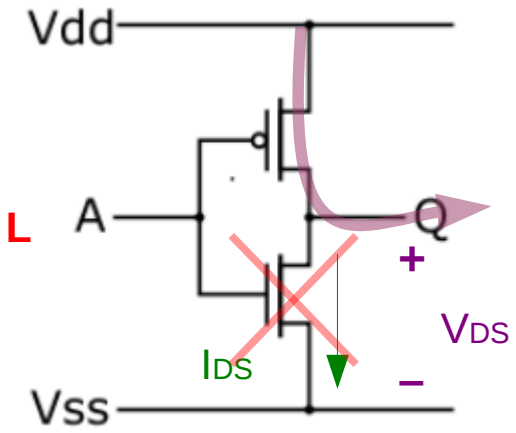


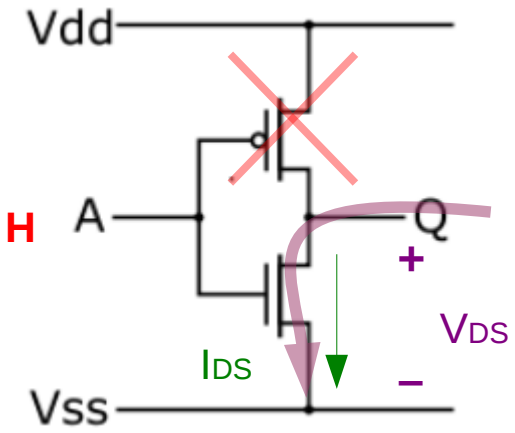






Rising and Falling Time (2)





Rise Time

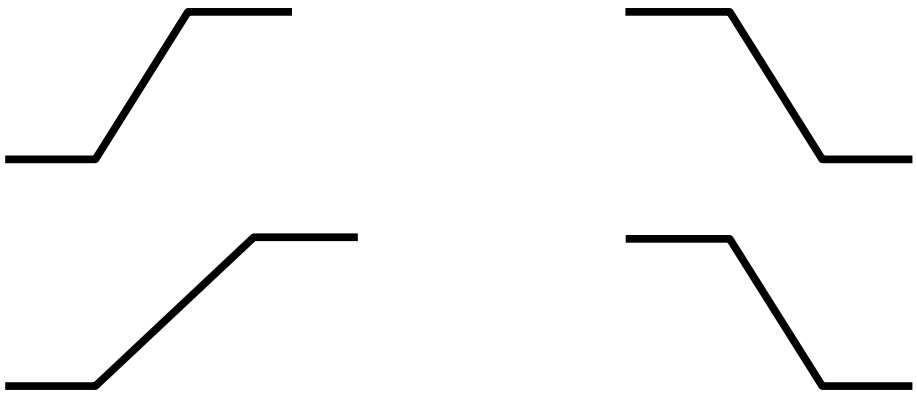
$$t_r = R_p C_L$$

Fall Time

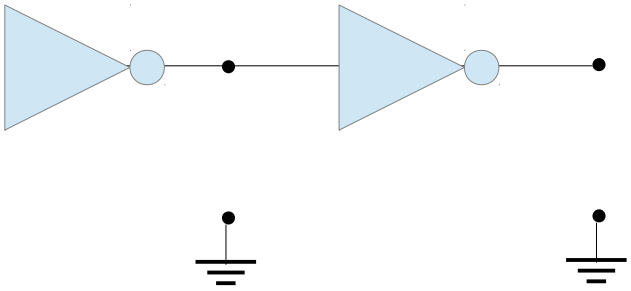
$$t_f = R_n C_L$$

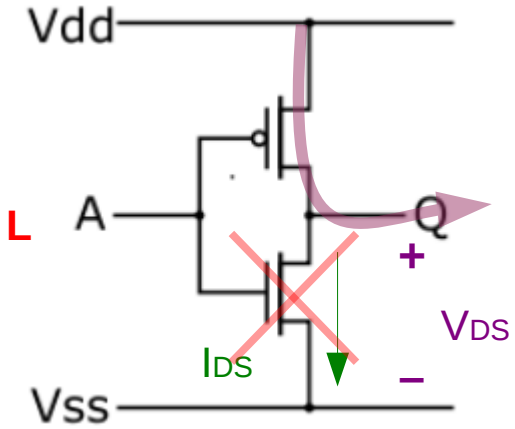
$$\frac{\beta_n}{\beta_p} = 1.0 \qquad R_n = R_p$$

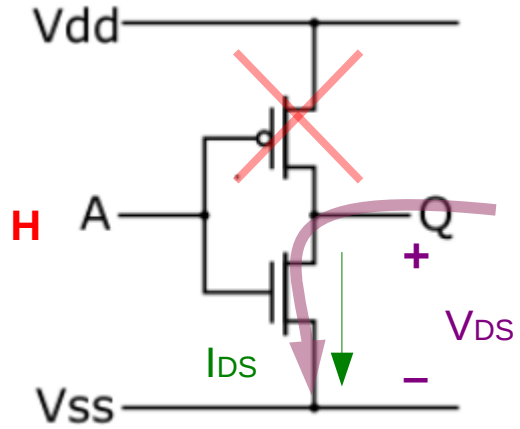
$$\frac{\beta_n}{\beta_p} = 2.0 \qquad R_n < R_p$$

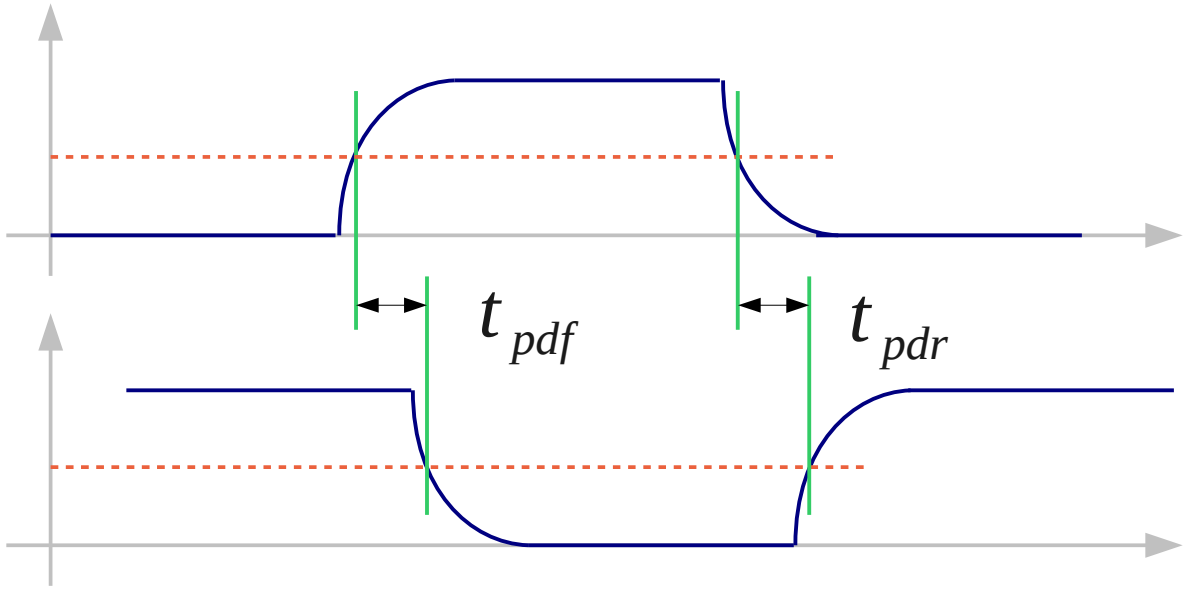


Propagation Delay

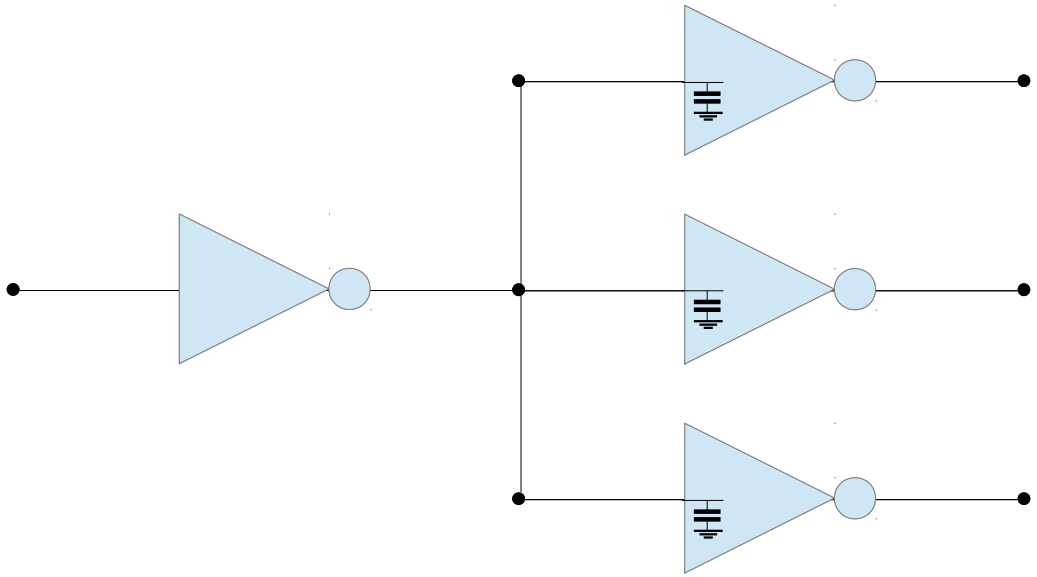








Load Capacitance



$$C_{in} = 3C_g$$

Big Capacitance

- A signal connected off-chip
- A signal with very long wire
- A clock signal driving many flip-flops

Characteristic Curve

References

[1] http://en.wikipedia.org/
[2] http://www.allaboutcircuits.com/
[3] W. Wolf, “Modern VLSI Design : Systems on Silicon
[4] N. Weste, D. Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”
[5] J. P. Uyemura, “Introduction to VLSI Circuits and Systems”