PERFORMANCE OF A DIGITAL DATA TRANSMISSION SYSTEM USING MATCHED FILTER PROCESSING OF AN AUXILIARY SIGNAL FOR SYNCHRONIZATION

Serdar Yurdakul

NAVAL POSTGRADUATE SCHOOL
Monterey, California

THESIS

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by

Serdar Yurdakul

and

Sedat Senturk

December 1979

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In this report a digital communication system (transmitter and receiver) is presented which uses noncoherent carrier demodulation and coherent bit recovery utilizing an

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integrate-and-dump detector. The synchronization (timing) pulses for this detector are derived from the response of a matched filter to the low level synchronization signal transmitted with high level data modulated carrier. This system is designed, built and tested; noise is added to simulate the channel. Probability of error versus signal-to-noise ratio curves are plotted to obtain system performance.

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by

Serdar Yurdakul
Lieutenant, Turkish Navy
B.S.E.E., Naval Postgraduate School, 1979

and

Sedat Senturk
Lieutenant, Turkish Navy
B.S.E.E., Naval Postgraduate School, 1979

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December 1979

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In digital communication, coherent systems are used in order to provide small probability of error with small signal-to-noise ratios.

In this report a digital communication system (transmitter and receiver) is presented which uses noncoherent carrier demodulation and coherent bit recovery utilizing an integrate-and-dump detector. The synchronization (timing) pulses for this detector are derived from the response of a matched filter to the low level synchronization signal transmitted with high level data modulated carrier. This system is designed, built and tested; noise is added to simulate the channel. Probability of error versus signal-to-noise ratio curves are plotted to obtain system performance.

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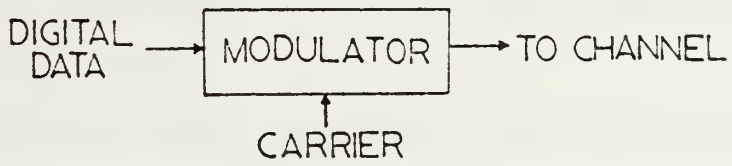
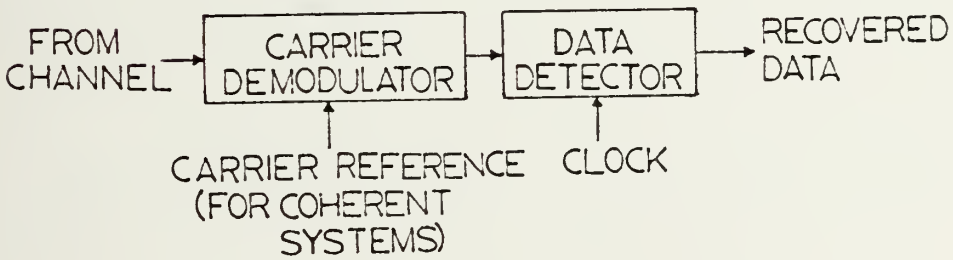
I. INTRODUCTION

This research investigates the use of an auxiliary low power level synchronization signal transmitted in the same frequency band as the high power level modulated data signal. In the receiver, a filter matched to the synchronization signal is used to derive the timing signal.

A typical digital communication system is shown in Fig. 1.



(a) Transmitter



(b) Receiver

Fig. 1. A Typical Digital Communication System.

As shown in Fig. 1(a), digital data modulates the carrier in one of three ways: amplitude, frequency or phase. This modulated carrier may be upconverted, amplified and then transmitted through the channel.

In the receiver shown in Fig. 1(b), the received signal including channel noise is applied to the carrier demodulator. After carrier demodulation the data or bit detector decides if the bit is either 1 or 0.

In the experimental system described in this report, amplitude modulation (Amplitude Shift Keying or ASK) and noncoherent demodulation (bandpass filter and envelope detector) are used. Coherent pulse recovery is accomplished by utilizing an integrate-and-dump detector. The synchronization signal for coherent pulse recovery is obtained from the matched filter response to the low level transmitted synchronization signal.

An objective of this research is to investigate the division of transmitter power between data and synchronization signals which minimizes the probability of error caused by the noise in channel.

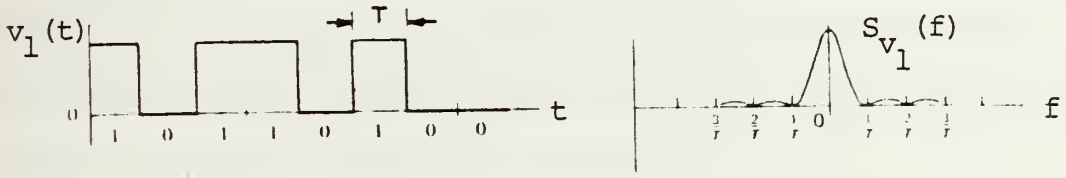
II. BACKGROUND

A. TYPES OF DIGITAL COMMUNICATION

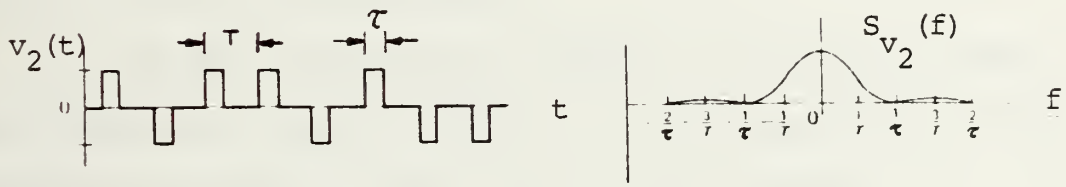
The objective of a digital communication system is to transmit the data at a certain rate with a minimum number of errors. Data rate and error probability are related to system bandwidth and signal-to-noise ratio.

1. Waveforms

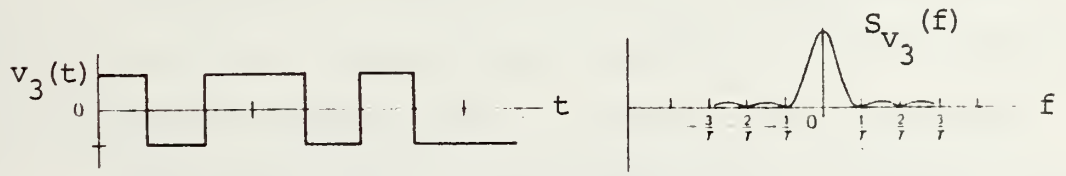
Typical voltage representations of digital data are shown in Fig. 2.



(a) Unipolar Synchronous,



(b) Bipolar Return-to-Zero (RZ)



(c) Bipolar Non-Return-to-Zero (NRZ)

Fig. 2. Typical Digital Data Waveforms and Corresponding Power Spectra

Fig. 2(a) shows the binary data 10110100 as it might appear at the output of a TTL (transistor-transistor logic) circuit. This waveform is said to be unipolar because it has only one polarity, and synchronous because all pulses have equal duration and there is no separation between them. Unipolar signals contain a nonzero DC component that is difficult to transmit, carries no information and is a waste of power. Also, since the signal is synchronous, timing coordination between transmitter and receiver is needed.

The bipolar return-to-zero (RZ) represenation, shown in Fig. 2(b), avoids the DC and synchronization problems but the "spaces" which make the signal self-clocking result in use of additional bandwidth.

If efficient use of bandwidth and power is a dominant consideration, the bipolar non-return-to zero (NRZ) signal of Fig. 2(c), is preferable.

In the experimental system, all three of these waveforms are used at different points depending on the waveform desired at that point in the circuit.

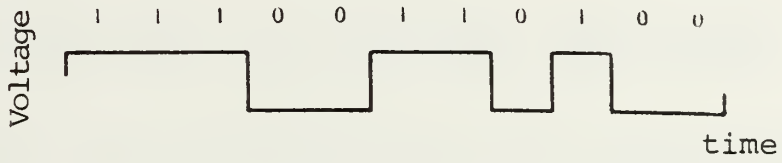
2. Digital Modulation

The digital information can be impressed upon a carrier wave using amplitude, frequency or phase modulation. Amplitude shift keying (ASK) is used in this research.

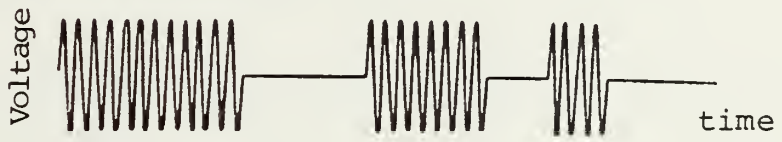
With ASK, the carrier amplitude is switched between two values, usually ON and OFF for binary signals. The resultant modulated wave consists of RF pulses or marks,

representing binary 1, and spaces, representing binary 0, as shown in Fig. 3(b). ASK is often referred to as on-off-keying (OOK).

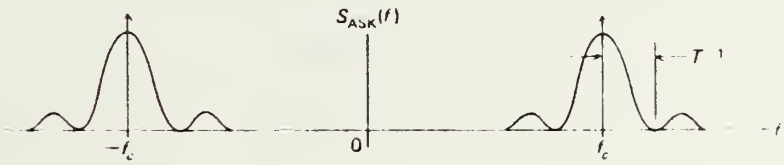
Demodulation of an ASK carrier is accomplished by detecting the envelope of the received signal. Such a noncoherent detection system is diagrammed in Fig. 4.



(a) Binary data



(b) Modulated carrier



(c) Power spectra

Fig. 3. ASK Modulation and Its Power Spectra

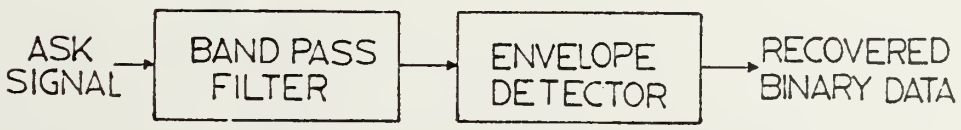


Fig. 4. Noncoherent Detection of ASK

3. P_e vs SNR for ASK

For ASK the received data is

$$y(t) = \begin{cases} n(t), & \text{for binary 0 sent} \\ A\cos(2\pi f_o t + \phi) + n(t), & \text{for binary 1 sent} \end{cases}$$

where $n(t)$ is noise and ϕ is an arbitrary phase angle.

Now, let $r(t)$ be the output of the envelope detector (Fig. 4). The probability of error P_e due to noise in the receiver is given as (see Ref. [1]):

$$P_e = \frac{1}{2} \cdot \frac{e^{-z/2}}{\sqrt{2\pi z}} + \frac{1}{2} e^{-z/2} \approx \frac{1}{2} e^{-z/2} \quad \text{for} \quad z >> 1$$

where $z = \dfrac{\text{average signal power}}{\text{average noise power}} = \text{SNR}$.

This assumes errors for 0 and 1 transmitted are equiprobable. Fig. 5 shows the P_e vs SNR curve for noncoherent ASK.

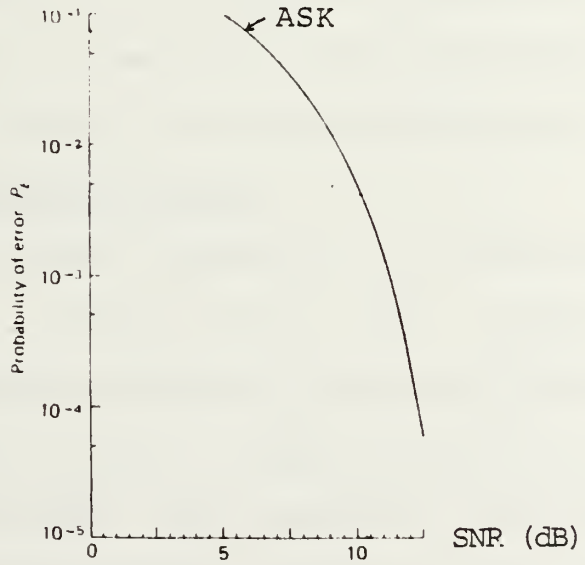


Fig. 5. P_e vs SNR for ASK

B. MATCHED FILTERS

There exists an optimum linear filter as shown in Fig. 6 for detecting the presence of a pulse f(t) of known shape in additive noise n(t) of known spectral density $G_n(f)$. Such filters are called matched filters.

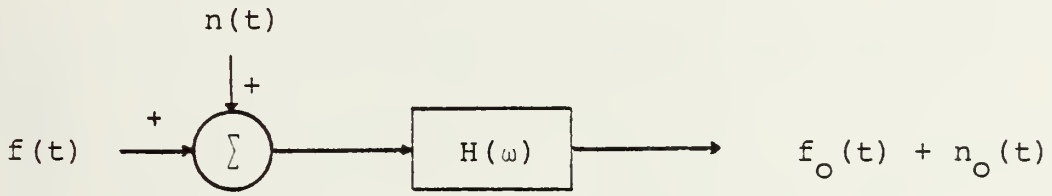
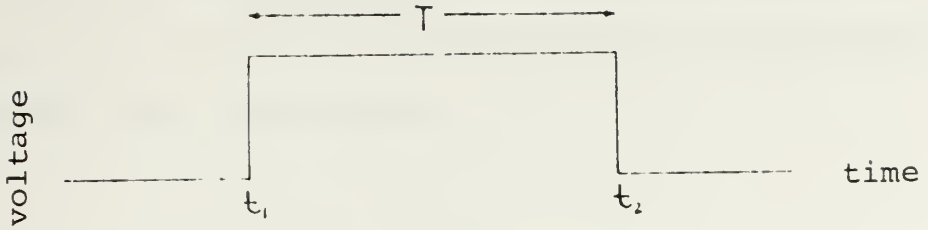


Fig. 6. An Optimum Filter

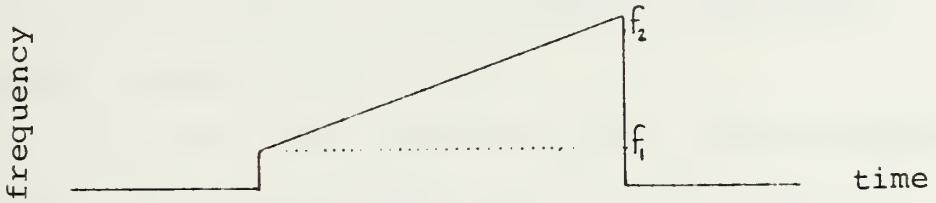
In the experimental system, two types of matched filters are used in the receiver. In the synchronization subsystem a filter matched to a chirp waveform is used to obtain a narrow high level output pulse from the low level chirp waveform transmitted. In the data subsystem, an integrate-and-dump detector is used as a filter matched to rectangular pulse waveform output of the envelope detector.

1. Chirp-Matched Filters

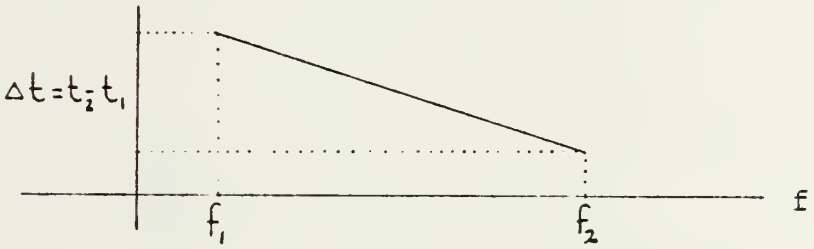
If the carrier frequency of a transmitted pulse is linearly swept, as shown in Fig. 7(b), a pulse compression filter with the time-delay vs. frequency characteristics of Fig. 7(c), could be used to delay one end of the pulse relative to the other. That produces a narrower (compressed) pulse at the filter output, as shown in Fig. 7(d).



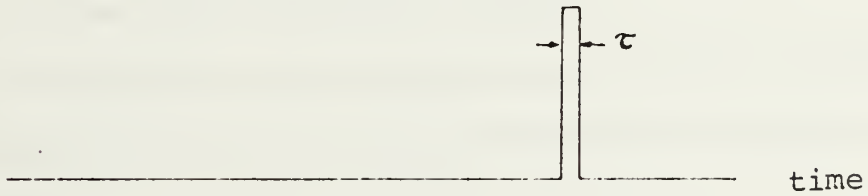
(a) Wide Pulse Envelope



(b) Carrier Frequency Modulation



(c) Filter Time-Delay Characteristics



(d) Compressed Pulse Envelope

(e) Input Output Pulse Waveforms of Compression Filter

Fig. 7. Idealized Pulse Compression Characteristics

The buildup in peak power of the compressed pulse is proportional to the ratio of the widths of the pulses at the filter input and output

$$\frac{P_{op}}{P_{ip}} = \frac{T}{\tau}$$

where P_{ip} and P_{op} are the peak powers of input and compressed pulses, respectively.

The actual time function of the output compressed pulse has a Sin x/x envelope with a pulse width of τ which is equal to $1/\Delta f$ where Δf is the bandwidth of the output pulse. Then, the peak power improvement between input and output is

$$\frac{P_{op}}{P_{ip}} = \frac{T}{\tau} = T \cdot \Delta f$$

$T \cdot \Delta f$ is called time bandwidth product.

In practice, pulse compression or chirp matched filter implementation is accomplished with dispersive delay lines (DDL).

2. Present Technology

Fig. 8 shows the typical numbers and technologies used to produce dispersive delay line matched filters. This figure is reproduced from Andersen Laboratories Inc. dispersive delay line products data sheet.

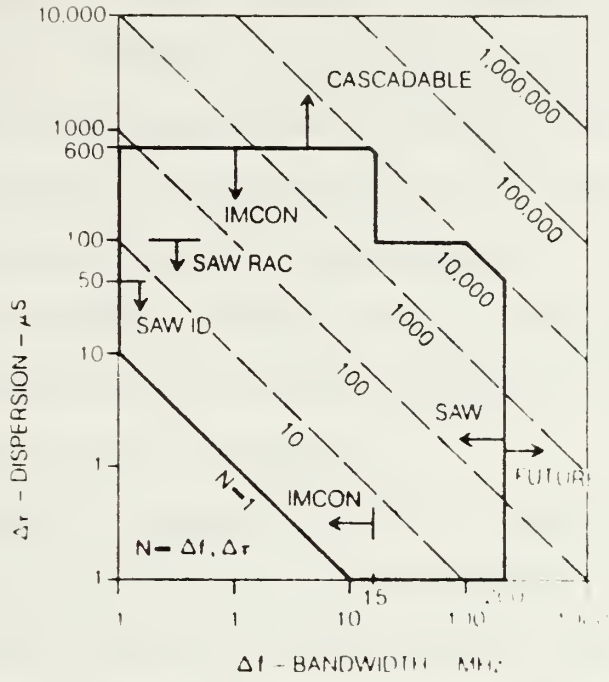


Fig. 8. Range of Performance for SAW and IMCON DDL's

The technologies used are IMCON, SAW RAC (surface acoustic wave-reflective array compressor) and SAW ID (surface acoustic wave interdigital). IMCON's are reflection mode delay lines fabricated on steel acoustic media and are most suited for the applications requiring dispersions of greater than 50 μsec at center frequencies below 30 MHz with bandwidths of less than 15 MHz.

SAW (surface acoustic wave) dispersive delay lines are more suited for lower dispersion (less than 100 μsec), wide band applications. The SAW-ID approach uses non-uniform

interdigital (ID) transducers in a conventional SAW configuration. The other SAW approach is a surface wave implementation of IMCON, which is called SAW-RAC, which is most useful for larger time-bandwidth products ($T \cdot \Delta f$).

The same company has a DDL with time bandwidth product of 25.000 and dispersion of 10 msec at 7.5 MHz center frequency with 3.0 MHz bandwidth. This value is obtained by cascading single units. These devices have sidelobe levels of 20 to 40 db relative to main lobe level and insertion loss of 30-50 db.

Generally, dispersive delay lines with center frequencies up to 250 MHz are available. They have bandwidths from 100 kHz to 200 MHz with time bandwidth products up to 25.000. The dispersion time can vary from 1 μsec up to 10 msec.

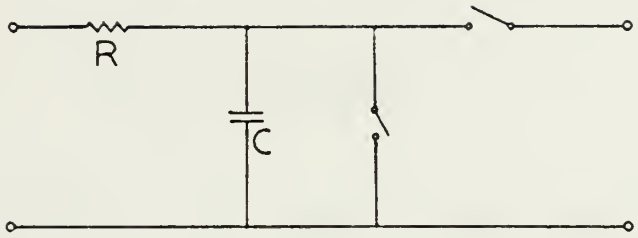
3. Integrate-and-Dump Detector

The integrate-and-dump circuit is a matched filter for a rectangular pulse. Fig. 9(a) shows the schematic diagram of this filter.

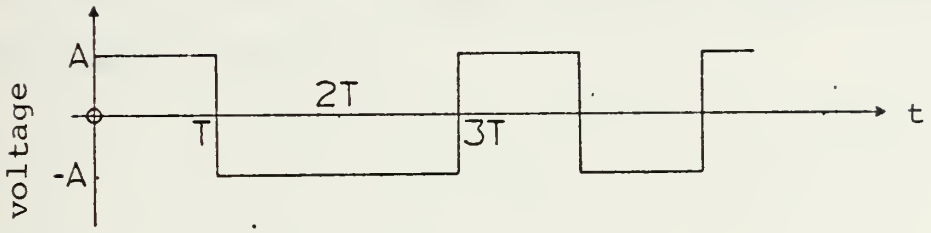
The circuit time constant, RC, is equated to the bit duration. This provides a maximum time of integration which results in minimum probability of error by removing (filtering) noise effects.

An important issue is the timing needed to sample the filter output and dump the capacitor.

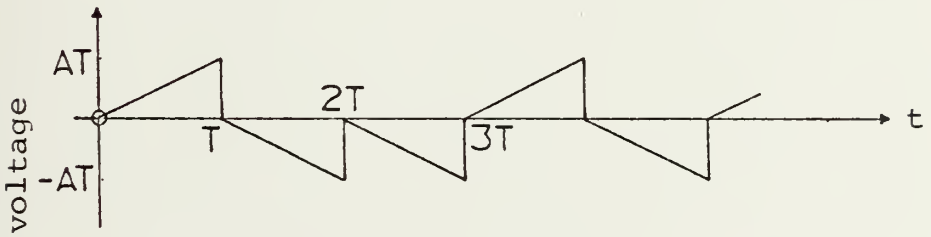
This research is concerned with one means of obtaining this timing. Fig. 9(b) and (c) shows arbitrary



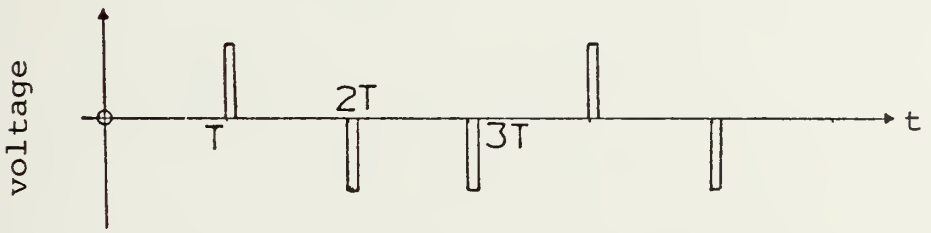
(a) Circuit



(b) Input



(c) Integrator Output



(d) Output After Sampling Switch

Fig. 9. Integrate-and-Dump Detector

input pulse trains and the output of the filter before the sampling switch when the noise is absent.

The probability of error expression for this receiver structure as derived in Ref. [1] is

$$P_e = \frac{1}{2} \operatorname{erfc} \sqrt{s}$$

where $s = A^2T/N_o$, A = input signal amplitude, T = pulse duration, and N_o = noise power spectral density function. s is then the ratio of signal energy per pulse-to-noise power spectral density.

III. EXPERIMENTAL SYSTEM

The block diagram of the experimental system is shown in Fig. 10. In the transmitter, a high-level carrier modulated data signal and a low-level chirp signal which carries sync information are generated and summed. In this experimental set-up, there is no up-conversion which is a part of many operational transmitters. Gaussian noise is also added to simulate interference experienced by operating systems.

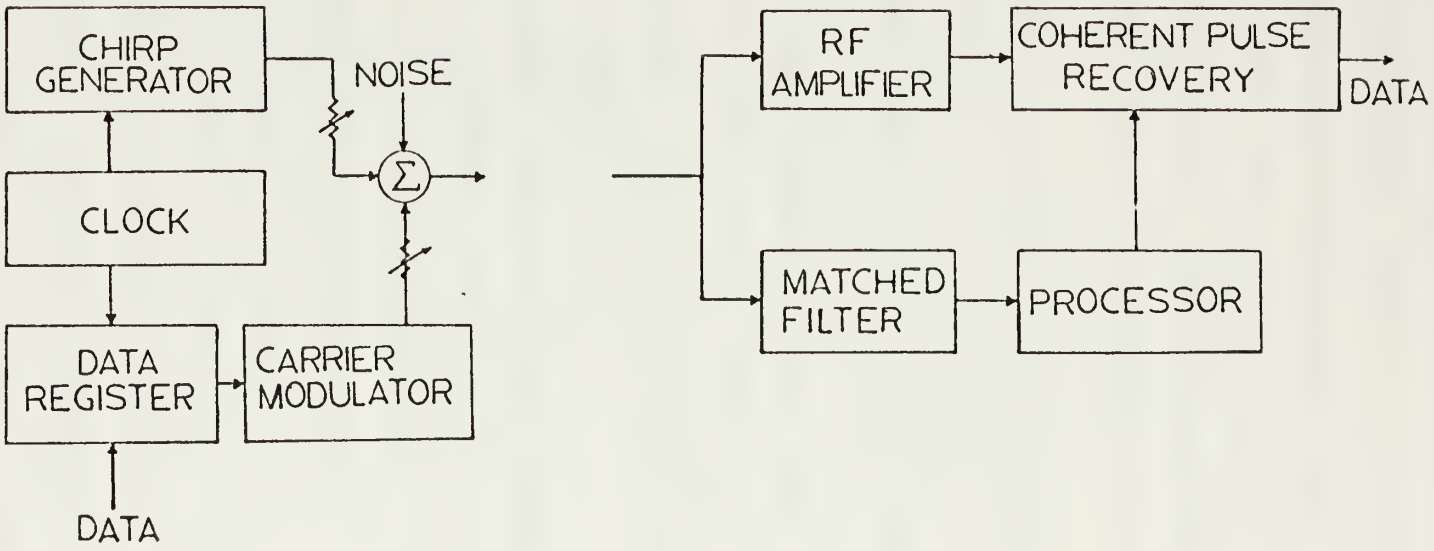
Isolation between the receiver and transmitter is provided. The receiver generates a synchronization signal used to demodulate the data signal by making use of the transmitted chirp signal.

The clock rate which is also the data rate and chirp rate is chosen according to specifications of the matched filter (MF). In this research, a dispersive delay line (DDL) is used as a MF to compress the up-chirp signal.

The received signal and noise are applied to two subsystems in the receiver:

1. Data subsystem,
2. Synchronization subsystem.

Coherent recovery of the data bits is accomplished by utilizing the processed output of the MF.



(a) Transmitter

(b) Receiver

Fig. 10. General Block Diagram

A. TRANSMITTER

The block diagram of the transmitter is shown in Fig. 11. An important task in the transmitter is generation of a usable synchronization signal from the MF output. In this research, the required signal for the DDL matched filter is an up-chirp (linear intra-pulse FM) signal. The specifications of this signal are as follows:

center frequency, $f_o = 3.0$ MHz

bandwidth, $\Delta f = 300$ kHz

pulse duration, $\Delta T = 415$ μsec.

The voltage-controlled-oscillator (VCO) circuit which generates the signal having these specifications is shown in the Appendix. The voltage versus frequency characteristic of the VCO is shown in Fig. 12.

To obtain the repeating chirp signal, a periodic linear ramp voltage is needed. The center frequency of the VCO is obtained by a dc-offset voltage and an external capacitor. Timing and amplitude adjustments of the ramp result in the best chirp signal for the MF. Fig. 13 shows the ramp (top trace) and chirp (bottom trace) waveforms.

Because of the necessity of precise timing in generating the ramp voltage, the ramp is generated first and then the system clock is derived from this voltage. Consequently, the ramp and clock rates are:

$$f_{clock} = \frac{1}{415\ \mu sec} \doteq 2.4\ kHz.$$

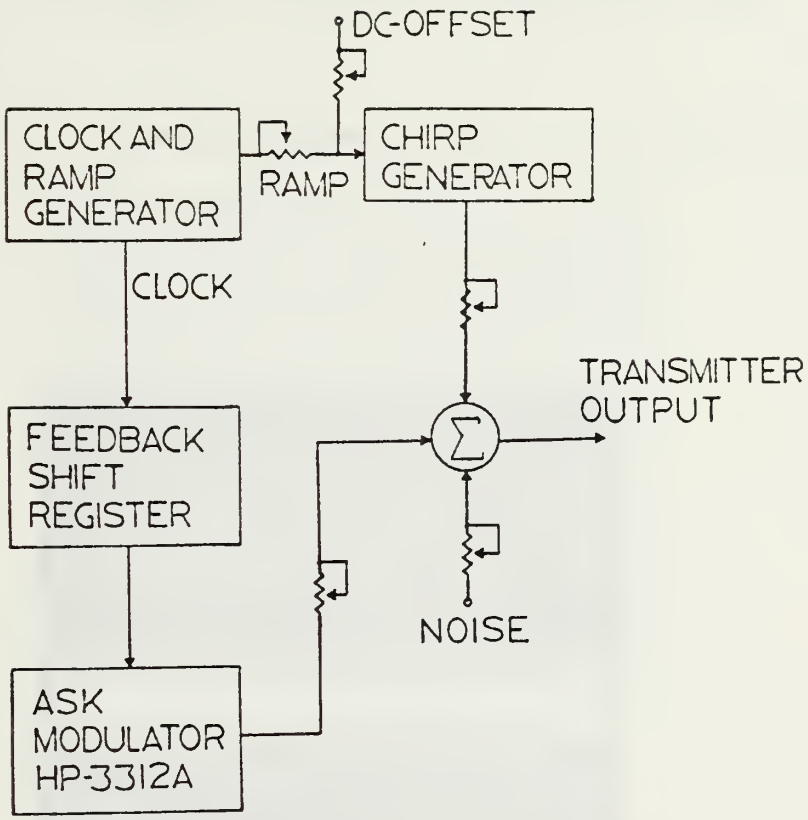


Fig. 11. Transmitter Block Diagram

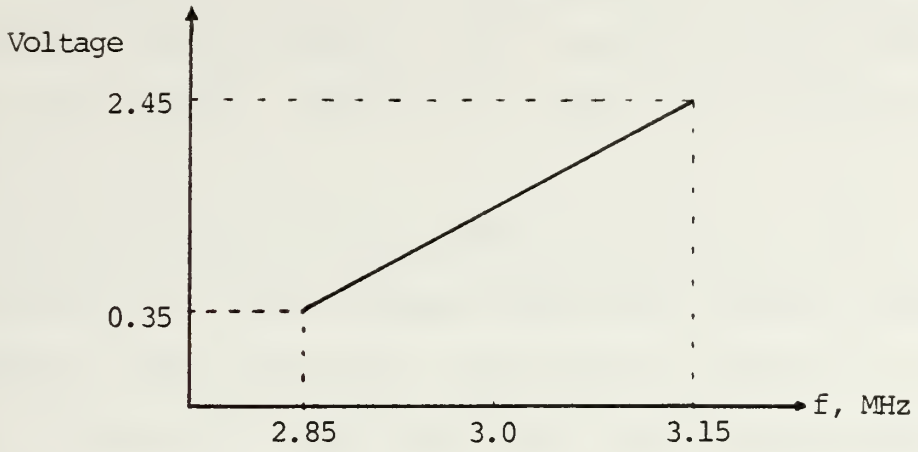


Fig. 12. Voltage-Frequency Characteristic of VCO

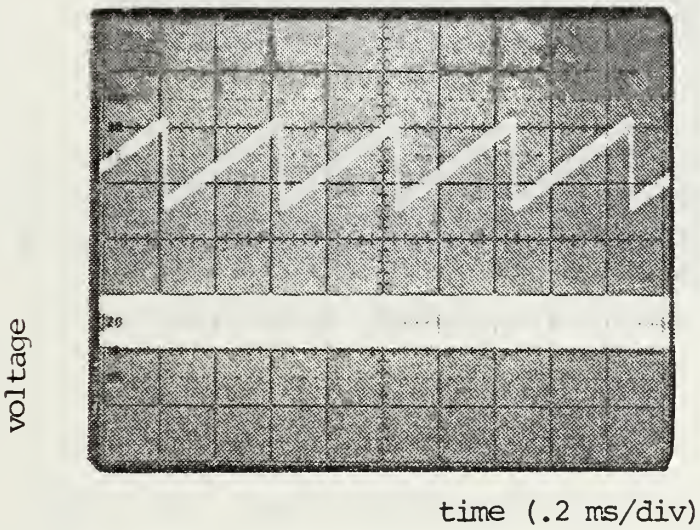


Fig. 13. Ramp and Chirp Waveforms

The random data in the transmitter is simulated using a maximal length feedback shift register (FSR) driven by the system clock. Appendix A-3 shows the schematic of the FSR.

Amplitude shift keying (ASK) is used as carrier modulation. In this system a HP-3312A function generator is used as the modulator. The carrier frequency is 3.0 MHz. Fig. 14 shows the data (top trace) and the modulated carrier (bottom trace).

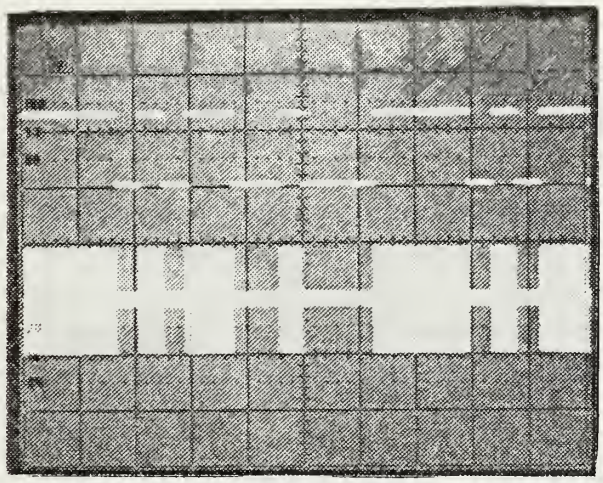


Fig. 14. Data and Modulated Carrier

To obtain the necessary power division between the modulated carrier and the chirp signal, a resistor summing network is used. Gaussian noise is added at this summing point to simulate channel noise. The chirp signal plus modulated carrier plus noise are shown in Fig. 15.

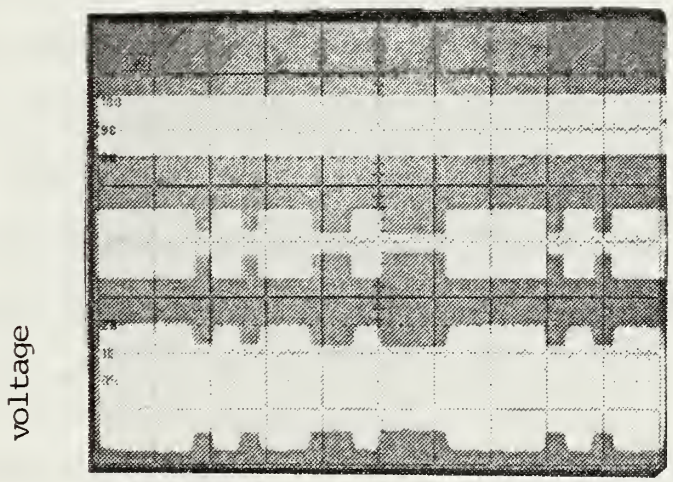


Fig. 15. Periodic Chirp, Modulated Carrier and Summing Network Output Waveforms

B. RECEIVER

A block diagram of the receiver is shown in Fig. 16. The receiver consists of two subsystems:

1. Synchronization subsystem,
2. Data (demodulation) subsystem.

In the receiver both data and sync subsystems receive the same signal plus noise (bottom trace of Fig. 15). These two subsystems function to recover the transmitted data.

1. Synchronization Subsystem

For coherent pulse recovery, a reference signal is needed. These timing pulses are generated in the synchronization subsystem shown in Fig. 17.

As noted previously, the received signal includes a low-level chirp signal. The processing gain (PG) inherent in MF operation is used to detect the chirp signal present amongst the noise and data voltages. The MF specifications are

center frequency	f_o = 3.0 MHz
bandwidth	Δf = 300 kHz
time delay	ΔT = 415 μsec
processing gain,	$T \cdot \Delta f$ = 125 or 21 dB

Fig. 18 shows the input (chirp signal) to the MF and its response.

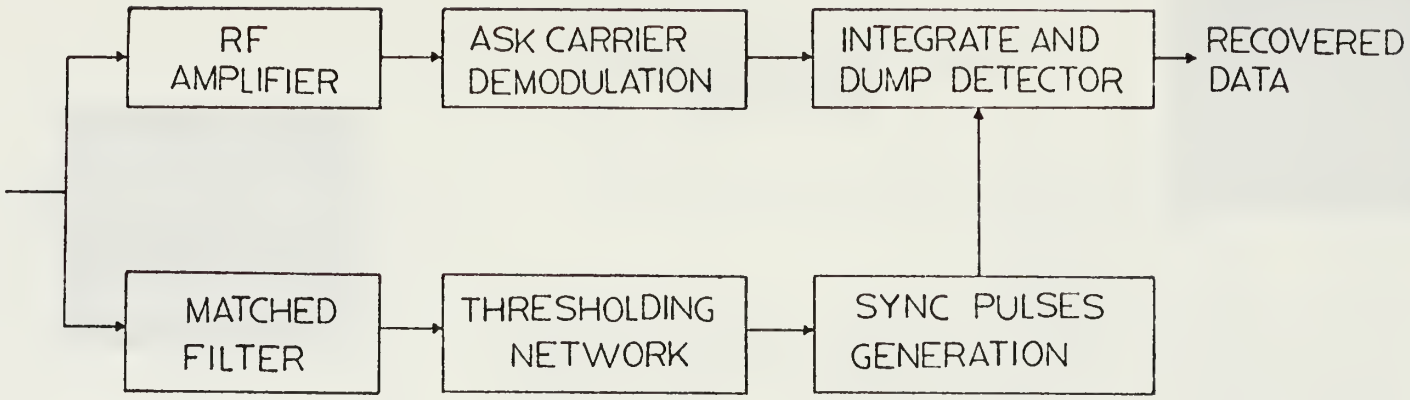


Fig. 16. General Receiver Block Diagram

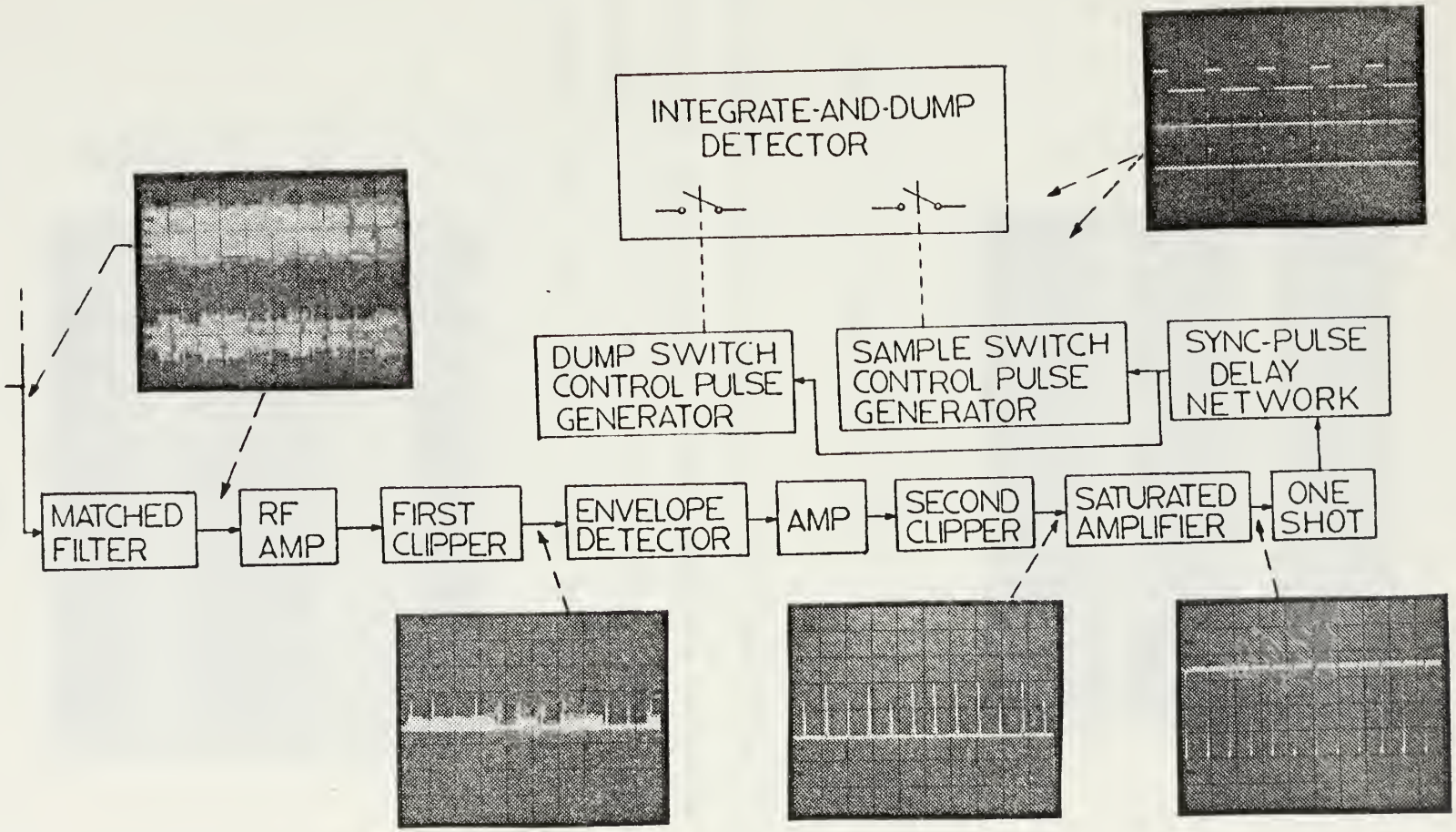
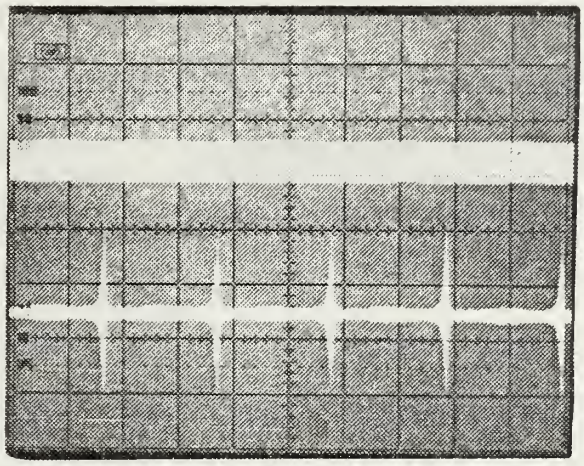


Fig. 17. The Synchronization Subsystem of Receiver

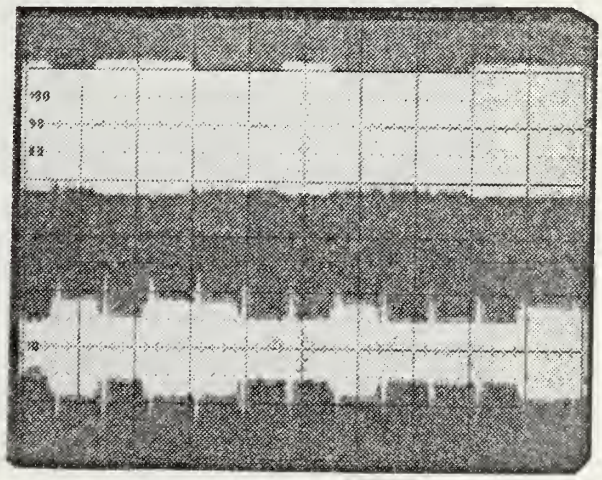


voltage

time (.5 ms/div)

Fig. 18. MF Input and Output

The receiver timing reference is derived from this MF response to the chirp signal. The composite received signal, including noise and data (top trace), and the MF response (bottom trace) are shown in Fig. 19.



voltage

time (.5 ms/div)

Fig. 19. Received Signal and Its MF Response

As shown in Fig. 17, the output of the MF is amplified and applied to a clipper circuit. The clipping level of the first clipper circuit is adjusted to a value depending on the expected signal to chirp power ratio and maximum expected noise level. This circuit serves to suppress the noise and data signals while preserving the response of the MF to the chirp signal.

The output of first clipper is applied to an envelope detector and then amplified. Detailed circuit descriptions are in the Appendix. Fig. 20 shows the MF output (top trace), the thresholding effect (middle trace) and the output of the envelope detector (bottom trace) following the first clipper.

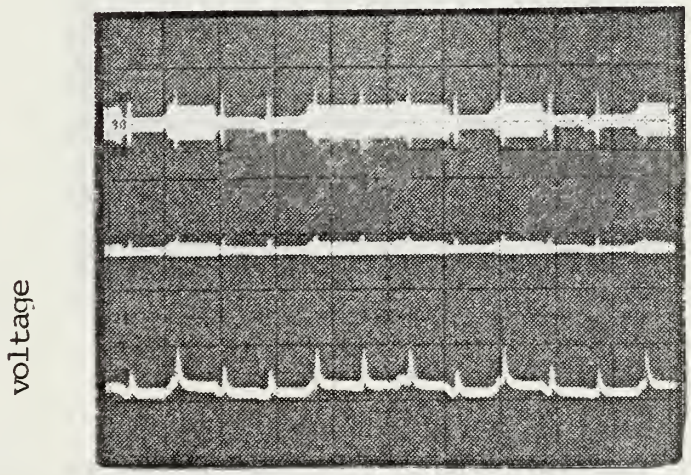


Fig. 20. Waveforms at the Output of MF, First Clipper, and Envelope Detector

A second clipper is used to further reduce the effects of interfering singals on the MF output. To remove amplitude changes at the output of the second clipper, a saturated amplifier is used. This amplified output drives a TTL one-shot circuit. The output of the one-shot is now ready to be used as a time reference synchronization signal. Fig. 21 shows the outputs of the second clipper, saturated amplifier and one-shot. The amplitude variations at the output of the second clipper are apparent (top trace).

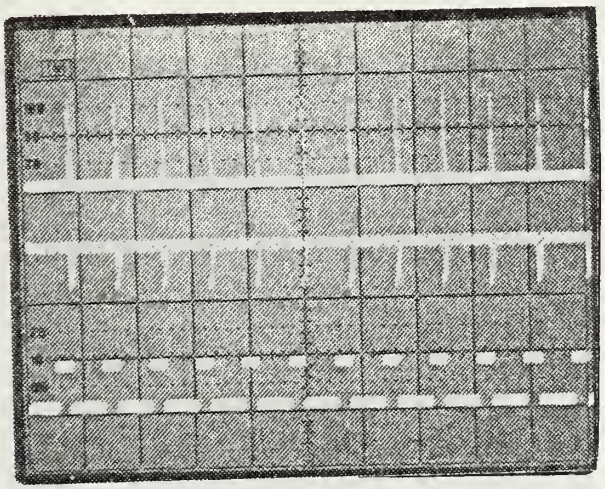


Fig. 21. Second Clipper, Saturated Amplifier and One-Shot Outputs

The sync-pulse delay network receives the output of the one-shot and compensates for the time delay involved in the MF and other circuit. Then the output of this circuit is applied to two circuits which are used to recover the data bits. One circuit generates the sample switch control pulse and the other generates the dump switch control pulse used to sample the integrator contents. The required time adjustment is achieved using the sync-pulse delay network. Fig. 22 shows the sync-pulse delay network output and the switch control generator outputs.

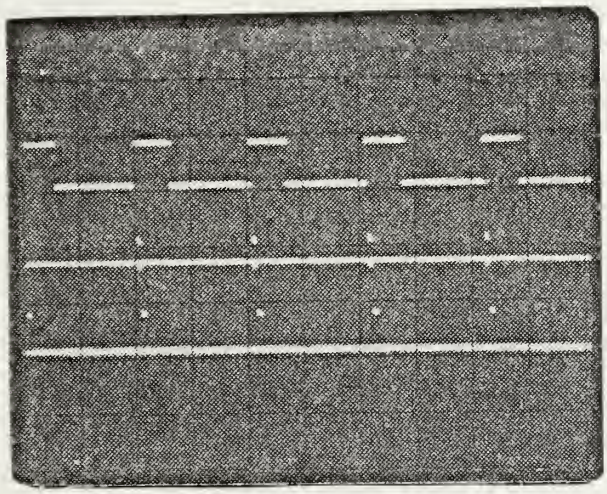


Fig. 22. The Trigger, Sample Switch Control Pulse, Dump Switch Control Pulse

2. Data Subsystem

This subsystem recovers the data in a coherent manner using the timing pulses generated by the sync subsystem.

The first function of this subsystem is carrier demodulation (envelope detection). Then coherent bit recovery is accomplished with the integrate-and-dump circuit. The noisy received signal is applied to a RF amplifier as shown in Fig. 24. The gain versus frequency characteristic of the RF amplifier is shown in Fig. 23.

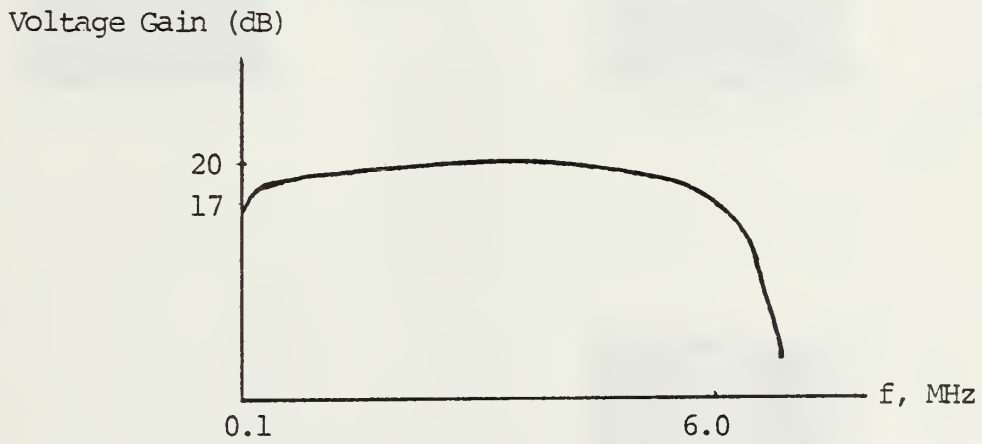


Fig. 23. Frequency Response of RF Amplifier

The RF amplifier output is applied to a band-pass filter (BPF). The frequency response of the BPF is shown in Fig. 25.

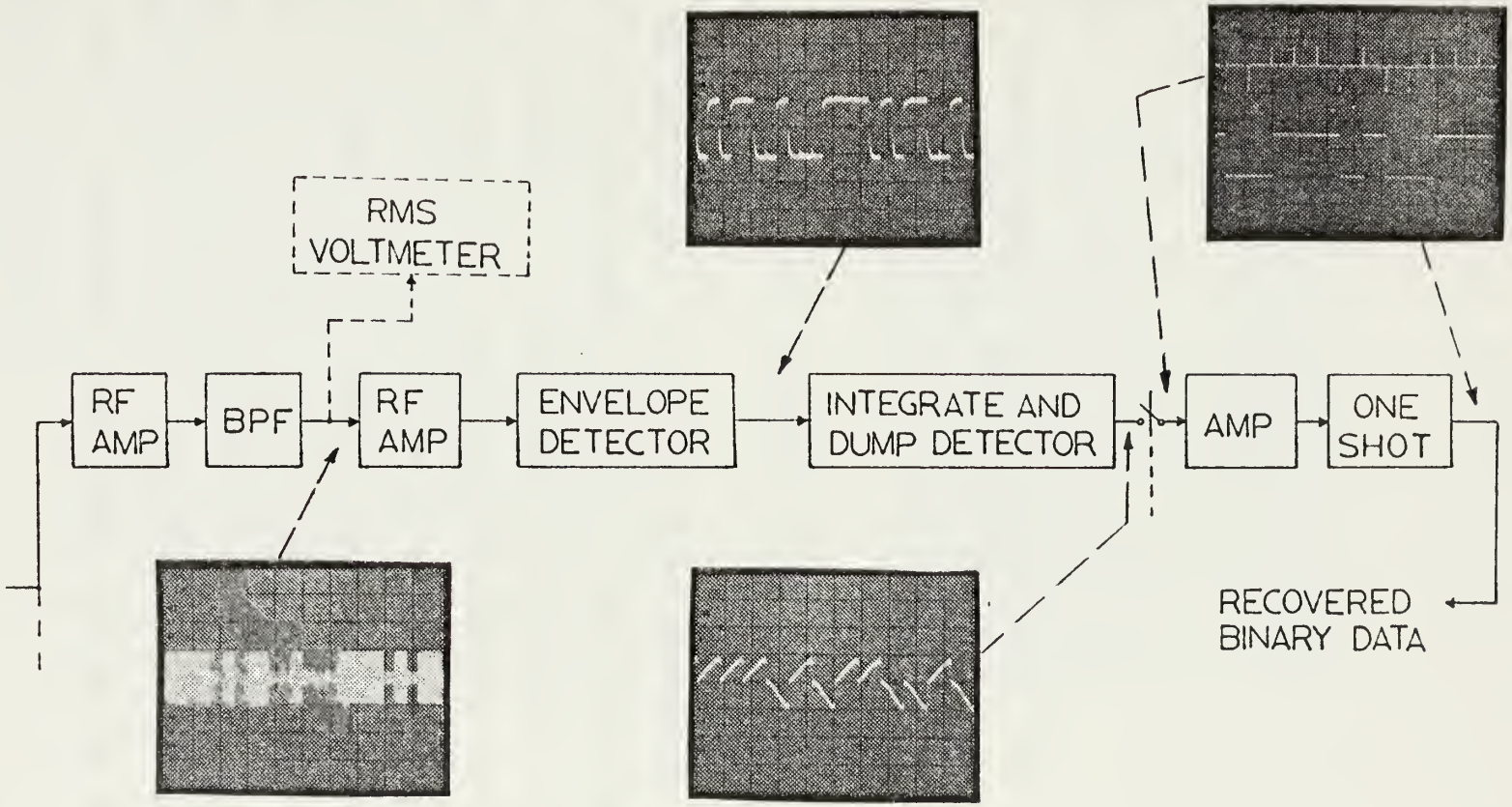


Fig. 24. The Data Subsystem of Receiver

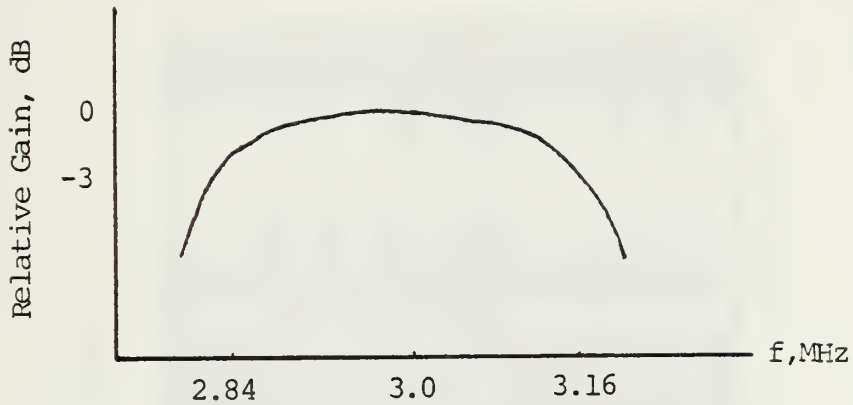


Fig. 25. BPF Frequency Response

The BPF is used to remove those frequency components of chirp and noise signals which are out of the passband of the data signal. In the experimental system, the 3 dB bandwidth of band pass filter is approximately 300 kHz which is the bandwidth of the chirp signal. Consequently, the filter serves only to remove noise terms. Since the data rate is 2.4 kbits/sec, the filter bandwidth need be no greater than about 15 kHz for a conventional system using amplitude modulation. Alternatively, the data bandwidth could be increased to 300 kHz using spread spectrum techniques or multiplexing.

The band pass filter output is amplified again and applied to an envelope detector. Fig. 26 shows the band pass filter and envelope detector outputs.

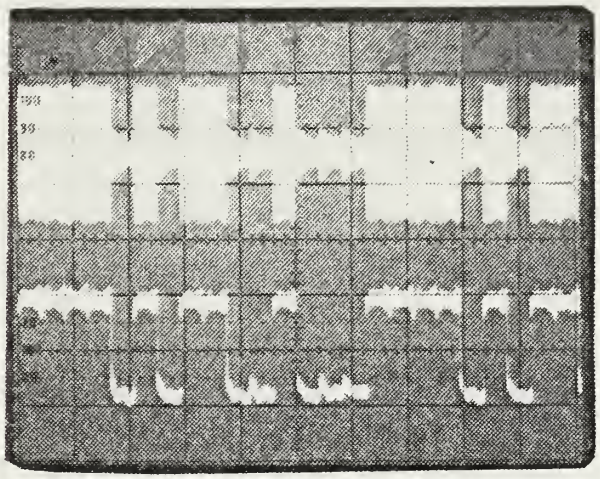


Fig. 26. BPF and Envelope Detector Outputs

The peaks observed at the output of the BPF and envelope detector are caused by the VCO output (chirp) in the transmitter.

The envelope detector output is applied to the integrate-and-dump circuit. The integrator circuit, shown in the Appendix in detail, has an integration time of 415 μsec which is the duration of one data bit. The best data decision occurs after the complete integration of one bit. After sampling the integrator value, the integrator value, the integrator output is set to zero. Then integration of the next data bit is initiated. Sampling

the integrator value and short-circuiting (dumping) the capacitor are accomplished by electronic switches controlled by pulses generated in the synchronization subsystem.

Since the envelope detector output is applied to the integrate-and-dump detector by capacitive coupling, the detector integrates binary ones in a positive direction, and integrates zeros in a negative direction. A proper decision threshold in this case is zero volts. Consequently, there is no other decision circuit used in the system. Fig. 27 shows the input (top trace) and the output (middle trace) of the integrator and the sampled output of the integrate-and-dump detector (bottom trace).

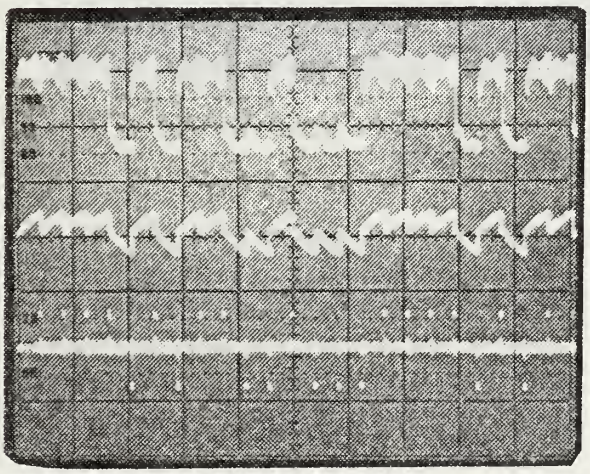


Fig. 27. The Input and Output of Integrate-and-Dump Detector

At this point the receiver decides if the data bit is a zero or one. The decision is in a return-to-zero (RZ) form. This form of the recovered data is amplified to a TTL level to drive a one-shot circuit. The output of the one-shot is the recovered binary data. Fig. 28 shows the input and the output of the one-shot.

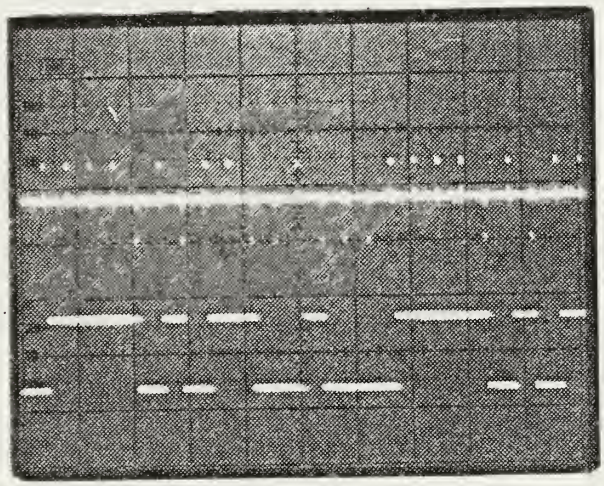


Fig. 28. RZ and Binary Form of Recovered Data at One-Shot

IV. RESULTS

The performance of this experimental system is described by a plot of the probability of error, P_e, versus received signal power-to-noise power ratio, SNR. The received signal power is composed of the amplitude modulated carrier signal power plus synchronization (chirp) signal power. The ratio of these signal components is set in the transmitter. Gaussian noise is used to simulate the noise power present in an actual system. All signal power and noise power measurements are performed after bandpass filtering in the receiver data subsystem as shown in Fig. 24.

P_e vs. SNR measurements are plotted as a function of modulated carrier to chirp power ratio (S/C) as shown in Fig. 29. This figure shows that for a given P_e, as SNR gets smaller, S/C increases which means more chirp power relative to modulated carrier power is required. Conversely, as SNR increases a large S/C (less chirp power) is needed for a constant P_e.

If S/C becomes too small, then performance suffers because an excess amount of chirp power is used at the expense of signal power. Errors then occur in the process of envelope detection (data subsystem). This effect is observed in Fig. 29 for the case of S/C = 2.8 dB. For

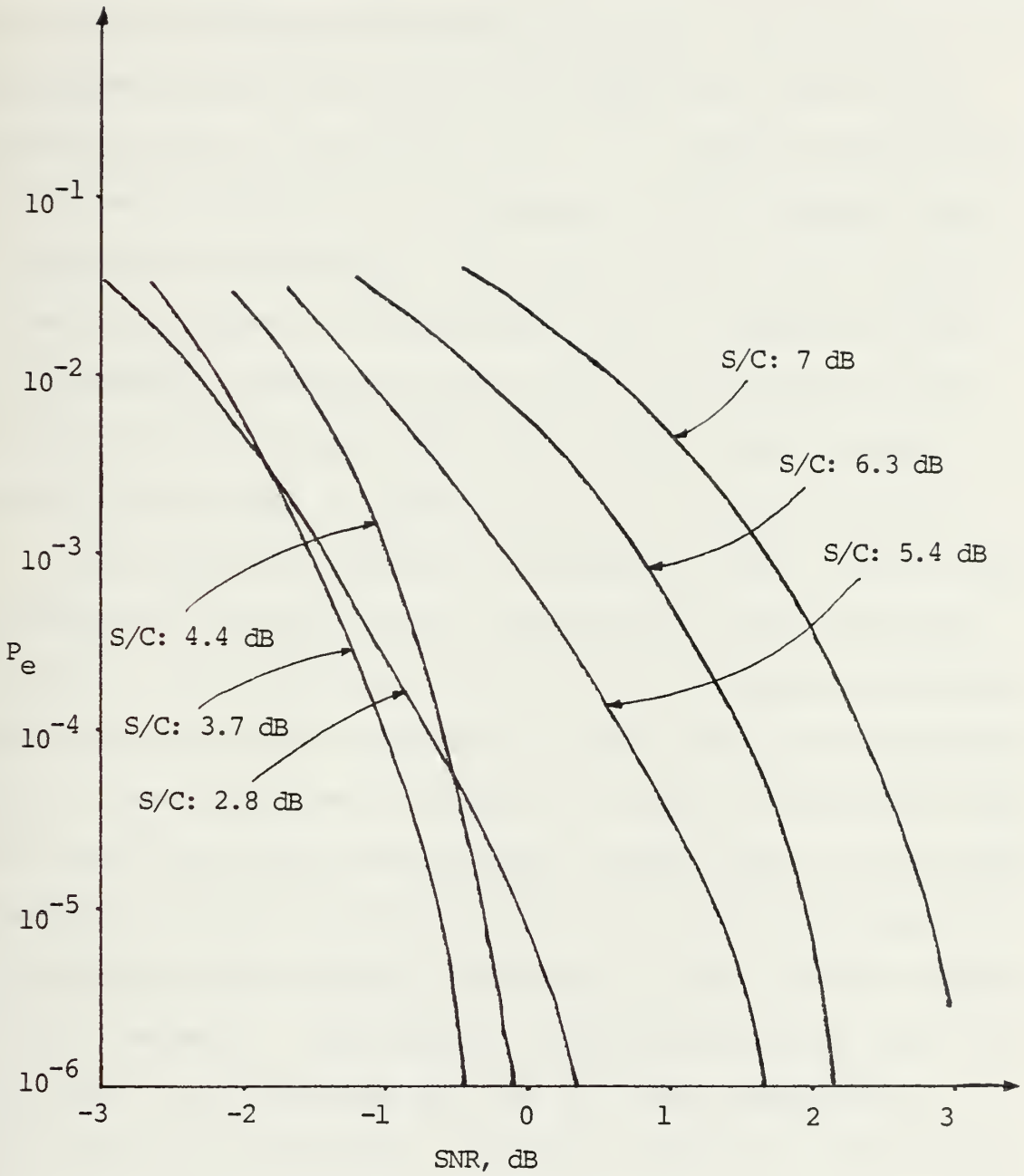


Fig. 29. P_e vs SNR Curves for Experimental System

a given value of SNR, values of S/C greater than 2.8 dB (less chirp power) provide better performance (fewer errors).

System performance is quite dependent on the effectiveness of the integrate-and-dump circuit. This circuit operates properly only when the sample and dump switch pulses occur at the correct time. So, system performance is closely related to the operation of the receiver synchronization subsystem. For large values of SNR and S/C (low chirp power), a large error rate is observed after the integrate-and-dump circuit even though there are no errors in the envelope detector output. These system errors are caused by timing errors in the sync pulses.

The difference between the results of Fig. 29 for the experimental system and the theoretical results plotted in Fig. 5 for noncoherent ASK can be explained as follows. The curves for the experimental system start with negative SNR. Some improvement relative to theory is obtained from the use of an integrate-and-dump circuit after the envelope detector. This circuit behaves like a matched filter for rectangular pulse shapes and hence it is an optimum linear "data" detector. The greatest difference between Fig. 29 and Fig. 5 is caused by the use of a BPF bandwidth of 300 kHz in the receiver. For a bit rate of 2.4 kbits/sec, a realistic bandwidth of the modulated carrier is approximately 15 kHz (assuming transmission of the 3^{rd} harmonic of a 2.4 kHz square wave). This means that the experimental

system possesses approximately 300/15 = 20 times (13 dB) the noise of a practical system. The difference between the curves of Fig. 29 and Fig. 5 is less than 13 dB because in the experimental system, the envelope detector does some filtering.

V. CONCLUSIONS AND RECOMMENDATIONS

A. CONCLUSIONS

It is well known that an integrate-and-dump circuit is useful when receiving rectangular pulses. In this system, a chirp signal is used to operate (synchronize) the integrate-and-dump circuit. This chirp signal interferes with the data modulated carrier. The results of this experiment indicate that the advantages of the integrate-and-dump circuit overcome the effects of the interference of the added chirp signal.

Fig. 30 shows the best S/C ratio obtained which is 3.7 dB. That ratio gives the lowest P_e for small SNR. ($P_e = 10^{-3}$ is a military standard).

B. RECOMMENDATIONS

The system requires a bandwidth of 300 kHz to transmit the chirp signal. The data rate is 2.4 kHz. This difference between system bandwidth and data rate provides an opportunity to spread the data spectrum to realize processing gain in the receiver data subsystem. In the receiver, a wideband matched filter would replace a narrowband filter in this case.

The experimental system uses ASK. It would be of interest to repeat the experiment for FSK and again for PSK which gives lower P_e for the same SNR.

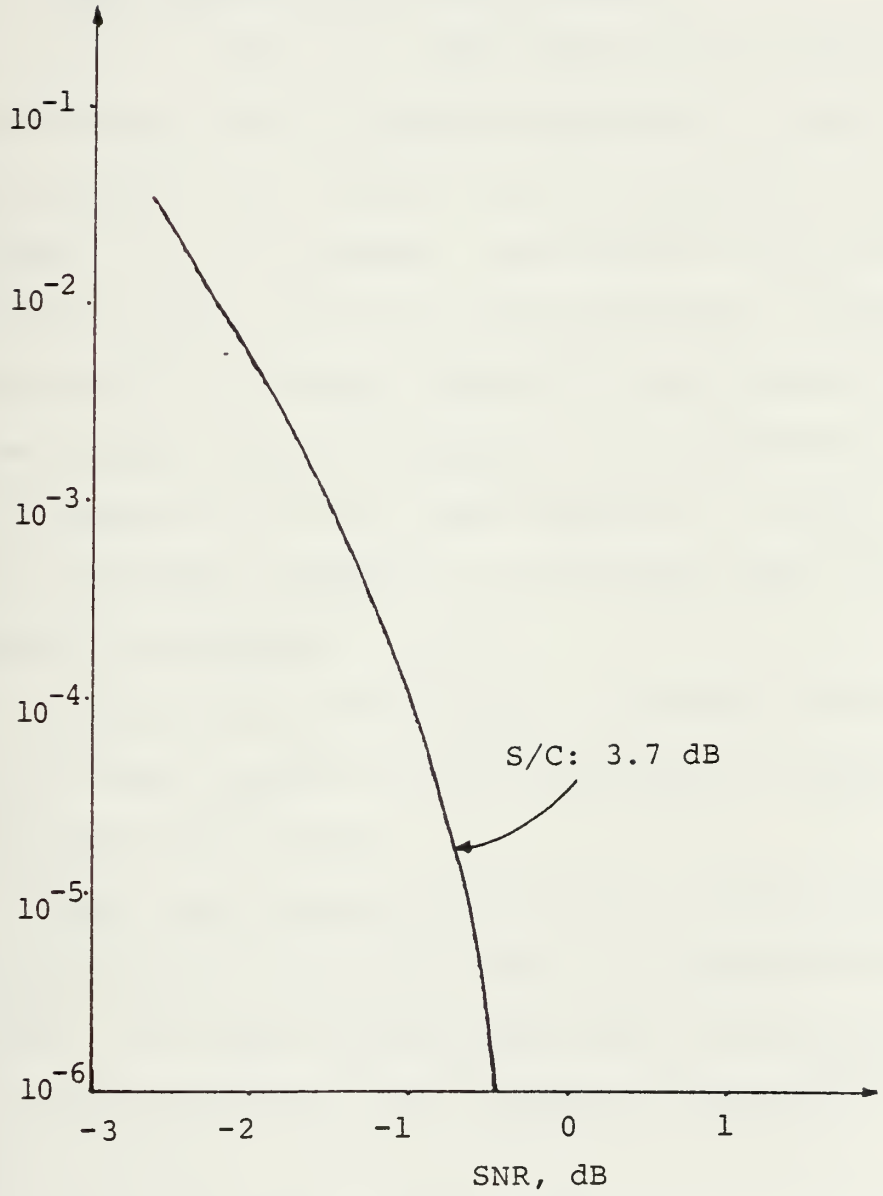


Fig. 30. P_e vs SNR for Best S/C

APPENDIX A

TRANSMITTER CIRCUITRY

1. Ramp Generator and Clock Circuit

Fig. A.1 shows the ramp generator and clock circuitry. An Intersil 8038 IC waveform generator is used to generate the periodic ramp waveform used to generate the chirp signal. In the receiver, the Matched Filter output is used as a time reference (synchronization signal) for coherent bit recovery. Therefore, the periodic ramp is the primary timing reference. The transmitter data clock is generated from this ramp waveform. In this way, the time coherence between the transmitted data and the chirp signal is obtained.

By using the 8038 circuit, the period and the amplitude of the ramp waveform can be controlled to obtain the best Matched Filter output.

The ramp waveform also drives a one-shot mulitivibrator using a 555 IC timer and that circuit generates the system clock. The ramp rate and also clock rate are set at 2.4 kHz by choosing the resistor and capacitor values given in Fig. A.1.

The system clock is used to drive the data register and to synchronize test equipment.

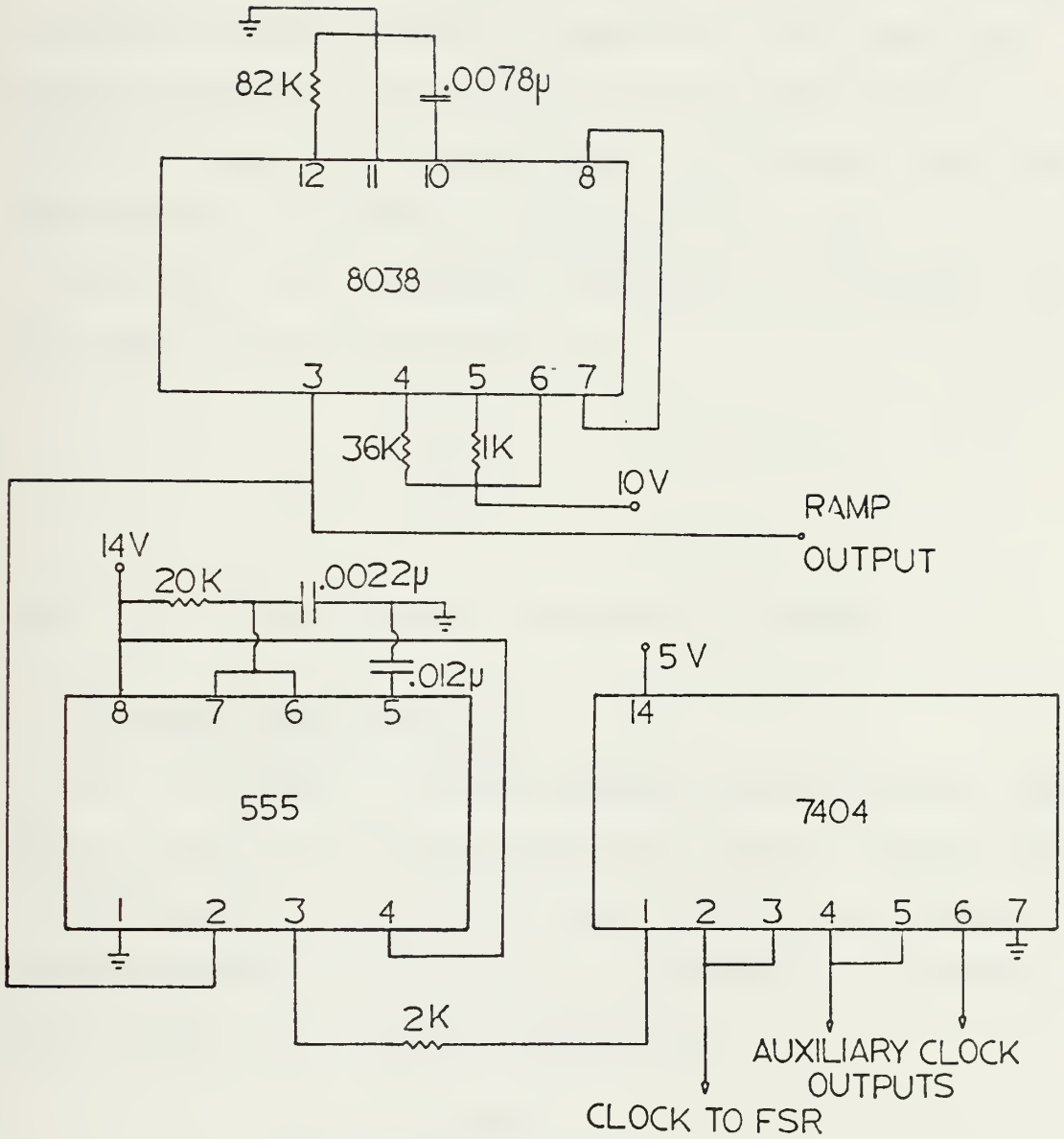


Fig. A.1. Ramp Generator and Clock Circuit

2. Chirp Generator

Fig. A.2 is the schematic of the chirp signal generator. The chirp signal is generated by using a 74LS325 TTL voltage-controlled-oscillator (VCO). The center frequency is set by a single external capacitor. The linear frequency variation (chirp) is obtained by applying the periodic linear ramp voltage plus a DC voltage, which also contributes to the center frequency to the VCO.

For this VCO, the center frequency, f_o, in Hertz, of the output can be approximated as

$$f_o \approx \frac{10^{-4}}{C_{ext}}$$

where C_{ext} is the external capacitor in farads.

3. Feedback Shift Register

Fig. A.3 shows a 4-stage feedback shift register (FSR) which is used to generate random data used in the system. In the case of a 4-stage FSR, the maximal length of the random sequence is 15 bits with the feedback connections shown in Fig. A.3, the bit sequence is

111101011001000 .

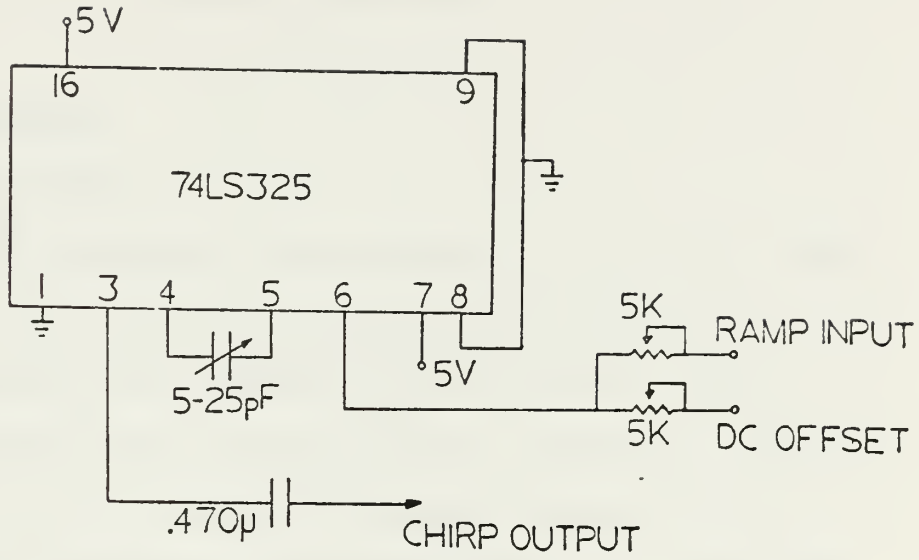


Fig. A.2. Chirp Generator

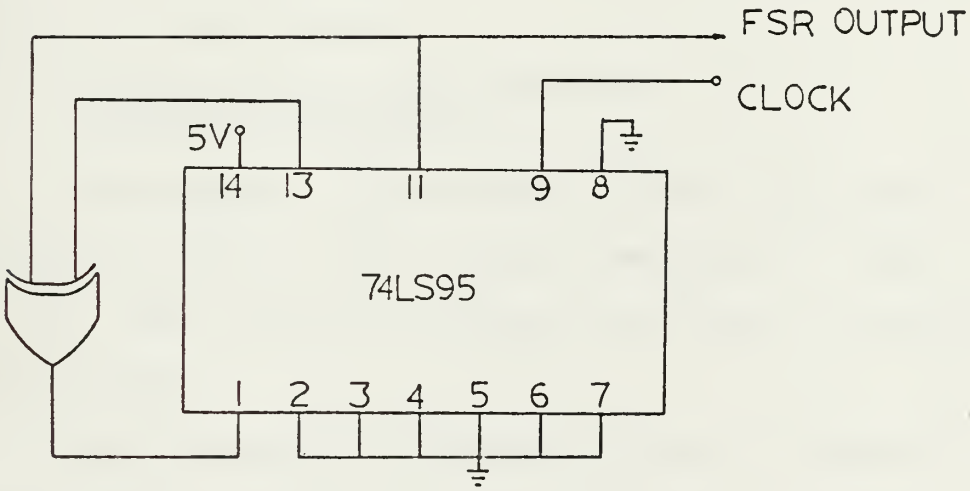


Fig. A.3. Feedback Shift Register (FSR)

APPENDIX B

RECEIVER CIRCUITRY

1. Data Subsystem

a. RF Amplifier

The RF amplifier circuit shown in Fig. B.1.a uses four silicon transistors on a single monolithic chip. It has a relatively wide bandwidth (100 kHz up to 6 MHz).

These amplifiers with different gains are used in the receiver, at the output of Matched Filter in the synchronization subsystem, and before and after the band pass filter in the data subsystem.

The amplifier has a voltage gain of about 20 dB across its 3 dB bandwidth.

b. Bandpass Filter, RF Amplifier and Envelope Detector

The bandpass filter shown in Fig. B.1.b has a 3 dB bandwidth of 300 kHz and a center frequency of 3 MHz ($Q \approx 10$). The attenuation through the filter is approximately 10 dB.

The output of the bandpass filter is applied to the RF amplifier described in section B.1.a of this Appendix. The amplified output voltage is applied to the envelope detector which recovers the data.

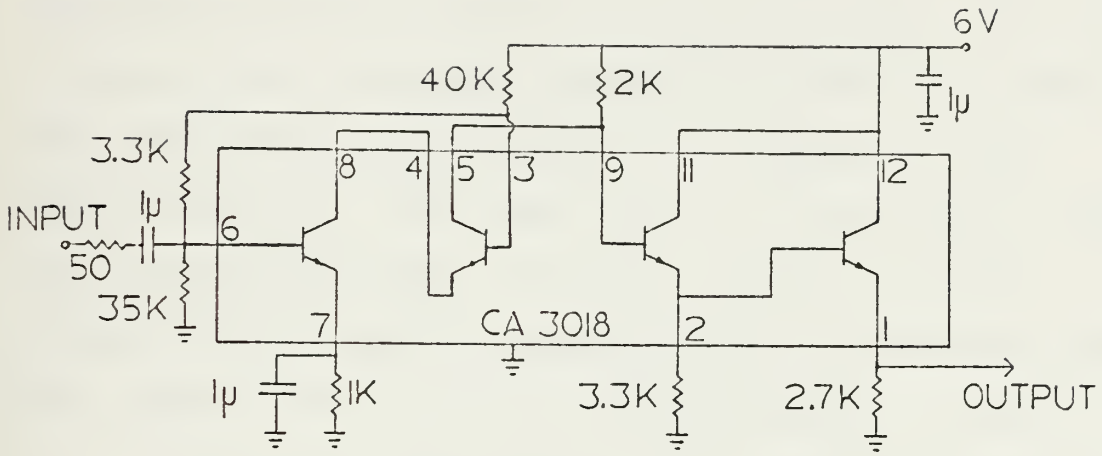


Fig. B.1.a. PF Amplifier

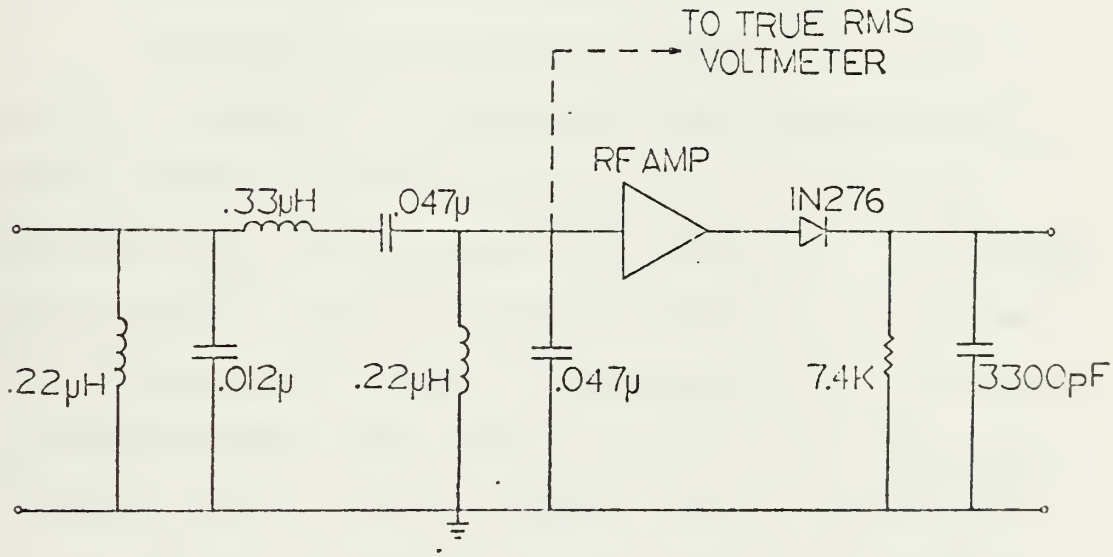


Fig. B.1.b. BPF, RF Amplifier, Envelope Detector Circuits

c. Integrate-and-Dump Detector

Fig. B.1.c is the schematic diagram of the integrate-and-dump detector. A passive RC integrator is used. After integration over the duration of every data bit (415 μsec), a sample of the integrator output is applied to an amplifier and a one-shot multivibrator to reconstruct the binary data bits. The sample switch is closed for 5 μsec. Five microseconds after the sample switch is opened, another switch dumps the capacitor for 10 μsec which sets the output of the integrate-and-dump detector to zero.

A CD 4016 CMOS electronically controlled switch is used to implement the switching needed. Switch control pulses come from the synchronization subsystem of the receiver.

d. Amplifier and One-Shot Multivibrator

The output of the integrate-and-dump detector circuit is applied to an amplifier and a one-shot multivibrator circuit as shown in Fig. B.1.d. An LM 3900 operational amplifier is used as an amplifier. Two stages provide almost 23 dB gain which is enough to drive the 74122 TTL one-shot circuit. The one-shot circuit accepts the Return-to-Zero (RZ) form of the recovered data and provides a unipolar binary output. The bit duration of 415 μsec is set by the RC circuit external to the 74122.

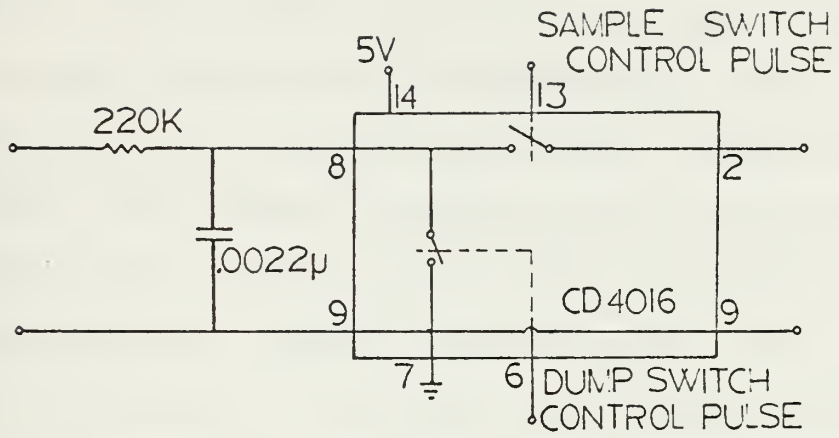


Fig. B.1.c. Integrate-and-Dump Detector

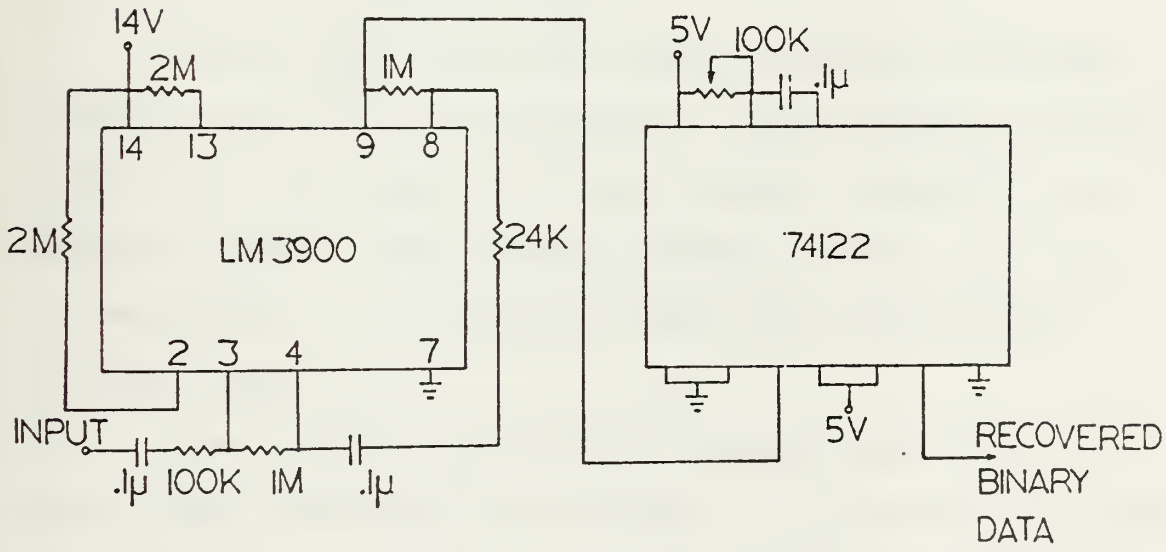


Fig. B.1.d. Amplifier and One-Shot Multivibrator

2. Synchronization Subsystem

a. Clipper, Envelope Detector and Amplifier

The amplified output of the Matched Filter is applied to the first clipper circuit shown in Fig. B.2.a. The clipper removes level changes due to the data and noise which are added to the Matched Filter output voltage spikes. The variable clipping level V_R is set for a certain ratio of data signal power to synchronization signal power and maximum expected noise. The output of the first clipper is applied to an envelope detector. The envelope detector output provides the synchronization signal for the receiver. This information is amplified 20 dB by a 2-stage operational amplifier and then applied to the second clipper.

b. Clipper, Saturated Amplifier and One-Shot Multivibrator

Fig. B.2.b. shows the second clipper, saturated amplifier and one-shot circuitry. Noise and data voltage appearing on the sync signal are further reduced by the second clipper. The variable clipping voltage level V_R is determined by the expected signal and interference voltage levels.

The output of the second clipper saturates a one stage opamp amplifier of 10 dB gain. This amplifier output is applied to a one-shot to generate the receiver sync pulses.

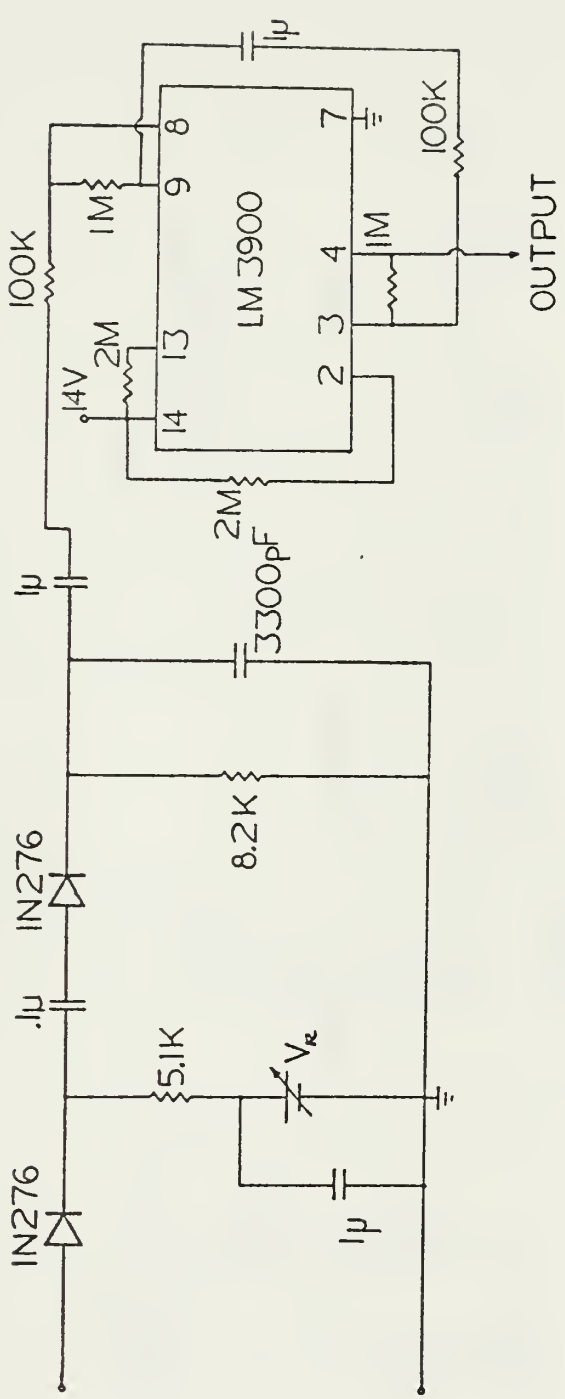


Fig. B.2.a. First Clipper, Envelope Detector and Amplifier Circuit

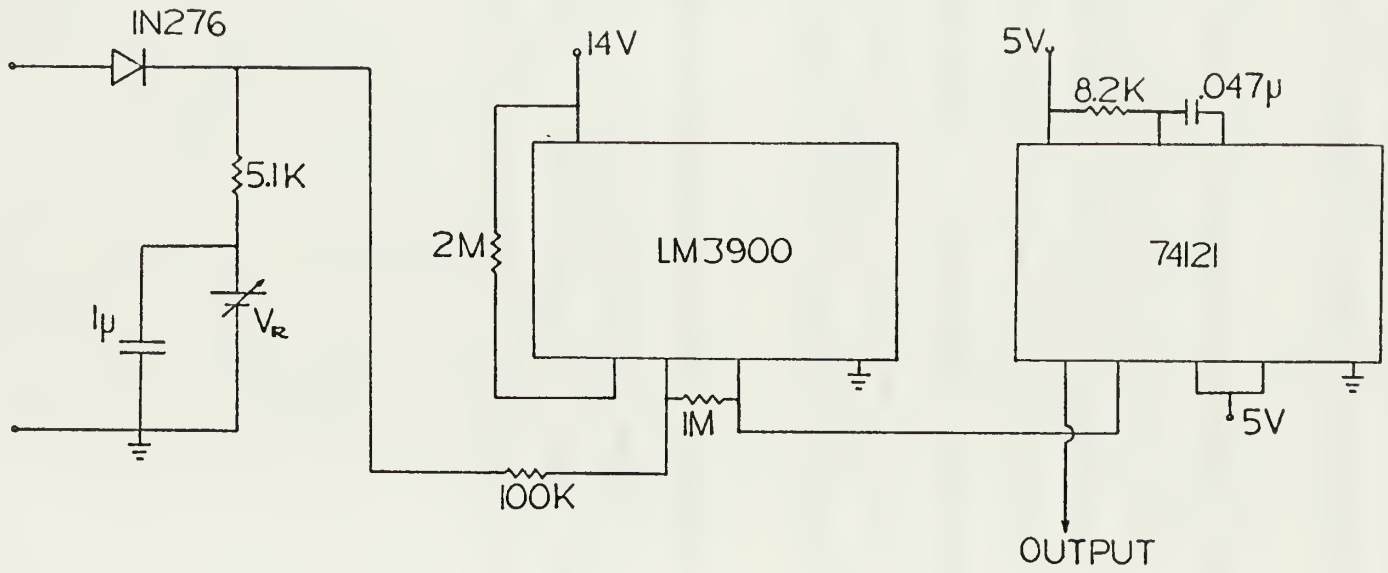


Fig. B.2.b. Second Clipper, Saturated Amplifier and One-Shot Multivibrator Circuits

c. Sync-Pulse Delay Network, Dump Switch/Short Circuit Switch Control Pulse Generators

The circuit shown in Fig. B.2.c receives the sync pulses and generates timing pulses needed to sample the integrator output and to short (dump) the capacitor to ground.

The first 74121 is triggered by the leading edge of the sync pulses. The duration of this output pulse can be varied. The second 74121 is triggered by the trailing edge of the output pulse of the first 74121. In this way, proper time delay is obtained. The pulse width of the output of the second 74121 is set for the time difference between sampling and shorting (dumping) the integrator.

The last two one-shots generate appropriate control pulses to drive the integrator sample switch and integrator dump switch. One triggers on the leading edge and the other on the trailing edge of the second 74121 output.

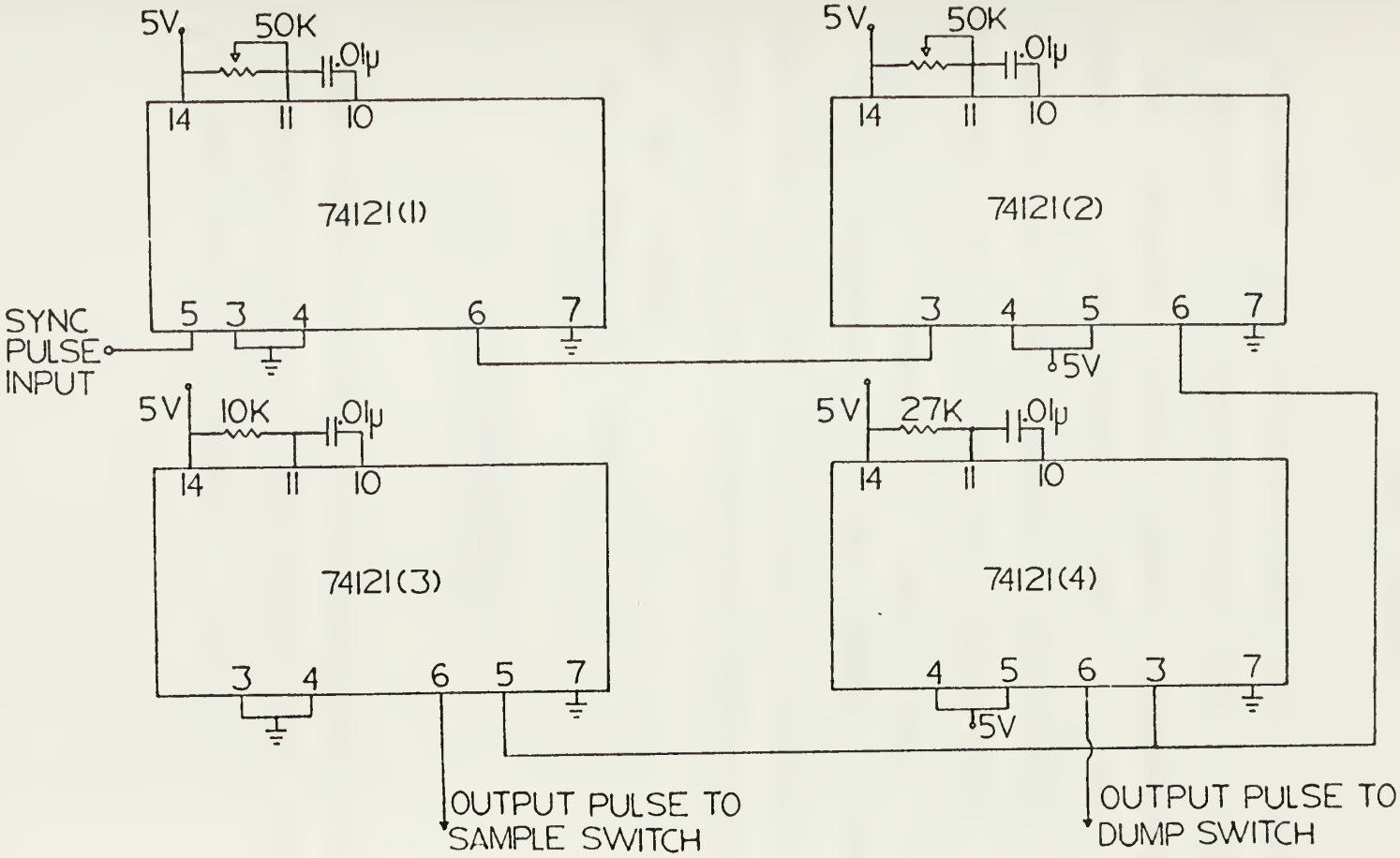


Fig. B.2.c. Sync-Pulse Delay Network, Sample Switch and Dump Switch Control Pulse Generators

APPENDIX C

TEST CIRCUIT

The test circuit shown in Fig. B.2.d is used to measure the error rate as signal-to-noise ratio is varied.

The recovered data and delayed transmitted data are applied to an EXCLUSIVE-OR circuit. Propogation delays in the receiver create spikes at the EXCLUSIVE-OR output when there are no errors in the received data. A one-shot (1) and an AND gate are used to remove these spikes.

Error measurements are made during a 20 second interval determined by another one-shot (2). A trigger pulse applied to this one-shot (2) initiates the count of errors and data bits clock pulses.

The probability of error P_e is

$$P_e = \frac{\text{Error Count}}{\text{Clock Pulse Count}}$$

All signal and noise power measurements were made at the output of the BPF in the receiver data subsystem using a HP-3400A true RMS voltmeter. (See Fig. 24 and Fig. B.1.b.)

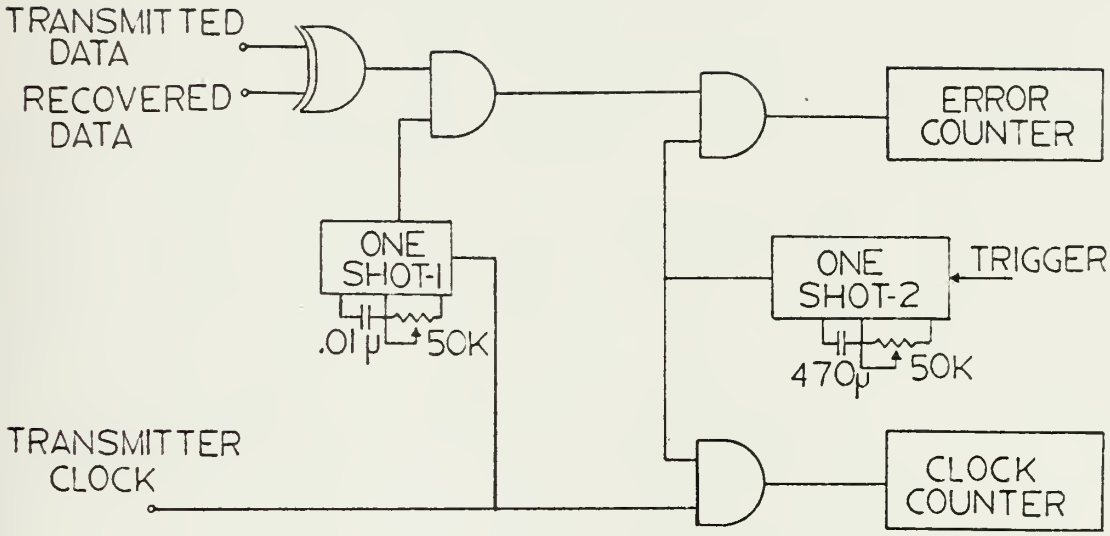


Fig. B.2.d. Test Circuit

LIST OF REFERENCES

1. Ziemer and Tranter, Principles of Communications, p. 329, p. 305-307.

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