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Generalized impedance converter (GIC) filter utilizing composite amplifier

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THESIS

GENERALIZED IMPEDANCE CONVERTER (GIC) FILTER UTILIZING COMPOSITE AMPLIFIER

by

Heng Wan Cheong

September 2005

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A composite operational amplifier utilizing the BiCMOS standard operational amplifier that was designed and introduced in a previous thesis is presented and its improved performance is investigated. The composite amplifier (C20A2) is designed using Silvaco EXPERT and simulated with Silvaco SmartSpice. The results show the gain bandwidth product (GBWP), common mode rejection ratio (CMRR), and open loop gain are considerably improved. This sets the basic foundation for future students to incorporate the newly designed composite operational amplifier into the GIC filter to further enhance filter performance.

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GENERALIZED IMPEDANCE CONVERTER (GIC) FILTER UTILIZING COMPOSITE AMPLIFIER

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EXECUTIVE SUMMARY

Electronic filters and their circuit applications can be found in almost any vital military systems hardware. They play an essential role in all comminaction systems, aviation electronis, GPS receivers, as well as in most digital systems. The use of an analog filter can eliminate some of the errors that occur during analog–to–digital conversion, digital processing, and digital–to–analog conversion. This thesis presents a continuous analog generalized impedance converter (GIC) 4th–order band pass Filter. MATLAB, P–SPICE and MAPLE software are utilized to simulate various circuit parameter changes in the Ideal and Non–Ideal GIC filter, such as network sensitivity, effects of resistor value, capactor value and reduction of the gain bandwidth product (GBWP), on the center frequency and Q factor. All simulated results are used to evaluate the actual circuit implementation prior to future GIC filter chip fabrication. The center frequency and Q factor are affected by capacitor values changes. The reduction of GBWP reduces the gain, center frequency and Q factor. All the P–SPICE program values, when compared to MATLAB program values, are well within a 10% error.

This thesis also researched the composite amplifier originally introduced by Professors Sherif Micheal and Wasty B. Mikhael at West Virginia University. The composite amplifier (C20A2) has shown that the GBWP, common mode rejection ratio (CMRR) and open loop gain have improved considerably. A composite operational amplifier, utilizing the BiCMOS standard operational amplifier that was designed and introduced in a previous thesis, is presented and its improved performance was investigated. This sets the basic foundation for future research to incorporate the newly designed composite operational amplifier into the GIC filter to enhance filter performance further.

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I. INTRODUCTION

A. BACKGROUND

Integrated circuit technology has seen a great deal of change in the past 30 years. Many advances have been made with digital circuits. Digital circuitry of the 2000's is capable of performing very complex computation functions. However, as good as digital circuits have become, they must still interface with the analog world. This is particularly true, especially in advanced military systems where the use of digital hardware is becoming more popular.

Filters are the main components in many electronic circuits. Electronic filters were initially constructed from resistors, capacitors, and inductors. They were complex, costly, and sensitive to component variation. Operational amplifiers (op–amps) allowed the construction of active filters, which can eliminate a costly passive element, the inductor.

In this thesis, the generalizedd impedance converter (GIC) 4th–order band pass filter presented is one of the common analog filters that can be used to aid in the interface between the digital and analog worlds. The GIC filter has proven itself a robust design that is highly insensitive to component variation.

B. OBJECTIVE

The primary objective of the research was to investigate the continuous analog Generalized Impedance Converter 4th–order band pass filter, ideal and non–ideal cases, in detail with software aids such as MATLAB, P–SPICE and MAPLE. Simulated results were used to compare the actual circuit implementation prior to future GIC filter chip fabrication.

The secondary objective was to investigate the previously designed BiCMOS standard operational amplifier, introduced in a former research [7], to be utilized to improve the performance of the composite operational amplifier. This sets the basic foundation for future students to incorporate the newly designed composite operational amplifier into the GIC filter to enhance filter performance further.

C. RELATED WORK

Previous theses have focused on the design of a standard operational amplifier. The latest design was developed by LCDR Paul R. Milne [7], who replaced the CMOS operational amplifier with a BiCOMS version. This thesis uses LCDR Paul R. Milne's design as a basis to improve it as a composite operational amplifier.

D. THESIS ORGANIZATION

All the basic analog material are included assuming the reader has no analog filter background. Chapter II discusses the basic types of filters and components used. It outlines the two main type of filters, passive and active, as well as the advantages and disadvantages of each type. The ideal and non–ideal characteristics, transfer function, and filter types of the GIC filter are also discussed. Chapter III discusses the VLSI design flow, the fabrication process, and some basic layouts for the common gates.

Chapter IV introduces the composite amplifier and investigates the author's simulated circuits and compares them to the standard operational amplifier. Chapter V focuses on a continuous analog Generalizedd Impedance Converter (GIC) 4^{th} order band pass filter. The effect of varies parameter such as network sensitivity, effects of resistor values, capactor values and GBWP on center frequency and Q factor are presented. All simulated results are used to evaluate the actual circuit implementation prior to future GIC filter chip fabrication. Chapter VI summarizes the results and makes further recommendations for future research topics.

II FILTERS

A FILTER BASICS

In this chapter a brief background on filters is presented. A filter is a device that consists of a group of components including resistors, capacitors, inductors and sometimes active devices such as operational amplifiers. The primary purpose of most filters is to modify the amplitude response of a circuit to a signal so that certain frequencies are attenuated or blocked, while others pass through unchanged. [1]

Most filters are placed in a group based on frequency ranges that are attenuated or passed. Generally, the ideal transmission characteristics of the four major filters are the low–pass (LP) filter (which passes low frequencies), the high–pass (HP) filter (which passes high frequencies), the band–pass (BP) filter that passes a limited range of midband frequencies, and the notch (N) filter (which is a type of band–stop filter that acts on a particularly narrow range of midband frequencies). Table 1 shows these characteristics. These idealized characteristics are known as brick–wall type responses because of their vertical edges. [2]

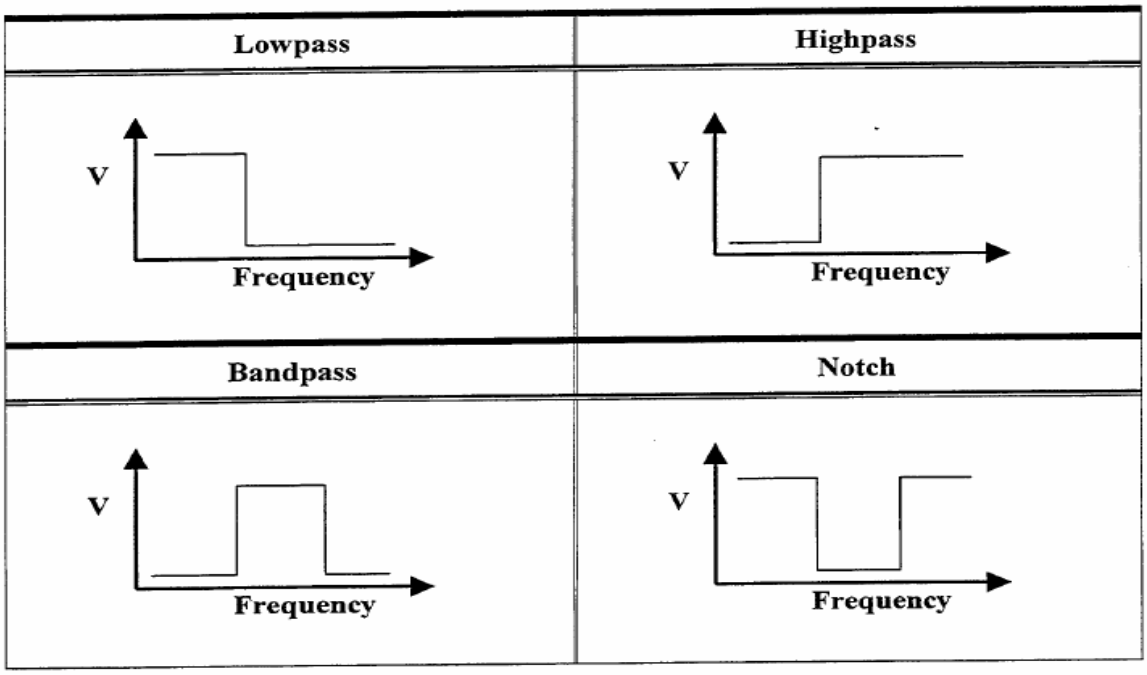


Table 1. Ideal Frequency Response of the Four Basic Filter Types. (From [2])

1. Filter Types

a. Low–Pass Filter (LP)

A low–pass filter is a filter that allows low frequencies to pass through but attenuates high frequencies [2 &3]. Low–pass filters are used to block unwanted high–frequency signals, while passing the lower frequencies. The low frequencies to be filtered out are relative to the unwanted higher frequencies and, therefore, do not have a definitive range. The frequencies that are cut vary from filter to filter. They are also called treble cut filters. They are the opposite of high–pass filters.

One example of low–pass filters is a physical barrier acting as a low–pass filter for waves. When music is playing in another room, the low notes are easily heard, while the high notes are largely filtered out. Similarly, very loud music played in one car is heard as a low throbbing by occupants of other cars since the closed vehicles and air gap function as a very low frequency low–pass filter.

Low–pass filters are also used in subwoofers and other types of loudspeakers to block high pitches that they cannot efficiently reproduce. Radio transmitters use low–pass filters to block harmonic emissions, which might cause interference with other communications.

b. High–Pass Filter (HP)

A high–pass filter passes 'high' frequencies fairly well, but attenuates 'low' frequencies. Hence, it is useful as a filter to block any unwanted low frequency components of a complex signal while passing the higher frequencies, which is better known as a bass–cut filter [2 &3]. Of course, the meanings of 'low' and 'high' frequencies are relative.

The simplest high–pass filter consists of a capacitor in series with the signal path in conjunction with a resistor parallel to the signal path. The resistance times the capacitance (*RC*) is the time constant and its reciprocal is the cutoff frequency, at which the output voltage is 70.7% of the input. Such a circuit might be used in combination with a tweeter and a loudspeaker.

c. Band–Pass Filter (BP)

A band–pass filter passes a limited range of frequencies, and possibly is created as a combination of a low–pass filter and a high–pass filter [2 &3].

A band–pass filter will allow only frequencies to pass that are in a previously specified range. For example, in atmospheric sciences, it is common to perform band–pass filtering of the data with a period range of, say 3 to 10 days, so that only cyclones remain as fluctuations in the fields.

A band–pass filter is an electronic circuit that passes through signals between two given frequencies. For example, an ideal band–pass filter might allow all signals to pass above 30 Hz but below 100 Hz. All signals outside this range are attenuated.

In practice, most band–pass filters do not attenuate frequencies just outside the desired frequency range completely.

d. Notch Filter

A notch filter, also called a narrow band–stop filter or T–notch filter, is an electronic filter typically used when the high frequency and the low frequency are less than 1 to 2 decades apart. In other words, the high frequency is less than 10 to 20 times the low frequency [2 &3].

In the audio band, a notch filter uses high and low frequencies that may be only semitones apart [2].

2. Filter Quality Factor

The quality factor, or "Q", is a parameter used to describe the selectivity performance of a filter. For a first–order filter, the Q parameter relates the distance of the filter pole to the $j\omega$–axis. For a more selective filter, the Q value must be high. A high Q implies that the poles of the filter have to be closer to the $j\omega$–axis. The Q of a filter can be calculated by taking the inverse of the normalized bandwidth of the filter. Calculations for normalization can be achieved by using the half power (3dB) point of the filter. Figure 1 illustrates the Q calculation. [3]

$$Q = \frac{\omega_0}{\omega_1 - \omega_2} \tag{2.1}$$

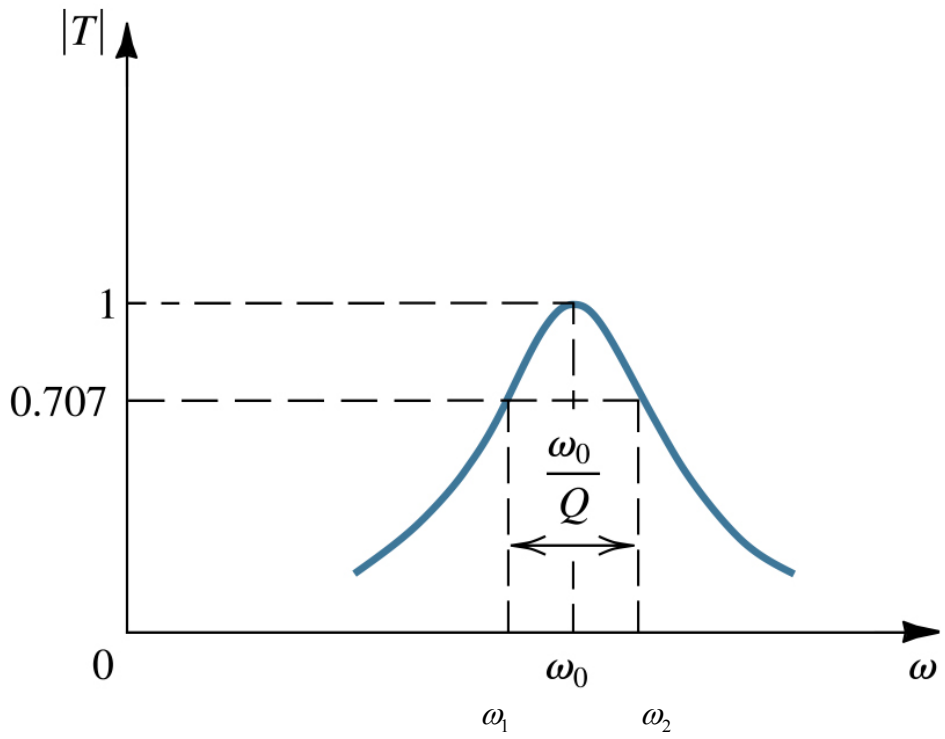


Figure 1. Quality Factor for a Band–Pass Filter (From [3])

B. PASSIVE FILTERS

The simplest electronic filters are based on combinations of resistors, inductors and capacitors. Since resistance has the symbol *R*, inductance the symbol *L* and capacitance the symbol *C*, these filters exist in so–called RC, RL, LC and LCR varieties. All these types are collectively known as passive filters, because they are activated by the power in the signal and not by an external power supply.

The figures in Table 2 show the *RLC* network and the non–ideal response characteristics of the four basic types of filters. Although ideal filters cannot be realized, their concepts aid in filter analysis. Non–ideal filters, unlike their ideal counterparts, do not transition perfectly but have a transition band from the pass–band to the stop–band.

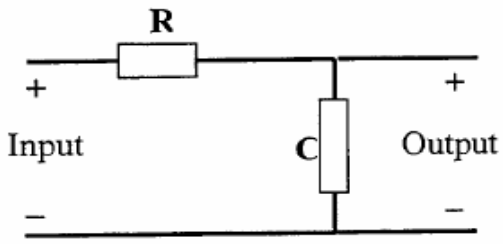
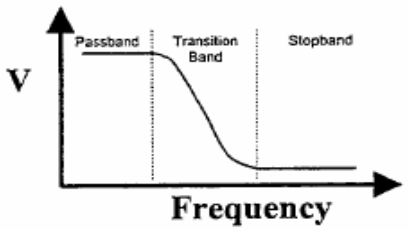
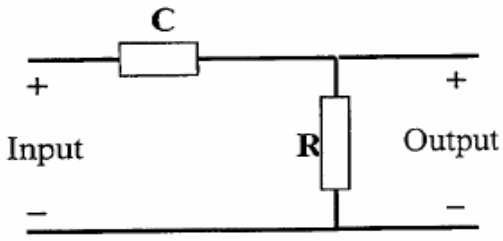
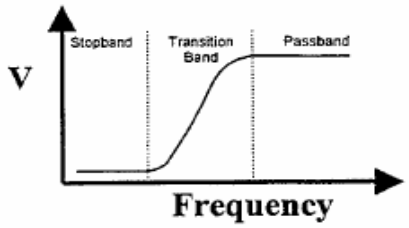
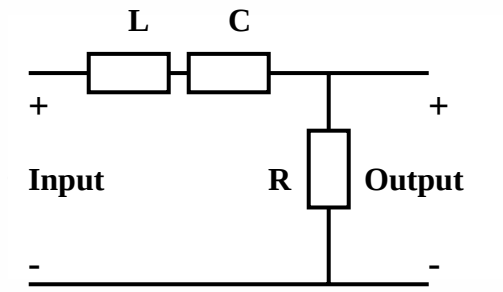
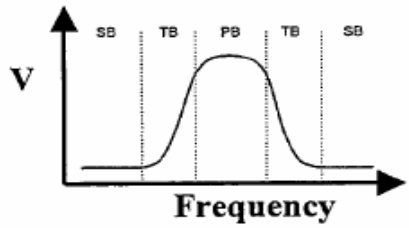
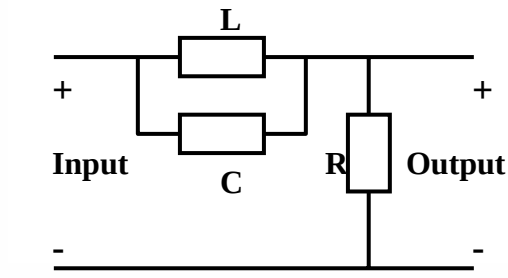
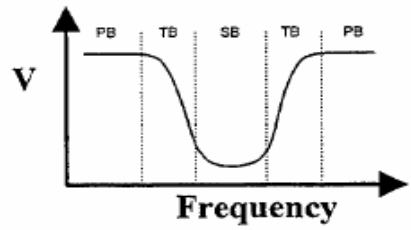
RC Low-Pass Filter	Non-Ideal Response
	
RC High-Pass Filter	**Non-Ideal Response**
	
RLC Band-Pass Filter	**Non-Ideal Response**
	
RLC Notch Filter	**Non-Ideal Response**
	

Table 2. Non–Ideal Filters Response [From 3]

1. How Passive Filters Work

Inductors block high–frequency signals and conduct low–frequency signals, while capacitors do the reverse. A filter in which the signal passes through an inductor, or in which a capacitor provides a path to ground, therefore transmits low–frequency signals more strongly than high–frequency signals and is a low–pass filter. If the signal passes through a capacitor, or has a path to ground through an inductor, then the filter transmits high–frequency signals more strongly than low–frequency signals and is a high–pass filter. Resistors on their own have no frequency–selective properties, but are added to inductors and capacitors to determine the time–constants of the circuit, and therefore, the frequencies to which it responds [2 &3].

At very high frequencies above approximately 100 megaHertz, sometimes the inductors consist of single loops or strips of sheet metal, and the capacitors consist of adjacent strips of metal. These are called stubs. It is possible to add other components to LC filters to make them more precise.

2. Mathematical Model

Filter characteristics are specified using a mathematical model, the transfer function. The exponential degree of the denominator is known as the order of the filter. To achieve all the basic filter types, the transfer function must be at least second order.

Based on the mathematical model, the actual physical filters using the resistors (*R*), capacitor (*C*) and inductor (*L*) can be realized. Table 3 shows the generalizedd transfer functions for each filter type. The center frequency is given by ω_p, while Q_p gives the quality factor, and a_i is a constant. [3]

Filter Type	Transfer Function
Low-Pass	$T(s)=\frac{a_0}{s^2+\frac{\omega_p}{Q_p}s+\omega_p^2}$
High-Pass	$T(s)=\frac{a_2 s^2}{s^2+\frac{\omega_p}{Q_p}s+\omega_p^2}$
Band-Pass	$T(s)=\frac{a_1 s}{s^2+\frac{\omega_p}{Q_p}s+\omega_p^2}$
Notch	$T(s)=\frac{s^2+\omega_p^2}{s^2+\frac{\omega_p}{Q_p}s+\omega_p^2}$

Table 3. Transfer Function of Four Basic Filter Types. (From [3])

C. ACTIVE FILTER

Active filters are a special kind of electronic filter. They use additional energy than that of the signal to filter the signal. They are commonly constructed using an operational amplifier.

The topologies correspond to *R* and *C* components along a retro alimented loop around the operational amplifier. These can have high Q, and achieve resonance without the use of inductors. However, their upper frequency limit is lower than that of a passive filter. Some common kinds of filters are Chebyshev, Butterworth, Bessel, Gaussian, Sallen and Key, and Elliptic.

1. Operational Amplifier

An operational amplifier or op–amp is an electronic circuit module normally built as an integrated circuit, which has a non–inverting input (+), an inverting input (–) and one output. The output voltage is the difference between the + and – inputs multiplied by the open–loop gain $V_{out} = (V_+ - V_-) * G_{openloop}$. Since op–amps have uniform parameters and often standardized packaging as well as standard power supply needs, they help in

designing an application quickly. Figure 2 illustrates a typical circuit symbol for an op–amp, where V_{+} is the non–inverting input, V_{-} the inverting input, V_{out} the output, V_{S+} the positive power supply and V_{S-} the negative power supply.

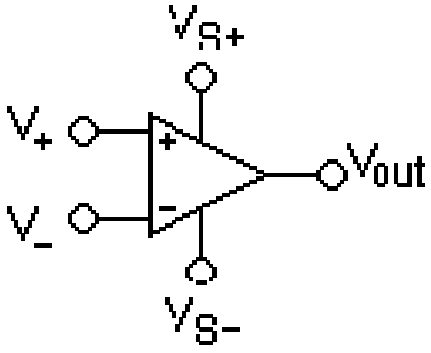


Figure 2. Op–Amp Symbol

The power supply pins (V_{S+} and V_{S-}) can be labeled in many different ways. For field–effect–transistor (FET) based op–amps, the positive, common drain supply is labeled V_{DD} and the negative, common source supply is labeled V_{SS}. For a bipolar junction transistor (BJT) based opamps, the V_{S+} pin becomes V_{CC} and V_{S-} becomes V_{EE}. They are also sometimes labeled V_{CC+} and V_{CC-}, or even V_{+} and V_{-}, in which case the inputs would be labeled differently. The function remains the same. Often these pins are not included in the diagram for purposes of clarity, and the power configuration described or assumed from the circuit.

The input pin polarity is often reversed in diagrams for clarity. In this case, the power supply pins remain in the same position. The more positive power pin is always on the top, and the more negative on the bottom. The entire symbol is not flipped; only the inputs.

a. dc Behavior

Open–loop gain is defined as the amplification from input to output without any feedback applied. For most practical calculations, the open–loop gain is assumed to be infinite. This allows the gain in the application to be set simply and exactly by using

negative feedback. Of course, theory and practice differ, since op–amps have limits that the designer must keep in mind and sometimes adjust the work.

b. ac Behavior

The op–amp gain calculated at dc does not apply at higher frequencies. This effect is due to limitations within the op–amp itself, such as its finite bandwidth, and to the ac characteristics of the circuit in which it is placed. The best–known impediment in designing with op–amps is the tendency for the device to resonate at high frequencies, where negative feedback changes to positive feedback due to internal parasitics capacitances.

c. Applications

The op–amp can be used for various applications such as audio and video pre–amplifiers, voltage comparators, differential amplifiers, differentiators and integrators, filters, precision rectifiers, voltage and current regulators, analog calculators, analog–to–digital converters, digital–to–analog converters and many more.

The operational amplifier is thus called because it performs mathematical operations by using voltage as an analog of another quantity. This is the basis for the analog computer. As mentioned before, the generic op–amp differential gain is given by:

$$Vout = G\,(V+ - V-). \tag{2.2}$$

G is the open–loop gain of the op–amp. The inputs are assumed to have very high impedance, and negligible current will flow into or out of the inputs. Op–amp outputs have very low source impedance. If the output is connected to the inverting input, after being scaled by a voltage divider, $K = R_1 / (R_1 + R_2)$ as shown in Figure 3.

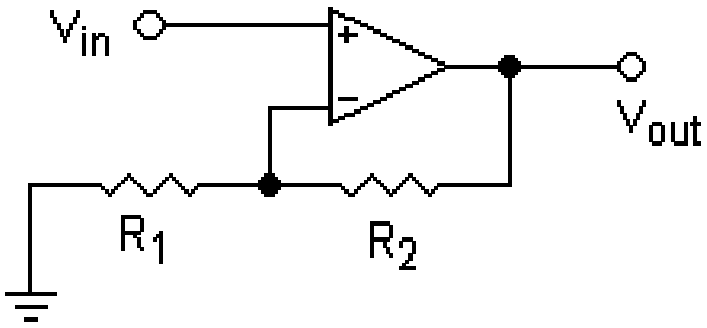


Figure 3. Voltage Divider

$$V_{out} = G(V_{in} - K\,V_{out}). \quad (2.3)$$

The result is a linear amplifier with gain:

$$V_{out} / V_{in} = G / (1 + G\,K). \quad (2.4)$$

If G is very large, this comes close to $1 / K = 1 + (R_2 / R_1)$.

This negative feedback connection is the most typical use of an op–amp, but many different configurations are possible, making it one of the most versatile of all electronic building blocks.

When connected in a negative feedback configuration, the op–amp will tend to produce whatever voltage is necessary to make the input voltages equal. This, and the high input impedance, are sometimes called the two “golden rules” of op–amp design for circuits that use feedback. No current will flow into the inputs and the input voltages will be equal to each other. The exception is if the voltage required is greater than the op–amp's supply, in which case, the output signal stops at a value very close to the voltages, V_{S+} or V_{S-}.

Most integrated single, dual and quad op–amps circuits available have a standardized pin out, which permits one type to be substituted for another without wiring changes. A specific op–amp may be chosen for its open loop gain, bandwidth, noise performance, input impedance, power consumption, or a compromise between any of these factors.

Historically, the first integrated op–amp to become widely available was the Fairchild UA–709, in the late 1960's, but this was rapidly superseded by the much better performing 741, which is easier to use, and probably ubiquitous in electronics. Most manufacturers produce a version of this classic chip. The 741 is a bipolar design, and by modern standards has fairly average performance. Better designs based on the FET arrived in the late 1970's, and MOSFET versions in the early 1980's. It is possible to substitute many of these more modern devices into an older 741–based circuit and work with no other changes to provide better performance.

d. Op–Amp Limitation

Although the design of most op–amp circuits relies on the "golden rules" above, designers should also be aware that no real op–amp can match these characteristics exactly. Listed below are some of the limitations of real op–amps, as well as how this affects circuit design.

(1) DC Imperfection. There are five main DC imperfections as discussed in this section. Finite gain is the effect that is most pronounced when the overall design attempts to achieve gain close to open loop gain of the op–amp. Finite input resistance puts an upper bound on the resistances in the feedback circuit. Nonzero output resistance is important for low resistance loads. Except for very small voltage outputs, power considerations usually come into play first. Input bias current, a small amount of current, typically ~10nA, into the input pins, is required for proper operation. This effect is aggravated because this current is mismatched slightly between the input pins (i.e., input offset current). This effect is usually important only for very low power circuits. Input offset voltage is the op–amp that will produce an output even when the input pins are at exactly the same voltage. For circuits which require precise DC operation, it is necessary

to compensate for this effect. Most commercial op–amps provide an offset pin for this purpose.

(2) AC Imperfections. Two AC imperfections are discussed. The first is a finite bandwidth which all amplifiers possess. However, this is more pronounced in op–amps which use frequency compensation to avoid unintentionally producing positive feedback. The second is the input capacitance, which is the most important for high frequency operation.

(3) Nonlinear Imperfections. Two nonlinear imperfection are discussed. Saturation refers to output voltage that is limited to a peak value slightly less than the power supply voltage. The slew rate is the limit of the rate of change of the output voltage.

(4) Power Considerations. Most op–amps are not designed for high power operation. For high power op–amp circuits, an op–amp specifically designed for that purpose must be used. Short circuit protection is more a feature than a limitation, although it does limit the design. Most commercial op–amps shut off when the load resistance is below a specified level.

e. Internal Circuitry

Although it is useful and easy to treat the op–amp as a black box with a perfect input/output characteristic, it is important to understand the inner workings, so that it is possible to deal with problems arising due to internal parasitic capacitances.

Although designs vary between products and manufacturers, all op–amps have basically the same internal structure, which consists of three stages. The differential amplifier input stage provides low noise amplification, high input impedance and drives a current mirror load. The voltage amplifier provides high gain. The output amplifier output stage provides high current driving capability, low output impedance, current limiting and short circuit protection.

f. Common Configuration

The resistors used in these configurations are typically in the $k\Omega$ range. The $<1\ k\Omega$ range resistors cause excessive current flow and possible damage to the device. The $>1\ M\Omega$ range resistors cause excessive thermal noise and undesired bias cur-

rents. The Z_{out} for all amplifiers is ideally $0\ \Omega$. Realistically, it is $1\ \Omega$ to $1\ k\Omega$, depending on the device.

(1) Inverting Amplifier. Figure 4 shows the configuration for an inverting amplifier. It inverts and amplifies a voltage, which multiplies by a negative constant, and because V_- is a virtual ground.

$$V_{out} = -V_{in} (R_f / R_{in}) \tag{2.5}$$

$$Z_{in} = R_{in}. \tag{2.6}$$

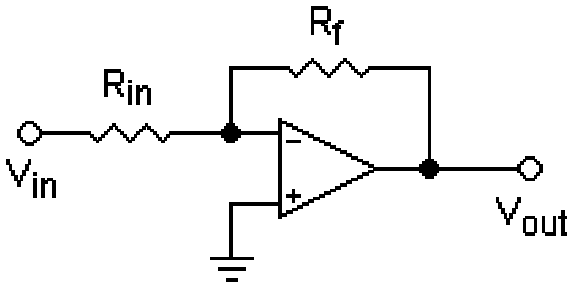


Figure 4. Inverting Amplifier

(2) Non–Inverting Amplifier. Figure 5 shows the configuration for a non–inverting amplifier. It amplifies a voltage, which multipies by a constant greater than 0 but less than 1. Realistically, the input impedance of the circuit is the input impedance of the op–amp itself, $1\ M\Omega$ to $10^{12}\ \Omega$.

$$V_{out} = V_{in} (1 + R_2 / R_1) \tag{2.7}$$

$$Z_{in} = \infty \tag{2.8}$$

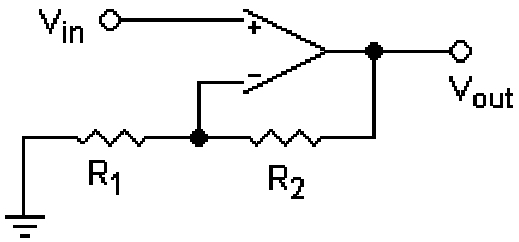


Figure 5. Non–Inverting Amplifier

(3) Voltage Follower. Figure 6 shows the configuration for a voltage follower, which is used as a buffer to eliminate loading effects or to interface impedances connecting a device with a high source impedance to a device with a low input impedance.

$$V_{out} = V_{in} \tag{2.9}$$

$$Z_{in} = \infty \tag{2.10}$$

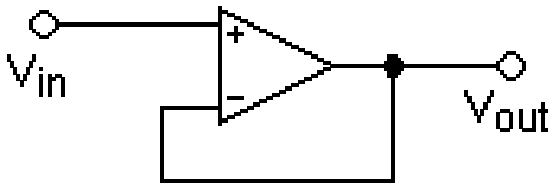


Figure 6. Voltage Follower

(4) Summing Amplifier. Figure 7 shows the configuration for a summing amplifier. It sums several (weighted) voltages and the output is inverted. The input impedance is $Z_n = R_n$ for each input and V_- is a virtual ground). For independent $R_1, R_2, \ldots R_n$,

$$V = -R_f (V_1 / R_1 + V_2 / R_2 + \ldots + V_n / R_n) \tag{2.11}$$

For $R_1 = R_2 = \ldots = R_n$

$$V = -(R_f / R_1)(V_1 + V_2 + \ldots + V_n) \tag{2.12}$$

For $R_f = R_1 = R_2 = \ldots = R_n$

$$V = -(V_1 + V_2 + \ldots + V_n). \tag{2.13}$$

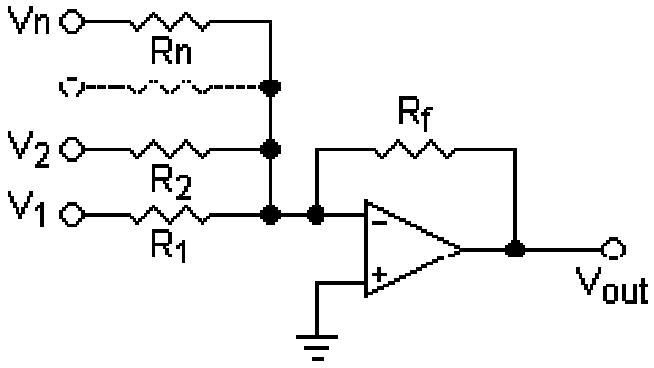


Figure 7. Summing Amplifier

(5) Integrator and Differentiator. Figures 7 and 8 show the configuration for an integrator and differentiator, respectively. The integrator integrates the signal over time. The differentiator differentiates the signal over time.

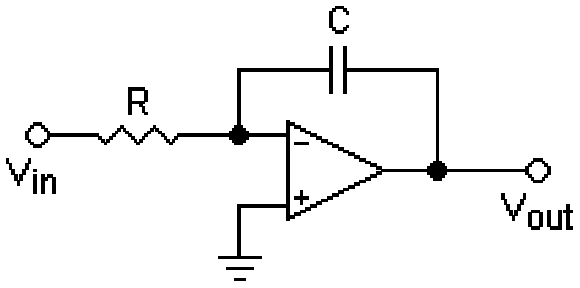


Figure 8. Intertegrator

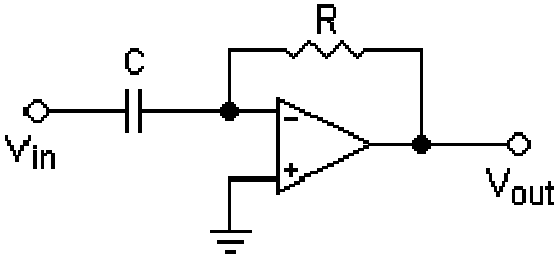


Figure 9. Differentiator

2. Type of Filters

Several common types of filters are Chebyshev, Butterworth, Bessel, Gaussian, Sallen and Key, and Elliptic.

a. Chebyshev Filter

The Chebyshev Type I filter is the filter type that results in the sharpest pass band cut off and contains the largest group delay. The most notable feature of this filter is the ripple in the pass band magnitude.

The pass band attenuation of the standard Chebyshev Type I filter is defined to be the same value as the pass band ripple amplitude. However, Filter Solutions allows the user the option of selecting any pass band attenuation that will define the filter's cut off frequency.

The Chebyshev Type II filter, also known as the Inverse Chebyshev filter, contains a Butterworth style, or maximally flat, pass band, a moderate group delay, and an equiripple stop band. Like the Butterworth filter, the pass band attenuation of the Chebyshev Type II filter is defined to be –3.01 dB. However, Filter Solutions allows the user the option of selecting any pass band attenuation in dB's that will define the filter's cut off frequency.

b. Butterworth Filter

The Butterworth filter is the filter type that results in the flattest pass band and contains a moderate group delay. A standard Butterworth filter's pass band attenuation is –3.01dB. However, Filter Solutions allows the user the option of selecting any pass band attenuation in dB's that will define the filter's cut off frequency.

Filter Solutions also offers the user the option of placing user–defined zeros in the stop band. Such a filter with stop band zeros is no longer a true Butterworth Filter, but is still in the Maximally Flat filter family.

c. Bessel Filter

The Bessel filter's distinguishing characteristic is the near constant group delay throughout the pass band of the low pass filter. Filter Solutions normalizes the Bessel filter such that the prototype high frequency attenuation matches the Butterworth filter. The pass band attenuation of the Bessel filter increases with the order of the filter

when this normalization is applied. However, Filter Solutions allows the user the option of selecting the desired pass band attenuation in dB's. 3dB attenuation is a popular choice for some.

d. Gaussian Filter

The Gaussian filter is the filter type that results in the most gradual pass band roll–off and the lowest group delay. The step response of the Gaussian filter NEVER overshoots the steady state value. As the name states, the Gaussian filter is derived from the same basic equations used to derive the Gaussian distribution. The significant characteristic of the Gaussian filter is that the step response contains no overshoot at all.

Filter Solutions normalizes the Gaussian filter such that the prototype high frequency attenuation matches the Butterworth filter. The pass band attenuation of the Gaussian filter increases with the order of the filter when this normalization is applied. However, Filter Solutions allows the user the option of selecting the desired pass band attenuation. 3dB attenuation is a popular choice.

e. Sallen Key Filter

A Sallen Key filter is a two poles filter topology. It is sometimes called VCVS, which stands for voltage controlled voltage source. It is available in low pass, high pass, bandpass, and notch versions, although the notch variety owes more to the Twin T topology. The bandpass version of the Sallen Key topology is not recommended, because the input resistor tends to be a very low value. The Sallen Key topology is often seen in a unity gain version, although the addition of gain resistors is an obvious enhancement. The designer is cautioned, however, that changing the gain also changes other filter characteristics. As in the other single opamp topologies, changing gain will also affect the frequency and filter type (Butterworth, Chebyshev, and Bessel).

The Sallen Key topology is suited for operation from a single supply. Current feedback amplifiers can be used, with the restriction that the connection from the op amp output to inverting input must be the recommended feedback resistor value. This is true whether or not this resistor is part of a gain stage. It is not possible to use the Sallen Key topology with fully differential amplifiers.

f. Elliptic Filters

The Elliptic filter contains a Chebyshev Type I style equiripple pass band, an equipped stop band, a sharp cut off, high group delay, and the greatest stop band attenuation.

Like the Chebyshev Type I filter, the Elliptic pass band attenuation is defined to be the same value as the pass band ripple amplitude. However, Filter Solutions allows the user the option of selecting any pass band attenuation that will define the filter's cut off frequency.

3. Advantages and Disadvantages

A filter is a circuit that allows certain frequencies to pass and blocks others. This selective nature can be done two ways, either with passive components or with active components. Passive filters are completely comprised of passive elements; namely resistors, capacitors and/or inductors. Active filters use active devices, i.e., an op–amp, to filter out unwanted signals.

Passive filters have some important disadvantages in certain applications, however. Since they use no active elements, they cannot provide signal gain. Input impedances can be lower than desirable, and output impedances can be higher than optimal for some applications, and therefore, buffer amplifiers may be needed. Inductors are necessary for the synthesis of the most useful passive filter characteristics, and these can be prohibitively expensive if high accuracy, 1% or 2% for example, small physical size, or a large value are required. Standard values of inductors are not very closely spaced, and it is diffcult to find an off–the–shelf unit within 10% of any arbitrary value. Thus, adjustable inductors are often used. Tuning these to the required values is time–consuming and expensive when producing large quantities of filters. Futhermore, complex passive filters higher than 2nd–order can be difficult and time–consuming to design.

On the other hand, active filters have high gain and it is easy to adjust and tune the frequency. There are no inductors, which will reduce the cost and size of the circuit. It has no loading effects. Some disadvantages of active filters include the bandwidth limitations, fabrication tolerances, and that it can only respond to a specific range of signal magnitudes.

D. GIC FILTER

The generalizedd impedance converter (GIC) is highly insensitive to component variation [1],[4]. The GIC filter design was introduced by Mikhael and Bhattachararyya [2] and proved to be very insensitive to non–ideal component characteristics and variations in component values [5]. Figure 10 shows the general topology of the GIC filter.

GIC Biquads are two op–amp biquads with good high frequency performance. All but the even notch stages are tunable. The high pass, low pass and band pass stages are gain adjustable. The notch and all pass stages have a fixed gain of unity. All GIC stages have equal capacitor values, unless a capacitor is required to adjust the gain. Notch stages do not rely on element value subtractions for notch quality and are thus immune from degradations in notch quality due to element value errors.

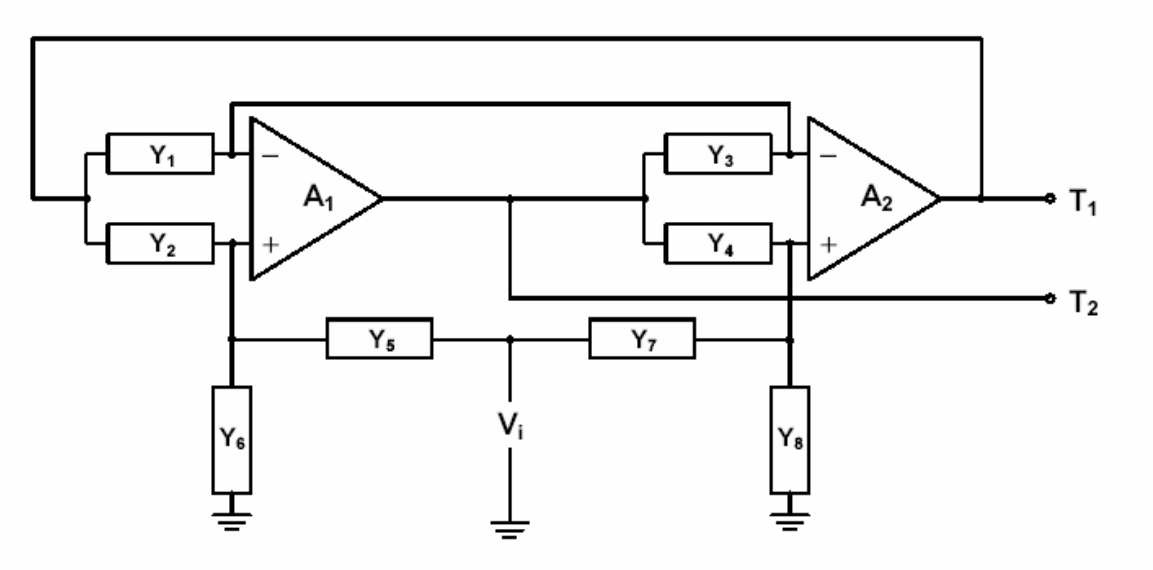


Figure 10. Basic GIC Filter (From [2])

The transfer functions for the GIC filter are as follows [2].

$$T_1 = \frac{V_1}{V_i} = \frac{Y_1Y_4Y_5 + Y_3Y_7(Y_2 + Y_6) - Y_3Y_5Y_8}{Y_1Y_4(Y_5 + Y_6) + Y_2Y_3(Y_7 + Y_8)} \tag{2.14}$$

$$T_2 = \frac{V_2}{V_i} = \frac{Y_1Y_4Y_5 + Y_1Y_5Y_8 + Y_2Y_3Y_7 - Y_1Y_6Y_7}{Y_1Y_4(Y_5 + Y_6) + Y_2Y_3(Y_7 + Y_8)} \tag{2.15}$$

Choosing the appropriate elements and substituting the proper admittance for each element into the transfer functions in Equations 2.14 and 2.15 yields transfer functions representing the four filter types. Table 4 depicts the transfer functions and admittance selection for each of the eight elements.

Filter Type	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	Y_8	Transfer Function
Low-Pass	G	sC	$sC+\frac{G}{Q_p}$	G	G	0	0	G	$T_2=\frac{2\omega_p^2}{s^2+\frac{\omega_p}{Q_p}s+\omega_p^2}$
High-Pass	G	G	sC	G	0	G	C	$\frac{G}{Q_p}$	$T_1=\frac{2s^2}{s^2+\frac{\omega_p}{Q_p}s+\omega_p^2}$
Band-Pass	G	G	sC	G	0	G	$\frac{G}{Q_p}$	C	$T_1=\frac{2\frac{\omega_p}{Q_p}s}{s^2+\frac{\omega_p}{Q_p}s+\omega_p^2}$
Notch	G	G	sC	G	G	0	C	$\frac{G}{Q_p}$	$T_2=\frac{s^2+\omega_p^2}{s^2+\frac{\omega_p}{Q_p}s+\omega_p^2}$

Table 4. Admittance Selection and Transfer Functions (From [1])

These transfer functions are based on the use of ideal op–amps. Non–ideal transfer functions are derived and shown below [1].

The non–ideal transfer function for T1 is:

$$T_1 = \frac{V_1}{V_i} = \frac{\frac{[Y_7(Y_1+Y_3)(Y_2+Y_5+Y_6)]}{\omega_{t_1}} S + [Y_{1\,4\,5}Y + Y_{2\,3\,7}YY + Y_{3\,6\,7}YY - Y_{3\,5\,8}YY]}{\frac{(Y_1+Y_3)(Y_4+Y_7+Y_8)(Y_2+Y_5+Y_6)}{\omega_{t_1}\omega_{t_2}} S^2 + \frac{Y_1(Y_4+Y_7+Y_8)(Y_2+Y_5+Y_6)}{\omega_{t_1}} S + \frac{Y_3(Y_4+Y_7+Y_8)(Y_2+Y_5+Y_6)}{\omega_{t_2}} S + [Y_{1\,4}Y(Y_5+Y_6) + Y_{2\,3}Y(Y_7+Y_8)]} \quad (2.16)$$

The non–ideal transfer function for T2 is:

$$T_2 = \frac{V_2}{V_i} = \frac{\frac{[Y_5(Y_1+Y_3)(Y_4+Y_7+Y_8)]}{\omega_{t_1}} S + [Y_{1\,4\,5}Y + Y_{1\,5\,8}YY + Y_{2\,3\,7}YY - Y_{1\,6\,7}YY]}{\frac{(Y_1+Y_3)(Y_4+Y_7+Y_8)(Y_2+Y_5+Y_6)}{\omega_{t_1}\omega_{t_2}} S^2 + \frac{Y_1(Y_4+Y_7+Y_8)(Y_2+Y_5+Y_6)}{\omega_{t_1}} S + \frac{Y_3(Y_4+Y_7+Y_8)(Y_2+Y_5+Y_6)}{\omega_{t_2}} S + [Y_{1\,4}Y(Y_5+Y_6) + Y_{2\,3}Y(Y_7+Y_8)]} \quad (2.17)$$

where ω_{t_1} and ω_{t_2} are the gain bandwidth product (GBWP) of the two op amps used. Note that ($\omega_t \to \infty$), assuming ideal op–amps, the non–ideal transfer function equations simplify the ideal equations from Table 4.

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III. VLSI DESIGN THEORY

Over the last two decades, the electronics industry has experienced phenomenal growth, mainly due to the rapid advances in integration technologies and large–scale systems design. The number of applications of integrated circuits in high–performance computing, telecommunications, and consumer electronics has been rising steadily at a very fast pace. The fast development of this field is driven by the requirement of the computational power of these applications.

A. INTRODUCTION [10],[11]

In the area of low–bit–rate video and cellular communications, the current leading–edge technologies has already provide the end–users a certain amount of processing power and portability. With this trend expected to continue, it will have very important implications for VLSI and systems design. Figure 11 gives an overview of the prominent trends in information technologies over the next few decades.

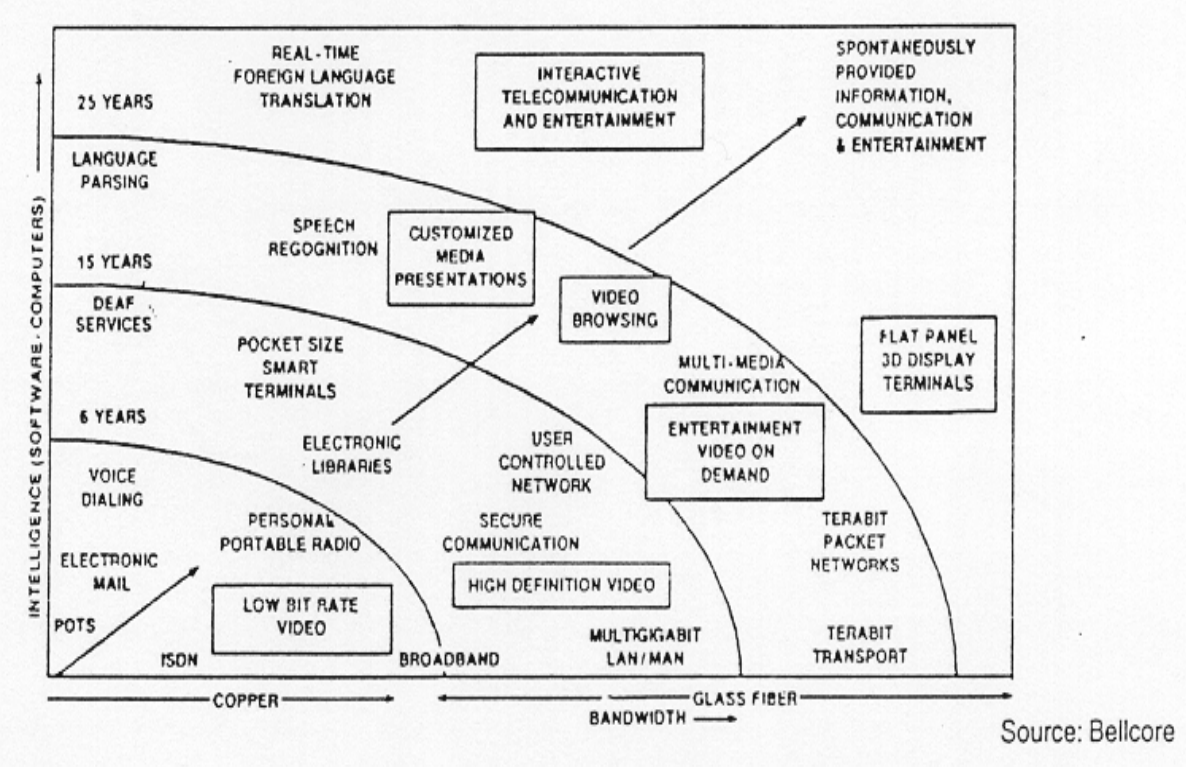

Figure 11. Prominent Trends in Information Service Technologies. (From [10])

The need to integrate these functions into a small system or package is increasing as more and more complex functions are required in various data processing and telecommunications devices. For the past three decades, the level of integration as measured by the number of logic gates in a monolithic chip has been steadily rising, mainly due to the rapid progress in processing technology and interconnects technology. The logic complexity per chip has been increasing exponentially over the past few years.

Figure 12 shows the history and forecast of chip complexity, and minimum feature size over time, as seen in the early 1980's. At that time, it was expected that it would be around 2000 before a minimum feature size of 0.3 microns could be realized. The actual development of the technology has far exceeded these expectations. A minimum size of 0.25 microns was readily achievable by 1995 and the integration density has also exceeded previous expectations. By the end of 1994, the first 64 Mbit DRAM, and the INTEL Pentium microprocessor chip containing more than three million transistors were available, thus pushing the envelope of integration density.

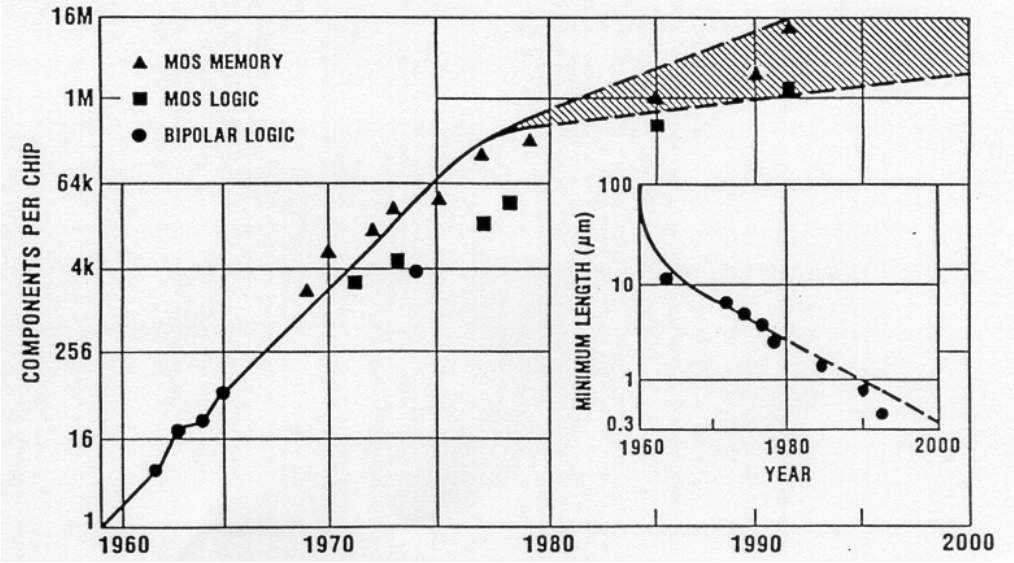

Figure 12. Evolution of Integration Density and Minimum Feature Size, as Seen in the Early 1980's (From [10])

B. VLSI DESIGN FLOW [10],[11]

The VLSI design process starts with a given set of requirements. The initial design is developed and tested against the requirements and improvements made when requirements are not met. If such improvement is either not possible or too costly, it is then necessary to consider the revision of requirements and its impact analysis.

Figure 13 shows a simplified view of the VLSI design flow, taking into account the various representations, or abstractions of design–behavioral, logic, circuit and mask layout. During this process, the verification of design plays a very important role in every step. The failure to verify a design properly in its early phases typically causes significant and expensive re–design at a later stage, which ultimately increases the time–to–market.

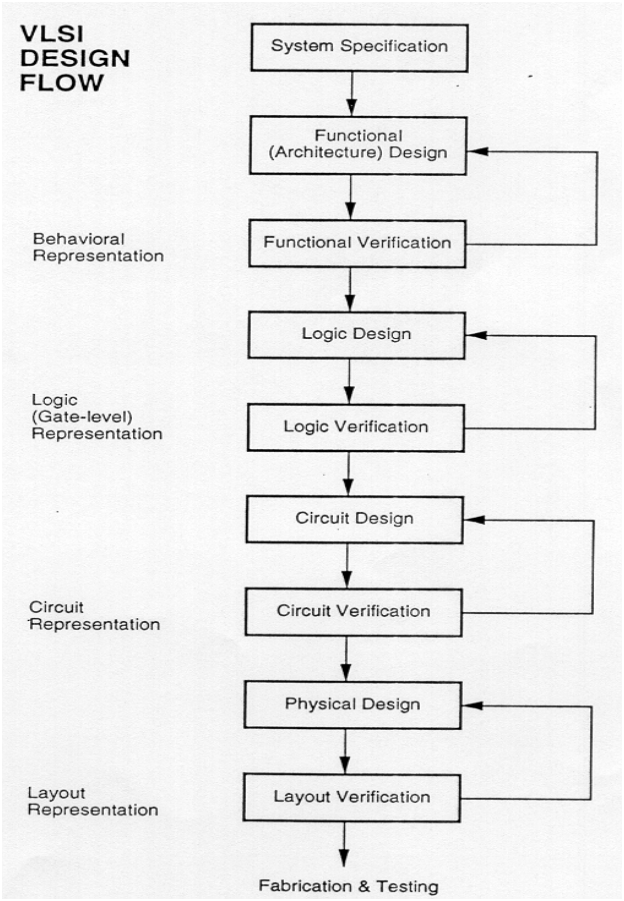

Figure 13. VLSI Design Flow (From [10])

In reality, there is no truly unidirectional top–down design flow, although top–down design flow provides an excellent design process control. Both top–down and bottom–up approaches have to be combined. For example, if a chip designer defined architecture without close estimation of the corresponding chip area, then it is very likely that the resulting chip layout exceeds the area limit of the available technology. When this happened, in order to fit the architecture into the allowable chip area, some functions may have to be removed and the design process must be repeated. This change may require significant modification of the original requirements. Thus, it is very important to feed forward low–level information to higher levels (bottom up) as early as possible to prevent wastage.

C. FABRICATION PROCESS FLOW – BASIC STEPS [12]

Each processing step requires certain areas be defined on the chip by the appropriate masks during the fabrication flow. The integrated circuit is viewed as a set of patterned layers of doped silicon, polysilicon, metal and insulating silicon dioxide. In common practice, a layer must be patterned before the next layer of material is applied on the chip. Lithography is the process used to transfer a pattern to a layer on the chip. Since each layer has its own distinct patterning requirements, by using a different mask, it is necessary to repeat the lithographic sequence for every layer.

To illustrate the fabrication steps involved in patterning silicon dioxide through optical lithography, first examine the process flow shown in Figure 14.

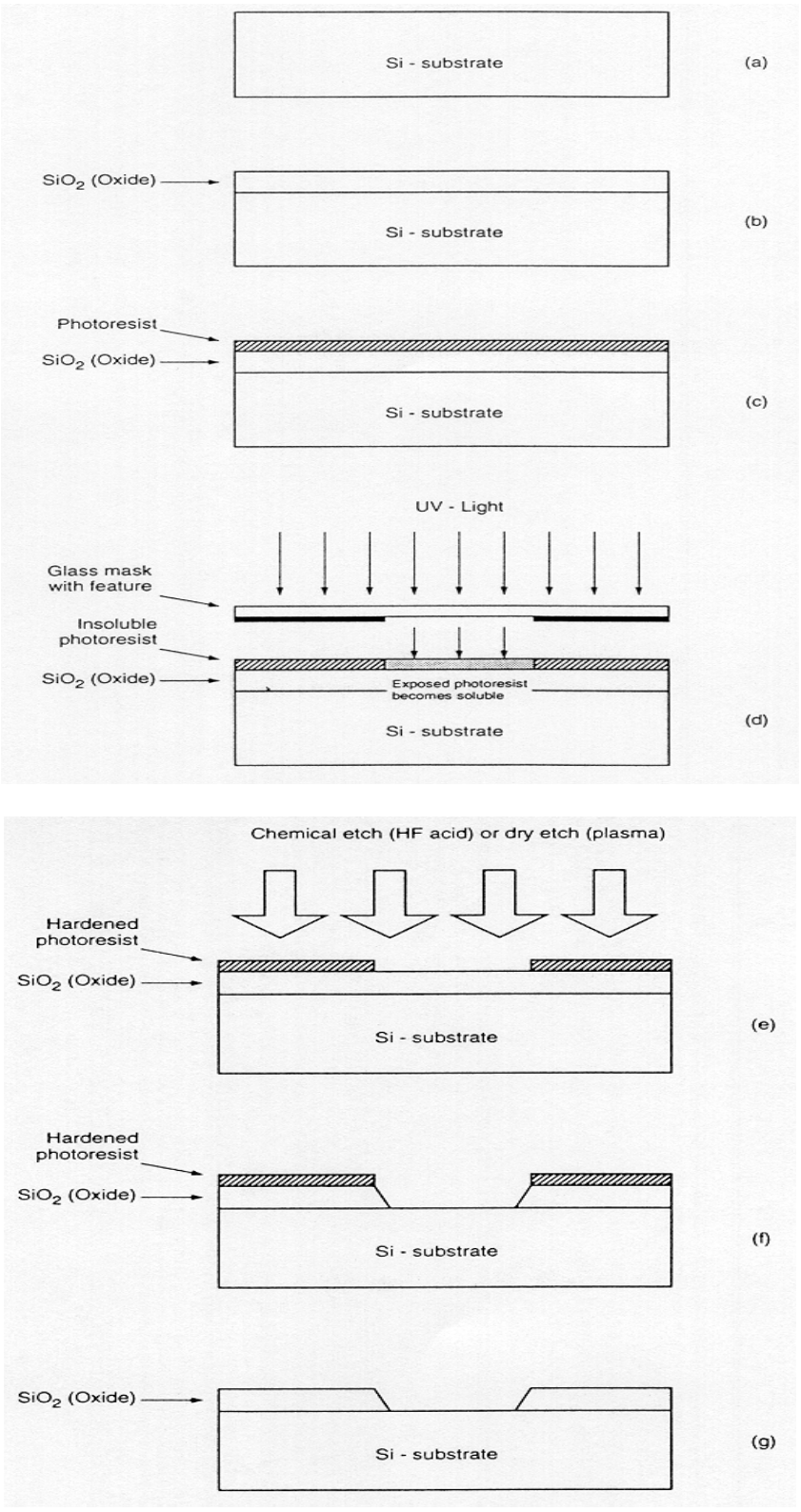

Figure 14. Process Steps Required for Patterning of Silicon Dioxide (From [12])

The thermal oxidation of the silicon surface is the process beginning, where an oxide layer of about one micrometer thickness is created on the substrate (Figure 14(b)). The entire oxide surface is then covered with a layer of photoresist that is essentially a light–sensitive, acid–resistant organic polymer, initially insoluble in the developing solution (Figure 14(c)). The exposed areas become soluble so they are no longer resistant to etching solvents if the photoresist material is exposed to ultraviolet (UV) light. To expose the photoresist selectively, it is necessary to cover some of the areas on the surface with a mask during exposure. When the structure with the mask on top is exposed to UV light, areas covered by the opaque features on the mask are shielded. In the areas where the UV light can pass through, on the other hand, the photoresist is exposed and becomes soluble (Figure 14(d)).

The type of photoresist that is initially insoluble and then becomes soluble after exposure to UV light is called positive photoresist. The process sequence shown in Figure 14 uses positive photoresist. There is another type of photoresist that is initially soluble and becomes insoluble (hardened) after exposure to UV light, called negative photoresist. If negative photoresist is used in the photolithography process, the areas which are not shielded from the UV light by the opaque mask features become insoluble, whereas the shielded areas can subsequently be etched away by a developing solution. Negative photoresists are more sensitive to light, but their photolithographic resolution is not as high as that of the positive photoresists. Therefore, the manufacturing of high–density integrated circuits use negative photoresits less commonly.

Following the UV exposure step, a solvent can remove the unexposed portions of the photoresist. Therefore, the silicon dioxide regions not covered by hardened photoresist can be etched away either by using a chemical solvent (HF acid) or by using a dry etch (plasma etch) process (Figure. 14(e)). Note that at the end of this step, an oxide window is obtained that reaches down to the silicon surface (Figure 14(f)). It is now possible to strip the remaining photoresist from the silicon dioxide surface by using another solvent, leaving the patterned silicon dioxide feature on the surface as shown in Figure 14(g).

The sequence of process steps illustrated in detail in Figure 14 actually accomplishes a single pattern transfer onto the silicon dioxide surface, as shown in Figure 15. The fabrication of semiconductor devices requires several such pattern transfers to be performed on silicon dioxide, polysilicon, and metal. The basic patterning process used in all fabrication steps, however, is quite similar to the one shown in Figure 14. Also note that for the accurate generation of high–density patterns required in sub–micron devices, electron beam (E–beam) lithography is used instead of optical lithography.

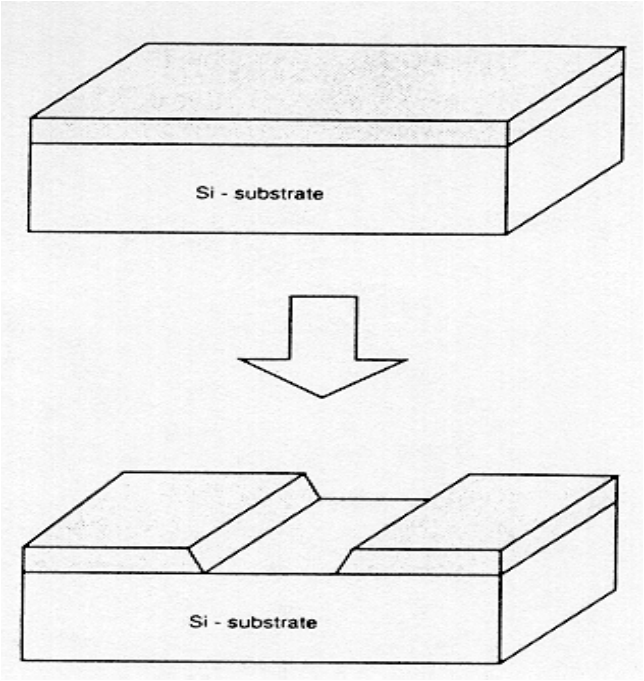

Figure 15. The Result of a Single Lithographic Patterning Sequence on Silicon Dioxide, without Showing the Intermediate Steps. (From [12])

D. LAYOUT DESIGN RULES [11]

The physical mask layout of any circuit to be manufactured using a particular process must conform to the layout design rules. These rules usually specify the minimum allowable line widths for physical objects on–chip such as metal and polysilicon interconnects or diffusion areas, minimum feature dimensions, and minimum allowable separations between two such features. If a metal line width is made too small, for example, it is possible for the line to break during the fabrication process or afterwards, resulting in an open circuit. If two lines are placed too close to each other in the layout, they may form an unwanted short circuit by merging during or after the fabrication process.

The main objective of design rules is to achieve a high overall yield and reliability while using the smallest possible silicon area for any circuit manufactured with a particular process.

Note that there is usually a trade–off between higher yield, which is obtained through conservative geometries, and better area efficiency, obtained through aggressive, high–density placement of various features on the chip. The layout design rules which are specified for a particular fabrication process normally represent a reasonable optimum point in terms of yield and density. It must be emphasized, however, that the design rules do not represent strict boundaries which separate "correct" designs from "incorrect" ones. A layout which violates some of the specified design rules may still result in an operational circuit with reasonable yield, whereas another layout observing all specified design rules may result in a circuit which is not functional and/or has very low yield. In general, observing the layout design rules will significantly increase the probability of fabricating a successful product with high yield.

The design rules are usually described in two ways.

- Micron rules, in which the layout constraints such as minimum feature sizes and minimum allowable feature separations, are stated in terms of absolute dimensions in micrometers, or,
- Lambda rules, which specify the layout constraints in terms of a single parameter and, thus, allow linear, proportional scaling of all geometrical constraints.

E. LAYOUT OF CMOS INVERTER [12]

The circuit consists of one nMOS and one pMOS transistor. First, it is necessary to create the individual transistors according to the design rules. Assume an attempt to design the inverter with minimum–size transistors. The minimum diffusion contact size then determines the width of the active area, which is necessary for source and drain connections, and the minimum separation from diffusion contact to both active area edges.

The width of the polysilicon line over the active area, which is the gate of the transistor, is typically taken as the minimum poly width (Figure 16). Then, the overall length of the active area is simply determined by the following sum: (minimum poly width) + 2 (minimum poly–to– contact spacing) + 2 (minimum spacing from contact to

active area edge). It is necessary to place the pMOS transistor in an n–well region and the pMOS active area, and the minimum n–well overlap over n+ dictate the minimum size of the n–well.

The distance between the nMOS and the pMOS transistor is determined by the minimum separation between the n+ active area and the n–well (Figure 17). The polysilicon gates of the nMOS and the pMOS transistors are usually aligned. The final step in the mask layout is the local interconnections in metal, for the output node and for the VDD and GND contacts (Figure 18). Notice that in order to be biased properly, the n–well region must also have a VDD contact.

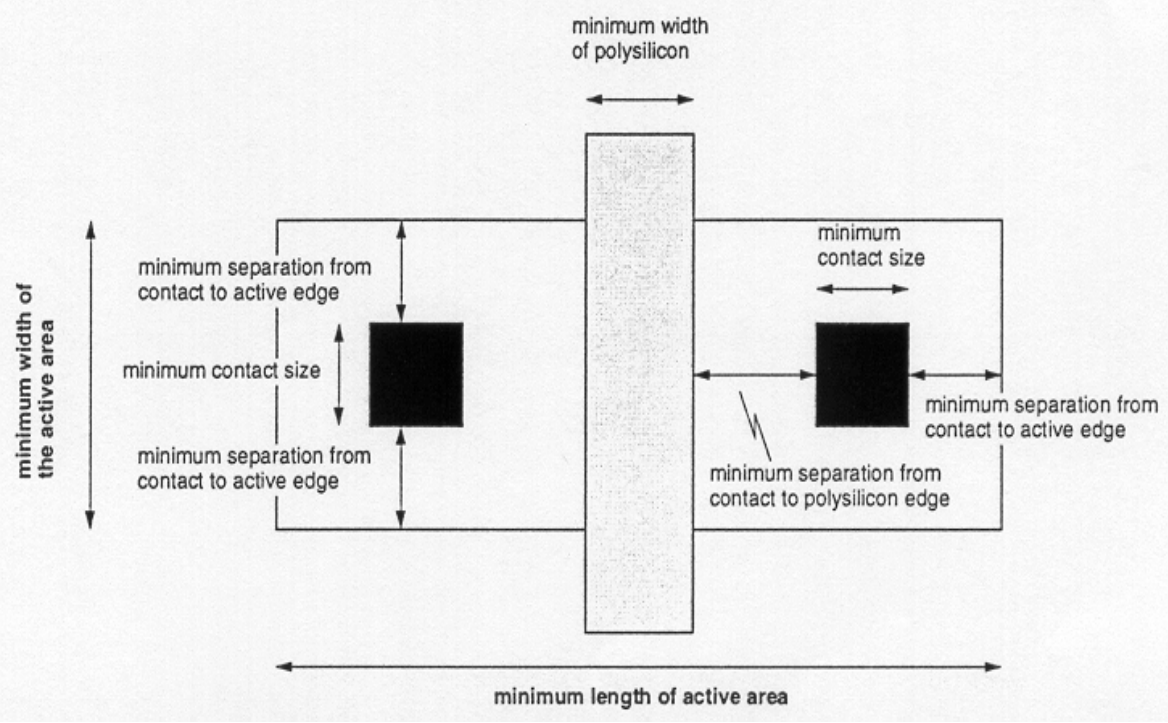

Figure 16. Design Rule Constraints which Determine the Dimensions of a Minimum–Size Transistor (From [12])

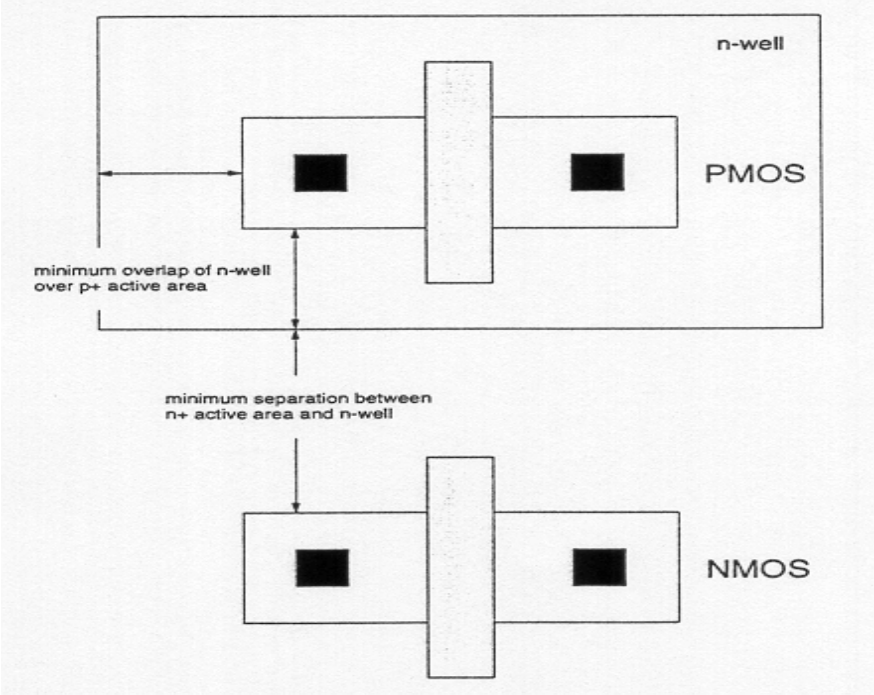

Figure 17. Placement of One nMOS and One pMOS Transistor (From [12])

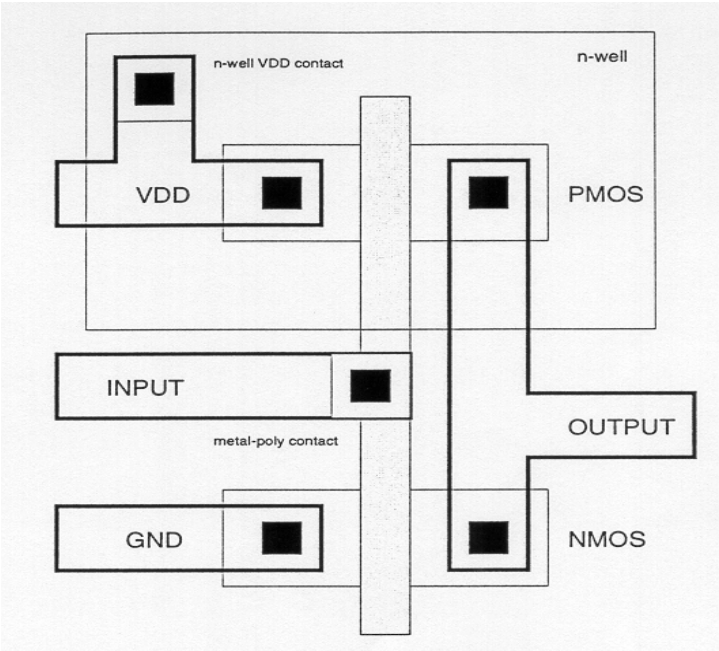

Figure 18. Complete Mask Layout of the CMOS Inverter (From [12])

F. LAYOUT OF CMOS NAND AND NOR GATES [12]

The mask layout designs of the CMOS NAND and NOR gates follow the general principles examined earlier for the CMOS inverter layout. Figure 19 shows the layouts of a two–input NOR gate and a two–input NAND gate, using a single–layer polysilicon and a single–layer metal.

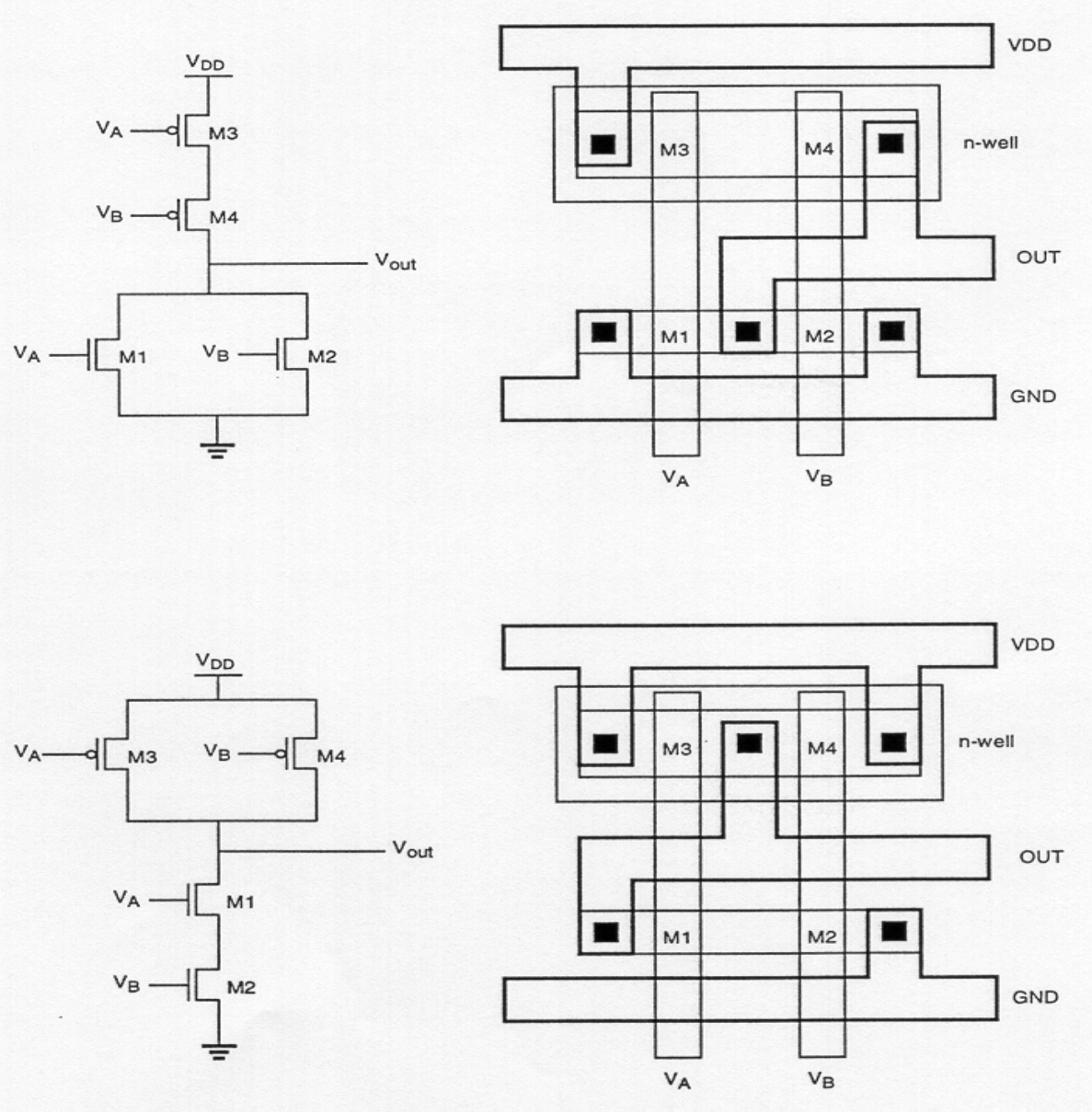

Figure 19. Layouts of a CMOS NOR2 Gate and a CMOS NAND2 Gate. (From [10])

Here, the p–type diffusion area for the pMOS transistors and the n–type diffusion area for the nMOS transistors are aligned in parallel to allow simple routing of the gate signals with two parallel polysilicon lines running vertically. Also notice that the two mask layouts show a very strong symmetry, because the NAND and the NOR gate have a symmetrical circuit topology.

IV. BICMOS COMPOSITE OPERATIONAL AMPLIFIER SIMULATION RESULTS

BiCMOS technology can make op–amp improvements possible by adding the capabilities of bipolar transistors to standard CMOS designs. Since bipolar transistors have a larger transconductance than their CMOS equivalents, they can produce op–amps with a larger gain bandwidth product (GBWP), arguably the most important op–amp characteristic. Bipolar transistors are limited in that they do not have high input impedance like their CMOS equivalents. In addition, BiCMOS technology requires more advanced process techniques leading to additional steps in the fabrication process. [3]

In this chapter, the author will investigate and improve the performance of the Lee Configuration B op–amp [7], standard op–amp. The first part of the chapter will cover the basic information on the composite op–amp design. The second part of the chapter covers the details of the simulation of the newly designed composite amplifier, C20A2. This sets the basic foundation for future students to incorporate the newly designed composite amplifier into the GIC filter to further enhance the filter performance. The following chapter investigates in detail the Non–Ideal performance of GIC filter, with effects from the various parameters.

A. BACKGROUND

Composite amplifiers were developed in 1980. Initial investigations were centered on increasing the GBWP and decreasing the passive and active sensitivity of a single op–amp. Active compensation was examined and applied to the design of active filter networks. The resulting composite devices had three external terminals which resembled the input and output terminals of a single op–amp. [16]

In the design of two op–amp composite amplifiers (C20A), a nullator–norator pairing [14] was used which yielded 136 possible combinations of op–amps. Four of the 136 possible combination yielded acceptable results based on the following criteria:

- The non–inverting and inverting open loop gains of each of the 136 C2A's were to have no change in sign in the denominator polynomial coefficients, satisfying the necessary but not sufficient conditions for stability.

Also, the need for a single op–amps with matched GBWP's was to be eliminated resulting in low component sensitivity.

- The external three terminal performance of the C20As was to resemble, as close as possible, the terminal performance of the single op–amp.
- No right half plane zeros due to the single op–amp pole were allowed in the closed loop gains of the C20As (to minimize the phase shift).
- The C20A had to have minimum gain and phase deviation from the ideal transfer function and extended frequency operation to justify the increased number of op–amps.

Based on these criteria, the following designs in Figures 20 to 23 were found to yield the highest response and most accurate results.

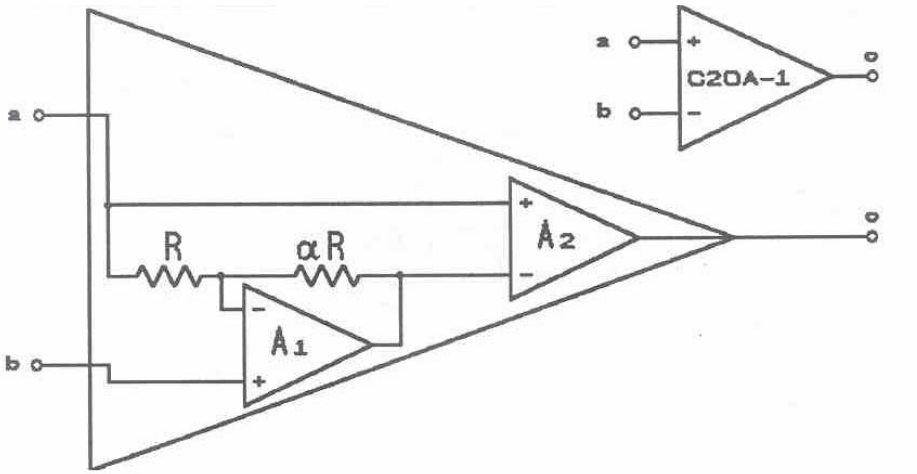

Figure 20. C20A1 (From [15])

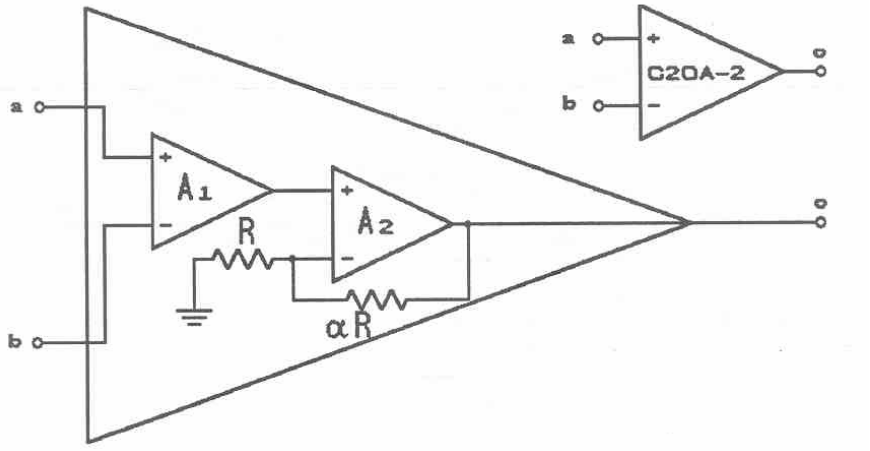

Figure 21. C20A2 (From [15])

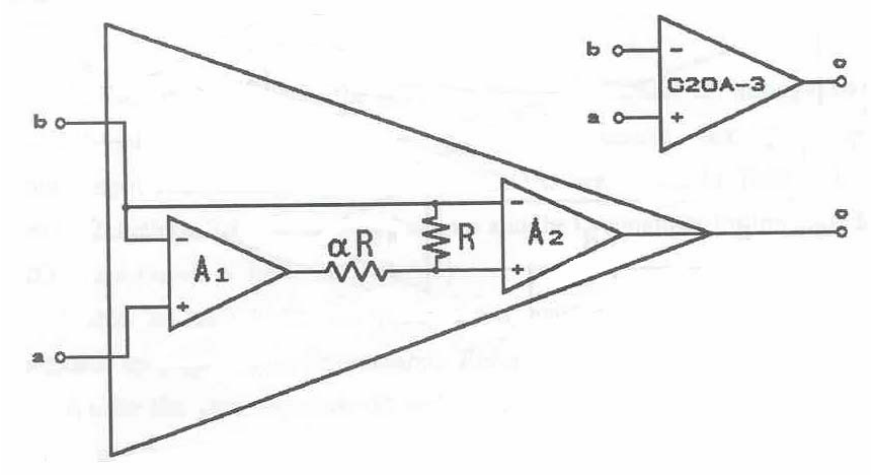

Figure 22. C20A3 (From [15])

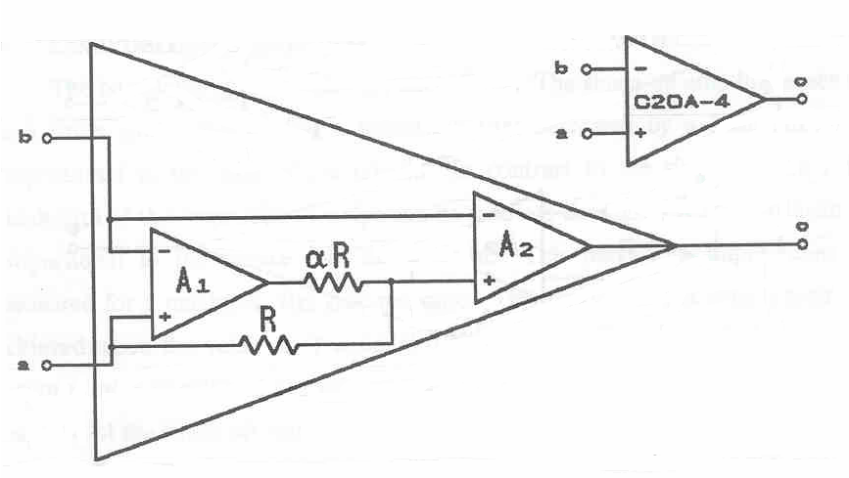

Figure 23. C20A4 (From [15])

B. OPEN LOOP GAIN, 3 DB FREQUENCY AND Q_P FUNCTION

The open loop gain input output relationships for these four C20As are shown in Table 5. Table 6 shows the C20A 3 dB frequency and *Qp* functions. Finally, Table 7 shows the stability criteria for C20As.

$$V_{Oi} = V_a A_{ai}(s) - V_b A_{bi}(s) \qquad (i = 1 \text{ to } 4)$$

forC2OA-1:

$$V_{O1} = V_a \frac{A_2 (1 + A_1) (1 + \alpha)}{A_1 + (1 + \alpha)} - V_b \frac{A_1 A_2 (1 + \alpha)}{A_1 + (1 + \alpha)}$$

forC2OA-2:

$$V_{O2} = V_a \frac{A_1 A_2 (1 + \alpha)}{A_2 + (1 + \alpha)} - V_b \frac{A_1 A_2 (1 + \alpha)}{A_2 + (1 + \alpha)}$$

forC2OA-3:

$$V_{O3} = V_a \frac{A_1 A_2}{A_1 + (1 + \alpha)} - V_b \frac{A_2 (1 + A_1)}{(1 + \alpha)}$$

forC2OA-4:

$$V_{O4} = V_a \frac{A_2 (A_1 + \alpha)}{(1 + \alpha)} - V_b \frac{A_2 A_1 + (1 + \alpha)}{(1 + \alpha)}$$

where α is the internal compensation resistor ratio

Table 5. C20As Open Loop Gain Input–Output Relationships (From [15])

forC2OA-1:

$$\omega_p = \sqrt{\frac{\omega_1 \omega_2}{1 + K}} \qquad Q_p = \frac{(1 + \alpha)}{\sqrt{1 + k}} \sqrt{\frac{\omega_2}{\omega_1}}$$

forC2OA-2:

$$\omega_p = \sqrt{\frac{\omega_1 \omega_2}{1 + k}} \qquad Q_p = \frac{(1 + \alpha)}{\sqrt{1 + k}} \sqrt{\frac{\omega_1}{\omega_2}}$$

forC2OA-3:

$$\omega_p = \sqrt{\frac{\omega_1 \omega_2}{(1 + k)(1 + \alpha)}} \qquad Q_p = \sqrt{\frac{(1 = k)(1 + \alpha)\omega_1}{\omega_2}}$$

forC2OA-4:

$$\omega_p = \sqrt{\frac{\omega_1 \omega_2}{(1 + k)(1 + \alpha)}} \qquad Q_p = \sqrt{\frac{(1 + k)}{(1 + \alpha)} \frac{\omega_1}{\omega_2}}$$

where α is the internal resistor ratio and ω_p is the three dB point

Table 6. C20A 3dB Frequency and *Qp* Functions (From [15])

$1 + \alpha < \frac{1 + K}{2}$	*for C2OA-1/2*
$1 + \alpha < 1 + K$	*for C2OA-3*
$1 + \alpha < 4(1 + K)$	*for C2OA-4*

Table 7. Stability Criteria for C20As (From [15])

C. COMPOSITE OPERATIONAL AMPLIFIER BANDWIDTH IMPROVEMENT

The bandwidth of the single op–amp is finite. The single op–amp implemented as a finite gain amplifier has a bandwidth that decreases by a factor inversely proportional to the gain of the circuit. In contrast to the single op–amp, the bandwidth of the composite op–amps can be made to decrease by a factor inversely proportional to the square root of the gain response. This bandwidth improvement is measured for a maximally flat gain response. This maximally flat gain response is achieved when the value of Q is equal to 0.707. [15] The theoretical frequency response of a negative finite gain composite op–amp compared to the frequency response of the single op–amp shows an increase in bandwidth of about a decade for high gain applications.

The excellent results and the superior stability properties of the C20A1 and C20A2 provide the most attractive configuration for a finite gain implementation from a bandwidth and stability and stability point of view. [15] The C20A2 will be the configurations implemented in this thesis.

D. COMPOSITE OPERATIONAL AMPLIFIERS SENSITIVITIVES

In addition to the significant bandwidth improvements, the C20A configuration also offers a decreased sensitivity to active and passive components. The 3 dB frequency and Q are functions of the GBWPs of the single op–amps and α, the value of the ratio between the two resistors in the composite op–amp.

The finite gain transfer functions for the C20As have the general form of

$$\frac{1+as}{1+b_1 s+b_2 s^2} \tag{5.1}$$

where

$$b_1 = \frac{1}{\omega_p Q} \tag{5.2}$$

and

$$b_2 = \frac{1}{\omega p^2}. \tag{5.3}$$

None of the *a* or *b* coefficients are realized through differences which guarantee the low sensitivity of the transfer functions, the 3 dB frequencies and Q to the circuit parameters. The *b* coefficients are always positive which is a necessary element for the transfer functions stability.

E. BLOCK DIAGRAM OF AUTHOR'S STANDARD AND COMPOSITE DESIGN USED IN THESIS

The standard op–amp as shown in Figure 24 has an inverting and non–inverting input and produces an amplified version of the input signal at the output. The value of the positive rail V_{DD} and negative rail V_{SS} governs the maximum amplifications, provided by DC power sources external to the op–amp.

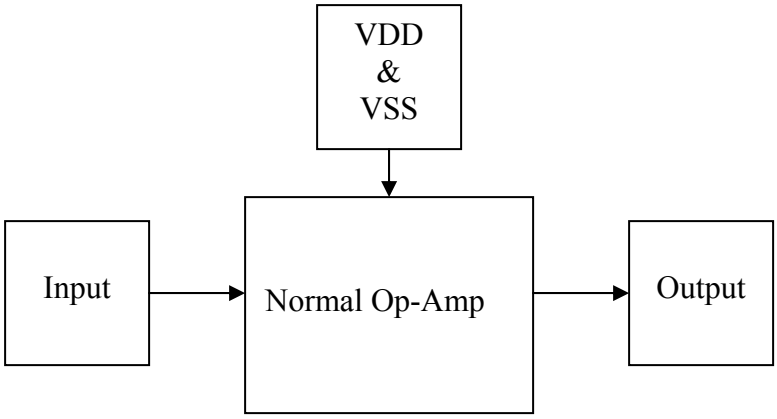

Figure 24. Block Diagram of Standard Op–Amp

The composite op–amp shown in Figure 25 consists of two lower–order op–amps, i.e., Lee configuration op–amp, coupled through resistors. The C20A2 consists of two–coupled standard op–amps. These arrangements can produce a higher GBWP and increase the useful operating frequency over that which a lower–order device can achieve. The input, V_{DD} and V_{SS} requirements, and output signal are of the same overall configuration as the standard op–amp.

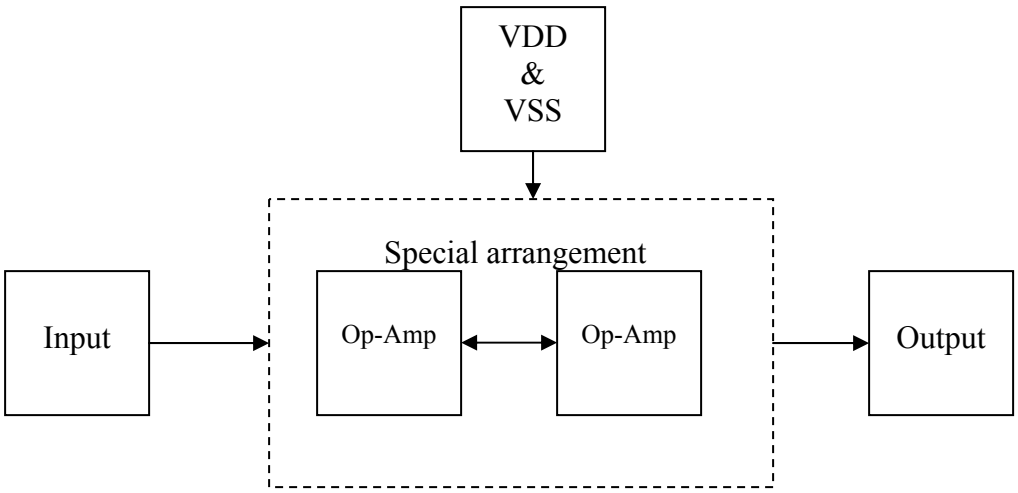

Figure 25. Block Diagram of Composite Op–Amp C20A2

F. SCHEMATIC DIAGRAM OF AUTHOR'S STANDARD AND COMPOSITE DESIGN USED IN THESIS

Figure 26 is the circuit layout for the Lee configuration BiCMOS versions of the circuit. [6]

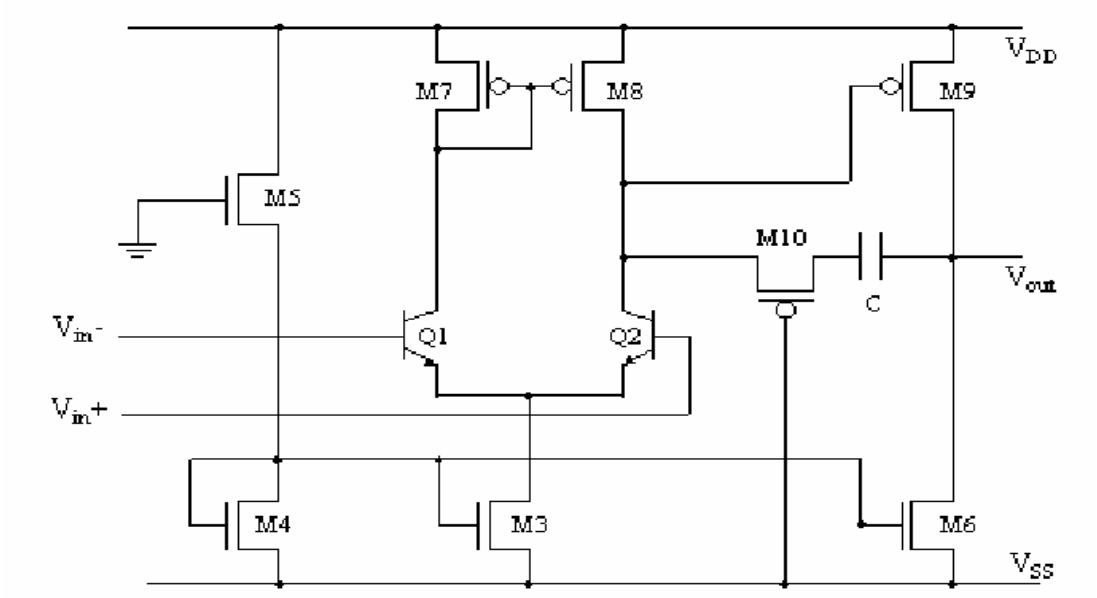

Figure 26. Circuit Layout of Lee Configuration

This op–amp design was used to produce the composite op–amps C2OA2. Figure 27 shows the symbolic diagram of a C20A2 and Figure 28 shows the schematic diagram of a C2OA2. C2OA2 is the combination of two op–amps connected in series with the forward op–amp having a negative feedback loop.

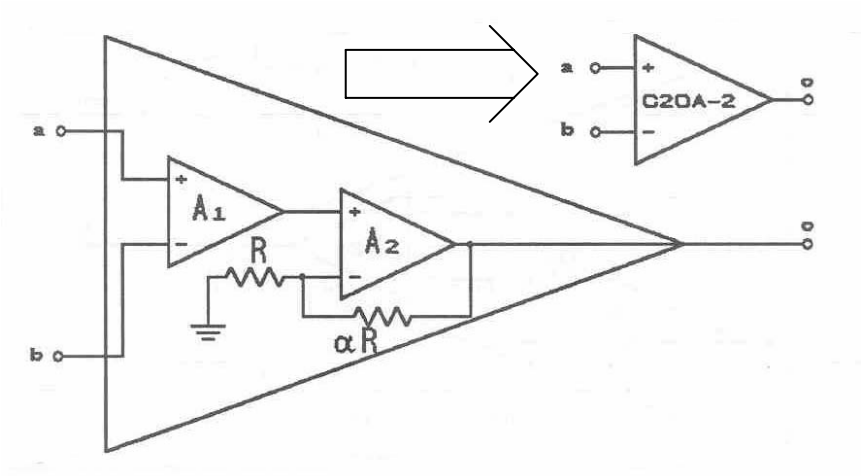

Figure 27. Symbolic Diagram of C2OA2

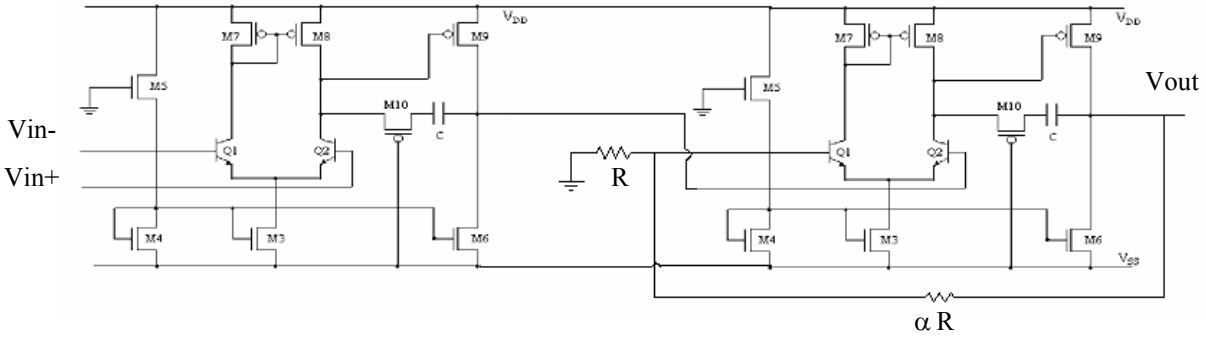

Figure 28. Schematic Diagram of C2OA2 Design

G. SIMULATION OF AUTHOR'S STANDARD AND COMPOSITE DESIGN USED IN THESIS

This section simulates and compares the open loop gain, closed loop gain, slew rate and common rejection ratio of the composite op–amp to the standard op–amp.

1. Open Loop Gain

Each op–amp was designed in Silvaco EXPERT then extracted and tested with Silvaco SMARTSPICE. Figures 29 and 30 show the open loop transfer function for Lee's Configuration and C20A2, respectively. Lee's configuration displays an open loop gain of 45dB while C20A2 registers an open loop gain of 49dB. The gain and α of the composite amplifier is 100 and 6, respectively.

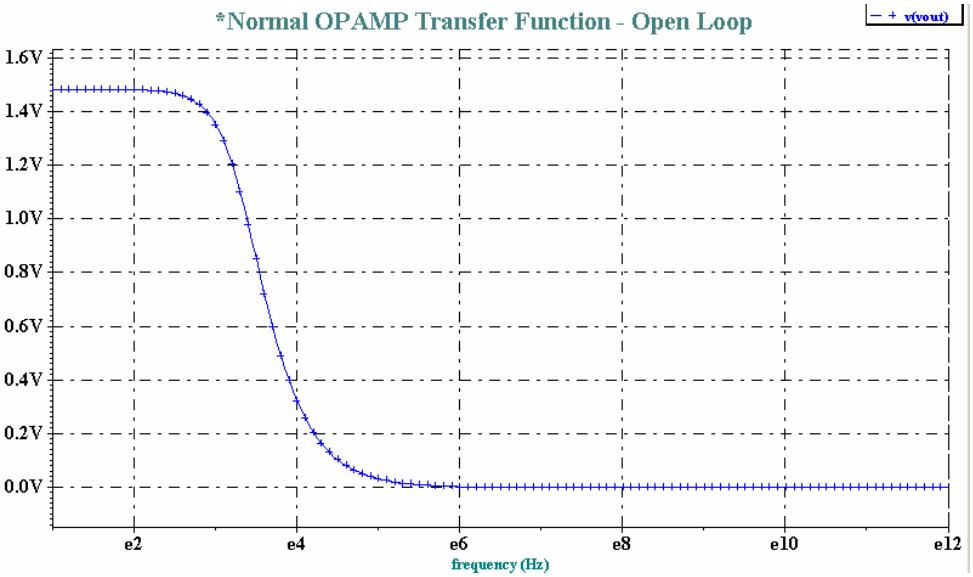

Figure 29. Open Loop Transfer Function of Lee's Configuration B

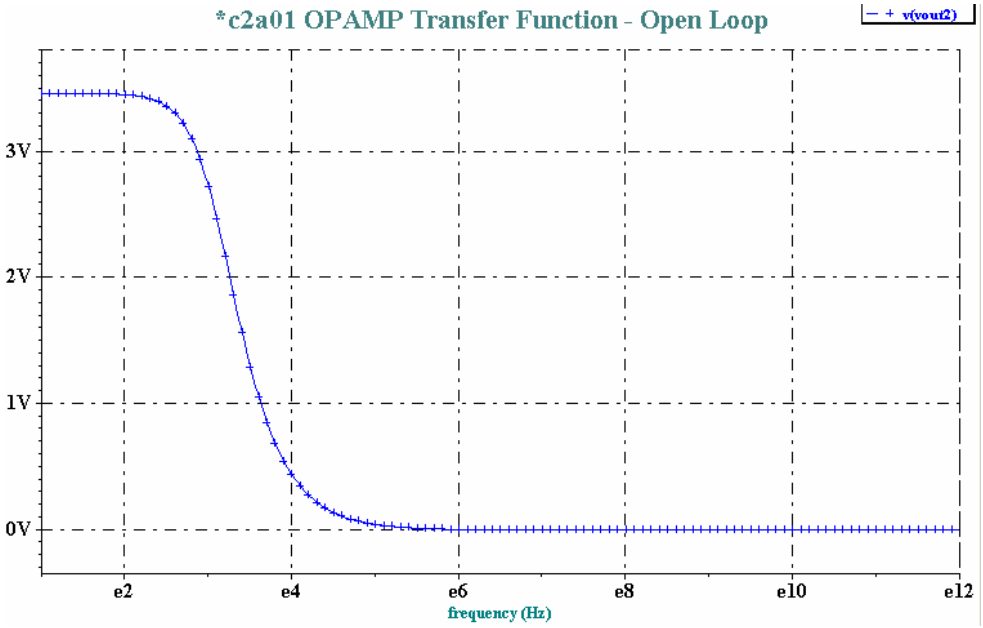

Figure 30. Open Loop Transfer Function of C20A2

Figure 31 shows the comparison between them. It shows that C20A2 has a higher open gain loop as compared to Lee's basic configuration. All codes for the simulation appear in Appendix A.

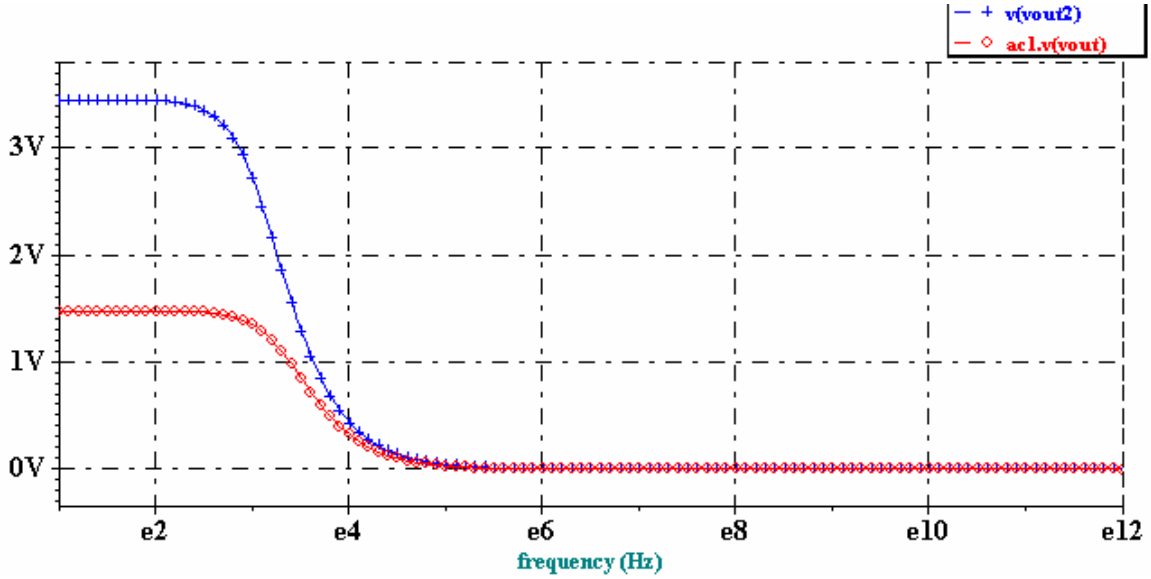

Figure 31. Open Loop Transfer Function – Comparison

2. Closed Loop Gain

Both operational amplifiers were arranged in the configuration shown in Figure 32 to analyze the closed loop gain. The gain of the amplifier is configured to 100.

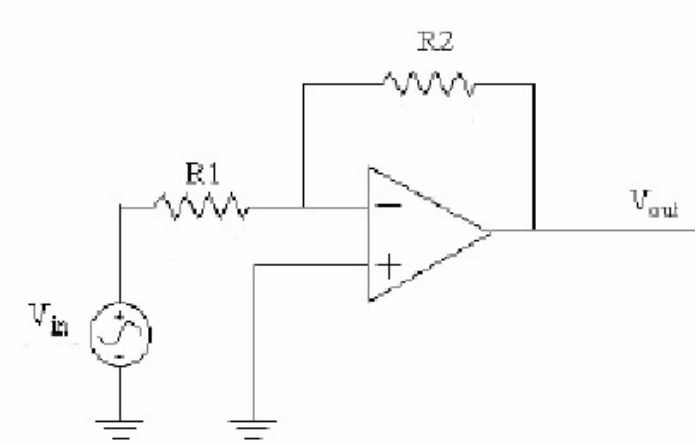

Figure 32. Closed Loop Gain Configuration

Figure 33 shows the closed loop gain of 100 for Lee's configuration. It has a 3dB corner frequency of 110 kHz. Which yielded an equivalent GBWP of about 11 MHz.

On the other hand, Figure 34 shows the C20A2 3dB corner frequency of 1.2 MHz, for the same gain, with a 22.4 MHz 0dB crossing frequency. The corresponding GBWP has improved to to the equivalent of 120 MHz. All codes for the simulation appear in Appendix B.

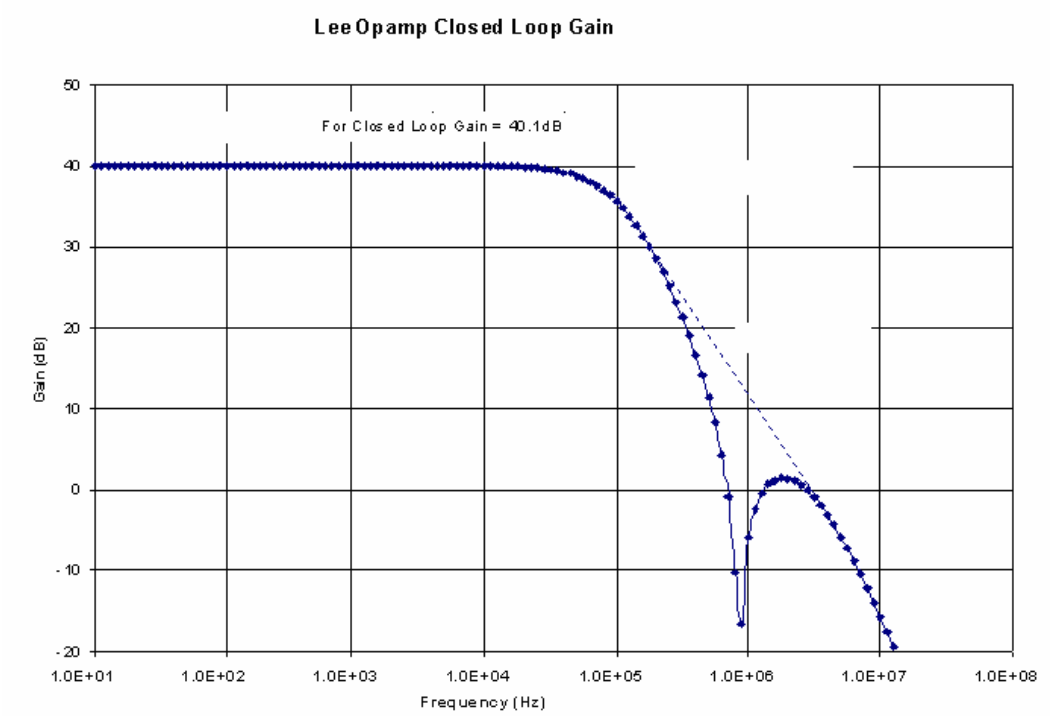

Figure 33. Closed Loop Gain of Lee's Configuration

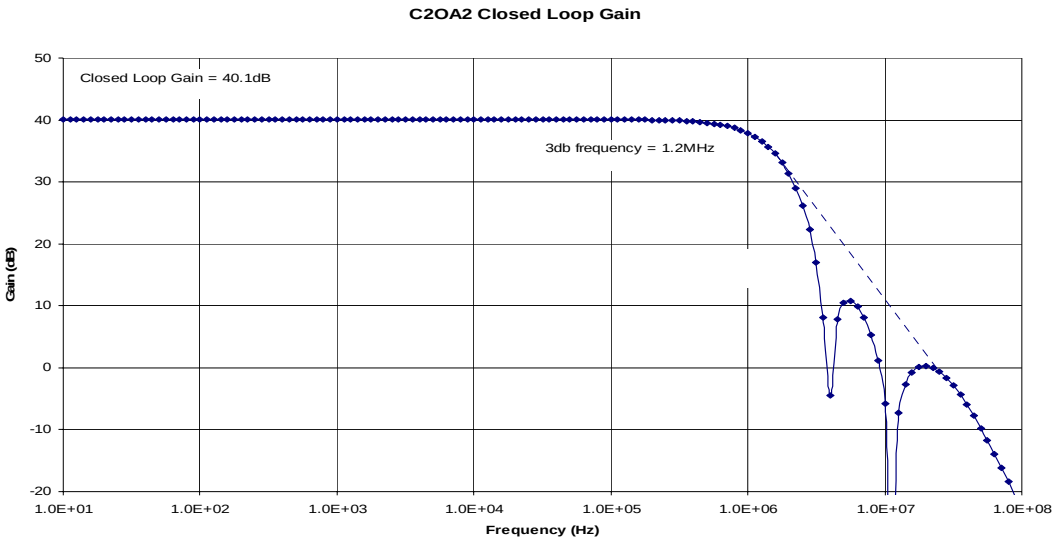

Figure 34. Closed Loop Gain of C20A2

3. Slew Rate

A pulse was injected into the amplifier to observe the output response. Figure 35 shows the slew rate of Lee's configuration. It exhibits a slew rate of 20MV/sec.

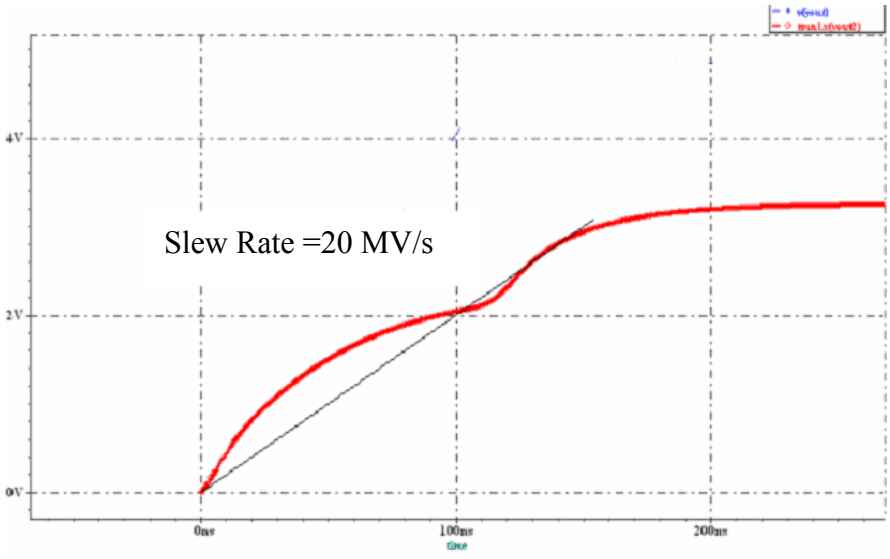

Figure 35. Slew Rate of Lee's Configuration

Figure 36 shows the slew rate of 40MV/sec for C20A2. The slew rate has increased by 20MV/sec in C20A2. All codes for the simulation appear in Appendix C.

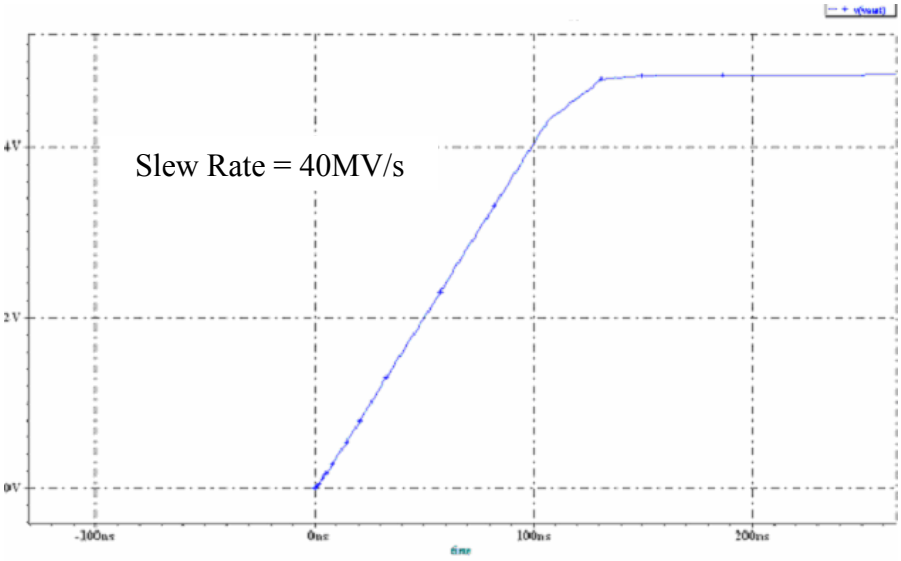

Figure 36. Slew Rate of C20A2

4 Common Mode Rejection Ratio (CMRR)

CMRR is the ability of an operational amplifier to reject the common–mode signal. It is expressed in terms of dB. Figure 37 shows a comparison between Lee's configu-

ration and C20A2. It shows that C20A2 has a higher CMRR. All codes for the simulation appear in Appendix D.

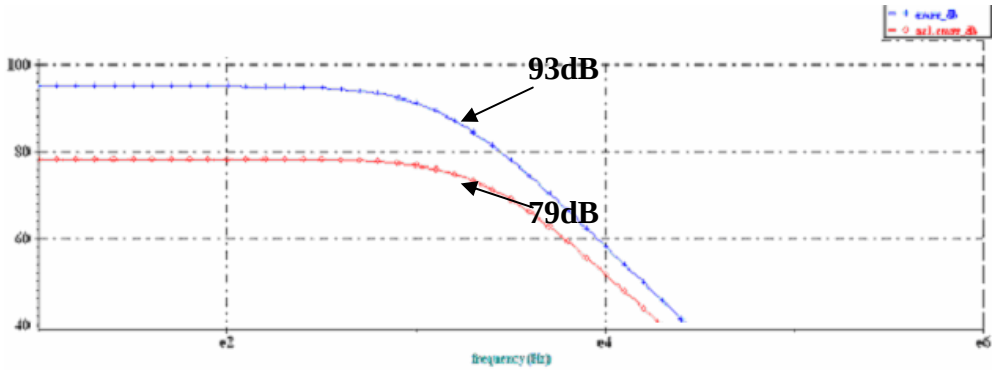

Figure 37. CMRR of Lee's Configuration and C20A2

H. SUMMARY OF SIMULATION PERFORMANCE INDICTOR

Table 8 summarizes the performance indictor for the composite op–amp. The addition of a second op–amp increases the number of poles at lower frequencies and drives down the curve of the transfer function at a steeper rate than Lee's configuration op–amp. This steeper curve allows the frequency of the 3dB point to be pushed higher, but yet still reduces the gain below 0dB before the impact of parasitic capacitances occur at higher frequencies. If these parasitic capacitances come into effect before the gain drops below 0dB, the op–amp may saturate due to positive feedback created by phase shifts and any small amount of noise. It is very clear that the C20A2 is a better op–amp because of improved performance and was easy to implement.

	Open Loop Gain (dB)	3dB Corner Frequency (Hz)	CMRR (dB)	Slew Rate (V/sec)	GBWP (Hz)
Lee's configuration	45	110k	79	20 M	10M
C20A2 (new design)	49.42	1.2M	93	40M	12M

Table 8. Summary of Performance Indictor

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V. GIC FILTER SIMULATION RESULTS

This chapter investigates a continuous analog generalizedd impedance converter (GIC) 4^{th}–order filter band pass filter in detail. Varies parameter like network sensitivity, effects of resistor and capacitor values and GBWP on center frequency (fo) and Q factor (Qp) are investigated. P–SPICE and MATLAB software are used to develop and investigate the simulation differences from the theory result for both the Ideal and Non–Ideal GIC Band Pass filter. Due to the complexity of the 4^{th} order transfer function, MAPLE 8 software is used to derive the Transfer Function for the Ideal and Non–Ideal Op–amp for the GIC filter. All the results from theory, MATLAB and P–SPICE are used to compare the actual circuit buildup prior to future GIC filter chip fabrication.

As mentioned in Chapter II, the GIC filter is well known for its stability and low sensitivity. Each GIC biquad employs two op–amps and has good high frequency performance. The previous chapter proved that the composite op–amp is better than the standard op–amplifier. The performance of the GIC filter will then be further improved by utilizing the newly designed composite op–amp that will not be covered in this thesis.

A. DESIGN DETAILS

The fourth–order filter is achieved by cascade realization. Two matching second–order filter blocks are connected in series (cascaded) to construct a fourth–order band pass filter. Although alternate design methods such as direct synthesis or follow–the–leader–feedback (FLF) may potentially yield slightly better performance, the simplicity and ease of troubleshooting make cascade realization the optimal method for designing this filter. The Band Pass stages are gain adjustable. All GIC stages have equal capacitor values, unless a capacitor is required to adjust the gain.

Figure 38 (schematic) and Figure 39 (circuit layout) depict the circuit topology.

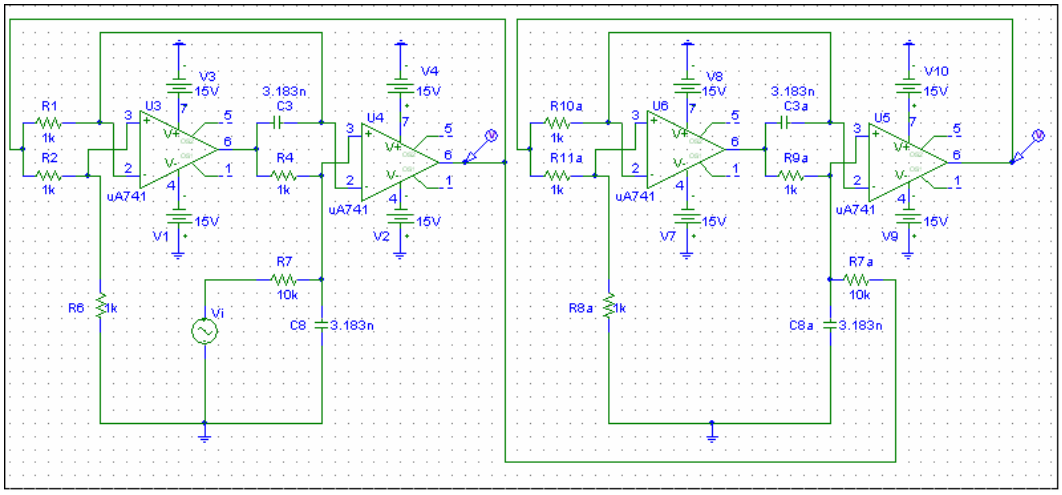

Figure 38. Circuit Schematic

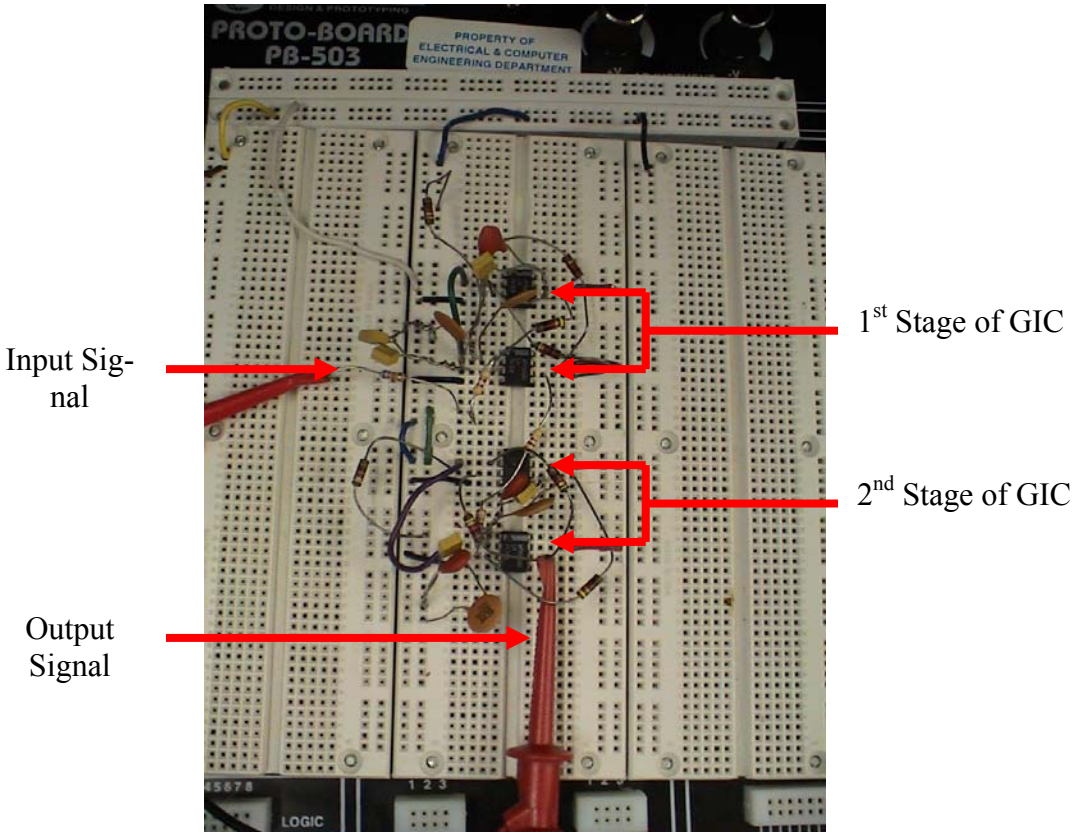

Figure 39. Circuit Layout

B. IDEAL AND NON IDEAL TRANSFER FUNCTIONS

The transfer function for the ideal and non–ideal op–amp for GIC have been derived using Maple 8 software. The initial parameters are set as center frequency (*fo*) of 50KHz and Q factor (*Qp*) of 1. Refer to Appendix E for the derivation of the ideal transfer function for the 4th–order GIC band pass filter.

4th–order TF (ideal):

$$T(s) = \frac{s^2}{(Q_p RC)^2 \cdot s^4 + (2Q_p RC)s^3 + (2{Q_p}^2 + 1)s^2 + \left(\frac{2Q_p}{RC}\right)s + \left(\frac{{Q_p}^2}{R^2C^2}\right)} \tag{5.1}$$

For the purposes of investigating the GIC band pass filter behaviors, resistor and capacitor values are chosen. Substituting design values ($R = 1\ \mathrm{k}\Omega$, $Qp = 10$, $C = 3.183$ nF) produce the transfer function below:

$$T(s) = \frac{(9.86e8)s^2}{s^4 + (6.28e4)s^3 + (1.98e11)s^2 + (6.20e15)s + 9.74e21}. \tag{5.2}$$

4th–order TF (non–ideal) = (with design values substituted into T(s)):

$$T(s) = \frac{(9.87e22)s^4 + (2.04e30)s^3 + (1.05e37)s^2}{s^8 + (2.13e7)s^7 + (2.27e14)s^6 + (1.21e21)s^5 + (3.28e27)s^4 + (4.06e32)s^3 + (5.67e38)s^2 + (2.62e42)s + 2.43e48}. \tag{5.3}$$

C. SENSITIVITIES ANALYSIS FOR $S_{T(S)}^{R}$, $S_{T(S)}^{C}$, $S_{\omega o}^{R}$ AND S_{QP}^{R}

Since the 4th–order filter is achieved by cascade realization, for the ease of calculation, the sensitivities are calculated based on the 1st stage (2nd order) and multiple a factor of 2 for the 2nd stage.

1. $S_{T(s)}^{R}$ = S(Numerator, R) – S(Denominator, R)

$$= \mathrm{R}(\ (\partial\ (\mathrm{Num})/\ \partial\,\mathrm{R})/\mathrm{Num} - (\partial\,\partial\ (\mathrm{Deno})/\partial\,\mathrm{R})/\mathrm{Deno} \tag{5.4}$$

where

$$T(s) = 2\frac{s}{r\,c\,Qp\left(s^2 + \frac{s}{r\,c\,Qp} + \frac{1}{r^2\,c^2}\right)} \tag{5.5}$$

$$\partial\ (\text{Num})/\ \partial\,\text{r} = \frac{\partial}{\partial r}\left(2\frac{s}{r\,c\,Qp}\right) \tag{5.6}$$

$$= -2\frac{s}{r^2\,c\,Qp} \tag{5.7}$$

$$\partial\ (\text{Deno})/\ \partial\,\text{r} = \frac{\partial}{\partial r}\left(s^2 + \frac{s}{r\,c\,Qp} + \frac{1}{r^2\,c^2}\right) \tag{5.8}$$

$$= -\frac{s}{r^2\,c\,Qp} - \frac{2}{r^3\,c^2} \tag{5.9}$$

$$S_{T(s)}{}^{R} = r\left(-\frac{1}{r} - \frac{-\frac{s}{r^2\,c\,Qp} - \frac{2}{r^3\,c^2}}{s^2 + \frac{s}{r\,c\,Qp} + \frac{1}{r^2\,c^2}}\right) \tag{5.10}$$

$$= -\frac{Qp\,(s^2\,r^2\,c^2 - 1)}{s^2\,r^2\,c^2\,Qp + s\,r\,c + Qp} \tag{5.11}$$

Therefore, $S_{T(s)}{}^{R}$ for the 2nd stage

$$= -2\frac{Qp\,(s^2\,r^2\,c^2 - 1)}{s^2\,r^2\,c^2\,Qp + s\,r\,c + Qp} \tag{5.12}$$

2. $\mathbf{S_{T(s)}{}^{C} = S(Num,C) - S(Deno,C)}$

$$= \text{C}(\ (\partial\,(\text{Num})/\ \partial\,\text{C})/\text{Num} - (\partial\ (\text{Deno})/\ \partial\,\text{C})/\text{Deno}) \tag{5.13}$$

$$\partial\ (\text{Num})/\ \partial\,\text{c} = \frac{\partial}{\partial c}\left(2\frac{s}{r\,c\,Qp}\right) \tag{5.14}$$

$$= -2\frac{s}{r\,c^2\,Qp} \tag{5.15}$$

$$\partial\ (\text{Deno})/\ \partial\, c = \frac{\partial}{\partial c}\left(s^2 + \frac{s}{r\ c\ Qp} + \frac{1}{r^2\ c^2}\right) \tag{5.16}$$

$$= -\frac{s}{r\ c^2\ Qp} - \frac{2}{r^2\ c^3} \tag{5.17}$$

$$S_{T(s)}{}^{C} = c\left(-\frac{1}{c} - \frac{-\frac{s}{r\ c^2\ Qp} - \frac{2}{r^2\ c^3}}{s^2 + \frac{s}{r\ c\ Qp} + \frac{1}{r^2\ c^2}}\right) \tag{5.18}$$

$$= -\frac{Qp\ (s^2\ r^2\ c^2 - 1)}{s^2\ r^2\ c^2\ Qp + s\ r\ c + Qp} \tag{5.19}$$

Therefore, $S_{T(s)}{}^{C}$ for the 2nd stage

$$= -2\ \frac{Qp\ (s^2\ r^2\ c^2 - 1)}{s^2\ r^2\ c^2\ Qp + s\ r\ c + Qp} \tag{5.20}$$

3. $\mathbf{S_{\omega o}{}^{R} = S(Num,r) - S(Deno,r)}$

$$= r(\ (\partial\ (\text{Num})/\ \partial\, r)/\text{Num} - (\partial\ (\text{Deno})/\ \partial\, r)/\text{Deno}) \tag{5.21}$$

where

$$\omega_o = 1 / RC \tag{5.22}$$

$$\partial\ (\text{Num})/\ \partial\, r = \frac{\partial}{\partial r}\, 1 \tag{5.23}$$

$$= 0$$

$$\partial\ (\text{Deno})/\ \partial\, r = \frac{\partial}{\partial r}\, r\ c \tag{5.24}$$

$$= c$$

$$S_{\omega o}{}^{R} = -1 \tag{5.25}$$

Therefore, $S_{\omega o}{}^{R}$ for the 2nd stage

$$= -2 \tag{5.26}$$

4. $\mathbf{S_{Qp}^{R} = S(Num,R) - S(Deno,R)}$

$$= R(\ (\partial\ (\text{Num})/\ \partial\ R)/\text{Num}\ -(\partial\ (\text{Deno})/\ \partial\ R)/\text{Deno}) \tag{5.27}$$

where

$$Qp = Rq/R \tag{5.28}$$

$$\partial\ (\text{Num})/\ \partial\ R\ = \frac{\partial}{\partial r}\frac{rq}{r} \tag{5.29}$$

$$= -\frac{rq}{r^2} \tag{5.30}$$

$$\partial\ (\text{Deno})/\ \partial\ R = \frac{\partial}{\partial r} r \tag{5.31}$$

$$= 1$$

$$S_{Qp}^{R} = r\left(-\frac{1}{r^2} - \frac{1}{r}\right) \tag{5.32}$$

$$= -\frac{1+r}{r} \tag{5.33}$$

Therefore, S_{Qp}^{R} for the 2nd stage

$$= -2\frac{1+r}{r} \tag{5.34}$$

D. PLOTTING THE IDEAL AND NON–IDEAL TRANSFER FUNCTION USING MATLAB AND P–SPICE SOFWARE

Please refer to Appendix F for the ideal GIC filter MATLAB program and Appendix G for the non–ideal GIC filter MATLAB program.

For the ideal case, the fo, Gain and Qp are set as 50KHz, 12 dB and Qp=10, respectively. Figure 40 shows the MATLAB Ideal transfer function plot at the second stage output. Figure 41 shows the MATLAB non–ideal transfer function plot at the second stage output.

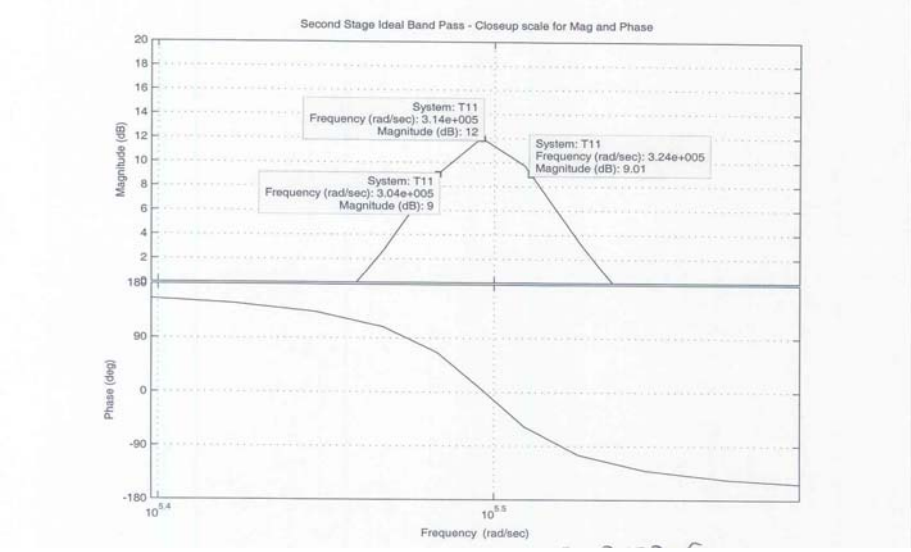

Figure 40. MATLAB Ideal Transfer Function

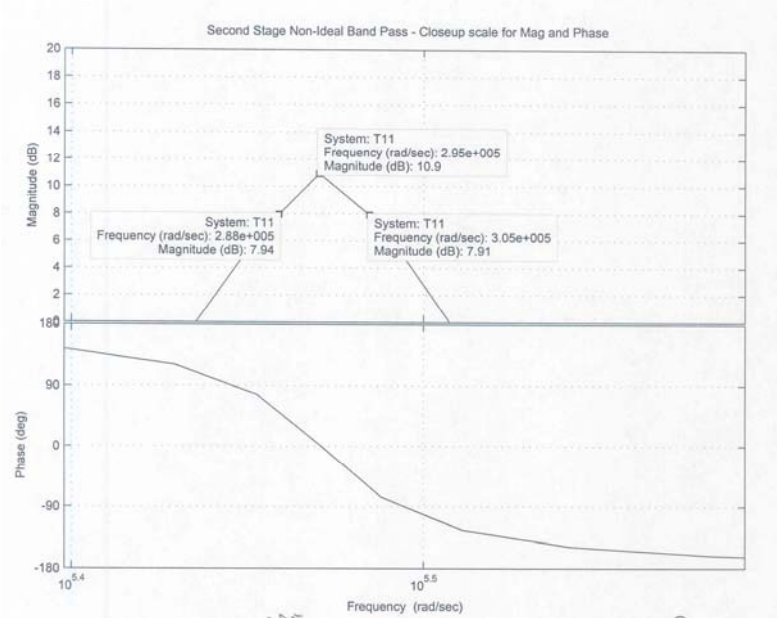

Figure 41. MATLAB Non–Ideal Transfer Function

From the MATLAB simulation, the results are as follows:

Non–Ideal (1st stage): fo =46.951 kHz, Gain=10.9 dB, Qp =9.516

Ideal (1st stage): fo =49.815 kHz, Gain=12 dB, Qp =10.097

Non–Ideal (2nd stage): fo =46.951 kHz, Gain=10.9 dB, Qp =17.353

Ideal (2nd stage): fo =49.975 kHz, Gain=12 dB, Qp =15.7

Figure 42 shows the P–SPICE Frequency response plot. From the P–SPICE simulation, the results are as follows:

fo = 45.394 kHz, Gain=11.997 dB, Qp =16.091

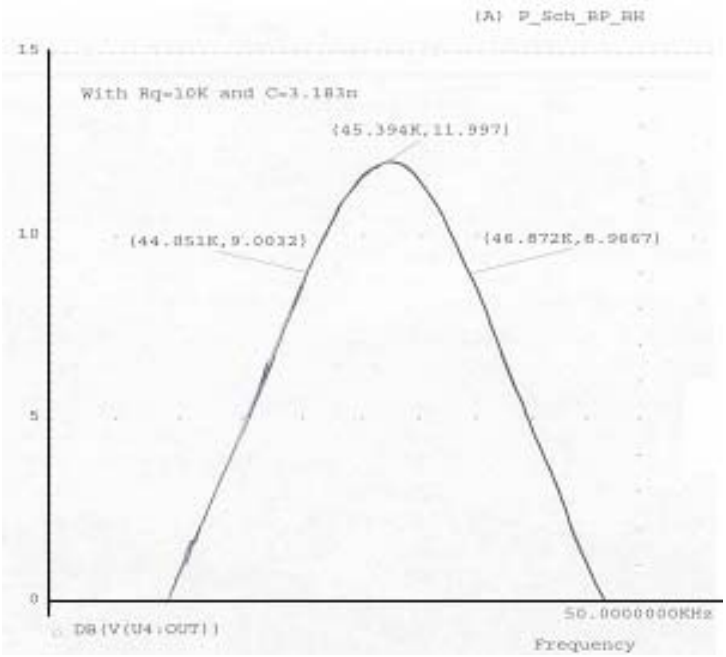

Figure 42. P–SPICE Frequency Response Plot

1. Comparing the Ideal Values with MATLAB Program Values

With the ideal simulation, the fo is closer to 50 kHz in the 2nd stage as compared to the 1st stage. However, the Qp has increased from 10.097 to 15.7 in the 2nd stage. When compared to the non–ideal case, the fo is slightly lower than those in the ideal case second stage. However, the Qp is 10% higher than in the ideal case 2nd stage. Both in MATLAB are quite close.

2. Comparing the MATLAB Program Values and P–SPICE Values

With non–ideal simulation, the fo has decreased to 45.395 kHz. The Qp has also dropped slightly to 16.01. The main reason is due mainly to the operation of this fre-

quency near the GBWP of the op–amp. The P–SPICE shows the actual values to expect in real circuit construction.

***Note**: Reference is taken from the non–ideal MATLAB program values or all the remaining comparisons.

E. ANALYSIS OF THE EFFECT OF 10% VARIATION ON VALUE OF RESISTOR ON *fo* AND *Qp* OF THE NON–IDEAL TRANSFER FUNCTION

Please refer to Appendix H for the non–ideal MATLAB program (non–ideal case with 10% increase in resistor value). The MATLAB simulation for the non–ideal case with no resistor value and capacitor value changes is as follows:

Non–Ideal: fo =46.951 kHz, Gain=10.9, Qp =17.353

Figure 43 shows the non–ideal MATLAB plot (non–ideal case with 10% increase in resistor value). The MATLAB simulation (non–ideal case with 10% increase in resistor value) is as follows.

Non–Ideal: fo =46.951 kHz, Gain=10.9, Qp =17.353

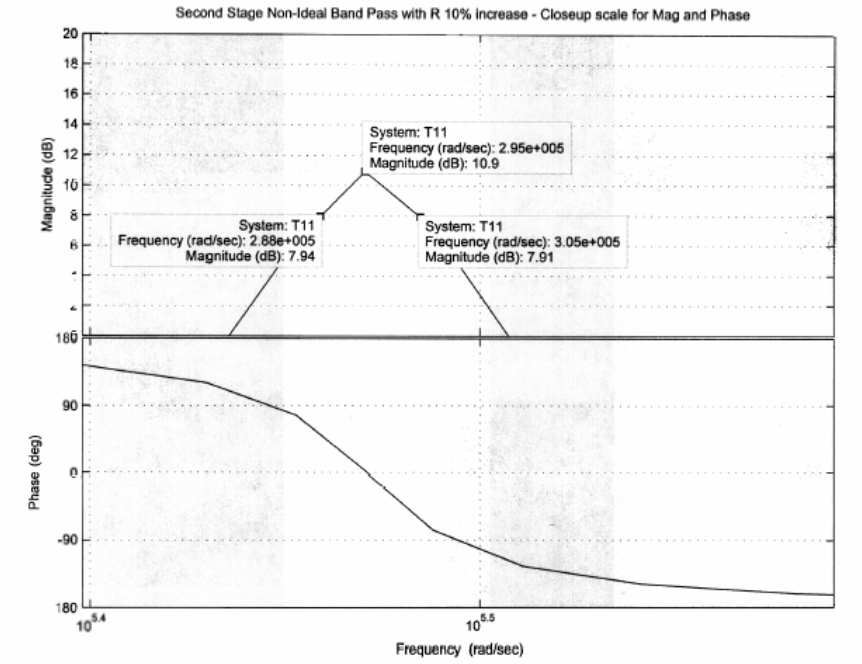

Figure 43. MATLAB Simulation (Non–Ideal Case with 10% Increase in Resistor

Value)

Figure 44 shows the P–SPICE Frequency response plot. From the P–SPICE simulation, the results are as follows.

fo =41.687 kHz, Gain=11.877, Qp =14.499

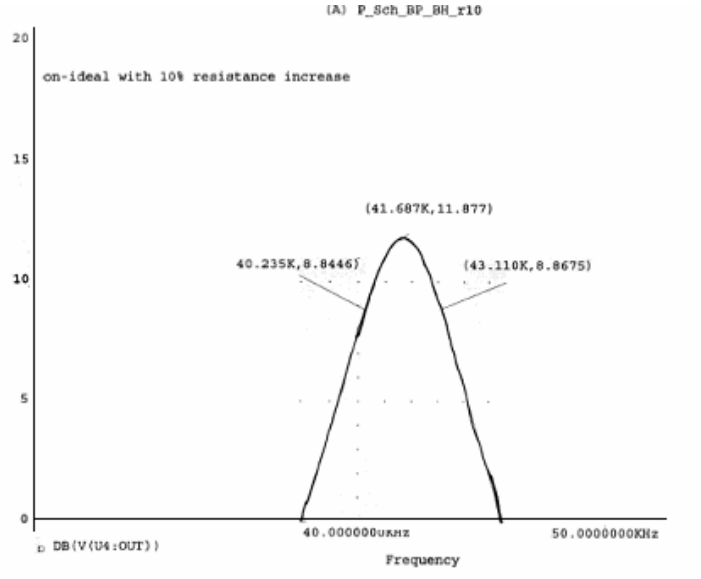

Figure 44. P–SPICE Frequency Response Plot (with 10% Increase in Resistor Value)

1. Comparing the Values in Both MATLAB Programs (with and without 10% Increase in Resistor Value)

With 10% increase in Resistor value, there is no difference between the gain, and there is no difference in fo and Qp. The results show that an increase of 10% in Resistor value does not affect Gain, Qp and fo for this circuit.

2. Comparing the MATLAB Simulation Program Values (with 10% Increase in Resistor Value) and P–SPICE Values (with 10% Increase in Resistor Value)

With a 10% increase in resistor value, the fo has dropped to 41.687 kHz, Qp has also dropped to 14.499. However, the gain has increased to 11.877.

F. ANALYSIS OF THE EFFECT OF 10% VARIATION ON VALUE OF CAPACITOR ON *fo* AND *Qp* OF THE NON–IDEAL TRANSFER FUNCTION

Please refer to Appendix I for the non–ideal MATLAB program (non–ideal case with 10% increase in capacitor value). The MATLAB simulation for the non–ideal case with no resistor value and capacitor values changes is as follows.

Non–Ideal: fo =46.951 kHz, Gain=10.9, Qp =17.353

Figure 45 shows the non–ideal MATLAB plot (non–ideal case with 10% increase in capacitor value). The MATLAB simulation (non–ideal case with 10% increase in capacitor value) is as follows.

Non–Ideal: fo =42.971 kHz, Gain=11.1, Qp =16.875

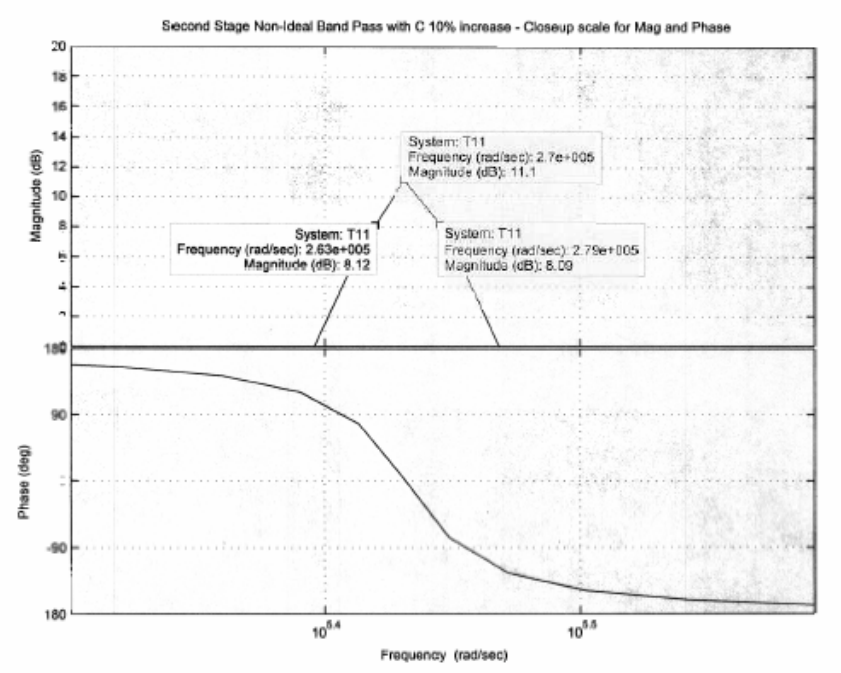

Figure 45. MATLAB Simulation (Non–Ideal Case with 10% Increase in Capacitor Value)

Figure 46 shows the P–SPICE Frequency response plot. From the P–SPICE simulation, the results are as follows.

fo =41,687 kHz, Gain=12.053, Qp =16.595

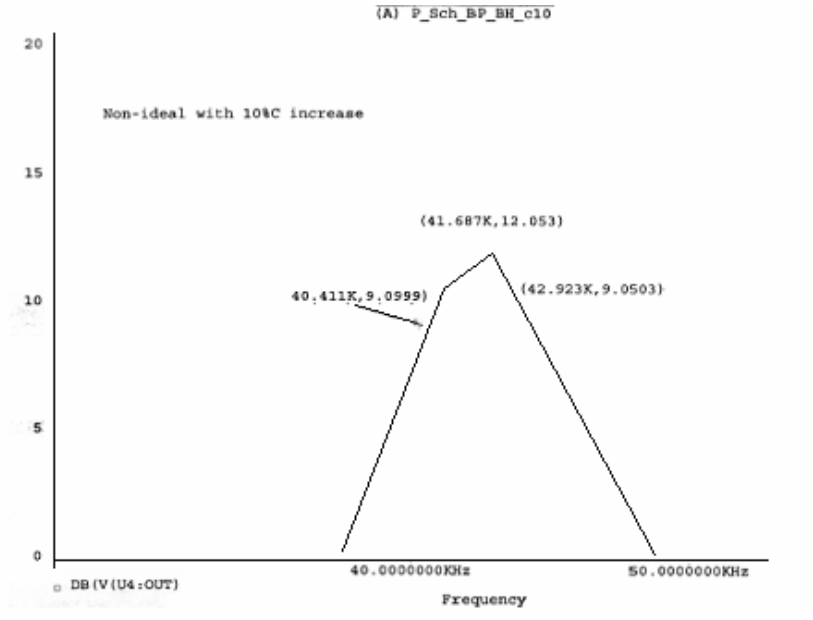

Figure 46. P–SPICE Frequency Response Plot (with 10% Increase in Capacitor Value)

1. Comparing the Values in Both MATLAB Programs (with and without 10% Increase in Capacitor Value)

With 10% increase in capacitor value, the gain has increased slightly to 11.1, both *fo* and *Qp* have decreased to 42.97kHz and 16.875, respectively. In summary, with an increase of capacitor value, *fo* and *Qp* will decrease and gain will increase.

2. Comparing the MATLAB Program Values (with 10% Increase in Capacitor Value) and P–SPICE Values (with 10% Increase in Capacitor Value)

With 10% increase in capacitor value, the *fo* has dropped to 41.687kHz, *Qp* has also dropped slightly to 16.595. However, the gain has increased to 12.053.

G. ANALYSIS OF THE EFFECT OF 10% VALUE INCREASE IN RESISTOR AND 50% DECREASE IN GBWP OF THE NON–IDEAL TRANSFER FUNCTION

Please refer to Appendix J for the non–ideal MATLAB program (non–ideal case with 10% increase in resistor value and 50% decrease of GBWP). The MATLAB simula-

tion for the non–ideal case with a 10% increase in resistor value and 100% of GBWP is as follows.

Non–ideal case with 10% increase in resistor value, 100% GBWP: fo =46.951 kHz, Gain=10.9, Qp =17.353

Refer to Figure 47 for the MATLAB plot (non–ideal case with 10% increase in resistor value, 50% GBWP). The MATLAB simulation for the non–ideal case with 10% increase in resistor value with 50% decrease of GBWP is as follows.

Non–Ideal case: fo =44.563 kHz, Gain=9.18, Qp =15.56

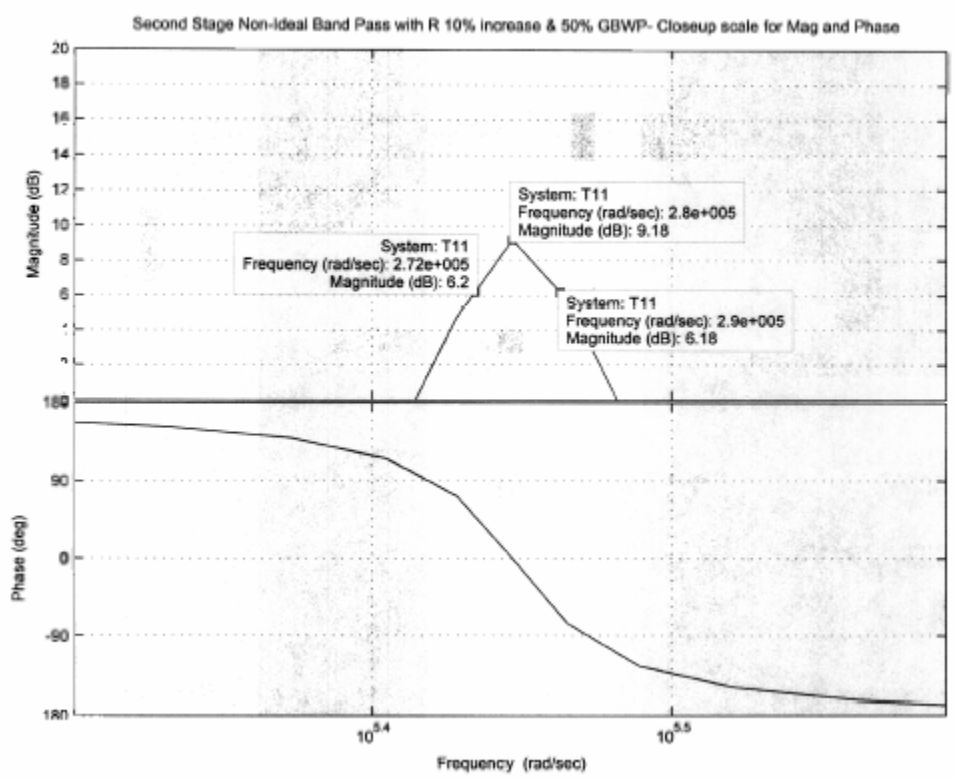

Figure 47. MATLAB Plot (Non–Ideal Case with 10% Increase in Resistor Value and 50% Decrease of GBWP)

Figure 48 shows the P–SPICE Frequency response plot. From the P–SPICE simulation, the results are as follows.

fo =41.687 kHz, Gain=11.877, Qp =14.83

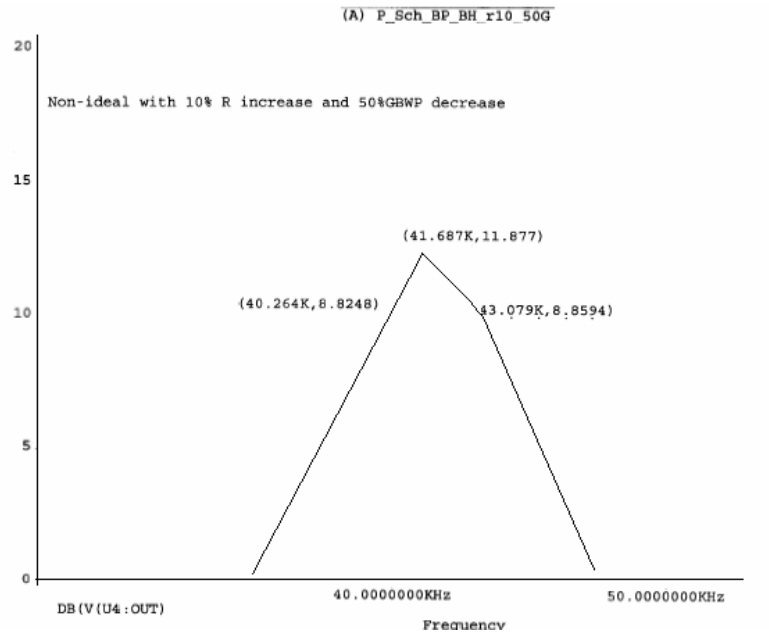

Figure 48. P–SPICE Frequency Response Plot (with 10% Increase in Resistor Value and 50% Decrease of GBWP)

1. Comparing the Values in Both MATLAB Programs (with 10% Increase in Resistor Value for 100% and 50% Reduction of GBWP)

With 50% GBWP reduction, the gain has reduced to 9.18, the *fo* is reduced to 44.563 kHz, and *Qp* is reduced to 15.56. In summary, with 50% GBWP reduction, it will reduce the gain, *fo* and *Qp*.

2. Comparing the MATLAB Program Values (with 10% Increase in Resistor Value for 50% Reduction of GBWP) and P–SPICE Values (with 10% Increase of Resistor Value for 50% Reduction of GBWP)

With 50% GBWP reduction, the *fo* and *Qp* has reduced slightly while the gain has increased slightly to 11.877.

H. ANALYSIS OF THE EFFECT OF 10% VALUE INCREASE IN CAPACITOR AND 50% DECREASE IN GBWP OF THE NON–IDEAL TRANSFER FUNCTION

Please refer to Appendix K for the non–ideal MATLAB program (non–ideal case with 10% increase in capacitor value and 50% decrease of GBWP). The MATLAB simulation for the non–ideal case with 10% increase in capacitor value and 100% of GBWP are as follows.

Non–Ideal case: *fo* =46.951 kHz, Gain=10.9, *Qp* =17.353

Refer to Figure 49 for the MATLAB plot (non–ideal case with 10% increase in capacitor value, 50% GBWP). The MATLAB simulation for the non–ideal case with a 10% increase in capacitor value and 50% of GBWP are as follows.

non–ideal case with 10% increase in capacitor value, 50% GBWP:

fo =40.90ckHz, Gain=9.53, Qp =16.06

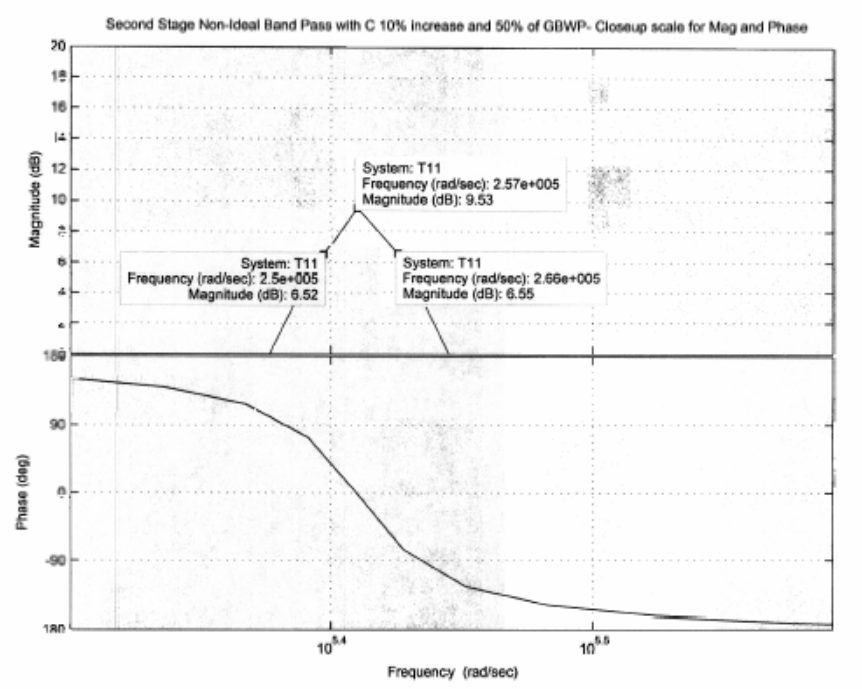

Figure 49. MATLAB Plot (Non–Ideal Case with 10% Increase in Capacitor Value and 50% Decrease of GBWP).

Figure 50 shows the P–SPICE frequency response plot. From the P–SPICE simulation, the results are as follows.

fo =41.687 kHz, Gain=12.053, Qp =16.522

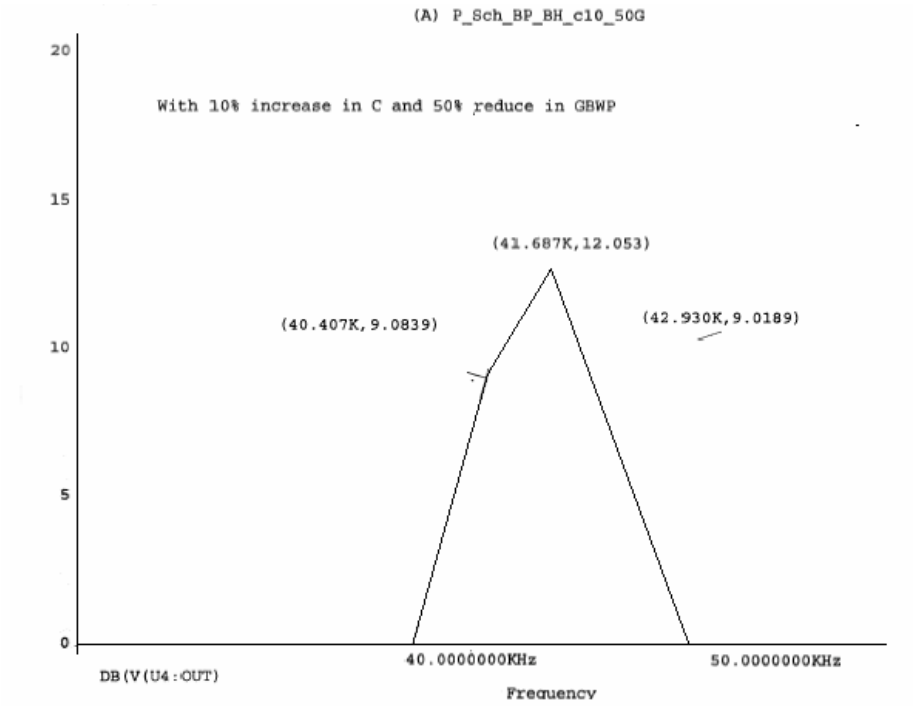

Figure 50. P–SPICE Frequency Response Plot (with 10% Increase in Capacitor Value and 50% Decrease of GBWP)

1. Comparing the Values in Both MATLAB Programs (with 10% Increase in Capacitor Value for 100% and 50% Reduction of GBWP)

With 50% GBWP reduction, the gain has reduced to 9.53, the *fo* has reduced to 40.90kHz, and *Qp* has reduced to 16.06. In summary, with 50% GBWP reduction, it will reduce the gain, *fo* and *Qp*.

2. Comparing the MATLAB Program Values (with 10% Increase in Capacitor Value for 50% Reduction of GBWP) and P–SPICE Values (with 10% Increase in Capacitor Value for 50% Reduction of GBWP)

With 50% GBWP reduction, the *fo*, gain and *Qp* have reduced slightly as compared to P–SPICE.

I. SUMMARY OF SIMULATION RESULTS

There are some differences when comparing the MATLAB program ideal with non–ideal cases. When the operating frequency is close to ideal, the percentage errors become zero, i.e., toward the ideal case.

A 10% increase in resistor values does not affect gain, Qp and fo. However, with 10% increase of capacitor values, fo and Qp decrease with an increase in gain. With 50% GBWP reduction (in the case of 10% increase in resistor value and capacitor value), it reduces the gain, fo and Qp. All values from the P–SPICE program when compared with MATLAB program values are well within 10% error.

After adjusting for non–ideal conditions, the final theoretical value of the circuit built in the laboratory performed very close to the theoretical value. The final value of the center frequency was 50.560 kHz compared to the target value of 50.0 kHz (1.1% higher). The value of Qp was 9.711 compared to a target of 10.0, which is less than 3% error.

J. PRACTICAL CIRCUIT ANALYSIS

In the process of practical circuit building, it was observed that none of the models, i.e., MATLAB and P–SPICE, exactly matches the actual, but P–SPICE shows closer values. However, replacing the Rq and C to achieve the said fo of 50 kHz did several iteration processes. Please refer to Table 9 for the results.

		MATLAB Ideal		MATLAB non-ideal	
Rq	C	fo	Qp	fo	Qp
10k	3.183n	49.975k	15.7	46.951k	17.353
6.667k	3.183n	49.656k	10.4	46.792k	10.138
6.667k	2.86n	53.386k	10.54	51.725k	10.156
6.667k	3.01n	52.521k	10.645	49.338k	10.33

		P-SPICE		Actual	
Rq	C	fo	Qp	fo	Qp
10k	3.183n	45.395k	16.091	47.9	14.5
6.667k	3.183n	45.394k	10.584	47.9	9.39
6.667k	2.86n	50.119k	10.605	52.5	8.89
6.667k	3.01n	47.863k	10.655	50.560k	9.711

Table 9. Summary of Component Values

All the practical values used in the circuit are also calculated as shown in Table 10.

Wp	C	R	Rq	0.667Rq	Remarks
314159.2654	3.18E-12	1000031.06	10000310.59	6700208.10	3.18p
314159.2654	1.00E-07	31.83	318.31	213.27	0.1u
314159.2654	1.00E-08	318.31	3183.10	2132.68	0.01u
314159.2654	2.00E-08	159.15	1591.55	1066.34	0.02u
314159.2654	1.50E-07	21.22	212.21	142.18	0.15u
314159.2654	2.20E-07	14.47	144.69	96.94	0.22u
314159.2654	2.50E-07	12.73	127.32	85.31	0.25u
314159.2654	7.50E-10	4244.13	42441.32	28435.68	750p
314159.2654	6.80E-10	4681.03	46810.28	31362.89	680p
314159.2654	5.60E-10	5684.11	56841.05	38083.50	560p
314159.2654	4.70E-10	6772.55	67725.51	45376.09	470p
314159.2654	3.30E-09	964.58	9645.75	6462.66	3.3n

Table 10. Summary of Calculated Values

MATLAB, P–SPICE and actual frequency response for the practical circuit are depicted in the Figures 51, 52 and 53, respectively.

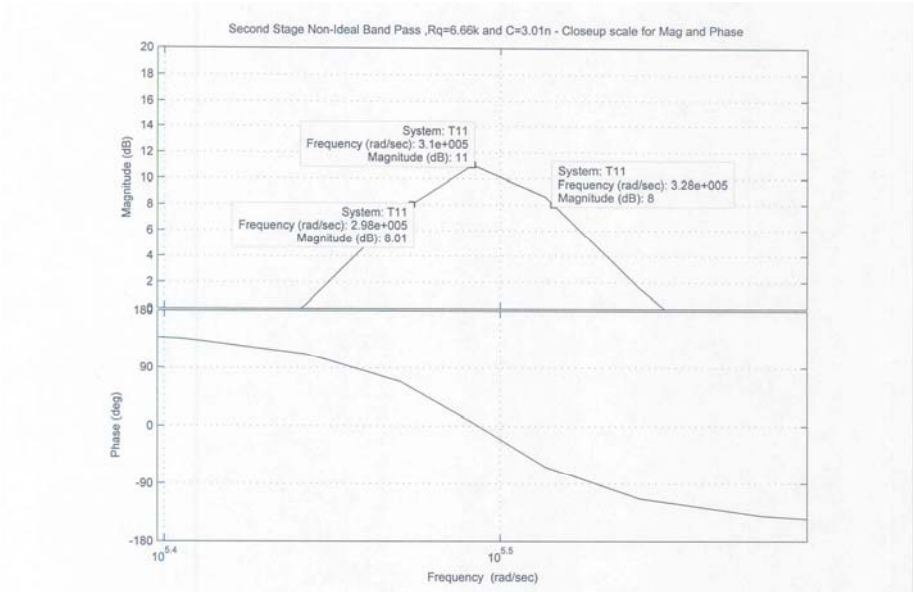

Figure 51. MATLAB Plot: Center Frequency = 49.338 kHz, Qp = 10.33

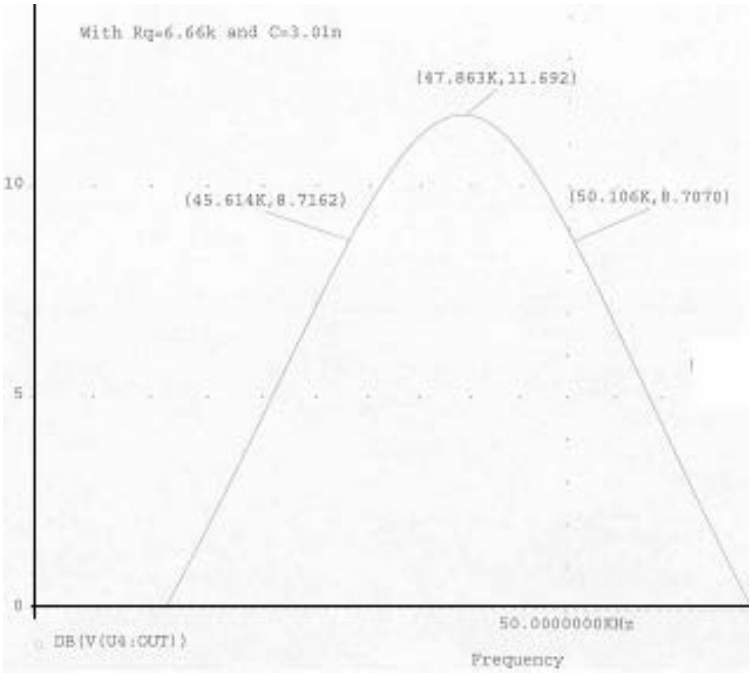

Figure 52. P–SPICE Frequency Response: Center Frequency = 47.853 kHz, Qp = 10.655

Figure 53. Actual Frequency Response: Center Frequency = 50.560 kHz, Qp = 9.711

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VI. CONCLUSIONS AND RECOMMENDATIONS

The primary goal of this thesis was to investigate the continuous analog generalized impedance converter (GIC) 4th–order band pass filter, ideal and non–ideal cases, in detail with software aids such as MATLAB, P–SPICE and MAPLE. MATLAB software depicted more accurate data when compared to theoretical results whereas P–SPICE demonstrated the practice aspect of the circuit design. In the actual circuit setup, there are too many components variation like tolerates in resistor value and capacitor value. However, all this can be overcome by implementing the design in VLSI.

The gain, *fo* and Q factor are not affected by 10% increase in resistor values. However, 10% increase in capacitor value causes center frequency and Q factor to decrease and gain to increase. With 50% GBWP reduction (for 10% increase in Resistor value and capacitor values), it will reduce the gain, center frequency and Q factor. All the P–SPICE program values when compared to MATLAB program values are all well within 10% error. The final design of the circuit built in the laboratory performed very close to the stated specifications. The final value of the center frequency was 50.560 kHz compared to the target value of 50.0 kHz (1.1% higher). The value of Q factor was 9.711 compared to a target of 10.0, which is less than 3% error.

The secondary objective was to investigate the previous student's designed BiCMOS standard operational amplifier and improve it as a composite operational amplifier. The composite amplifier was introduced during the Analog VLSI course taught by Professor Michael at the Naval Postgradute School, and the author was very impressed by the design and has proven its worth in this thesis. The results show that the gain bandwidth product (GBWP), common mode rejection ratio (CMRR), and open loop gain improved considerably.

The author tried to simulate the filter design initially using PSPICE and found it very difficult as the actual component technical data are different from the design requirements. Efforts were made to contact http://www.orcadpcb.com for the details. However, those parameters were unable to be alttered to suit the filter design. The author sub-

sequently designed the composite amplifier (C20A2) in Silvaco EXPERT software, and then extracted and simulated it with the Silvaco SmartSpice software. It was possible to alter all parameters by changing the width and length of the gates using the Silvaco EXPERT software.

With the improvements from the composite operational amplifier, it sets the basic foundation for future students to incorporate the newly designed composite operational amplifier into the GIC filter to enhance the filter performance further.

APPENDIX A. OPEN LOOP

A. OPEN LOOP – LEE'S CONFIGURATION [6], SPICE NETLIST

```
*Normal OPAMP Transfer Function – Open Loop
.INCLUDE AMIparams.txt
*Power Supplies
VDD VDD GND DC 5.0
VSS VSS GND DC –5.0
*Signal
VI+ VIn+ GND DC 0.0 AC 10m
VI– VIn– GND DC 0.0
*OPAMP CIRCUIT
.MODEL CMOSP1 PMOS
.MODEL CMOSP2 PMOS
.MODEL CMOSN1 NMOS
.MODEL CMOSN2 NMOS
.MODEL NPN1 NPN
Q1 VN1 VIN– VN5 NPN1 AREA=2.560P
Q2 VN2 VIN+ VN5 NPN1 AREA=2.560P
M3 VN5 VN4 VSS VSS CMOSN1 W= 27.2U L= 5.2U
M4 VN4 VN4 VSS VSS CMOSN1 W= 13.2U L= 5.2U
M5 VDD GND VN4 vss CMOSN1 W= 5.2U L= 33.2U
M9 VDD VN2 VOUT VDD CMOSP1 W= 150U L= 5.2U
M6 VOUT VN4 VSS VSS CMOSN1 W= 67.2U L= 5.2U
C1 VOUT VN3 1.032P
ckill vout gnd 1.966p
M10 VN3 VSS VN2 VDD CMOSP1 W= 5.2U L= 5.2U
M7 VN1 VN1 VDD VDD CMOSP1 W= 30U L= 5.2U
M8 VN2 VN1 VDD VDD CMOSP1 W= 30U L= 5.2U
*R1 R1in Vin– 1k
*R2 VOut Vin– 100k
*Input Stimulus, Options and Measurments
*.TRAN 1p 16n 0n
.AC DEC 20 10 1E+12
.plot v(VOut) v(VDD) v(VSS)
.plot v(VDD)
.plot v(VSS)
.end
```

B. OPEN LOOP – C20A2 CONFIGURATION SPICE NETLIST

```
*c2a01 OPAMP Transfer Function – Open Loop
.INCLUDE AMIparams.txt
*Power Supplies
VDD VDD GND DC 5.0
VSS VSS GND DC –5.0
*Signal
VI+ VIn+ GND DC 0.0 AC 10m
VI– Vin– GND DC 0.0
*OPAMP_1 CIRCUIT
.MODEL CMOSP1 PMOS
.MODEL CMOSP2 PMOS
.MODEL CMOSN1 NMOS
.MODEL CMOSN2 NMOS
.MODEL NPN1 NPN
Q1 VN1 VIN– VN5 NPN1 AREA=2.560P
Q2 VN2 VIN+ VN5 NPN1 AREA=2.560P
M3 VN5 VN4 VSS VSS CMOSN1 W= 27.2U L= 5.2U
M4 VN4 VN4 VSS VSS CMOSN1 W= 13.2U L= 5.2U
M5 VDD GND VN4 vss CMOSN1 W= 5.2U L= 33.2U
M9 VDD VN2 vin+2 VDD CMOSP1 W= 150U L= 5.2U
M6 Vin+2 VN4 VSS VSS CMOSN1 W= 67.2U L= 5.2U
C1 vin+2 VN3 1.032P
M10 VN3 VSS VN2 VDD CMOSP1 W= 5.2U L= 5.2U
M7 VN1 VN1 VDD VDD CMOSP1 W= 30U L= 5.2U
M8 VN2 VN1 VDD VDD CMOSP1 W= 30U L= 5.2U
*OPAMP_2 CIRCUIT
Q12 VN12 VIN–2 VN52 NPN1 AREA=2.560P
Q22 VN22 VIN+2 VN52 NPN1 AREA=2.560P
M32 VN52 VN42 VSS VSS CMOSN1 W= 27.2U L= 5.2U
M42 VN42 VN42 VSS VSS CMOSN1 W= 13.2U L= 5.2U
M52 VDD GND VN42 vss CMOSN1 W= 5.2U L= 33.2U
M92 VDD VN2 VOUT2 VDD CMOSP1 W= 150U L= 5.2U
M62 VOUT2 VN42 VSS VSS CMOSN1 W= 67.2U L= 5.2U
C12 VOUT2 VN32 1.032P
M102 VN32 VSS VN22 VDD CMOSP1 W= 5.2U L= 5.2U
M72 VN12 VN12 VDD VDD CMOSP1 W= 30U L= 5.2U
M82 VN22 VN12 VDD VDD CMOSP1 W= 30U L= 5.2U
*interconnect bet op1 and op2, alpha=6.10 1k 10k
R1c vin–2 gnd 1k
R2c vin–2 vout2 8k
*feedback R
*R1 r1in Vin– 1k
*R2 VOut2 Vin– 100k
ckill vin+2 gnd 1.966p
```

```
ckill2 vout2 gnd 1.966p
*Input Stimulus, Options and Measurments
*.TRAN 1p 16n 0n
.AC DEC 20 10 1E+12
.plot v(VOut2)
.plot v(VDD)
.plot v(VSS)
```

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APPENDIX B. CLOSED LOOP

A. CLOSED LOOP – LEE'S CONFIGURATION [6] , SPICE NETLIST

```
*Normal OPAMP Transfer Function – closed loop
.INCLUDE AMIparams.txt
*Power Supplies
VDD VDD GND DC 5.0
VSS VSS GND DC –5.0
*Signal
VI+ VIn+ GND DC 0.0 AC 10m
VI– R1in GND DC 0.0
*OPAMP CIRCUIT
.MODEL CMOSP1 PMOS
.MODEL CMOSP2 PMOS
.MODEL CMOSN1 NMOS
.MODEL CMOSN2 NMOS
.MODEL NPN1 NPN
Q1 VN1 VIN– VN5 NPN1 AREA=2.560P
Q2 VN2 VIN+ VN5 NPN1 AREA=2.560P
M3 VN5 VN4 VSS VSS CMOSN1 W= 27.2U L= 5.2U
M4 VN4 VN4 VSS VSS CMOSN1 W= 13.2U L= 5.2U
M5 VDD GND VN4 vss CMOSN1 W= 5.2U L= 33.2U
M9 VDD VN2 VOUT VDD CMOSP1 W= 150U L= 5.2U
M6 VOUT VN4 VSS VSS CMOSN1 W= 67.2U L= 5.2U
C1 VOUT VN3 1.032P
ckill vout gnd 1.966p
M10 VN3 VSS VN2 VDD CMOSP1 W= 5.2U L= 5.2U
M7 VN1 VN1 VDD VDD CMOSP1 W= 30U L= 5.2U
M8 VN2 VN1 VDD VDD CMOSP1 W= 30U L= 5.2U
R1 R1in Vin– 1k
R2 VOut Vin– 100k
*Input Stimulus, Options and Measurments
*.TRAN 1p 16n 0n
.AC DEC 20 10 1E+12
.plot v(VOut) v(VDD) v(VSS)
.plot v(VDD)
.plot v(VSS)
.end
```

B. CLOSED LOOP – C20A2 CONFIGURATION SPICE NETLIST

```
*c2a01 OPAMP Transfer Function –closed Loop
.INCLUDE AMIparams.txt
*Power Supplies
VDD VDD GND DC 5.0
VSS VSS GND DC –5.0

*Signal
VI+ VIn+ GND DC 0.0 AC 10m
VI– R1in GND DC 0.0
*OPAMP_1 CIRCUIT
.MODEL CMOSP1 PMOS
.MODEL CMOSP2 PMOS
.MODEL CMOSN1 NMOS
.MODEL CMOSN2 NMOS
.MODEL NPN1 NPN
Q1 VN1 VIN– VN5 NPN1 AREA=2.560P
Q2 VN2 VIN+ VN5 NPN1 AREA=2.560P
M3 VN5 VN4 VSS VSS CMOSN1 W= 27.2U L= 5.2U
M4 VN4 VN4 VSS VSS CMOSN1 W= 13.2U L= 5.2U
M5 VDD GND VN4 vss CMOSN1 W= 5.2U L= 33.2U
M9 VDD VN2 vin+2 VDD CMOSP1 W= 150U L= 5.2U
M6 Vin+2 VN4 VSS VSS CMOSN1 W= 67.2U L= 5.2U
C1 vin+2 VN3 1.032P
M10 VN3 VSS VN2 VDD CMOSP1 W= 5.2U L= 5.2U
M7 VN1 VN1 VDD VDD CMOSP1 W= 30U L= 5.2U
M8 VN2 VN1 VDD VDD CMOSP1 W= 30U L= 5.2U
*OPAMP_2 CIRCUIT
Q12 VN12 VIN–2 VN52 NPN1 AREA=2.560P
Q22 VN22 VIN+2 VN52 NPN1 AREA=2.560P
M32 VN52 VN42 VSS VSS CMOSN1 W= 27.2U L= 5.2U
M42 VN42 VN42 VSS VSS CMOSN1 W= 13.2U L= 5.2U
M52 VDD GND VN42 vss CMOSN1 W= 5.2U L= 33.2U
M92 VDD VN2 VOUT2 VDD CMOSP1 W= 150U L= 5.2U
M62 VOUT2 VN42 VSS VSS CMOSN1 W= 67.2U L= 5.2U
C12 VOUT2 VN32 1.032P
M102 VN32 VSS VN22 VDD CMOSP1 W= 5.2U L= 5.2u
M72 VN12 VN12 VDD VDD CMOSP1 W= 30U L= 5.2U
M82 VN22 VN12 VDD VDD CMOSP1 W= 30U L= 5.2U
*interconnect bet op1 and op2, alpha=6.10 1k 10k
R1c vin–2 gnd 1k
R2c vin–2 vout2 8k
*feedback R
R1 r1in Vin– 1k
R2 VOut2 Vin– 100k
```

```
ckill vin+2 gnd 1.966p
ckill2 vout2 gnd 1.966p
*Input Stimulus, Options and Measurments
*.TRAN 1p 16n 0n
.AC DEC 20 10 1E+12
.plot v(VOut2)
.plot v(VDD)
.plot v(VSS)
.end
```

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APPDENDIX C. SLEW RATE

A. SLEW RATE – LEE'S CONFIGURATION [6] , SPICE NETLIST

```
*Normal OPAMP Transfer Function – slew rate
.INCLUDE AMIparams.txt
*Power Supplies
VDD VDD GND DC 5.0
VSS VSS GND DC –5.0
*Signal
VI+ vin+ gnd PULSE(0 5 0 0.01pS 0.01ps 10mS )
VI– VIn– vout 0.0
*OPAMP CIRCUIT
.MODEL CMOSP1 PMOS
.MODEL CMOSP2 PMOS
.MODEL CMOSN1 NMOS
.MODEL CMOSN2 NMOS
.MODEL NPN1 NPN
Q1 VN1 VIN– VN5 NPN1 AREA=2.560P
Q2 VN2 VIN+ VN5 NPN1 AREA=2.560P
M3 VN5 VN4 VSS VSS CMOSN1 W= 27.2U L= 5.2U
M4 VN4 VN4 VSS VSS CMOSN1 W= 13.2U L= 5.2U
M5 VDD GND VN4 vss CMOSN1 W= 5.2U L= 33.2U
M9 VDD VN2 VOUT VDD CMOSP1 W= 150U L= 5.2U
M6 VOUT VN4 VSS VSS CMOSN1 W= 67.2U L= 5.2U
C1 VOUT VN3 1.032P
ckill vout gnd 1.966p
M10 VN3 VSS VN2 VDD CMOSP1 W= 5.2U L= 5.2U
M7 VN1 VN1 VDD VDD CMOSP1 W= 30U L= 5.2U
M8 VN2 VN1 VDD VDD CMOSP1 W= 30U L= 5.2U
*R1 R1in Vin– 1k
*R2 VOut Vin– 100k
*Input Stimulus, Options and Measurments
*.TRAN 1m 20m 0n
.TRAN 10PS 400NS 1NS
*.AC DEC 20 10 1E+6
.plot v(VOut)
.plot v(VDD)
.plot v(VSS)
.end
```

B. SLEW RATE – C20A2 CONFIGURATION SPICE NETLIST

```
*c2a01 OPAMP Transfer Function –slew rate
.INCLUDE AMIparams.txt
*Power Supplies
VDD VDD GND DC 5.0
VSS VSS GND DC –5.0
*Signal
VI+ vin+ gnd PULSE(0 5 0 0.01pS 0.01ps 10mS )
VI– VIn– vout2 0.0
*OPAMP_1 CIRCUIT
.MODEL CMOSP1 PMOS
.MODEL CMOSP2 PMOS
.MODEL CMOSN1 NMOS
.MODEL CMOSN2 NMOS
.MODEL NPN1 NPN
Q1 VN1 VIN– VN5 NPN1 AREA=2.560P
Q2 VN2 VIN+ VN5 NPN1 AREA=2.560P
M3 VN5 VN4 VSS VSS CMOSN1 W= 27.2U L= 5.2U
M4 VN4 VN4 VSS VSS CMOSN1 W= 13.2U L= 5.2U
M5 VDD GND VN4 vss CMOSN1 W= 5.2U L= 33.2U
M9 VDD VN2 vin+2 VDD CMOSP1 W= 150U L= 5.2U
M6 Vin+2 VN4 VSS VSS CMOSN1 W= 67.2U L= 5.2U
C1 vin+2 VN3 1.032P
M10 VN3 VSS VN2 VDD CMOSP1 W= 5.2U L= 5.2U
M7 VN1 VN1 VDD VDD CMOSP1 W= 30U L= 5.2U
M8 VN2 VN1 VDD VDD CMOSP1 W= 30U L= 5.2U
*OPAMP_2 CIRCUIT
Q12 VN12 VIN–2 VN52 NPN1 AREA=2.560P
Q22 VN22 VIN+2 VN52 NPN1 AREA=2.560P
M32 VN52 VN42 VSS VSS CMOSN1 W= 27.2U L= 5.2U
M42 VN42 VN42 VSS VSS CMOSN1 W= 13.2U L= 5.2U
M52 VDD GND VN42 vss CMOSN1 W= 5.2U L= 33.2U
M92 VDD VN2 VOUT2 VDD CMOSP1 W= 150U L= 5.2U
M62 VOUT2 VN42 VSS VSS CMOSN1 W= 67.2U L= 5.2U
C12 VOUT2 VN32 1.032P
M102 VN32 VSS VN22 VDD CMOSP1 W= 5.2U L= 5.2u
M72 VN12 VN12 VDD VDD CMOSP1 W= 30U L= 5.2U
M82 VN22 VN12 VDD VDD CMOSP1 W= 30U L= 5.2U
*interconnect bet op1 and op2, alpha=6.10 1k 10k
R1c vin–2 gnd 1k
R2c vin–2 vout2 8k
*feedback R
*R1 r1in Vin– 1k
*R2 VOut2 Vin– 100k
ckill vin+2 gnd 1.966p
```

```
ckill2 vout2 gnd 1.966p
*Input Stimulus, Options and Measurments
*.TRAN 1m 20m 0n
.TRAN 10PS 400NS 1NS
*.AC DEC 20 10 1E+6
.plot v(VOut2)
.plot v(VDD)
.plot v(VSS)
.end
```

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APPENIDX D. CMRR

A. CMRR – LEE'S CONFIGURATION [6] , SPICE NETLIST

```
*Normal OPAMP Transfer Function – CMRR
.INCLUDE AMIparams.txt
*Power Supplies
VDD VDD GND DC 5.0
VSS VSS GND DC –5.0
*Signal
VI+ VIn+ Vin– DC 0.0 AC 1000p
VI– Vin– GND DC 0.0
*VI+ VIn+ GND DC 0.0 AC 1000p
*VI– Vin– GND DC 0.0 AC 1000p
*OPAMP CIRCUIT
.MODEL CMOSP1 PMOS
.MODEL CMOSP2 PMOS
.MODEL CMOSN1 NMOS
.MODEL CMOSN2 NMOS
.MODEL NPN1 NPN
Q1 VN1 VIN– VN5 NPN1 AREA=2.560P
Q2 VN2 VIN+ VN5 NPN1 AREA=2.560P
M3 VN5 VN4 VSS VSS CMOSN1 W= 27.2U L= 5.2U
M4 VN4 VN4 VSS VSS CMOSN1 W= 13.2U L= 5.2U
M5 VDD GND VN4 vss CMOSN1 W= 5.2U L= 33.2U
M9 VDD VN2 VOUT VDD CMOSP1 W= 150U L= 5.2U
M6 VOUT VN4 VSS VSS CMOSN1 W= 67.2U L= 5.2U
C1 VOUT VN3 1.032P
ckill vout gnd 1.966p
M10 VN3 VSS VN2 VDD CMOSP1 W= 5.2U L= 5.2U
M7 VN1 VN1 VDD VDD CMOSP1 W= 30U L= 5.2U
M8 VN2 VN1 VDD VDD CMOSP1 W= 30U L= 5.2U
*R1 R1in Vin– 1k
*R2 VOut Vin– 100k
*Input Stimulus, Options and Measurments
*.TRAN 1p 16n 0n
.AC DEC 20 10 1E+6
.plot v(VOut)
.plot v(VDD)
.plot v(VSS)
.end
```

B. CMRR – C20A2 CONFIGURATION SPICE NETLIST

```
*c2a01 OPAMP Transfer Function –CMRR
.INCLUDE AMIparams.txt
*Power Supplies
VDD VDD GND DC 5.0
VSS VSS GND DC –5.0
*Signal
VI+ VIn+ vin– DC 0.0 ac 1000p
VI– Vin– GND DC 0.0
*OPAMP_1 CIRCUIT
.MODEL CMOSP1 PMOS
.MODEL CMOSP2 PMOS
.MODEL CMOSN1 NMOS
.MODEL CMOSN2 NMOS
.MODEL NPN1 NPN
Q1 VN1 VIN– VN5 NPN1 AREA=2.560P
Q2 VN2 VIN+ VN5 NPN1 AREA=2.560P
M3 VN5 VN4 VSS VSS CMOSN1 W= 27.2U L= 5.2U
M4 VN4 VN4 VSS VSS CMOSN1 W= 13.2U L= 5.2U
M5 VDD GND VN4 vss CMOSN1 W= 5.2U L= 33.2U
M9 VDD VN2 vin+2 VDD CMOSP1 W= 150U L= 5.2U
M6 Vin+2 VN4 VSS VSS CMOSN1 W= 67.2U L= 5.2U
C1 vin+2 VN3 1.032P
M10 VN3 VSS VN2 VDD CMOSP1 W= 5.2U L= 5.2U
M7 VN1 VN1 VDD VDD CMOSP1 W= 30U L= 5.2U
M8 VN2 VN1 VDD VDD CMOSP1 W= 30U L= 5.2U
*OPAMP_2 CIRCUIT
Q12 VN12 VIN–2 VN52 NPN1 AREA=2.560P
Q22 VN22 VIN+2 VN52 NPN1 AREA=2.560P
M32 VN52 VN42 VSS VSS CMOSN1 W= 27.2U L= 5.2U
M42 VN42 VN42 VSS VSS CMOSN1 W= 13.2U L= 5.2U
M52 VDD GND VN42 vss CMOSN1 W= 5.2U L= 33.2U
M92 VDD VN2 VOUT2 VDD CMOSP1 W= 150U L= 5.2U
M62 VOUT2 VN42 VSS VSS CMOSN1 W= 67.2U L= 5.2U
C12 VOUT2 VN32 1.032P
M102 VN32 VSS VN22 VDD CMOSP1 W= 5.2U L= 5.2u
M72 VN12 VN12 VDD VDD CMOSP1 W= 30U L= 5.2U
M82 VN22 VN12 VDD VDD CMOSP1 W= 30U L= 5.2U
*interconnect bet op1 and op2, alpha=6.10 1k 10k
R1c vin–2 gnd 1k
R2c vin–2 vout2 8k
*feedback R
*R1 r1in Vin– 1k
*R2 VOut2 Vin– 100k
ckill vin+2 gnd 1.966p
```

```
ckill2 vout2 gnd 1.966p
*Input Stimulus, Options and Measurments
*.TRAN 1p 16n 0n
.AC DEC 20 10 1E+6
.plot v(VOut2)
.plot v(VDD)
.plot v(VSS)
.end
```

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APPENDIX E. DERIVATION OF IDEAL TRANSFER FUNCTION FOR 4TH–ORDER GIC BANDPASS FILTER

Derivation of Ideal Transfer Function for 4th Order GIC Bandpass Filter

(via Maple 8 software)

```
eq2 :=s^2+(1/(R*C*Qp))*s+(1/(R^2*C^2));
```

$$eq2 := s^2 + \frac{s}{RCQp} + \frac{1}{R^2C^2}$$

```
> eq3 :=eq2^2;
```

$$eq3 := \left(s^2 + \frac{s}{RCQp} + \frac{1}{R^2C^2}\right)^2$$

```
> eval(eq3);
>
```

$$\left(s^2 + \frac{s}{RCQp} + \frac{1}{R^2C^2}\right)^2$$

```
> expand(eq3);
```

$$s^4 + \frac{2s^3}{RCQp} + \frac{2s^2}{R^2C^2} + \frac{s^2}{R^2C^2Qp^2} + \frac{2s}{R^3C^3Qp} + \frac{1}{R^4C^4}$$

```
> den :=Qp^2*R^2*C^2;
```

$$den := Qp^2R^2C^2$$

```
> den1 :=den*eq3;
```

$$den1 := Qp^2R^2C^2\left(s^2 + \frac{s}{RCQp} + \frac{1}{R^2C^2}\right)^2$$

```
> expand(den1);
```

$$Qp^2R^2C^2s^4 + 2QpRCs^3 + 2Qp^2s^2 + s^2 + \frac{2Qps}{RC} + \frac{Qp^2}{R^2C^2}$$

```
>
```

Derivation of Non-Ideal Transfer Function

```
> num :=(C*G/Qp)*s+((G/Qp)*(G+s*C)*2*G)*(1/wt1)*s;
```

$$num := \frac{CGs}{Qp} + \frac{2G^2(G+sC)s}{Qp\,wt1}$$

```
> num1 :=expand(num);
```

$$num1 := \frac{CGs}{Qp} + \frac{2G^3s}{Qp\,wt1} + \frac{2G^2s^2C}{Qp\,wt1}$$

```
> a1 :=G*s*C*(G/Qp+s*C)+G^3;
```

$$a1 := Gs C\left(\frac{G}{Qp} + s C\right) + G^3$$

```
> a2:=2*G^2*(G+G/Qp+s*C)*(1/wt1)*s;
```

$$a2 := \frac{2 G^2 \left(G + \frac{G}{Qp} + s C\right) s}{wt1}$$

```
> a3:=s*C*(G+G/Qp+s*C)*2*G*(1/wt2)*s;
```

$$a3 := \frac{2 s^2 C \left(G + \frac{G}{Qp} + s C\right) G}{wt2}$$

```
> a4:=(G+s*C)*(G+G/Qp+s*C)*2*G*(1/(wt1*wt2))*s^2;
```

$$a4 := \frac{2 (G + s C) \left(G + \frac{G}{Qp} + s C\right) G s^2}{wt1\, wt2}$$

```
> den:=a1+a2+a3+a4;
```

$$den := Gs C\left(\frac{G}{Qp} + s C\right) + G^3 + \frac{2 G^2 \left(G + \frac{G}{Qp} + s C\right) s}{wt1} + \frac{2 s^2 C \left(G + \frac{G}{Qp} + s C\right) G}{wt2} + \frac{2 (G + s C) \left(G + \frac{G}{Qp} + s C\right) G s^2}{wt1\, wt2}$$

```
> den1:=expand(den);
```

$$den1 := \frac{G^2 s C}{Qp} + G s^2 C^2 + G^3 + \frac{2 G^3 s}{wt1} + \frac{2 G^3 s}{Qp\, wt1} + \frac{2 G^2 s^2 C}{wt1} + \frac{2 s^2 C G^2}{wt2} + \frac{2 s^2 C G^2}{wt2\, Qp} + \frac{2 s^3 C^2 G}{wt2} + \frac{2 G^3 s^2}{wt1\, wt2} + \frac{2 G^3 s^2}{wt1\, wt2\, Qp} + \frac{4 G^2 s^2 C}{wt1\, wt2} + \frac{2 G^2 s^2 C}{wt1\, wt2\, Qp} + \frac{2 G s^3 C^2}{wt1\, wt2}$$

```
> den2:=den1;
```

$$den2 := \frac{G^2 s C}{Qp} + G s^2 C^2 + G^3 + \frac{2 G^3 s}{wt1} + \frac{2 G^3 s}{Qp\, wt1} + \frac{2 G^2 s^2 C}{wt1} + \frac{2 s^2 C G^2}{wt2} + \frac{2 s^2 C G^2}{wt2\, Qp} + \frac{2 s^3 C^2 G}{wt2} + \frac{2 G^3 s^2}{wt1\, wt2} + \frac{2 G^3 s^2}{wt1\, wt2\, Qp} + \frac{4 G^2 s^2 C}{wt1\, wt2} + \frac{2 G^2 s^2 C}{wt1\, wt2\, Qp} + \frac{2 G s^3 C^2}{wt1\, wt2}$$

```
> denboth:=den1*den2;
```

$$denboth := \left(\frac{G^2 s C}{Qp} + G s^2 C^2 + G^3 + \frac{2 G^3 s}{wt1} + \frac{2 G^3 s}{Qp\, wt1} + \frac{2 G^2 s^2 C}{wt1} + \frac{2 s^2 C G^2}{wt2} + \frac{2 s^2 C G^2}{wt2\, Qp} + \frac{2 s^3 C^2 G}{wt2} + \frac{2 G^3 s^2}{wt1\, wt2} + \frac{2 G^3 s^2}{wt1\, wt2\, Qp} + \frac{4 G^2 s^2 C}{wt1\, wt2} + \frac{2 G^2 s^2 C}{wt1\, wt2\, Qp} + \frac{2 G s^3 C^2}{wt1\, wt2}\right)^2$$

```
> denboth1:=collect(denboth,s);
```

$$denboth1 := \frac{4G^2C^4s^8}{wt1^2\,wt2^2} + \frac{4\left(\frac{2C^2G}{wt2} + \frac{4G^2C}{wt1\,wt2} + \frac{2G^2C}{wt1\,wt2\,Qp}\right)GC^2s^7}{wt1\,wt2} + \left(\frac{4\left(GC^2 + \frac{2G^2C}{wt1} + \frac{2CG^2}{wt2} + \frac{2CG^2}{wt2\,Qp} + \frac{2G^3}{wt1\,wt2} + \frac{2G^3}{wt1\,wt2\,Qp}\right)GC^2}{wt1\,wt2} + \left(\frac{2C^2G}{wt2} + \frac{4G^2C}{wt1\,wt2} + \frac{2G^2C}{wt1\,wt2\,Qp}\right)^2\right)s^6 + \left(\frac{4\left(\frac{G^2C}{Qp} + \frac{2G^3}{wt1} + \frac{2G^3}{Qp\,wt1}\right)GC^2}{wt1\,wt2} + 2\left(GC^2 + \frac{2G^2C}{wt1} + \frac{2CG^2}{wt2} + \frac{2CG^2}{wt2\,Qp} + \frac{2G^3}{wt1\,wt2} + \frac{2G^3}{wt1\,wt2\,Qp}\right)\left(\frac{2C^2G}{wt2} + \frac{4G^2C}{wt1\,wt2} + \frac{2G^2C}{wt1\,wt2\,Qp}\right)\right)s^5 + \left(\frac{4G^4C^2}{wt1\,wt2} + 2\left(\frac{G^2C}{Qp} + \frac{2G^3}{wt1} + \frac{2G^3}{Qp\,wt1}\right)\left(\frac{2C^2G}{wt2} + \frac{4G^2C}{wt1\,wt2} + \frac{2G^2C}{wt1\,wt2\,Qp}\right) + \left(GC^2 + \frac{2G^2C}{wt1} + \frac{2CG^2}{wt2} + \frac{2CG^2}{wt2\,Qp} + \frac{2G^3}{wt1\,wt2} + \frac{2G^3}{wt1\,wt2\,Qp}\right)^2\right)s^4 + \left(2G^3\left(\frac{2C^2G}{wt2} + \frac{4G^2C}{wt1\,wt2} + \frac{2G^2C}{wt1\,wt2\,Qp}\right) + 2\left(\frac{G^2C}{Qp} + \frac{2G^3}{wt1} + \frac{2G^3}{Qp\,wt1}\right)\left(GC^2 + \frac{2G^2C}{wt1} + \frac{2CG^2}{wt2} + \frac{2CG^2}{wt2\,Qp} + \frac{2G^3}{wt1\,wt2} + \frac{2G^3}{wt1\,wt2\,Qp}\right)\right)s^3 + \left(2G^3\left(GC^2 + \frac{2G^2C}{wt1} + \frac{2CG^2}{wt2} + \frac{2CG^2}{wt2\,Qp} + \frac{2G^3}{wt1\,wt2} + \frac{2G^3}{wt1\,wt2\,Qp}\right) + \left(\frac{G^2C}{Qp} + \frac{2G^3}{wt1} + \frac{2G^3}{Qp\,wt1}\right)^2\right)s^2 + 2G^3\left(\frac{G^2C}{Qp} + \frac{2G^3}{wt1} + \frac{2G^3}{Qp\,wt1}\right)s + G^6$$

> num2 :=num1 ;

$$num2 := \frac{CGs}{Qp} + \frac{2G^3s}{Qp\,wt1} + \frac{2G^2s^2C}{Qp\,wt1}$$

> numboth :=num1*num2 ;

$$numboth := \left(\frac{CGs}{Qp} + \frac{2G^3s}{Qp\,wt1} + \frac{2G^2s^2C}{Qp\,wt1}\right)^2$$

> numboth1 :=collect(numboth,s) ;

$$numboth1 := \frac{4G^4C^2s^4}{Qp^2\,wt1^2} + \frac{4\left(\frac{CG}{Qp} + \frac{2G^3}{Qp\,wt1}\right)G^2Cs^3}{Qp\,wt1} + \left(\frac{CG}{Qp} + \frac{2G^3}{Qp\,wt1}\right)^2s^2$$

> Ts :=numboth1/denboth1 ;

$$Ts := \left(\frac{4G^4C^6s^4}{Qp^2\,wt1^2} + \frac{4\left(\frac{CG}{Qp} + \frac{2G^3}{Qp\,wt1}\right)G^2Cs^3}{Qp\,wt1} + \left(\frac{CG}{Qp} + \frac{2G^3}{Qp\,wt1}\right)^2 s^2 \right) \Big/ \left(\right.$$

$$\frac{4G^2C^4s^6}{wt1^2\,wt2^2} + \frac{4\left(\frac{2C^5G}{wt2} + \frac{4G^2C}{wt1\,wt2} + \frac{2G^2C}{wt1\,wt2\,Qp}\right)GC^2s^7}{wt1\,wt2} + \left(\right.$$

$$\frac{4\left(GC^3 + \frac{2G^2C}{wt1} + \frac{2CG^2}{wt2} + \frac{2CG^2}{wt2\,Qp} + \frac{2G^3}{wt1\,wt2} + \frac{2G^3}{wt1\,wt2\,Qp}\right)GC^4}{wt1\,wt2}$$

$$+\left(\frac{2C^2G}{wt2} + \frac{4G^2C}{wt1\,wt2} + \frac{2G^2C}{wt1\,wt2\,Qp}\right)^2\Bigg)s^6 + \left(\frac{4\left(\frac{G^2C}{Qp} + \frac{2G^3}{wt1} + \frac{2G^3}{Qp\,wt1}\right)GC^5}{wt1\,wt2} + 2 \right.$$

$$\left(GC^3 + \frac{2G^2C}{wt1} + \frac{2CG^2}{wt2} + \frac{2CG^2}{wt2\,Qp} + \frac{2G^3}{wt1\,wt2} + \frac{2G^3}{wt1\,wt2\,Qp}\right)$$

$$\left.\left(\frac{2C^2G}{wt2} + \frac{4G^2C}{wt1\,wt2} + \frac{2G^2C}{wt1\,wt2\,Qp}\right)\right)s^5 + \left(\frac{4G^4C^6}{wt1\,wt2}\right.$$

$$+2\left(\frac{G^2C}{Qp} + \frac{2G^3}{wt1} + \frac{2G^3}{Qp\,wt1}\right)\left(\frac{2C^3G}{wt2} + \frac{4G^2C}{wt1\,wt2} + \frac{2G^2C}{wt1\,wt2\,Qp}\right)$$

$$\left.+\left(GC^2 + \frac{2G^2C}{wt1} + \frac{2CG^2}{wt2} + \frac{2CG^2}{wt2\,Qp} + \frac{2G^3}{wt1\,wt2} + \frac{2G^3}{wt1\,wt2\,Qp}\right)^2\right)s^4 + \left(\right.$$

$$2G^3\left(\frac{2C^3G}{wt2} + \frac{4G^2C}{wt1\,wt2} + \frac{2G^2C}{wt1\,wt2\,Qp}\right) + 2\left(\frac{G^2C}{Qp} + \frac{2G^3}{wt1} + \frac{2G^3}{Qp\,wt1}\right)$$

$$\left.\left(GC^2 + \frac{2G^2C}{wt1} + \frac{2CG^2}{wt2} + \frac{2CG^2}{wt2\,Qp} + \frac{2G^3}{wt1\,wt2} + \frac{2G^3}{wt1\,wt2\,Qp}\right)\right)s^3 + \left(\right.$$

$$2G^3\left(GC^2 + \frac{2G^2C}{wt1} + \frac{2CG^2}{wt2} + \frac{2CG^2}{wt2\,Qp} + \frac{2G^3}{wt1\,wt2} + \frac{2G^3}{wt1\,wt2\,Qp}\right)$$

$$\left.+\left(\frac{G^2C}{Qp} + \frac{2G^3}{wt1} + \frac{2G^3}{Qp\,wt1}\right)^2\right)s^2 + 2G^3\left(\frac{G^2C}{Qp} + \frac{2G^3}{wt1} + \frac{2G^3}{Qp\,wt1}\right)s + G^6\Bigg)$$

=

APPENDIX F. IDEAL GIC FILTER MATLAB PROGRAM

```
%Cheong,Heng Wan
Syms s
R=1E3;
G=1/R;
Qp=5;
f=10^4;
wp=2*pi*f;
C=(R*wp)^–1;
s=tf('s');
Y1=G;
Y2=G;
Y3=s*C;
Y4=G;
Y5=0;
Y6=G;
Y7=G/Qp;
Y8=s*C;
T1=(Y1*Y4*Y5+Y3*Y7*(Y2+Y6)–Y3*Y5*Y8)/(Y1*Y4*(Y5+Y6)+Y2*Y3*(Y7+Y8));
T2=(Y1*Y4*Y5+Y1*Y5*Y8+Y2*Y3*Y7–
Y1*Y6*Y7)/(Y1*Y4*(Y5+Y6)+Y2*Y3*(Y7+Y8));
T3=(Y1*Y4*Y5+Y2*Y3*Y7)/(Y1*Y4*(Y5+Y6)+Y2*Y3*(Y7+Y8));
T1
[num1,den1]=tfdata(T1,'v')
figure(1)
step(T1)
figure(2)
bode(T1)
```

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APPENDIX G. NON– IDEAL GIC FILTER MATLAB PROGRAM

```
%Cheong,Heng Wan
%Non–ideal GIC opamp
clear all;
Syms s
%parameters
R=1e03;
G=1/R;
Qp=1;
f=20e03;
wp=2*pi*f
C=(R*wp)^–1;
s=tf('s');
wt1=1e07   %as given
wt2=1e07    %as given
A1=wt1/s;
A2=wt2/s;
Y1=G;
Y2=G;
Y3=s*C;
Y4=G;
Y5=0;
Y6=G;
Y7=G/Qp;
Y8=s*C;
T1= ((Y1*Y4*Y5+Y3*Y7*(Y2+Y6)–Y3*Y5*Y8) +
((Y7*(Y1+Y3)*(Y2+Y5+Y6))/A1)) / ( (Y2*Y3*(Y7+Y8)+Y1*Y4*(Y5+Y6)) +
(Y1*(Y4+Y7+Y8)*(Y2+Y5+Y6))/A1 + (Y3*(Y4+Y7+Y8)*(Y2+Y5+Y6))/A2 +
((Y1+Y3)*(Y4+Y7+Y8)*(Y2+Y5+Y6))/(A1*A2));
T2= ((Y2*Y3*Y7+Y1*Y5*(Y4+Y8)–Y1*Y6*Y7) + (Y5*(Y1+Y3)*(Y4+Y7+Y8))/A2 )
/ ((Y2*Y3*(Y7+Y8)+Y1*Y4*(Y5+Y6)) + (Y1*(Y4+Y7+Y8)*(Y2+Y5+Y6))/A1 +
(Y3*(Y4+Y7+Y8)*(Y2+Y5+Y6))/A2 +
((Y1+Y3)*(Y4+Y7+Y8)*(Y2+Y5+Y6))/(A1*A2));
[num1,den1]=tfdata(T1,'v');
%Full scale for Mag and phase
figure(1);
Bode(T1);
title('Non Ideal Band Pass – Full scale for Mag and Phase');
grid;
%Closeup scale for Mag and phase
figure(2);
Bode(T1);
title('Non Ideal Band Pass – Closeup scale for Mag and Phase');
```

```
axis([1.1e05,1.4e05,0,6.2]);
grid;
%Closeup scale for Mag only
[MAG1,PHASE1,W1] = BODE(T1);
MAGDB1= 20*log10(MAG1);
figure(3);
semilogx(W1,MAGDB1(:,:));
title('Non Ideal Band Pass – Closeup scale for Mag only');
xlabel('W in log scale');
ylabel('Mag in DB');
axis([1.1e05,1.4e05,0,6.2]);
grid;
MAGDBmax=max(MAGDB1)
[Y,I] = max(MAGDB1);
W1max = W1(I,1)
```

APPENDIX H. NON–IDEAL MATLAB PROGRAM (NON IDEAL CASE WITH 10% INCREASE IN R)

```
%effect of 10% R on Wo,Qp
%Cheong,Heng Wan
%Non–ideal GIC opamp
clear all;
clc;
Syms s
%parameters
R=(1e03)*1.1;
G=1/R;
Qp=10;
f=20e03;
wp=2*pi*f
C=(R*wp)^–1;
s=tf('s');
wt1=1e07 %as given
wt2=1e07   %as given
A1=wt1/s;
A2=wt2/s;
Y1=G;
Y2=G;
Y3=s*C;
Y4=G;
Y5=0;
Y6=G;
Y7=G/Qp;
Y8=s*C;
T1= ((Y1*Y4*Y5+Y3*Y7*(Y2+Y6)–Y3*Y5*Y8) +
((Y7*(Y1+Y3)*(Y2+Y5+Y6))/A1)) / ( (Y2*Y3*(Y7+Y8)+Y1*Y4*(Y5+Y6)) +
(Y1*(Y4+Y7+Y8)*(Y2+Y5+Y6))/A1 + (Y3*(Y4+Y7+Y8)*(Y2+Y5+Y6))/A2 +
((Y1+Y3)*(Y4+Y7+Y8)*(Y2+Y5+Y6))/(A1*A2));
T2= ((Y2*Y3*Y7+Y1*Y5*(Y4+Y8)–Y1*Y6*Y7) + (Y5*(Y1+Y3)*(Y4+Y7+Y8))/A2 )
/ ((Y2*Y3*(Y7+Y8)+Y1*Y4*(Y5+Y6)) + (Y1*(Y4+Y7+Y8)*(Y2+Y5+Y6))/A1 +
(Y3*(Y4+Y7+Y8)*(Y2+Y5+Y6))/A2 +
((Y1+Y3)*(Y4+Y7+Y8)*(Y2+Y5+Y6))/(A1*A2));
[num1,den1]=tfdata(T1,'v');
%Closeup scale for Mag and phase
figure(1);
Bode(T1);
title('Non Ideal Band Pass');
axis([1.1e05,1.4e05,0,6.2]);
grid;
```

```
%Closeup scale for Mag only
[MAG1,PHASE1,W1] = BODE(T1);
MAGDB1= 20*log10(MAG1);
MAGDBmax=max(MAGDB1)
[Y,I] = max(MAGDB1);
W1max = W1(I,1)
MAFDB_3db=MAGDBmax–3
%Non–ideal GIC opamp – reference
%parameters
Ra=1e03;
Ga=1/Ra;
Qpa=10;
fa=20e03;
wpa=2*pi*fa
Ca=(Ra*wpa)^–1;
s=tf('s');
wt1a=1e07   %as given
wt2a=1e07    %as given
A1a=wt1a/s;
A2a=wt2a/s;
Y1a=Ga;
Y2a=Ga;
Y3a=s*Ca;
Y4a=Ga;
Y5a=0;
Y6a=Ga;
Y7a=Ga/Qpa;
Y8a=s*Ca;
T1a= ((Y1a*Y4a*Y5a+Y3a*Y7a*(Y2a+Y6a)–Y3a*Y5a*Y8a) +
((Y7a*(Y1a+Y3a)*(Y2a+Y5a+Y6a))/A1a)) / (
(Y2a*Y3a*(Y7a+Y8a)+Y1a*Y4a*(Y5a+Y6a)) +
(Y1a*(Y4a+Y7a+Y8a)*(Y2a+Y5a+Y6a))/A1a +
(Y3a*(Y4a+Y7a+Y8a)*(Y2a+Y5a+Y6a))/A2a +
((Y1a+Y3a)*(Y4a+Y7a+Y8a)*(Y2a+Y5a+Y6a))/(A1a*A2a));
T2a= ((Y2a*Y3a*Y7a+Y1a*Y5a*(Y4a+Y8a)–Y1a*Y6a*Y7a) +
(Y5a*(Y1a+Y3a)*(Y4a+Y7a+Y8a))/A2a ) / (
(Y2a*Y3a*(Y7a+Y8a)+Y1a*Y4a*(Y5a+Y6a)) +
(Y1a*(Y4a+Y7a+Y8a)*(Y2a+Y5a+Y6a))/A1a +
(Y3a*(Y4a+Y7a+Y8a)*(Y2a+Y5a+Y6a))/A2a +
((Y1a+Y3a)*(Y4a+Y7a+Y8a)*(Y2a+Y5a+Y6a))/(A1a*A2a));
[num1a,den1a]=tfdata(T1a,'v');
%Closeup scale for Mag and phase
figure(2);
Bode(T1a,T1);
title('Non Ideal Band Pass – 10% variable in R');
```

```
axis([1.1e05,1.4e05,0,6.2]);
grid;
%Closeup scale for Mag only
[MAG1a,PHASE1a,W1a] = BODE(T1a);
MAGDB1a= 20*log10(MAG1a);
MAGDBmaxa=max(MAGDB1a)
[Ya,Ia] = max(MAGDB1a);
W1maxa = W1a(Ia,1)
MAFDB_3dba=MAGDBmaxa–3
%Differences
Diff_in_db = abs(MAGDBmaxa–MAGDBmax)
Diff_in_db_percent = abs(((MAGDBmaxa–MAGDBmax)/MAGDBmaxa)*100 )
Diff_in_w = abs(W1maxa–W1max)
Diff_in_w_percent = abs(((W1maxa–W1max)/W1maxa)*100)
```

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APPENDIX I. NON–IDEAL MATLAB PROGRAM (NON IDEAL CASE WITH 10% INCREASE IN C)

```
%effect of 10% C on Wo,Qp
%Cheong,Heng Wan
%Non–ideal GIC opamp
clear all;
clc;
Syms s
%parameters
R=(1e03);
G=1/R;
Qp=10;
f=20e03;
wp=2*pi*f
C=((R*wp)^–1)*1.1;
s=tf('s');
wt1=1e07   %as given
wt2=1e07   %as given
A1=wt1/s;
A2=wt2/s;
Y1=G;
Y2=G;
Y3=s*C;
Y4=G;
Y5=0;
Y6=G;
Y7=G/Qp;
Y8=s*C;
T1= ((Y1*Y4*Y5+Y3*Y7*(Y2+Y6)–Y3*Y5*Y8) +
((Y7*(Y1+Y3)*(Y2+Y5+Y6))/A1)) / ( (Y2*Y3*(Y7+Y8)+Y1*Y4*(Y5+Y6)) +
(Y1*(Y4+Y7+Y8)*(Y2+Y5+Y6))/A1 + (Y3*(Y4+Y7+Y8)*(Y2+Y5+Y6))/A2 +
((Y1+Y3)*(Y4+Y7+Y8)*(Y2+Y5+Y6))/(A1*A2));
T2= ((Y2*Y3*Y7+Y1*Y5*(Y4+Y8)–Y1*Y6*Y7) + (Y5*(Y1+Y3)*(Y4+Y7+Y8))/A2 )
/ ((Y2*Y3*(Y7+Y8)+Y1*Y4*(Y5+Y6)) + (Y1*(Y4+Y7+Y8)*(Y2+Y5+Y6))/A1 +
(Y3*(Y4+Y7+Y8)*(Y2+Y5+Y6))/A2 +
((Y1+Y3)*(Y4+Y7+Y8)*(Y2+Y5+Y6))/(A1*A2));
[num1,den1]=tfdata(T1,'v');
%Closeup scale for Mag and phase
figure(1);
Bode(T1); hold on;
title('Non Ideal Band Pass');
axis([0.95e05,1.4e05,–1,6.2]);
grid;
```

```
%Closeup scale for Mag only
[MAG1,PHASE1,W1] = BODE(T1);
MAGDB1= 20*log10(MAG1);
MAGDBmax=max(MAGDB1)
[Y,I] = max(MAGDB1);
W1max = W1(I,1)
MAFDB_3db=MAGDBmax–3
%Non–ideal GIC opamp – reference
%parameters
Ra=1e03;
Ga=1/Ra;
Qpa=10;
fa=20e03;
wpa=2*pi*fa
Ca=(Ra*wpa)^–1;
s=tf('s');
wt1a=1e07   %as given
wt2a=1e07    %as given
A1a=wt1a/s;
A2a=wt2a/s;
Y1a=Ga;
Y2a=Ga;
Y3a=s*Ca;
Y4a=Ga;
Y5a=0;
Y6a=Ga;
Y7a=Ga/Qpa;
Y8a=s*Ca;
T1a= ((Y1a*Y4a*Y5a+Y3a*Y7a*(Y2a+Y6a)–Y3a*Y5a*Y8a) +
((Y7a*(Y1a+Y3a)*(Y2a+Y5a+Y6a))/A1a)) / (
(Y2a*Y3a*(Y7a+Y8a)+Y1a*Y4a*(Y5a+Y6a)) +
(Y1a*(Y4a+Y7a+Y8a)*(Y2a+Y5a+Y6a))/A1a +
(Y3a*(Y4a+Y7a+Y8a)*(Y2a+Y5a+Y6a))/A2a +
((Y1a+Y3a)*(Y4a+Y7a+Y8a)*(Y2a+Y5a+Y6a))/(A1a*A2a));
T2a= ((Y2a*Y3a*Y7a+Y1a*Y5a*(Y4a+Y8a)–Y1a*Y6a*Y7a) +
(Y5a*(Y1a+Y3a)*(Y4a+Y7a+Y8a))/A2a ) / (
(Y2a*Y3a*(Y7a+Y8a)+Y1a*Y4a*(Y5a+Y6a)) +
(Y1a*(Y4a+Y7a+Y8a)*(Y2a+Y5a+Y6a))/A1a +
(Y3a*(Y4a+Y7a+Y8a)*(Y2a+Y5a+Y6a))/A2a +
((Y1a+Y3a)*(Y4a+Y7a+Y8a)*(Y2a+Y5a+Y6a))/(A1a*A2a));
[num1a,den1a]=tfdata(T1a,'v');
%Closeup scale for Mag and phase
figure(2);
Bode(T1a,T1);
title('Non Ideal Band Pass – 10% variable in C');
```

```
axis([0.95e05,1.4e05,–1,6.2]);
grid;
%Closeup scale for Mag only
[MAG1a,PHASE1a,W1a] = BODE(T1a);
MAGDB1a= 20*log10(MAG1a);
MAGDBmaxa=max(MAGDB1a)
[Ya,Ia] = max(MAGDB1a);
W1maxa = W1a(Ia,1)
MAFDB_3dba=MAGDBmaxa–3
%Differences
Diff_in_db = abs(MAGDBmaxa–MAGDBmax)
Diff_in_db_percent = abs(((MAGDBmaxa–MAGDBmax)/MAGDBmaxa)*100 )
Diff_in_w = abs(W1maxa–W1max)
Diff_in_w_percent = abs(((W1maxa–W1max)/W1maxa)*100)
```

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APPENDIX J. NON–IDEAL MATLAB PROGRAM (NON–IDEAL CASE WITH 10% INCREASE IN R AND 50% DECREASE OF GBWP).

```
% effect of 10% R on Wo,Qp – 50% of GBWP
%Cheong,Heng Wan
%Non–ideal GIC opamp
clear all;
clc;
Syms s
%parameters
R=(1e03)*1.1;
G=1/R;
Qp=10;
f=20e03;
wp=2*pi*f
C=(R*wp)^–1;
s=tf('s');
wt1=(1e07)*0.5 %as given
wt2=(1e07)*0.5 %as given
A1=wt1/s;
A2=wt2/s;
Y1=G;
Y2=G;
Y3=s*C;
Y4=G;
Y5=0;
Y6=G;
Y7=G/Qp;
Y8=s*C;
T1= ((Y1*Y4*Y5+Y3*Y7*(Y2+Y6)–Y3*Y5*Y8) +
((Y7*(Y1+Y3)*(Y2+Y5+Y6))/A1)) / ( (Y2*Y3*(Y7+Y8)+Y1*Y4*(Y5+Y6)) +
(Y1*(Y4+Y7+Y8)*(Y2+Y5+Y6))/A1 + (Y3*(Y4+Y7+Y8)*(Y2+Y5+Y6))/A2 +
((Y1+Y3)*(Y4+Y7+Y8)*(Y2+Y5+Y6))/(A1*A2));
T2= ((Y2*Y3*Y7+Y1*Y5*(Y4+Y8)–Y1*Y6*Y7) + (Y5*(Y1+Y3)*(Y4+Y7+Y8))/A2 )
/ ((Y2*Y3*(Y7+Y8)+Y1*Y4*(Y5+Y6)) + (Y1*(Y4+Y7+Y8)*(Y2+Y5+Y6))/A1 +
(Y3*(Y4+Y7+Y8)*(Y2+Y5+Y6))/A2 +
((Y1+Y3)*(Y4+Y7+Y8)*(Y2+Y5+Y6))/(A1*A2));
[num1,den1]=tfdata(T1,'v');
%Closeup scale for Mag and phase
figure(1);
Bode(T1);
title('Non Ideal Band Pass');
axis([1.1e05,1.4e05,0,6.2]);
```

```
grid;
%Closeup scale for Mag only
[MAG1,PHASE1,W1] = BODE(T1);
MAGDB1= 20*log10(MAG1);
MAGDBmax=max(MAGDB1)
[Y,I] = max(MAGDB1);
W1max = W1(I,1)
MAFDB_3db=MAGDBmax–3
%Non–ideal GIC opamp – reference
%parameters
Ra=1e03;
Ga=1/Ra;
Qpa=10;
fa=20e03;
wpa=2*pi*fa
Ca=(Ra*wpa)^–1;
s=tf('s');
wt1a=(1e07)   %as given
wt2a=(1e07)   %as given
A1a=wt1a/s;
A2a=wt2a/s;
Y1a=Ga;
Y2a=Ga;
Y3a=s*Ca;
Y4a=Ga;
Y5a=0;
Y6a=Ga;
Y7a=Ga/Qpa;
Y8a=s*Ca;
T1a= ((Y1a*Y4a*Y5a+Y3a*Y7a*(Y2a+Y6a)–Y3a*Y5a*Y8a) +
((Y7a*(Y1a+Y3a)*(Y2a+Y5a+Y6a))/A1a)) / (
(Y2a*Y3a*(Y7a+Y8a)+Y1a*Y4a*(Y5a+Y6a)) +
(Y1a*(Y4a+Y7a+Y8a)*(Y2a+Y5a+Y6a))/A1a +
(Y3a*(Y4a+Y7a+Y8a)*(Y2a+Y5a+Y6a))/A2a +
((Y1a+Y3a)*(Y4a+Y7a+Y8a)*(Y2a+Y5a+Y6a))/(A1a*A2a));
T2a= ((Y2a*Y3a*Y7a+Y1a*Y5a*(Y4a+Y8a)–Y1a*Y6a*Y7a) +
(Y5a*(Y1a+Y3a)*(Y4a+Y7a+Y8a))/A2a ) / (
(Y2a*Y3a*(Y7a+Y8a)+Y1a*Y4a*(Y5a+Y6a)) +
(Y1a*(Y4a+Y7a+Y8a)*(Y2a+Y5a+Y6a))/A1a +
(Y3a*(Y4a+Y7a+Y8a)*(Y2a+Y5a+Y6a))/A2a +
((Y1a+Y3a)*(Y4a+Y7a+Y8a)*(Y2a+Y5a+Y6a))/(A1a*A2a));
[num1a,den1a]=tfdata(T1a,'v');
%Closeup scale for Mag and phase
figure(2);
Bode(T1a,T1);
```

```
title('Non Ideal Band Pass – 10% variable in R & 50% of GBWP');
axis([1.1e05,1.4e05,0,6.2]);
grid;
%Closeup scale for Mag only
[MAG1a,PHASE1a,W1a] = BODE(T1a);
MAGDB1a= 20*log10(MAG1a);
MAGDBmaxa=max(MAGDB1a)
[Ya,Ia] = max(MAGDB1a);
W1maxa = W1a(Ia,1)
MAFDB_3dba=MAGDBmaxa–3
%Differences
Diff_in_db = abs(MAGDBmaxa–MAGDBmax)
Diff_in_db_percent = abs(((MAGDBmaxa–MAGDBmax)/MAGDBmaxa)*100 )
Diff_in_w = abs(W1maxa–W1max)
Diff_in_w_percent = abs(((W1maxa–W1max)/W1maxa)*100)
```

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APPENDIX K. NON–IDEAL MATLAB PROGRAM (NON–IDEAL CASE WITH 10% INCREASE IN C AND 50% DECREASE OF GBWP).

```
% effect of 10% C on Wo,Qp & 50% of GBWP
%Cheong,Heng Wan
%Non–ideal GIC opamp
clear all;
clc;
Syms s
%parameters
R=(1e03);
G=1/R;
Qp=10;
f=20e03;
wp=2*pi*f
C=((R*wp)^–1)*1.1;
s=tf('s');
wt1=(1e07)*0.5   %as given
wt2=(1e07)*0.5   %as given
A1=wt1/s;
A2=wt2/s;
Y1=G;
Y2=G;
Y3=s*C;
Y4=G;
Y5=0;
Y6=G;
Y7=G/Qp;
Y8=s*C;
T1= ((Y1*Y4*Y5+Y3*Y7*(Y2+Y6)–Y3*Y5*Y8) +
((Y7*(Y1+Y3)*(Y2+Y5+Y6))/A1)) / ( (Y2*Y3*(Y7+Y8)+Y1*Y4*(Y5+Y6)) +
(Y1*(Y4+Y7+Y8)*(Y2+Y5+Y6))/A1 + (Y3*(Y4+Y7+Y8)*(Y2+Y5+Y6))/A2 +
((Y1+Y3)*(Y4+Y7+Y8)*(Y2+Y5+Y6))/(A1*A2));
T2= ((Y2*Y3*Y7+Y1*Y5*(Y4+Y8)–Y1*Y6*Y7) + (Y5*(Y1+Y3)*(Y4+Y7+Y8))/A2 )
/ ((Y2*Y3*(Y7+Y8)+Y1*Y4*(Y5+Y6)) + (Y1*(Y4+Y7+Y8)*(Y2+Y5+Y6))/A1 +
(Y3*(Y4+Y7+Y8)*(Y2+Y5+Y6))/A2 +
((Y1+Y3)*(Y4+Y7+Y8)*(Y2+Y5+Y6))/(A1*A2));
[num1,den1]=tfdata(T1,'v');
%Closeup scale for Mag and phase
figure(1);
Bode(T1); hold on;
title('Non Ideal Band Pass');
axis([0.95e05,1.4e05,–1,6.2]);
```

```
grid;
%Closeup scale for Mag only
[MAG1,PHASE1,W1] = BODE(T1);
MAGDB1= 20*log10(MAG1);
MAGDBmax=max(MAGDB1)
[Y,I] = max(MAGDB1);
W1max = W1(I,1)
MAFDB_3db=MAGDBmax–3
%Non–ideal GIC opamp – reference
%parameters
Ra=1e03;
Ga=1/Ra;
Qpa=10;
fa=20e03;
wpa=2*pi*fa
Ca=(Ra*wpa)^–1;
s=tf('s');
wt1a=1e07   %as given
wt2a=1e07    %as given
A1a=wt1a/s;
A2a=wt2a/s;
Y1a=Ga;
Y2a=Ga;
Y3a=s*Ca;
Y4a=Ga;
Y5a=0;
Y6a=Ga;
Y7a=Ga/Qpa;
Y8a=s*Ca;
T1a= ((Y1a*Y4a*Y5a+Y3a*Y7a*(Y2a+Y6a)–Y3a*Y5a*Y8a) +
((Y7a*(Y1a+Y3a)*(Y2a+Y5a+Y6a))/A1a)) / (
(Y2a*Y3a*(Y7a+Y8a)+Y1a*Y4a*(Y5a+Y6a)) +
(Y1a*(Y4a+Y7a+Y8a)*(Y2a+Y5a+Y6a))/A1a +
(Y3a*(Y4a+Y7a+Y8a)*(Y2a+Y5a+Y6a))/A2a +
((Y1a+Y3a)*(Y4a+Y7a+Y8a)*(Y2a+Y5a+Y6a))/(A1a*A2a));
T2a= ((Y2a*Y3a*Y7a+Y1a*Y5a*(Y4a+Y8a)–Y1a*Y6a*Y7a) +
(Y5a*(Y1a+Y3a)*(Y4a+Y7a+Y8a))/A2a ) / (
(Y2a*Y3a*(Y7a+Y8a)+Y1a*Y4a*(Y5a+Y6a)) +
(Y1a*(Y4a+Y7a+Y8a)*(Y2a+Y5a+Y6a))/A1a +
(Y3a*(Y4a+Y7a+Y8a)*(Y2a+Y5a+Y6a))/A2a +
((Y1a+Y3a)*(Y4a+Y7a+Y8a)*(Y2a+Y5a+Y6a))/(A1a*A2a));
[num1a,den1a]=tfdata(T1a,'v');
%Closeup scale for Mag and phase
figure(2);
Bode(T1a,T1);
```

```
title('Non Ideal Band Pass – 10% variable in C & 50% of GBWP');
axis([0.95e05,1.4e05,–1,6.2]);
grid;
%Closeup scale for Mag only
[MAG1a,PHASE1a,W1a] = BODE(T1a);
MAGDB1a= 20*log10(MAG1a);
MAGDBmaxa=max(MAGDB1a)
[Ya,Ia] = max(MAGDB1a);
W1maxa = W1a(Ia,1)
MAFDB_3dba=MAGDBmaxa–3
%Differences
Diff_in_db = abs(MAGDBmaxa–MAGDBmax)
Diff_in_db_percent = abs(((MAGDBmaxa–MAGDBmax)/MAGDBmaxa)*100 )
Diff_in_w = abs(W1maxa–W1max)
Diff_in_w_percent = abs(((W1maxa–W1max)/W1maxa)*100)
```

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