NAVAL POSTGRADUATE SCHOOL
Monterey, California

THESIS

A MICROPROCESSOR MANAGED SHIPBOARD

TANK LEVEL INDICATOR SYSTEM

by

Joseph C. Rieth, Jr.

September 1980

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well as roll and pitch movement, of the vessel. The stored program may be installed in programmable read only memory by a stand alone program transfer device (PTD) which was designed to facilitate use of a microprocessor development system, such as the Tektronics 8002A with high level language compiler, as a software design tool, thus extending the capabilities of the system in use at the Naval Postgraduate School. The TLI system may easily be expanded to service the full array of tanks in a typical vessel and to provide a variety of functions not implemented in the prototype.

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A Microprocessor Managed Shipboard Tank Level Indicator System

by

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Submitted in partial fulfillment of the
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ABSTRACT

A solid state, microprocessor managed, tank level indicator (TLI) system for shipboard applications is presented. The system derives tank level information from a capacitance meter whose output is processed by an INTEL 8085 based microcomputer. The system's stored program provides time averaging and interpolation functions which compensate for non uniform tank profiles, as well as roll and pitch movement, of the vessel. The stored program may be installed in programmable read only memory by a stand alone program transfer device (PTD) which was designed to facilitate use of a microprocessor development system, such as the Tektronics 8002A with high level language compiler, as a software design tool, thus extending the capabilities of the system in use at the Naval Postgraduate School. The TLI system may easily be expanded to service the full array of tanks in a typical vessel and to provide a variety of functions not implemented in the prototype.

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I. INTRODUCTION

Seagoing vessels, both civilian and military, require a continuous and accurate inventory of liquid levels in their water, fuel and lubricant storage tanks. Naval vessels, in particular, are ever more stringently constrained to manage their liquid resources with utmost accuracy by increasingly heavy economic and ecologic pressures. Throughout the active life of a ship each of her tanks must be monitored to preclude emergency conditions such as might occur when a fuel oil service tank either overflows while being filled or is drained completely while serving the ship's propulsion system. In addition, the routine requirements for inventory management and vessel stability make it desirable to have an efficient, reliable system for monitoring tank content levels.

Although a wide variety of methods exists for monitoring liquid tank levels aboard ship, three of the most common serve to illustrate the current norm in vessels built over the last twenty years; the sounding tape, external sight glasses or petcocks and variable capacitance probes serving a centralized or local array of electromechanical indicators. The ship using sounding tapes typically stations the operators at each tank. The level reports may be synchronized or left to the judgement of the individual operators. Communication among operators and the central

station during liquid replenishment, transfer or offload operations is commonly by sound powered telephone backed up by electrical intercom systems and messengers. The central operating station thus equipped may concurrently monitor both the remote sensing indicators and the reports of sounding tape operators at each tank site. In calm weather alongside a pier this system serves reasonably well to provide timely and accurate information. However, the control station is very much dependent upon the motivation and skill of each of the several operators. When the basic situation described above is complicated by large, erratic ship movements caused by non ideal weather conditions most often encountered while underway, the quality of system performance may be expected to rapidly deteriorate. Even the electromechanical system, although not prone to fatigue as are the human sounding tape operators, nevertheless calls upon some external operation to provide the time averaging process necessary to obtain an accurate reading of tank level as the vessel rolls and pitches about its quiescent point. Accurate interpretation of sounding tubes and sight glasses is similarly affected. Under even optimum conditions these systems possess an inherently long response time during which an alarm condition must first be recognized and then transmitted to the control station. When modern methods of underway replenishment are considered, it becomes apparent that long system

response times are completely incompatible with high rates of liquid transfer. In addition to the weaknesses of such human operator controlled systems in the real time environment, maintenance requirements also serve to severely limit overall system performance. With mechanical components such as meters, gauges and valves, periodic disassembly of system components is required for repair or replacement. Recalibration is normally required after each such maintenance routine, possibly under conditions not realistically attainable aboard ship. These common systems very rarely include anything more than a rudimentary fault alarm and may not be easily adapted to provide such capability. A serious consideration in modern warships is also pertinent to tank level indicator systems, namely size and weight requirements, not only of the functioning system, but additionally of system replacement parts and support materials.

The solid state, microprocessor managed system provides an alternative to the systems discussed above. Its advantages include inherently low bulk and weight, relatively low cost over the life cycle of the system and improved reliability. Electronic systems have no moving parts to wear out and do not require periodic adjustment and calibration. Faulty or damaged component modules may be easily replaced by technicians with minimal special training. The system may be designed to be sensor independent such that either a new form of variable capacitance probe may

be used or any of the currently installed, proven sensor systems provided with appropriate level translation devices to scale the transmitted signal. The microprocessor managed tank level indicator system is highly expandable, in terms of both facility physical size and output functions. Incremental improvements to the stored program may provide alarm functions, relay activated mechanical system control under electronic supervision, bookkeeping functions such as inventory, consumption rates, real time projections through software and memory expansion and the ability to function effectively independent of the type of liquid contained in each tank. The minimum tank level indicator (TLI) system proposed is easily capable of monitoring sixty four tanks at relatively low additional hardware cost per tank by control signal decoding applied to enable individual capacitance meter tank sensors. The low initial setup cost of such a system accrues from minimal operator training required to operate an automated system and from straightforward installation procedures using tank level documentation now existent in every operating vessel.

In summary, the microprocessor managed TLI system provides:

1. The potential for faster response.
2. Greater resolution.
3. Reduced bulk, power and labor requirements.

4. Enhanced administrative utility.

5. Significant expandability.

Developmental effort for the proposed system described herein was concentrated in the following distinct areas:

1. Problem Definition.

2. Component Selection Considerations.

3. System Hardware Development.

4. Data Processing Algorithm Composition.

Discussion of the specification, design and operation of each hardware subsystem precedes examination of the data processing algorithms because subsystem interactions govern the operations for which the software was later developed.

II. MODELING AND CONSTRAINTS

In recognition of the many configurations and capacities of tank systems encountered, it was decided to select for modeling purposes a representative, mid-size ship type. The ubiquitous post World War II destroyer or frigate was chosen to provide a set of typical specifications whose dimensions may be scaled up or down to adapt to yacht or aircraft carrier without significant effect on system architecture, save the number of sensors employed.

A. VESSEL ARCHITECTURE

Characteristics of the model chosen which are pertinent to architecture of the TLI system include:

1. Number of tanks.
2. Tank capacities.
3. Level to gallons conversion tables existing at present.
4. Tank vertical dimensions.
5. Tank separation from the central monitoring site.
6. Tank internal geometry.

Typically a system of twenty five to forty tanks is monitored, these tanks having capacities ranging from five to twenty five thousand gallons. Tank depths of twenty feet or less exist in the model ship type and separation of the most distant tank from a central station of less than

four hundred feet is the rule. Each tank possesses a geometry and array of internal interferences unique to itself. For each tank a table for conversion from depth of fluid to gallons contained is assumed to exist.

Based upon these assumed constraints a minimum system is proposed, limited to a size sufficient for demonstration of the concept but easily expanded in physical and functional scale to dimensions consistent with practical installations.

During the course of development of the tank level indicator system, several approaches to the problem of fluid level sensing were considered. These included examination of alternative sensor locations within the tank and examination of sensor types in an attempt to avoid use of a sensor dependent upon immersion in the fluid for its operation.

The final choice of sensor arrangement was intended to enhance system flexibility by permitting optional use of existing sensors without imposing dependence on their internal parameters onto the remainder of the system.

B. SENSOR LOCATION

Assuming a sonic sensor of unspecified type rather than the variable capacitance sensor proposed below, five alternative locations were considered:

1. Tethered, two module system with the sensor loosely tethered to a vertical slide within the tank and riding upon the liquid surface. The sensor transmits level

information to a receiver module attached to the tank top from whence data is sent to the TLI microcomputer.

2. Single module attached to the tank top monitoring distance to the fluid surface in a fixed direction.

3. Free floating, two module system in which the floating module senses distance to the tank bottom and transmits this information to a receiving unit mounted on the tank top.

4. Anchored module residing at the lowest point of the tank sensing distance to the fluid surface in a vertical direction with respect to the vessel's vertical axis.

5. Single module sensor located on the tank top using an omnidirectional transceiver to sense unfilled volume within the tank.

Each of the above schemes was rejected in turn on two major points. The nonlinearities implied by sensor movement, the effect of vapor pressure variations on the transmission of information from the remote sensor to the receiver, and the appreciable sensitivity to noise of such systems seem to make calibration of such a system impractical. Second, these sensor schemes require that the system be applied to tanks whose contents are relatively benign or that the devices subject to contact with the fluid be packaged in such fashion as to resist attack by fluids such as distillate fuels, yet still be capable of emitting data signals to the tank and the receiving set.

Such device packages are neither readily available commercially nor easily custom fabricated.

C. SENSOR TYPE

Three sensor types were considered:

1. Infrasonic systems.
2. Ultrasonic systems.
3. Immersed probe systems.

1. Infrasonic Concept

The use of an infrasonic system might employ measurement of the resonance variation of the vacant portion of the tank either directly or by spectral analysis of the return from a broadband pulse introduced into the tank or by the intensity of the returned signal. The system needed for implementation would necessarily be complex and thus present no cost, accuracy or maintenance benefit over systems currently in use. In addition, the introduction of low frequency noise into the hull structure of naval vessels is highly undesirable from a tactical standpoint.

2. Ultrasonic Concept

An ultrasonic system would avoid introducing low frequency noise into the hull structure and might be used to observe the resonant point of a tank and thus derive the proportion of total capacity occupied by fluid, or it might operate in sonar fashion by transmitting pulses and measuring the delay until the reflected pulse arrives. This

approach appeared to offer significant promise. The LM1812 monolithic ultrasonic transceiver is an inexpensive realization of the circuitry required for a single module system mounted on the tank top. It is capable of air operation at forty kilohertz with sufficient accuracy to provide resolution to the nearest inch of distance to the fluid surface. If mounted over the deepest section of the tank, the transducer, with proper shielding, would sense the time delay of a pulse sent straight downward and returned upward when reflected at the air/fluid interface. The strongest advantage of this concept is that it is entirely independent of the properties of the fluid such as conductivity and density. The flaw most apparent in this approach is that the transducer in a system aboard a moving vessel is subject to repeated immersion in the tank contents as the vessel movement sloshes the liquid. The requirement to protect the transducer from chemical attack while leaving it transparent to ultrasonic signals is not remediable with readily available transducers revealed. In addition, although the approach is well within the capabilities of the LM1812, transducer risetime and threshold characteristics introduce nonlinearities of their own and might require that the pulsewidth of the LM1812 be extended to several cycles to give the transducer time to rise above threshold. While apparently feasible, the limited resources and time available for

system development caused this approach to be rejected in favor of a more expedient and less complex sensor system.

3. Immersed Probe Concept

An immersed probe may generate an output voltage or current proportional to fluid level indirectly by sensing head pressure over the probe or directly by sensing the proportion of the probe which is actually immersed. This approach was selected for the prototype because of its simplicity and its similarity to existent installations. A specific example of this type of sensor is described below.

III. THE SYSTEM NUCLEUS

Practical considerations of component availability, software support and expandability governed the choice of microprocessor. The Intel SKD-85 system design kit was available and offered several attractive features. Built around the 8085A CPU, the system provides sufficient circuitry to permit straightforward interface with a console and with tank sensor circuitry. The monitor program resident in read only memory enables the user to concentrate on design of software pertinent to the application without the additional labor of providing system housekeeping functions. A significant advantage of the 8085A CPU is that it operates on a superset of popular 8080 instructions, thereby affording access to a wide range of literature and software support.

A. SYSTEM COMPONENT SELECTION CONSIDERATIONS

The following MCS-85 evolutionary improvements over the MCS-80 system support its application to moderate scale controller oriented systems which would formerly have been designed around MCS-80 components:

1. Single voltage operation.
2. Reduced component count.
3. Improved interrupt management.
4. Simplification of memory mapped input/output.
5. Instruction cycle time reduced from 2uSec to 1.3uSec .

These features enhance the design of the tank level indicator system by providing a flexible set of programmable ports which function either as data ports or as buffered control signal generators serving the data input of counters, system control and interrupt prioritizing functions, and the system clock, thus reducing overall system component count and complexity.

Unfortunately, the advantage of single power supply operation was largely negated by the requirements of data input system components and of the RS-232C interface.

The SDK-85 provides sufficient inherent expandability to serve as a nucleus for systems much larger than that described herein.

B. LSI DEVICE SALIENT FEATURES

The MCS-85 microcomputer system contained in the SDK-85 is a minimum system composed of central processor unit, read only memory, random access memory, keyboard display controller, address decoder, scan decoder, keypad and seven segment, six digit display with associated driver circuits. Detailed information concerning the architecture and operation of each of the MCS-85 large scale integrated (LSI) circuits may be obtained from Ref. 3 and from the appropriate manufacturer's user manuals. Only those features important to system conceptual operation are emphasized here.

1. 8085A CPU

The 8085A is a single chip, forty pin, eight bit N-channel microprocessor featuring software compatibility with the 8080A while providing an improved system of four vectored interrupts, on-chip clock generator and system controller, serial input and output ports and direct addressing capability to sixty four thousand bytes of memory. The system uses a multiplexed address and data bus which is facilitated by latches resident on each memory chip. The clock operates at a nominal three megahertz which permits freedom from execution time constraints on program design when operated in the relatively slow TLI environment.

2. 8355 Read Only Memory

The 8355 read only memory is arranged in two thousand forty eight words of eight bits each. In addition to the on-chip latches serving the address/data bus there are sixteen programmable input/output lines. The 8355 serving the SDK-85 is mask programmed with a monitor program which provides utility functions employing either the on-board keypad and display or teletype or, with level translation circuitry provided by the user, an RS-232C compatible console. The monitor program routines are user accessible and may be addressed by portions of the TLI program for input/output functions.

3. 8755A Erasable Programmable Read Only Memory

The 8755A presents itself to the remainder of the system exactly as does the 8355. The difference is that the 8755A is an ultraviolet light erasable and electrically reprogrammable device used in the minimal system to contain user provided stored program functions utilized in this case by the TLI system in the form of lookup tables and data manipulation algorithms.

4. 8155 Random Access Memory

The 8155 is a static MOS random access memory organized in two hundred fifty six words of eight bits each. The 8155 RAM communicates with the rest of the bussed system through on-chip latches and in addition provides two programmable input/output ports of eight bits each plus another port six bits wide which may be employed as a source of control signals for the other two ports or as an additional port for general purpose use. There is a fourteen bit down counter on-chip which serves as a timer. In the minimal system the single 8155 timer is used by the monitor routine in the single step mode and is not user accessible. However with the addition of a second 8155, five hundred twelve words of random access memory and a second, user accessible timer become available.

5. 8279 Programmable Keyboard/Display Interface

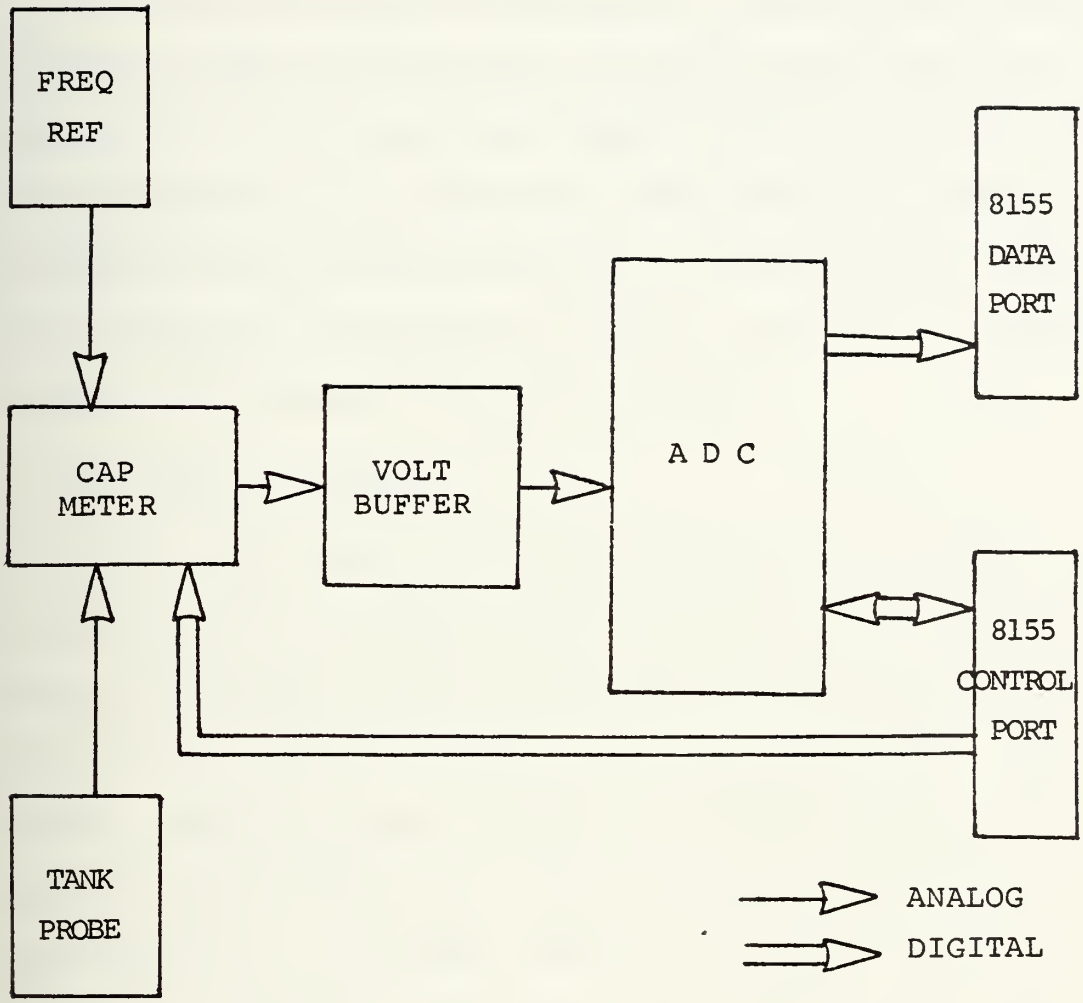
In an MCS-85 system the 8279 serves to relieve the CPU of routine housekeeping functions related to input and

output by providing keyboard scanning and display refresh operations. The CPU communicates with the 8279 by use of memory mapped addressing decoded to 8279 chip select by the system 8205 address decoder.

C. FUNCTIONAL DESCRIPTION OF THE MINIMAL SYSTEM

The minimal system consists of those components described above and is located on a single printed circuit board ten inches by twelve inches in size, served by a single five volt power supply. The 8085A is designed to be the controlling master of a multiplexed bus system. The information on the bus is time multiplexed to contain both data and the lower eight address bits. Arriving information is latched into the general purpose ports resident on the memory chips or passes through the buffer registers of the 8279 from the keyboard if used. Data manipulation under CPU control is accomplished according to instructions stored either in the lower section of read only memory reserved for the monitor program or from the upper section of read only memory which contains the user program. Temporary storage required by the TLI time averaging, linear interpolation and table lookup routines is afforded by five hundred words of read/write (random access) memory. Under program control the input/output ports on the RAM chips serve both to receive incoming eight bit parallel data from the analog to digital converter system discussed below, and to act as control signal generators

sending device enable signals to the remote rank sensor systems and exchanging control signals with the analog to digital converter. Operator control is possible through either the keypad or from a terminal, if provided.



1. Input System Functional Diagram

IV. DATA INPUT SYSTEM

In order to provide the necessary communication between the remote tanks and the basic, minimal system described above, as well as to provide communication of system outputs to the operator of an expanded system through a console, peripheral systems were designed to accomplish the tasks of level detection, frequency to voltage conversion, voltage scaling, and analog to digital conversion.

A. TANK PROBE SUBSYSTEM

In the event that the tank level sensors currently installed in the receiving vessel are retained, the general procedure involves scaling the sensor output voltage to a range of zero to ten volts by use of an operational amplifier circuit. Whether sensor output is directly or inversely proportional to tank level affects system design only in the organization of the lookup tables in read only memory, with no effect on hardware other than the scaling scheme used.

If the currently installed sensors are not retained and the nature of tank contents is sufficiently benign to permit its use, a variable capacitance probe of simple design may be substituted. The probe consists of a length of thirty gauge enameled magnet wire extending the vertical depth of the tank at its deepest point, commonly near the vessel's keel. The end of the probe where cut must also be sealed

and the probe must be mechanically supported in such fashion as to prevent movement or damage while not introducing points of electrical continuity with the ship's structure. The magnet wire has an inherent capacitance of approximately four hundred forty pico-farad per foot. As liquid level, assuming a conductive liquid, varies the capacitance of the probe is seen by a capacitance meter attached to the upper end of the probe. Thus the capacitance of the probe varies inversely but linearly with the level of the fluid in the tank.

Lacking the physical means to immerse a capacitive probe in a large tank for test of the capacitance meter subsystem and TLI system operation, a bank of five fixed capacitors, 0.002uF each, and one five pico-farad capacitor were arranged to permit manually time varying the capacitance between five pico-farad and 0.01uF by manipulation of switches. The five pico-farad capacitor is not switched, thus ensuring stability of the capacitance meter subsystem as the probe induced capacitive input reduces to zero, the full tank condition. Since 5pF is much less than the 0.002uF step capacitor size, the minor inaccuracy thus introduced is less than that caused by manufacturer's tolerance in the larger capacitors. During the calibration of the probe and capacitance meter pair the offset introduced by the unswitched small capacitor was compensated out of the system. The simulator produces an equivalent tank level variation of twenty three feet.

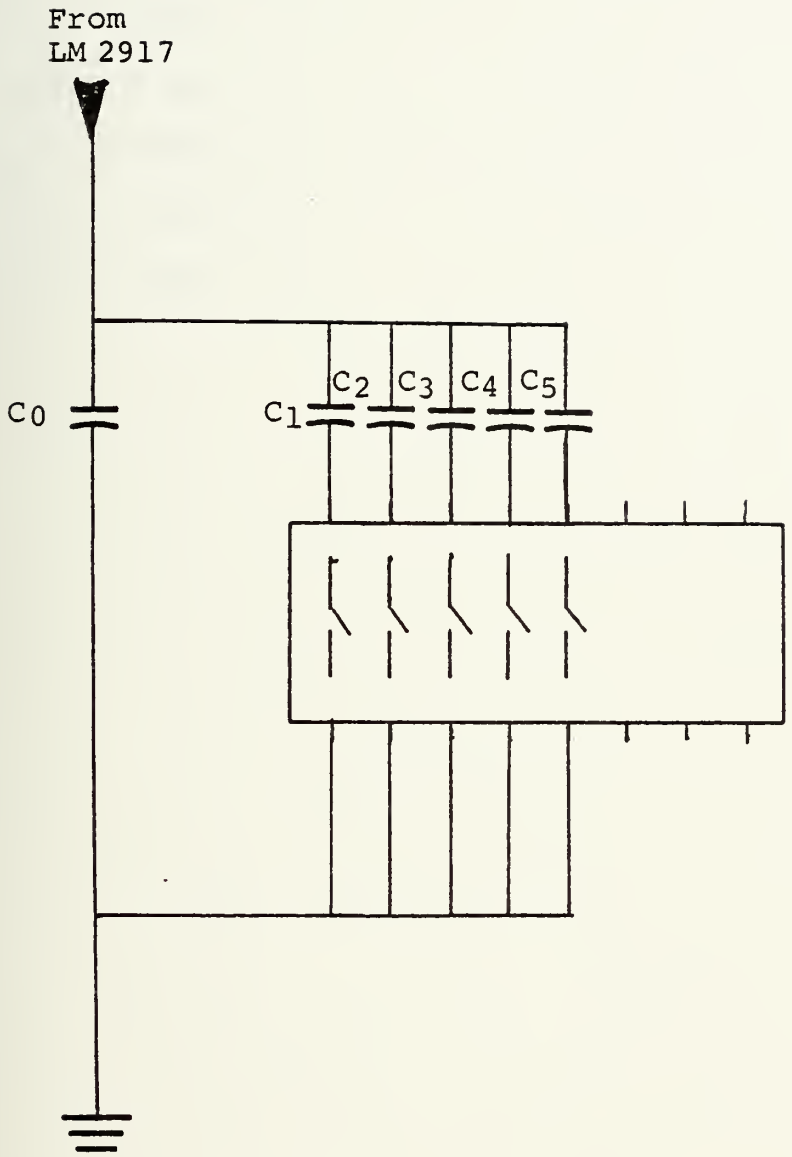
B. CAPACITANCE METER SUBSYSTEM

The capacitance meter subsystem is composed of three integrated circuits and their required discrete accessories. The subsystem senses tank probe capacitance as described above and translates it into a proportional voltage within the zero to ten volt tolerance acceptable to the system analog to digital converter. The heart of the capacitance meter is an LM2917N frequency to voltage converter. Following the differential amplifier first stage of the device is a charge pump with external timing capacitor, output register and filter capacitor. When the frequency reference input changes state due to zero crossing of the waveform, the timing capacitor is either charged or discharged linearly between two voltage levels separated by one half the supply voltage. The average amount of current pumped into or out of the timing capacitor is directly proportional to the capacitance, reference frequency and supply voltage according to

$$Vcc \times f_{in} \times C_{probe} = i_c(avg).$$

The output circuit, another operational amplifier stage, mirrors this current through the load register such that with proper filtering to integrate the current pulses then the output voltage becomes

$$V_o = V_{cc} \times f_{in} \times C_{probe} \times R.$$



2. Variable Capacitance Test Circuit

2a. VARIABLE CAPACITANCE TEST CIRCUIT EXTERNAL ELEMENTS

C0 - 5.00 uF

C1 - 0.002 uF

C2 - 0.002 uF

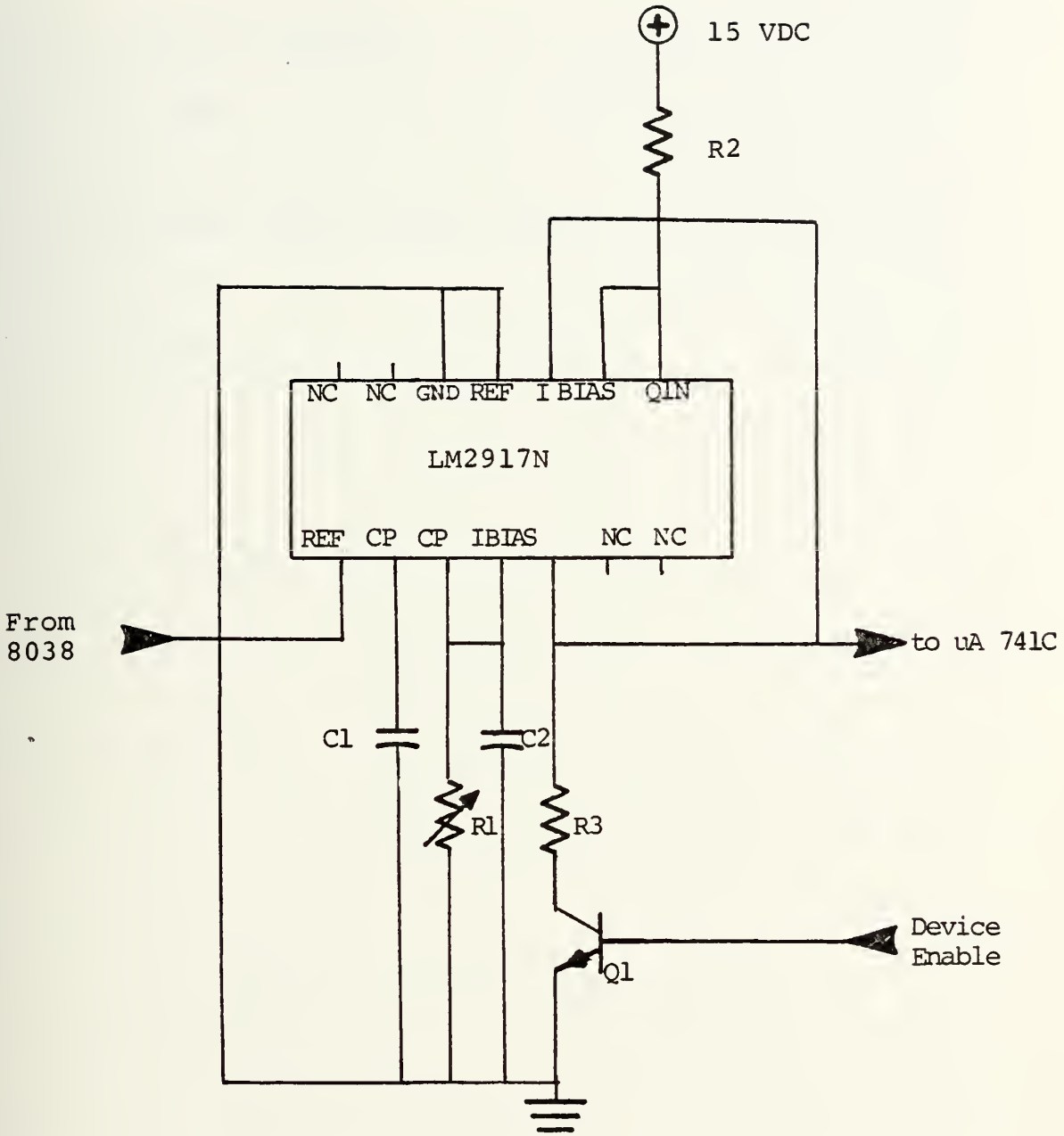
C3 - 0.002 uF

C4 - 0.002 uF

C5 - 0.002 uF

The output resistor R is chosen to provide sufficient output impedance and may be adjusted to vary output voltage magnitude provided to the voltage buffer. For the components shown, V_o is between seven and eighty millivolts as the probe capacitance is varied.

The accuracy of the capacitance to voltage translation is highly dependent on stability of the frequency reference supplied to the LM2817N by the external source. The Intersil 8038 precision waveform generator was chosen for this application over other common circuits employing timers or operational amplifiers as oscillators because of its low frequency drift with temperature (maximum 50ppm per degree centigrade) and supply voltage and because of the low number of external elements required. The frequency reference suggested by Intel in the pertinent LM2817N application note is sixty Hertz, ten volts AC. Although this input might easily be derived from the vessel's lighting circuits it was decided that a more stable source was desirable because the typical naval vessel does not consistently control its lighting circuit operating frequencies to sufficient accuracy. Experimentation disclosed that the absolute value of reference frequency is not critical so long as it remains stable, otherwise the calibration of device output voltage becomes unreliable. In addition, the LM2917N has been shown to operate reliably with sinusoidal or square wave inputs of less than one volt peak to peak. The output of the frequency



3. Capacitance Meter Subsystem

3a. CAPACITANCE METER
EXTERNAL ELEMENTS

R1 - 110K ohm variable

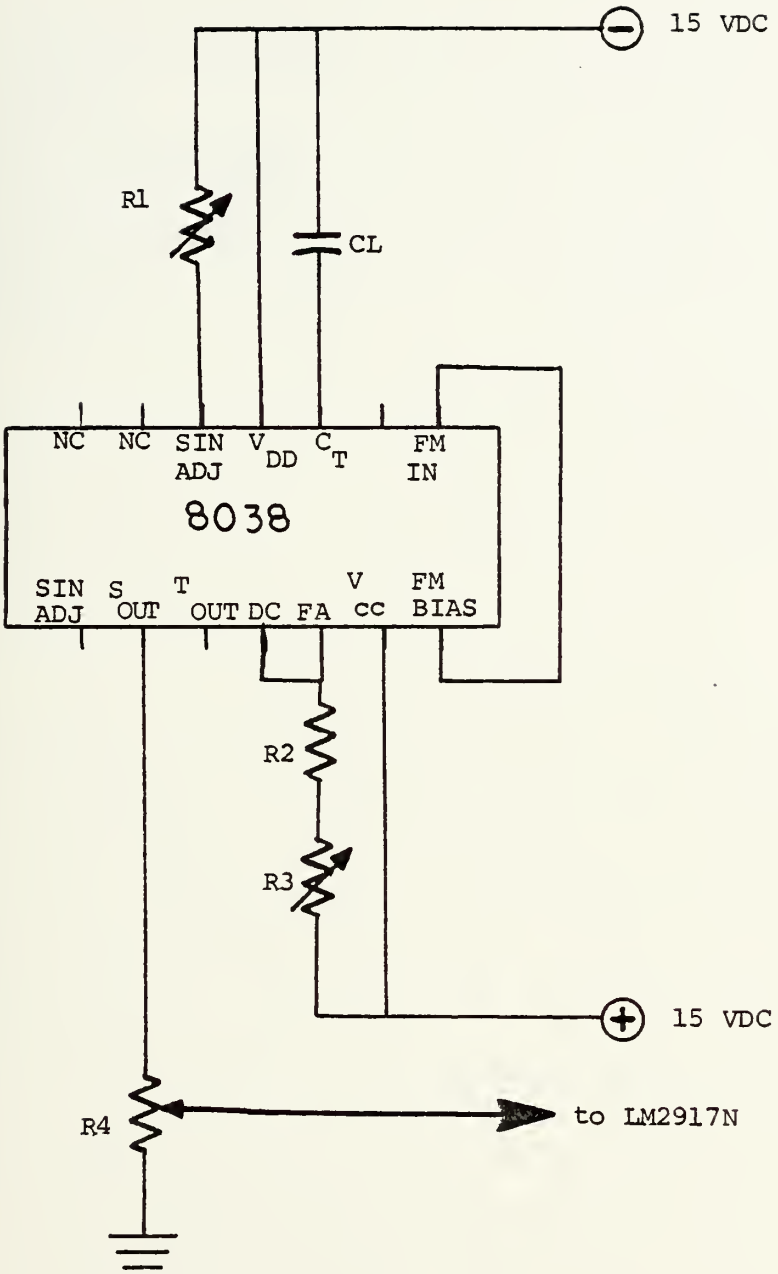
R2 - 470 ohm

R3 - 10K ohm

C1 - switched bank or tank probe

C2 - 1.0 uF

Q1 - 2N3904



4. Frequency Reference Subsystem

4a. FREQUENCY REFERENCE EXTERNAL COMPONENTS

R1 - 100K ohm variable

R2 - 3K ohm

R3 - 10K ohm variable

R4 - 100K ohm variable

C1 - 0.25 uF

reference was somewhat arbitrarily set at two volts RMS, sixty Hertz and supplied to the LM2817N without the need for an additional line buffer which would have been required had the original ten volt input been found to be necessary.

In order to most efficiently utilize the full ten volt scale of input voltages accepted by the analog to digital converter, while still operating with probe capacitances of realistically small value it was necessary to amplify the LM2917N output voltage from tens of millivolts to volts. This was inexpensively but accurately accomplished using a Signetics uA741C operational amplifier configured as a non-inverting voltage amplifier as shown with

$$V_{out} = V_{in} \times (R1+R2)/R1=15.$$

R2 is partially realized by a trimming resistor which provides a point of adjustment where compensation for device variations is necessary. As shown, the buffer amplifier supplies input voltages to the analog to digital converter in the range of 0.97 to 9.5 volts, thus using eighty five percent of the acceptable input range. Sufficient margin is retained at the voltage extremes to preclude the appearance of negative voltages or voltages above ten volts, due to temperature fluctuations or other causes, which might damage the analog to digital converter.

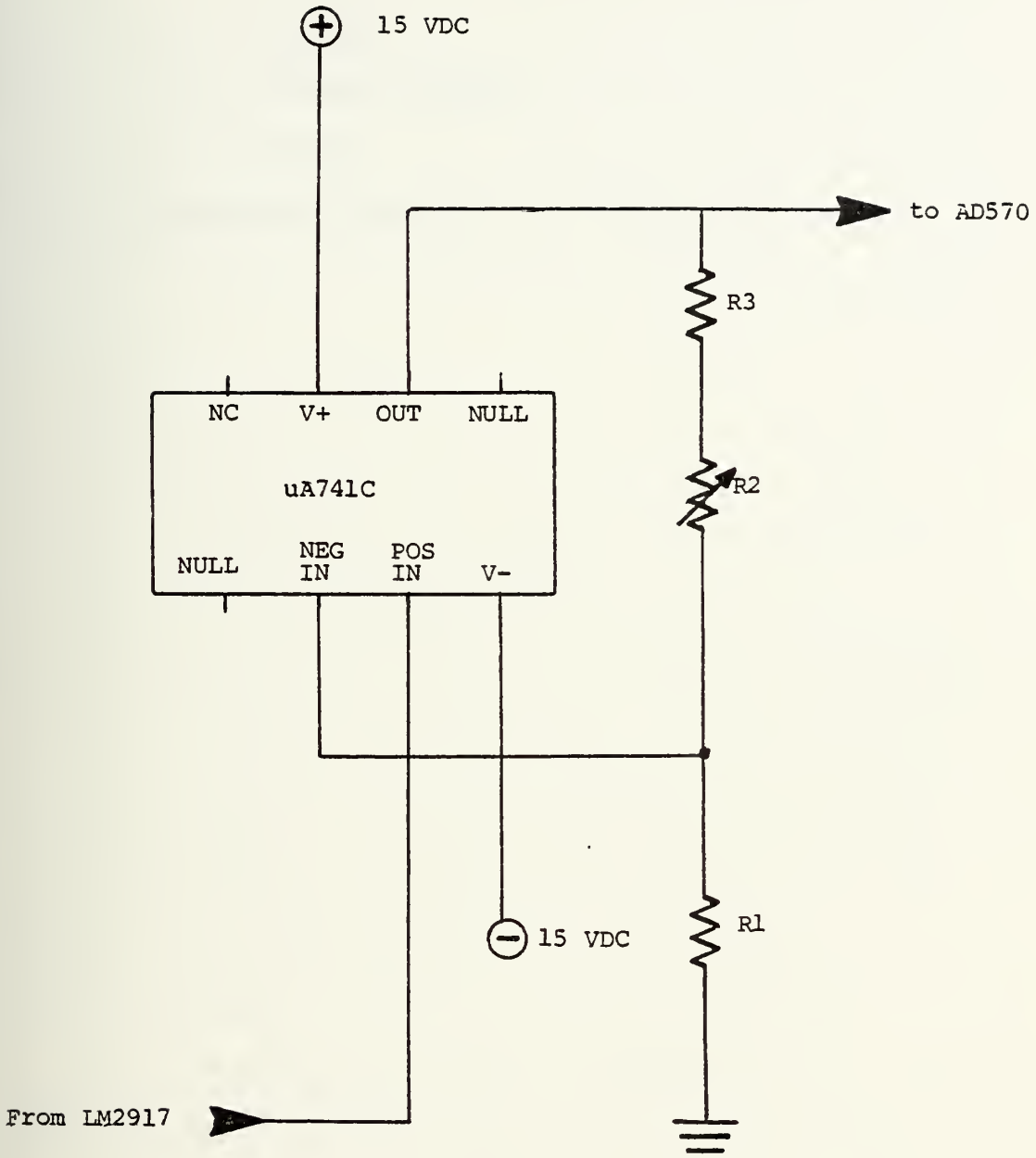
The capacitance meter subsystem required extensive initial adjustment to operate with acceptable current drain from the

frequency reference to the frequency to voltage converter. Performance thereafter was consistently accurate with no significant variation in output noted over the course of several hours' operation.

C. ANALOG TO DIGITAL CONVERSION

The TLI system serving several tanks is arranged such that individual tank probes are served by dedicated, inexpensive three chip sets, as described above, which are each calibrated to present a uniform range of voltages to a single analog to digital converter serving all tanks in the system. Additional control logic is required to decode the control port signals presented by the CPU to port C on the low address 8155 chip. These decoded control signals are then employed as sensor enable signals by negative logic switching of base voltage on an NPN transistor such as the 2N3904 in series with the emitter of the LM2817N on-chip output driver transistor. Turning off the external transistor stops current flow through the 10K ohm resistor attached to pin five of the LM2917N, thus bringing the output voltage to within about 0.7 volts above ground, sufficiently low to be recognized as zero by the analog to digital converter.

In keeping with overall design goals of simplicity and low cost, a low speed system for analog to digital conversion was sought. Two readily available devices were considered.



5. Non-Inverting Voltage Amplifier

2a. Non-Inverting Voltage Amplifier
External Elements

R1 - 3K ohm

R2 - 5K ohm variable

R3 - 39K ohm

Operational Amplifier - Fairchild uA 741C

Leventhal suggests in Ref. 4 the use of an Analog Devices AD7570 ten bit monolithlic analog to digital converter (ADC). This realization was rejected because the scheme underutilizes the device and requires an external comparator such as the LM311. Instead, the device chosen was the less expensive Analog Devices AD570 eight bit ADC. While this device is significantly slower than the AD7570, conversion speed is not a critical factor in the TLI application. Advantages of the AD570 are:

1. Economical cost.
2. Relatively rugged I^2L technology.
3. Insensitivity to supply voltage variations.
4. Onboard analog comparator.

The AD570 is a downgraded ten bit successive approximation analog to digital converter with on-chip DAC (Digital to Analog Converter), clock, comparator, successive approximation register and output buffers which requires no external components and performs conversion of unipolar signals in the range of zero to ten volts in approximately twenty five microseconds.

In operation, the BLANK and $\overline{\text{CONVERT}}$ line is normally held low by appropriate coding of the control word presented at the 8155A control port. Conversions are triggered by a positive pulse of about 2uSec duration. Since the organization of the TLI system requires only one ADC the eight bit output may be directly wired to port A of the lower 8155,

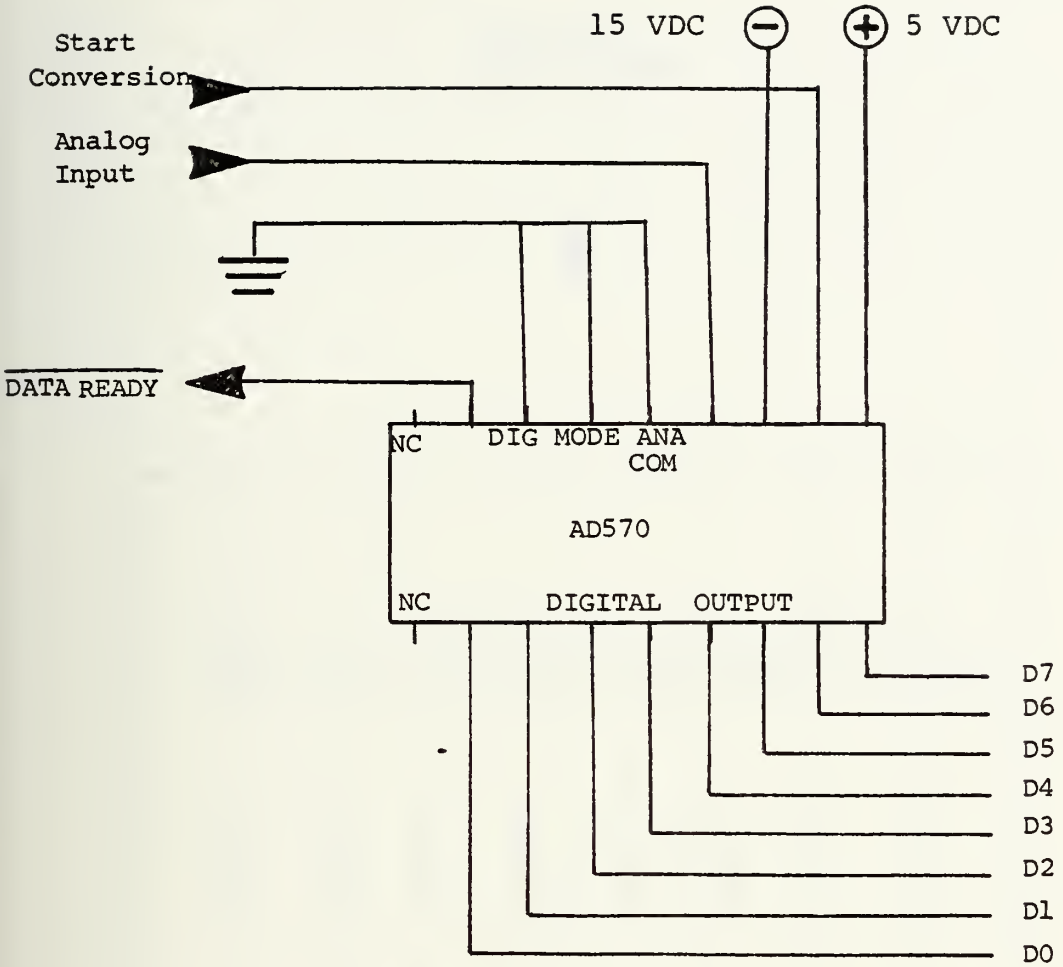
thus making use of the onboard latches of the RAM. No additional three state latches are required as would be the case were data entered via the bus. To command a conversion, the BLANK and $\overline{\text{CONVERT}}$ line is brought high which causes the DATA READY line to the control port to go high about 1.5uSec later. At the end of the conversion cycle the $\overline{\text{DR}}$ line again goes low, the data outputs become active with the new data and remain so until a new conversion is ordered. Since the rate of fluid level fluctuation is much slower than the 25uSec conversion time there is no requirement for sample and hold circuitry between the various LM2917N outputs and the analog to digital converter. Polling of the converter to determine whether conversion is complete may be accomplished by addressing the $\overline{\text{DR}}$ line where it enters the 8155 control port and executing a software comparison routine.

For initial calibration of the AD570, it was necessary to fabricate a simple array of eight common cathode, five volt LED's which were connected to the output data lines of the ADC. By adjustment of the trimming resistor in series with the input as recommended by the manufacturer, the output code transition from 11111110 to 11111111 may be set to occur at the full scale voltage level expected from the 741C capacitance meter buffer. By experiment it was ascertained that instability of the least two significant bits could be reduced by appropriate despiking capacitors in the neighborhood of the AD570. These instabilities were more

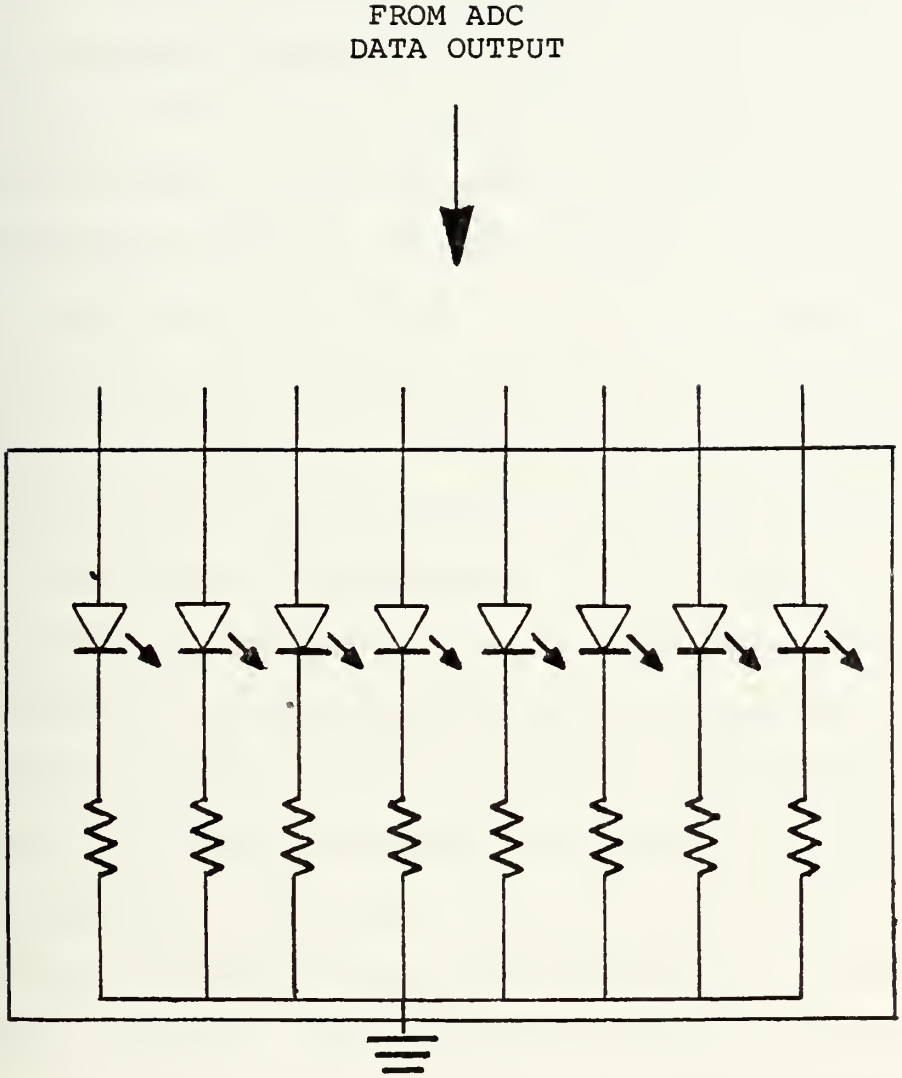
pronounced when the AD570 was under separate preliminary bench testing where the convert order was provided by an external pulse generator, than when the pulses were provided in the manner described above. In addition the LED calibration device as designed tended to tax the current sourcing capability of the AD570 when the data output lines were all simultaneously high. This deficiency may be remedied by substitution of 470 ohm current limiting resistors for the 360 ohm resistors used initially at the cost of slightly reduced brilliancy of the LED's.

D. DATA INPUT SYSTEM INTERACTION AND OPERATION

Each of the subsystems described was connected to the others as described above and operated with the switched capacitor array providing a time varying tank level input. For the single tank case observed the performance of the input system as a whole was satisfactory although initial adjustment of the trimming resistors in each of the several subsystems became an iterative process in the search for optimum interface voltage levels. The system showed good stability with temperature variation as the devices warmed to operating temperature and showed no need for recalibration from one test to the next.



6. Analog to Digital Converter Subsystem



7. ADC Calibration Device

V. TERMINAL INTERFACE

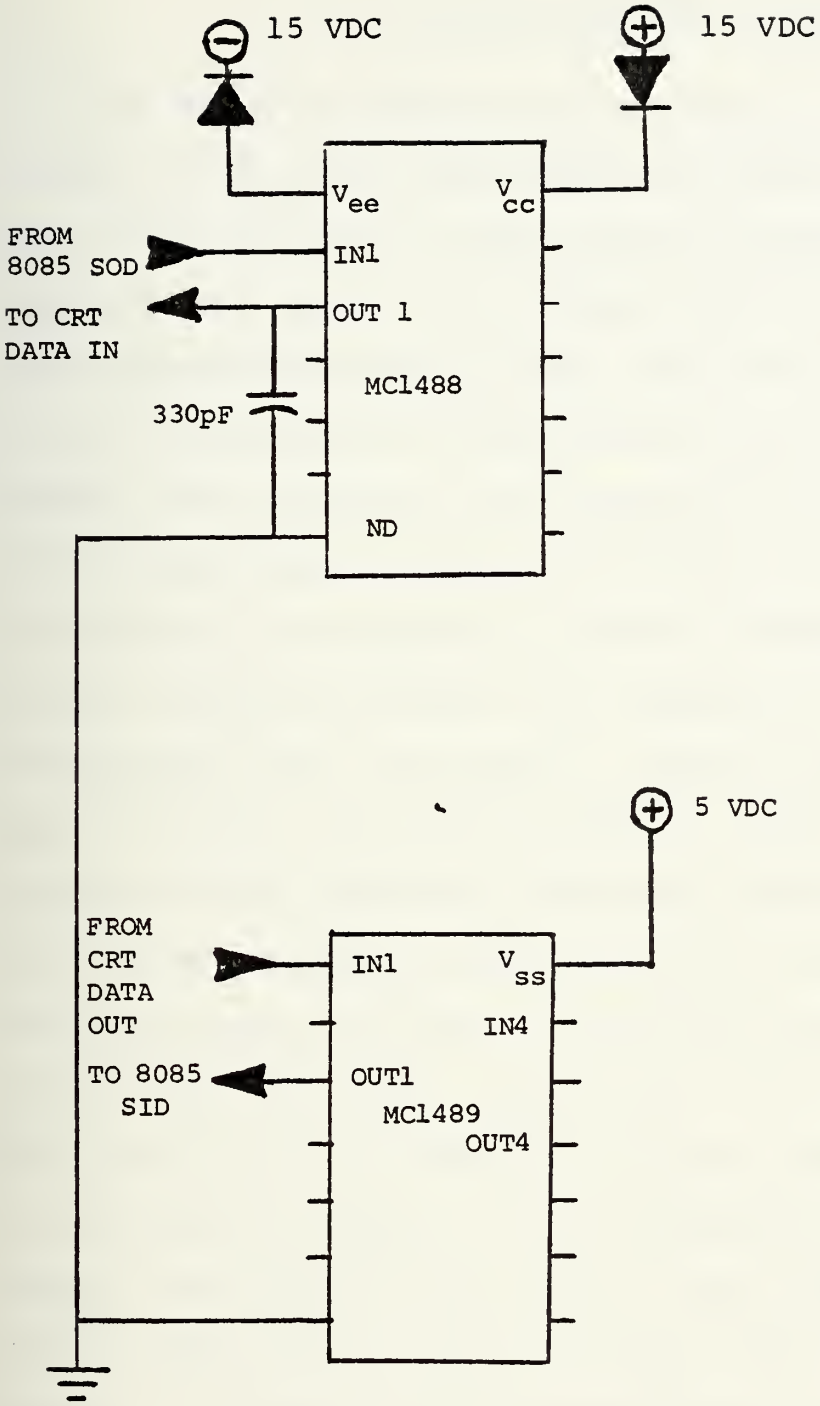
The terminal interface system was designed and built to permit operator communication with the TLI system through a standard CRT terminal by use of an RS-232C interface. Software timing and delay loops within the monitor program of the SDK-85 identify incoming signals at the serial input port, operating at 110 baud. The circuit shown interfaces positive logic TTL signals with the RS-232C high voltage inverted logic levels. The monitor program transmits information at 110 baud through the serial output port and this interface to the terminal. The MC1488 line driver and the MC1489 line receiver were attached to the basic SDK-85 circuitry at the point where serial information enters the teletype interface circuit, which was disconnected. In addition to the basic driver-receiver circuit, a 330 pF capacitor was required on the system output line to limit the output slew rate to thirty volts per microsecond in accordance with RS-232C standard. The capacitor value was determined using the relation

$$C = I_{sc} \times \text{slew rate}$$

where I_{sc} is the worst case output short circuit current of twelve milliamps specified in the manufacturer's data for the MC1488. The MC1488 chip includes a 300 ohm resistor to ensure that the output impedance of the driver will be at

least 300 ohms even when the power is off. Should the power supply malfunction and produce a low impedance path to ground from the resistor, excessive power dissipation would result. To preclude device damage, series diodes were provided in both positive and negative supply lines as shown. On the SDK-85 board a three position switch was installed to enable the operator to select either terminal or keypad/LED communication modes.

In operation, the terminal interface provided an expanded set of command instructions as described in Ref. 3. Additional development of display software is required to efficiently utilize terminal capabilities.



8. RS-232C Terminal Interface

VI. PROGRAM TRANSFER DEVICE

The choice of the 8085 microcomputer system as the nucleus of the tank level indicator system left two paths open for realization of the read only memory. The relative merits of each path were explored before the 8755 read only memory was finally chosen. The first alternative was to store programs in an appropriate number of Intel 2708 EPROMs whose capacity is one thousand bytes each. The Naval Postgraduate School employs a Tektronics 8002A microprocessor development system (MDS) to compose software and to transfer machine language programs from floppy disk storage to the programmable read only memory. However, the additional wire wrap circuitry and latches needed to install a bank of 2708's as part of the SDK-85 was considered excessive since the 8085 system components communicate via a multiplexed address/data bus while the older 2708 devices employ dedicated address and data lines. The second path to memory realization was to use the existing circuitry aboard the SDK-85 by storing the TLI program in an additional 8755 EPROM. Three unused chip select lines from the 8205 address decoder remain which may be used to further expand stored program memory to a total of ten thousand bytes, including monitor program, if required at a later date. The clear advantage of using this approach was somewhat lessened by the problem of programming the 8755.

As a relatively new device, no existing facility at the Naval Postgraduate School was capable of programming the 8755 EPROM. The alternatives were three:

1. Purchase the services of an outside firm to program the device using a program provided by the school.
2. Purchase an adapter module for the Tektronics 8002A or the PROMPT 475 module for use with the PROMPT 48 design aids in use at the school.
3. Develop an original device for transfer of the contents of one EPROM to another, such as from a series of 2708 devices to an 8755A.

The first two alternatives were rejected because of the excessive cost of hardware modules and the excessive cost and turn around time associated with programming by another facility. Thus the development of an efficient stand alone device for program transfer became necessarily part of the tank level indicator project.

A. PROGRAM TRANSFER DEVICE CONCEPT

The program transfer device is intended to retain software development capabilities of the Tektronics MDS without sacrificing the advantages of more modern memory devices which the MDS cannot directly program as presently configured. To achieve this goal, the PTD must automatically address and read in sequence the contents of 2708 EPROMs each containing one kilobyte of program, address the corresponding section of

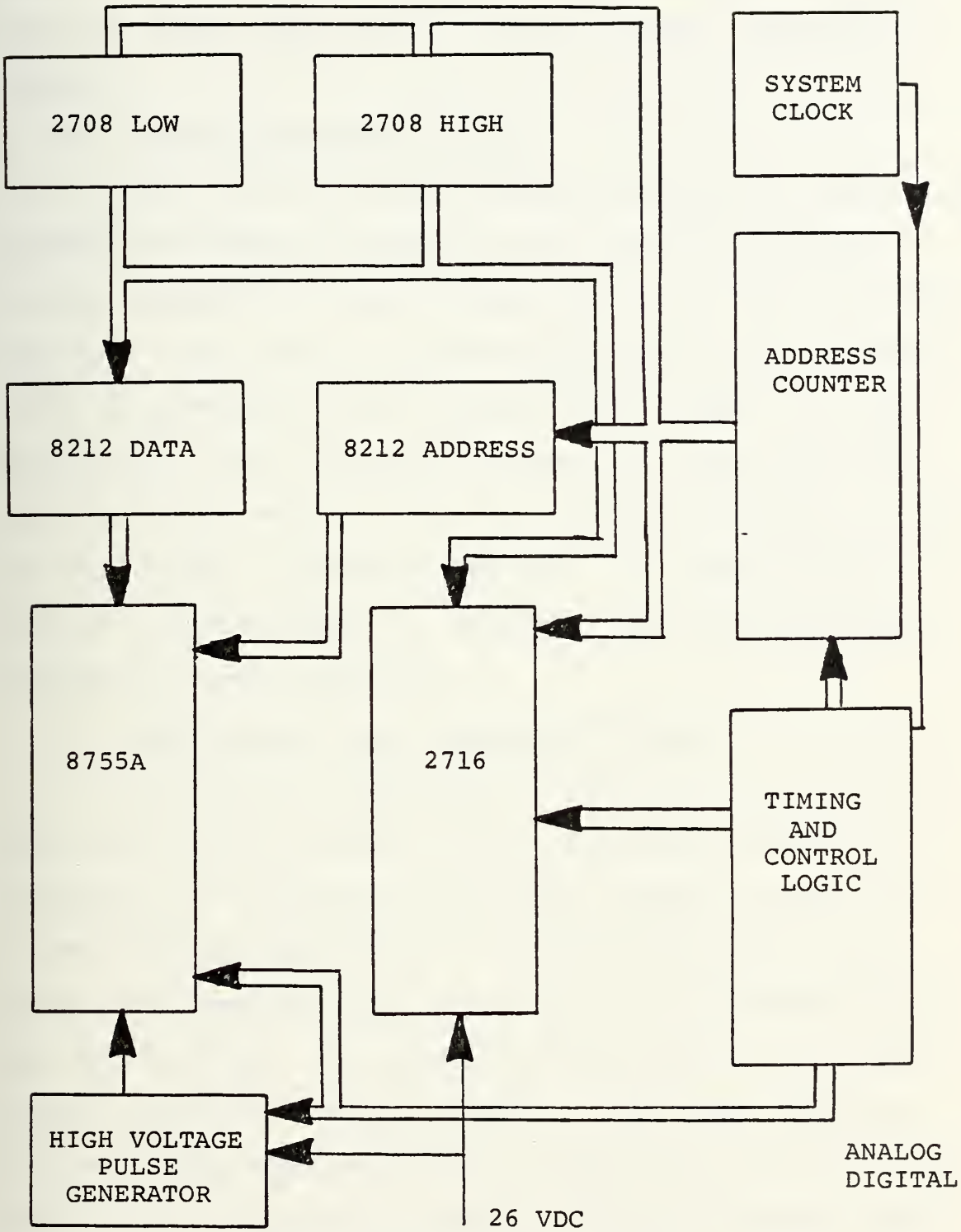
8755A memory, provide a high voltage programming pulse of proper duration and repeat the process after incrementing the address pointer. The entire sequence must provide for non-multiplexed addressing of the 2708 and for multiplexed addressing of the 8755A. In order to fully utilize the two kilobyte capacity of the 8755A, two 2708 EPROMs must be programmed in sequence with the same two kilobytes of data. The result is a two step process in which the desired program is composed in either Microsoft Fortran or assembly language, then tested and debugged using the Tektronics MDS and programmed into two 2708 EPROMs. The second step transfers the contents of these two 2708 devices automatically into one 8755A EPROM. Such an approach not only results in considerable saving of hardware dollars over the cost of a commercially produced equivalent, but also makes possible the short turn around programming desirable in an academic environment.

B. PTD SUBSYSTEMS

Subsystems of the PTD include a clock generator, address counter, clock control circuitry, timing and control logic, a high voltage pulse generator and operational controls.

1. Clock Generator Circuit

As shown, the clock generator is composed of a single TTL 7404 inverter set with three external components whose values were chosen to provide a nominal base clock frequency



9. Program Transfer Device Functional Diagram

of one kilohertz. The output waveform is of sufficient quality to operate most low speed TTL components and the clock is always self starting when energized. Reference 2 applies.

2. Address Generator Circuit

The eleven bit binary address required to access two kilobytes of memory is generated by a twelve bit binary counter composed of three cascaded four bit 74191 binary up-counters. The 74191 is a synchronous binary counter which may be preloaded with any desired initial count. In this application, when the system is reset all twelve bits are reset to zero. When activated the counter increments through the full range of addresses required. The twelfth bit is used as a control signal to determine when the programming operation has been completed.

3. Clock Enable Pulse Generator Circuit

Programming requirements of the 8755A are such that once during each iteration of the programming sequence all functions of the addressing and data transfer systems must be temporarily suspended while a fifty millisecond high voltage programming pulse is applied to the addressed location in the 8755A. To accomplish this pause in operation, a pulse generator circuit is used. A 555 timer employed as a monostable multi-vibrator is appropriate because of its simplicity. The precise duration of the programming pulse

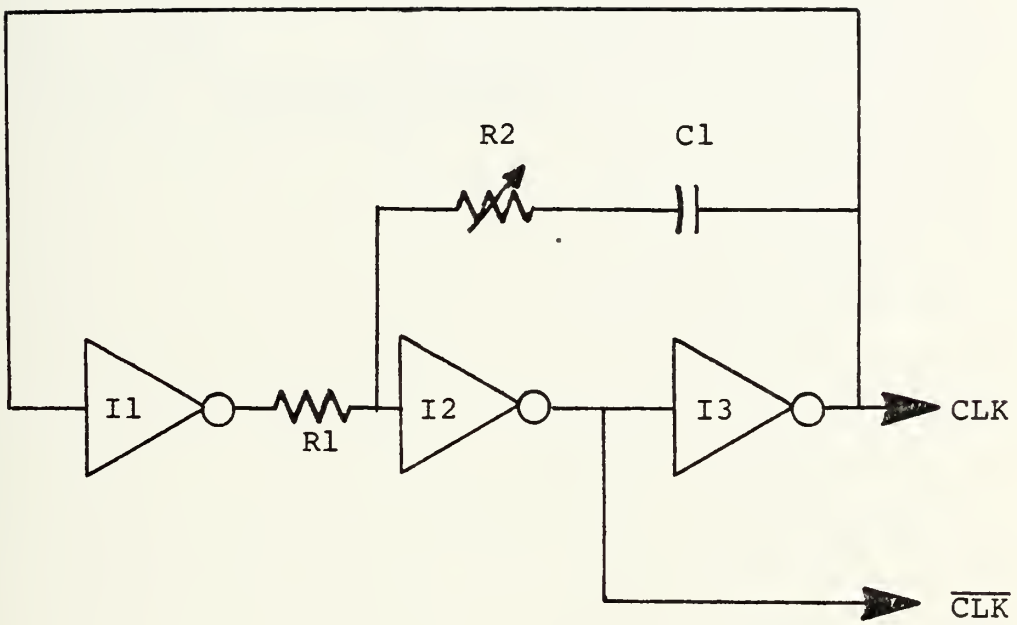
is not critical but should be at least forty five milliseconds and typically fifty milliseconds by specification. The propensity of the 555 timer to drift slightly from initial settings is not a significant disadvantage. The monostable is triggered at the appropriate time during the cycle by the control logic array discussed below. Component values were chosen according to the relation

$$T = 1.1RC$$

where the value of the timing capacitor C was arbitratily set at one tenth microfarad, leading to a timing resistor value of approximately 455K ohms. The trimmer resistor was used to enable compensation for variation in element values from the nominal in order to obtain the desired pulse width. The output of the monostable is one of four inputs to the clock enable logic as shown. This circuit disables the system lock when the programming pulse timer is in the triggered state and also when the twelfth address bit is set at the end of the two kilobyte programming sequence.

4. Timing and Control Logic Realization

The timing and control logic subsystem manages the proper sequencing of various address and data latches and chip enables throughout the system as well as providing the secondary clock which causes sequencing of the address generator described above. Rather than realize the control signal sequence with a programmable logic array or other



10. PTD System Clock Generator [1]

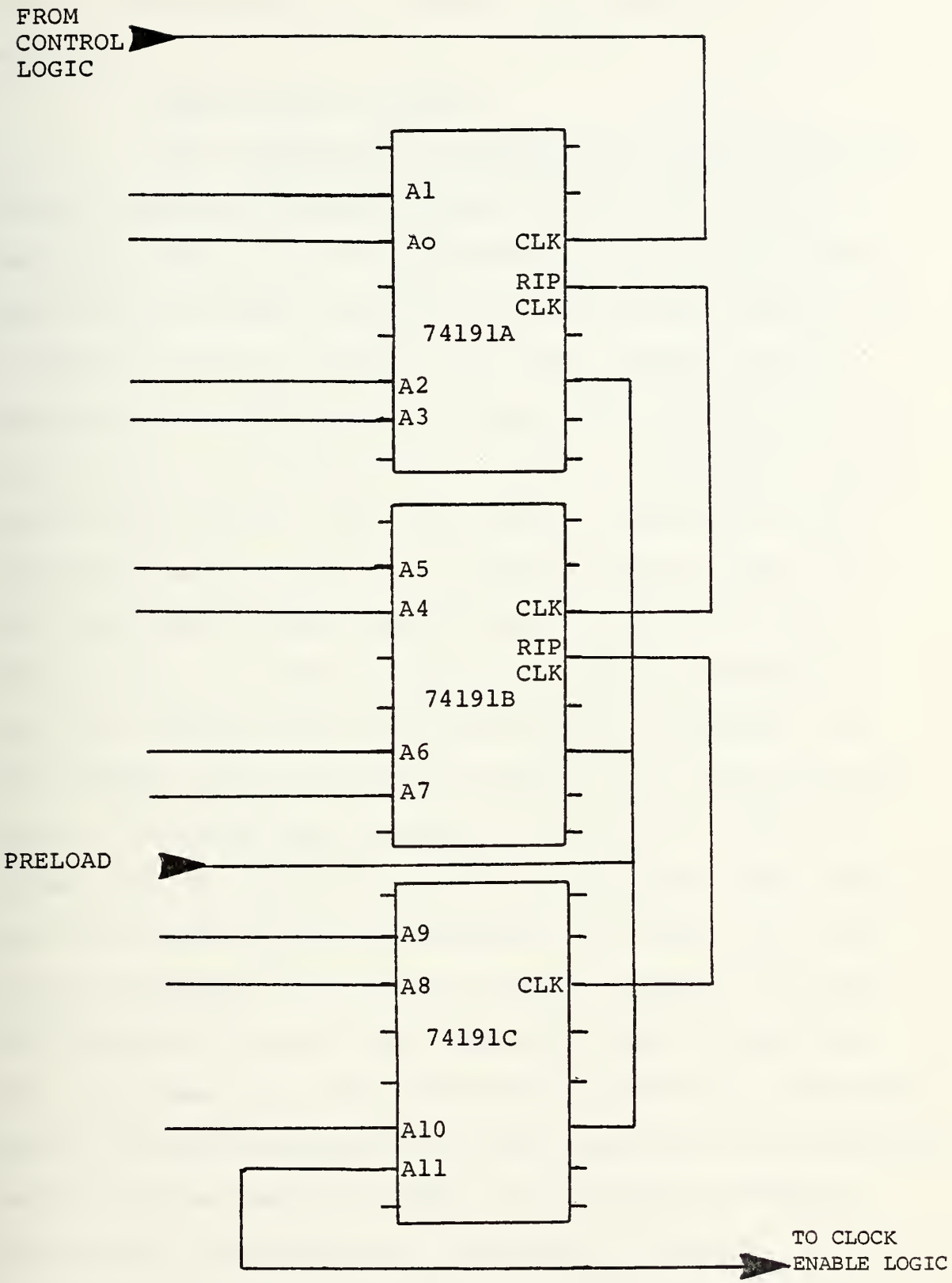
10a. Clock Generator
External Elements

R1 - 300 ohm

R2 - 100 ohm variable

C1 - 1.8 uF

I1,I2,I3 - 7404 HEX inverter

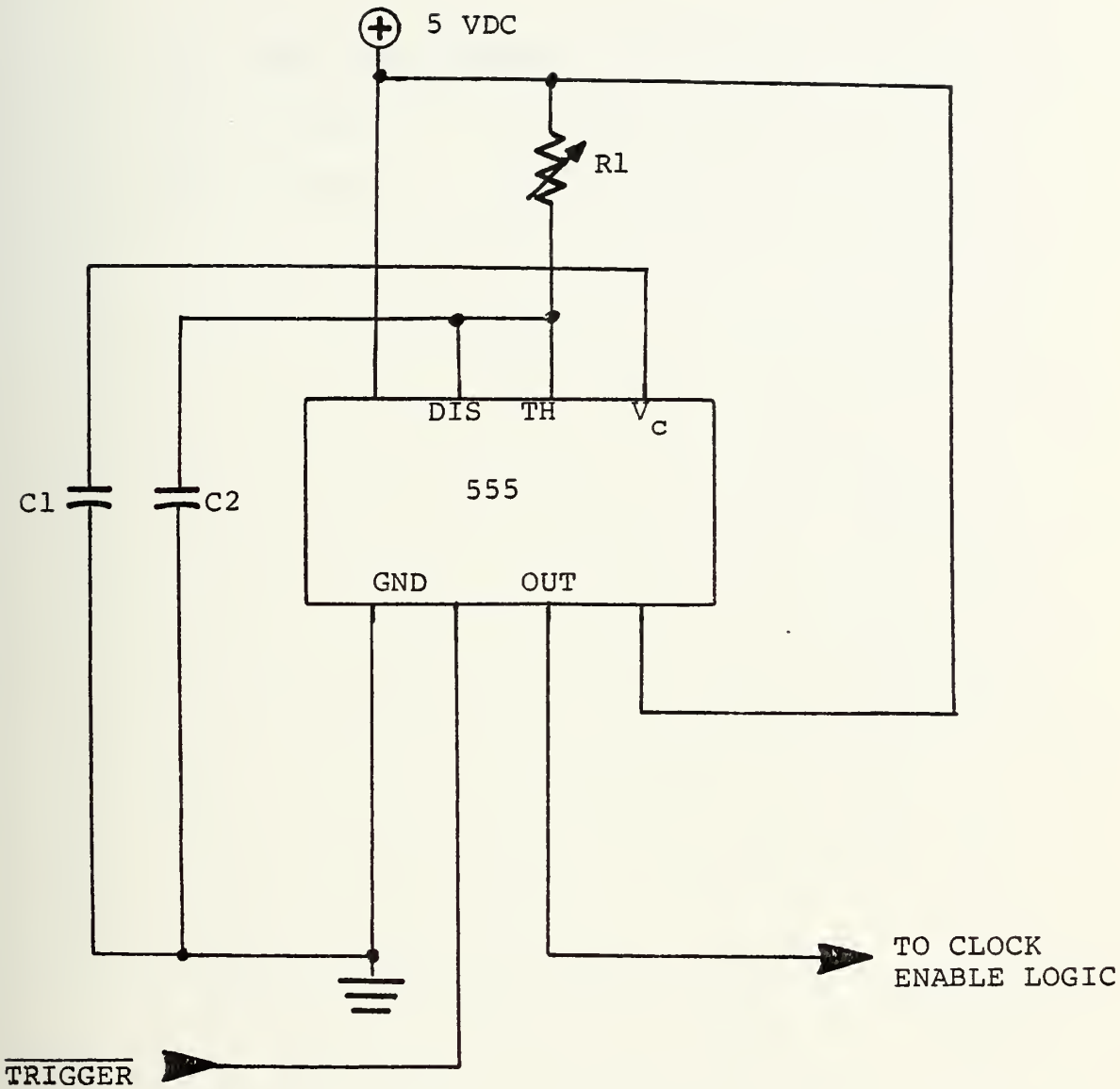


11. Binary Address Counter Functional Diagram

device it was decided to utilize five presettable shift registers.

a. Address/Data Latches

The requirement to transition from the dedicated address and data lines used by each of the 2708 EPROMs to the scheme used by the 8255A wherein the lower eight address lines are multiplexed with the eight data lines required the of address and data latches in the path between address generator, donor EPROM and receiving EPROM. The Intel 8212 input/output port consists of an eight bit latch with three state output buffers along with control and device select lines which permit its use as a gated buffer by tying the mode signal low and the strobe input high as shown. The output buffers are then enabled by the device selection logic upon command from the control signal generator. In this fashion, for each address iteration, the lower address bits are simultaneously presented to the active 2708 and latched into the address buffer resident on the 8755. Then, while the address remains unchanged at the 2708, the 8212 serving the address bus has its outputs disabled by signal from the control logic, after which the 8212 serving the data bus between the active 2708 and the 8755A has its outputs enabled, thereby presenting the data contained at the addressed location to the receiving EPROM. The mutually exclusive device select logic prevents contention on the bus.



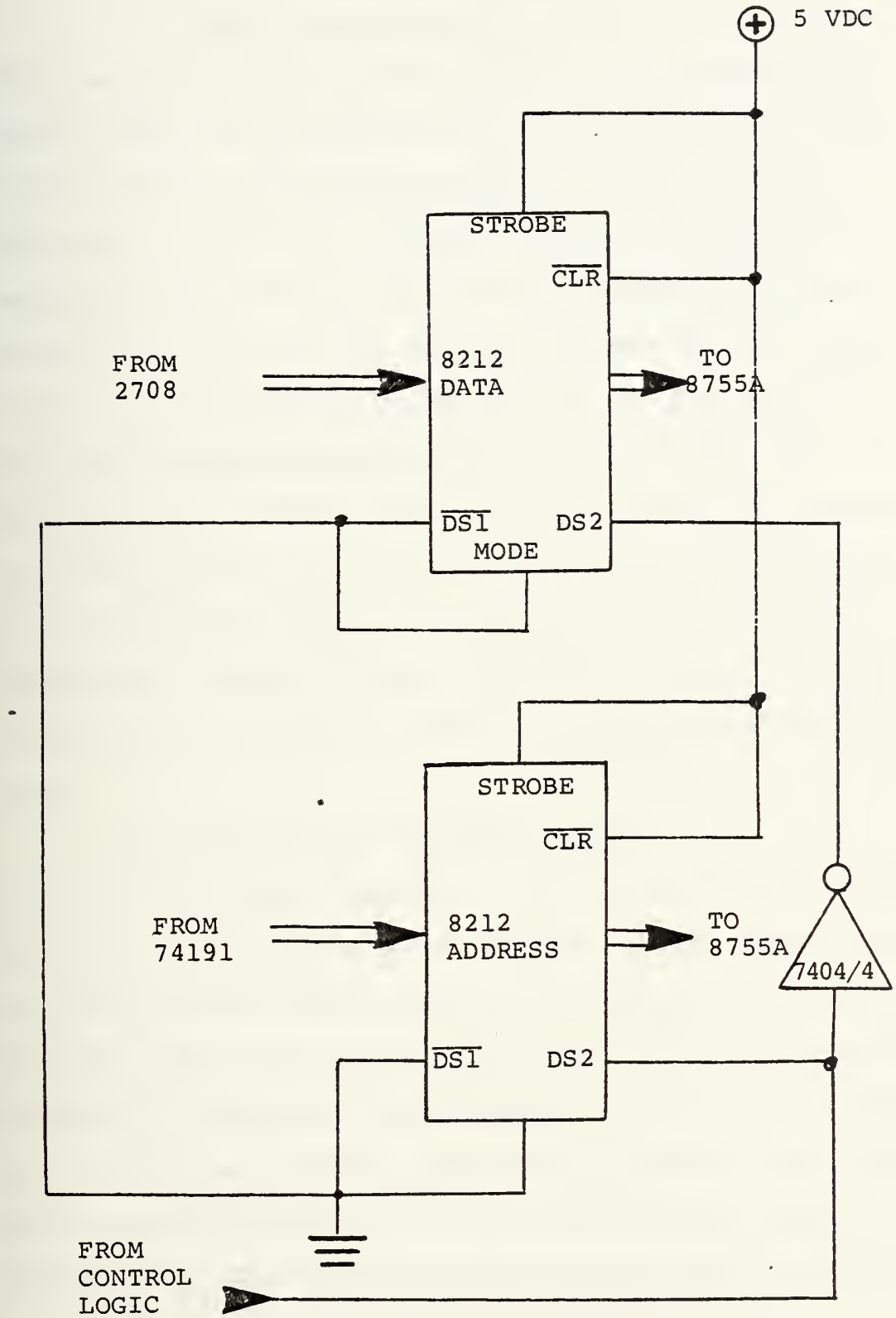
12. Control Pulse Generator

12a. Control Pulse Generator
External Elements

R1 - 455K ohm variable

C1 - 0.1 uF

C2 - 0.1 uF



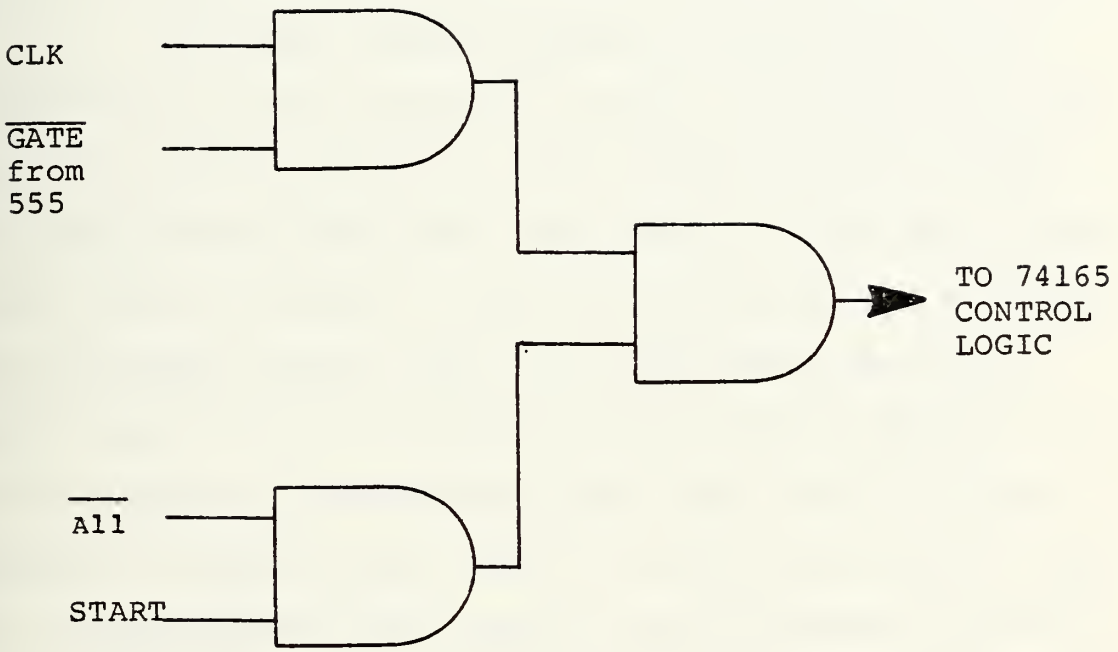
13. Address and Data Multiplexing System Functional Diagram

b. 8755A Timing Requirements

During the programming cycle at each address the 8755A requires three distinct inputs. The address latch enable (ALE) must be provided while the effective address is presented by the address buffer in order to latch in the lower eight bits of the address. After the sequencing of the system has halted the TTL level programming command must be presented to the 8755A in such a manner that it becomes active at least two microseconds prior to the arrival of the high voltage programming pulse and remains active at least two microseconds after the end of the high voltage programming pulse. The system clock rate of one kilohertz was intentionally chosen because the rather slow clock rate coupled with the gate delays involved with control signal realization guarantee that this two microsecond overlap will occur.

c. System Control Signal Timing

As shown, the five control signals are arranged such that after arrival at an address the sequence of events is such that the address buffer is enabled and the data buffer disabled, then the address lower eight bits are latched into the 8755A. The upper three address bits are not multiplexed and need not be latched to make way for data. The programming command is received by the 8755A followed shortly by triggering of the monostable which first halts the system



14. Clock Enable Logic

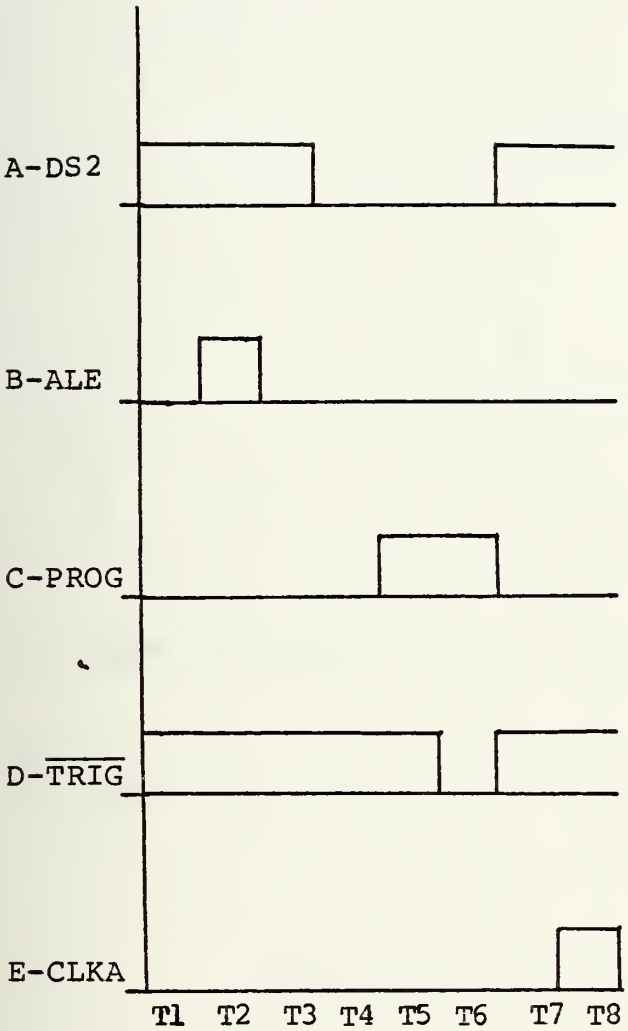
sequencing process and sends after a short delay the twenty five volt programming pulse to the 8755A. When the timer resets after fifty milliseconds the high voltage pulse ceases and then the program command becomes inactive. The system clock is re-enabled and the next address is requested from the address counter, thus repeating the cycle until the terminal address is recognized by the control logic and the clock disabled.

d. Control Signal Generator

The five control signals are generated by an array of five 74165 parallel in, serial out eight bit shift right only shift registers. The register parallel inputs are hardwired such that when the system is reset the initial control word is entered. Thereafter as pulses are received from the system master clock, the bits appearing at the serial output of each register form the proper sequence of control signals. The registers have their serial outputs connected to their serial inputs in end-around fashion such that the sequence of bits repeats itself endlessly as long as the clock is active. The first rising edge of the clock shifts from the initial state to state T2 shown in the timing diagram.

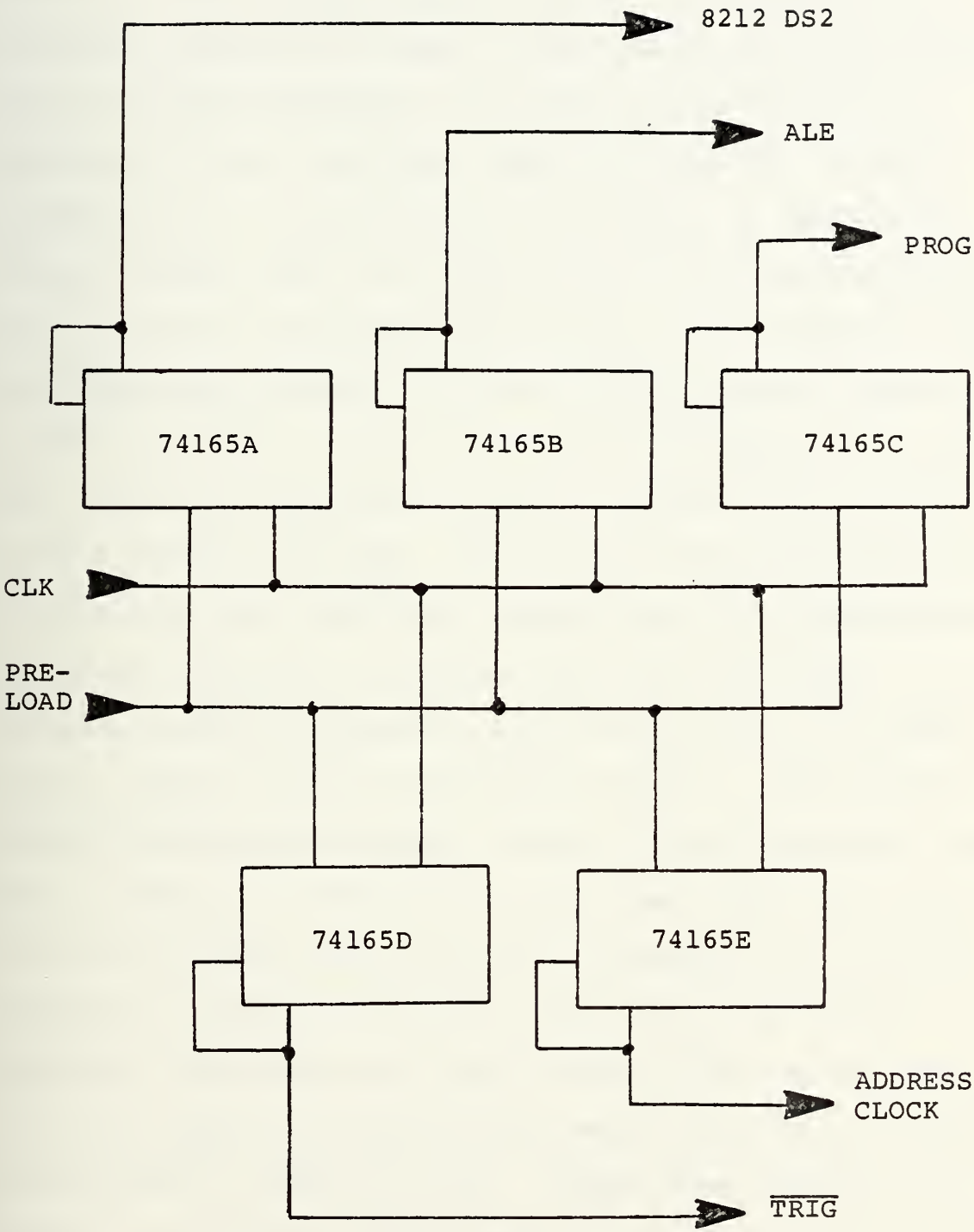
5. Programming Pulse Generator

The programming sequence of the 8755A requires the switching of twenty five volts DC at each address. The circuit shown uses a TTL signal derived from the output of



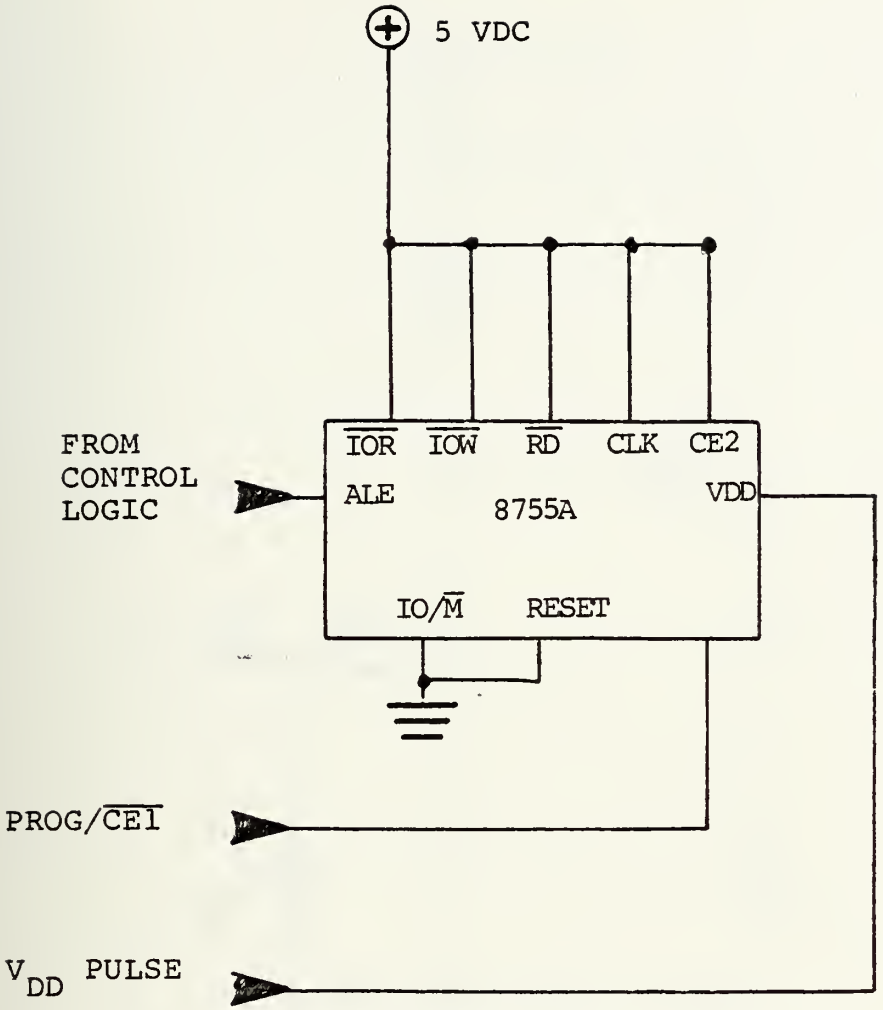
	A	B	C	D	E
T1	1	0	0	1	0
T2	1	1	0	1	0
T3	1	0	0	1	0
T4	0	0	0	1	0
T5	0	0	1	1	0
T6	0	0	1	0	0
T7	X	0	0	1	0
T8	X	0	0	1	1

15. Control Signal Timing and Truth Table

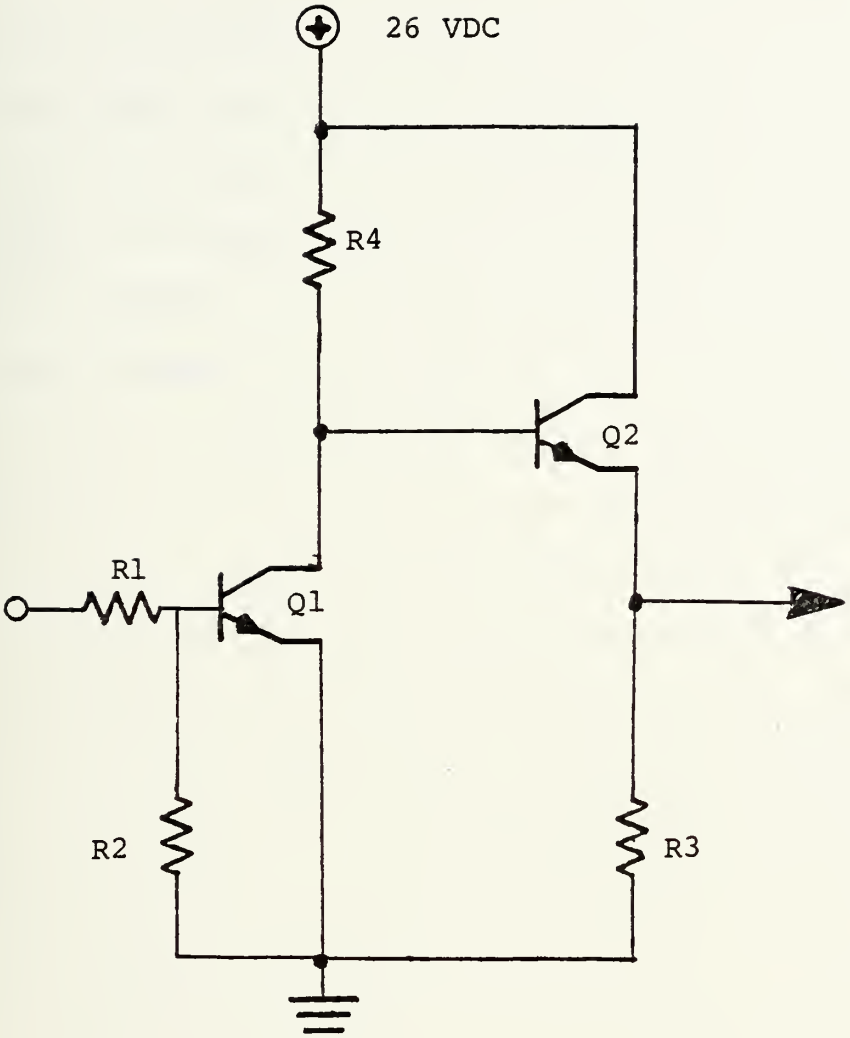


16. Control Signal Generator Functional Diagram

the monostable to control the base voltage of the first of a pair of transistors. A negative going pulse received at base one turns off Q1 causing current flow through its collector resistor to cease. This raises the base potential of the second transistor, Q2, which is configured as an emitter follower amplifier. When Q2 turns on a voltage appears across the emitter resistor equal to that of the supply voltage less the voltage drop across the transistor. In operation, the current drain into Q1 was measured at 590 microamps, well under the rated current sourcing capacity of 800 microamps of the 7404 inverter providing the signal. For input voltages greater than nine tenths of a volt the output voltage was zero. For input voltages less than nine tenths of a volt the output voltage into a one thousand ohm load was 24.9 volts at greater than fifty milliamps. The maximum current required by the 8755A is thirty milliamps, with a typical value of fifteen milliamps. These measurements were made with supply voltage to the transistor array set at 26VDC. A twenty seven volt zener diode with current limiting resistor was installed in parallel with the pulse generator in order to prevent application of excessive voltage (greater than twenty six volts) to the 8755A in the event that the supply voltage exceeds twenty seven volts through malfunction or operator error. Twenty seven volts at the supply is reduced to approximately 25.9 volts at the emitter of Q2. Each of the characteristics of the pulse generator



17. 8755A EPROM Programming Functional Diagram



18. High Voltage (VDD) Pulse Generator

18a. VDD Pulse Generator
External Components

R1 - 6.2K ohm

R2 - 10K ohm

R3 - 8.2K ohm

R4 - 5.1K ohm

Q1 - 2N3905

Q2 - 2N3905

was designed to provide adequate margin within the ratings of the 8755A to preclude damage and to make the design independent of the characteristics of the particular 2N3905 transistors installed.

6. Operating Controls and Indicators

A reset switch is provided to preload the initial state into the control signal generator and to reset the address counter to zero. The start switch provides one of four inputs to the clock enable logic. A green LED indicates when the start transfer circuitry has been enabled and a red LED indicates the completion of program transfer. In normal operation, upon power up of the PTD, the red light is on and the green light may be either on or off. The operator opens the start switch which disables the clock circuitry and turns off the green light. The reset switch is momentarily closed which loads the initial state and turns the red light off. When the start switch is closed the program transfer commences and the green light is on. Upon completion of program transfer, the red and green lights are on signalling the operator that action is complete.

7. Application of the PTD to 2716 Programming

Provision was made to permit programming of the Intel 2716 two kilobyte EPROM although such capability was not required directly during the development of the TLI system. The additional circuitry required is minor and serves only to bypass the address latch since the 2716 uses dedicated

address and data lines during programming. The 2716 is programmed differently from the 8755A in that the high voltage DC programming power is not switched, thus the Vpp input is connected directly to the input to the pulse generator serving the 8755A. The power supply must not be set higher than 26.5 volts during 2716 programming. Like the 8755A, the 2716 requires a fifty millisecond programming pulse. The TTL active high pulse is applied to the $\overline{CE}$ input and is again derived from the output of the monostable described above. This program pulse has a maximum width of fifty five milliseconds which is compatible with the requirements of the 8755A and does not call for additional circuitry. In all other respects, programming operation of the PTD is exactly the same for either 2716 or 8755A.

Zero insertion pressure (ZIP) sockets for the four EPROM stations were not available when the device was first constructed. Although operation of the circuitry was verified using standard wirewrap DIP sockets, it is desirable that ZIP sockets be installed in their place before further use of the device in order to preclude mechanical damage to the EPROMs.

VII. POWER SUPPLY REQUIREMENTS

Throughout the development of the Tank Level Indicator system and the Program Transfer Device, laboratory power supplies were used. The basic SDK-85 system claims as one of its advantages the capability to operate on a single five volt power supply. However, the addition of the input system and the RS-232C interface negated the advantage since additional positive and negative fifteen volt supplies were required by the MC1488,AD570, 8038, uA741C and LM2917N devices.

Because of the mix of relatively old and new technologies when operating both 2708 and 8755A EPROMs, the PTD requires an even broader mixture of supply voltages:

1. Positive fifteen volts.
2. Negative fifteen volts.
3. Positive twelve volts.
4. Positive twenty six volts.

With the exception of the five volt supply serving the SDK-85, the current requirements at other voltages are in all cases less than one hundred milliamps. The five volt power supply must be capable of sourcing up to 0.3 amps according to SDK-85 specification, although in actual operation the average current drain through the five volt system was less than one amp.

VIII. TLI SYSTEM SOFTWARE

The TLI system design approach was intended to first realize the hardware systems and then derive programs for the desired processes based on the hardware design. The above discussion of hardware systems provides a reference foundation for the following description of the proposed controlling algorithms.

In addition to the monitor program resident in the basic SDK-85, extensive programming was required to execute the algorithms which process the arriving raw data and control the sampling process. While the magnitude of the programs involved was not great, it was sufficient to call for mechanization wherever possible during the development stage. To this end the Tektronics 8002A was chosen as the microprocessor development system on which the bulk of programming effort was concentrated. This MDS offers a well documented text editor, sixty four kilobytes of fast memory and a dual floppy disk auxiliary memory, system emulation modes for program debugging prior to implantation in firmware, and the capability to program 2708 EPROMs from floppy disk memory. At the Naval Postgraduate School, the MDS is augmented by the Microsoft Fortran compiler described in Ref. 5, which permits the designer to use a reasonably efficient high level language to realize the algorithm rather than

laboriously coding the program directly in assembly language. The compiler converts the Fortran source program into 8080 assembly language and machine language object code compatible with the 8085 used in the TLI system. A minor disadvantage of this approach is that the 8085 interrupt mask instructions can only be used through manually inserted code. Otherwise, the only hand coding required is applied to the margins of subprograms where memory mapped addressing of SDK-85 ports or addressing of monitor routines cannot be accomplished without absolute addressing. The mechanized code is transferred to the pair of 2708 EPROMs by the MDS and thence is transferred by the Program Transfer Device described above to the user program 8755A installed in the TLI system.

A considerable amount of hand assembly is required to retrieve operands designated internally by the Microsoft compiler. These references are in most cases required to be available in the global reference pool to permit their use as subroutine entry arguments. This difficulty is a result of reliance upon the SDK-85 monitor program for delay and display functions. The alternative is to write input and output commands in Fortran and then modify the assembled version to correspond to the SDK-85 addressing system.

Each of the subprogram modules described below was tested in the MDS environment and performed satisfactorily. However, their combined operation in conjunction with the SDK-85 monitor could not be attempted in the time available because

of the further hand assembly required. A partial solution to the development problem must apparently include a method for downloading the SDK-85 monitor program to floppy disk memory, thereby permitting full program operation in the emulator environment. User access to the monitor routines themselves is also desirable for the purpose of modifying those routine.

A. MODULAR PROGRAM DEVELOPMENT

The development of processing routines naturally lends itself to modular development. The required TLI processes are:

1. Receive raw data from the ADC.
2. Time average several readings from each tank.
3. Enter reference lookup tables.
4. Execute linear interpolation.
5. Present results to the outside world.

Each module described has been constructed to permit a great deal of flexibility such that a prototype system may be expanded to cover an arbitrary number of tanks and to provide additional functions without excessive reprogramming.

The TLI program is composed of an input module which accomplishes round-robin sampling of each tank in the system until a predetermined number of samples has accumulated. The samples are time averaged and passed to a table lookup module which locates the pair of table entries which bracket

the time averaged input value and then performs a linear interpolation algorithm, returning to the main program the final value, in hundreds of gallons, of the contents of each tank. The main program then calls upon user accessible routines in the monitor to display these values. The main program also provides, through the monitor delay routine, the necessary timing which governs the interval between conversion orders sent to the ADC and control signals sent to the tank sensor chip sets.

B. INPUT MODULE 'SAMPLE'

The input subprogram named SAMPLE receives eight bit binary data from the 8155 input/output port and time averages a predetermined number of samples for each tank. The flowchart illustrates the sequence of events. After call to the module, the sample count and temporary storage locations are initialized. The first tank is read and its value stored. In sequence each of the other tanks is read until the tank counter reaches its terminal value. After each tank has been sampled the tank counter is reset, the sample counter is incremented, and the sampling process repeated. Each succeeding sample is averaged with those previously stored on an equally weighted basis and the result retained. When the sample counter reaches its terminal value, exit to the main program occurs, leaving the specified number of time averaged samples in memory for later use. The combined listing of

19. FIVE TANK TLI SYSTEM
STORED PROGRAM MEMORY REQUIREMENTS

MODULE	FPB	FDB	APB	ADP
SAMPLE	274	72	138	22
FINDIT	444	10,324	255	114
FILLTLU	226	10,257	NA	NA
MAIN	76	25	76	25
Total	1020	20,678	469	161

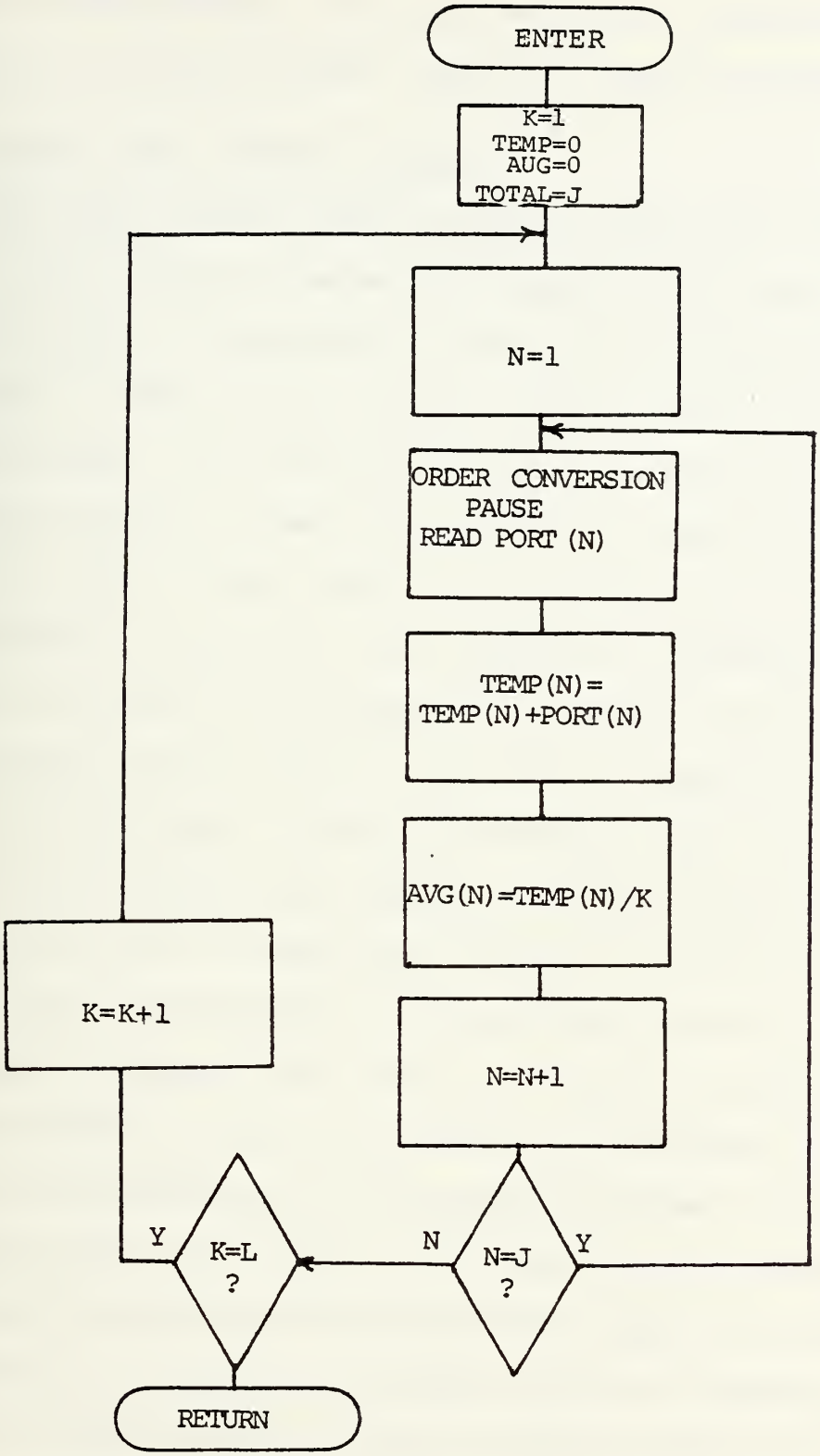
FPB-Full module size in bytes, including documentation.

FDB-Full module data (read/write memory) size, in bytes.

APB-Abbreviated module size, no documentation, single tank.

ADB-Abbreviated module data (read/write memory) size, single tank and ten pairs of tabulated data.

Note: FILLTLU is for ROM simulation only and is not required in RAM. However, a comparable block of ROM/EPROM memory is required for the operating system lookup tables.



20. Input Module Flowchart

Fortran and assembly language mnemonics in Appendix A illustrates the effect of each command on register status.

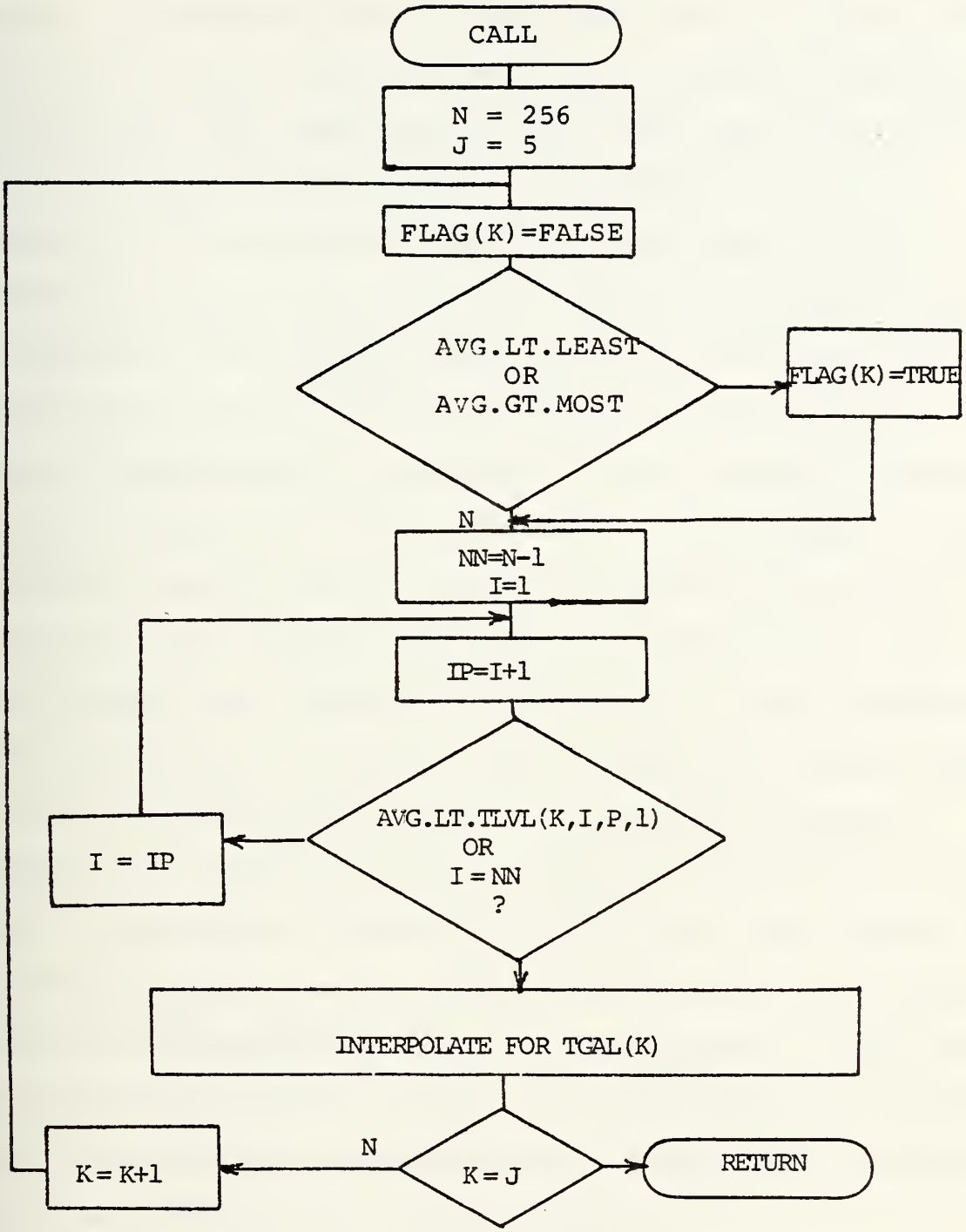
C. TABLE LOOKUP MODULE 'FINDIT'

The table lookup module operates upon those values previously stored in memory by SAMPLE as described above. The flowchart illustrates the sequence of events as suggested in Ref. 1. When called, FINDIT initializes the tank counter and proceeds, for each tank in order, to compare the time averaged value in memory with entries in read only memory lookup tables. These tables are organized as a three-dimensional array whose first dimension corresponds to the number of tanks in the system. The second and third dimensions correspond respectively to the number of recorded levels per tank and the number of entry columns per tank. For example, a five tank system would require storage of five vector pairs. The first vector in each pair contains up to two hundred fifty six values corresponding to the possible values of the eight bit word provided by the analog to digital converter. The second vector of the pair contains a like-number or fewer entries corresponding to the gallon equivalent of each recorded level, in hundreds of gallons. The routine tests the value of tank level retrieved from memory to determine whether it is outside the extreme limits of recorded values. If so, a flag is set which may be used to indicate that the interpolated value was obtained by extrapolation or may be

used to trigger high and low level alarms, if desired. Following the test, the routine does a search through vector one of the pair, the level vector, which is arranged in ascending order as described below, until a value is located which exceeds the input value. An interpolating factor is computed using the relative distance of the input value between successive table entries and this factor is applied to the adjacent entry in vector two, the gallons vector. The gallons vector is arranged in descending order because the variable capacitance sensing scheme causes the input value to decrease as tank level increases. The entries in vector two are scaled such that the output values are stored in memory in units of hundreds of gallons when exit occurs to return control to the main program. The combined listing of Fortran expressions and assembly language mnemonics in Appendix B illustrates the effect of each command on register status.

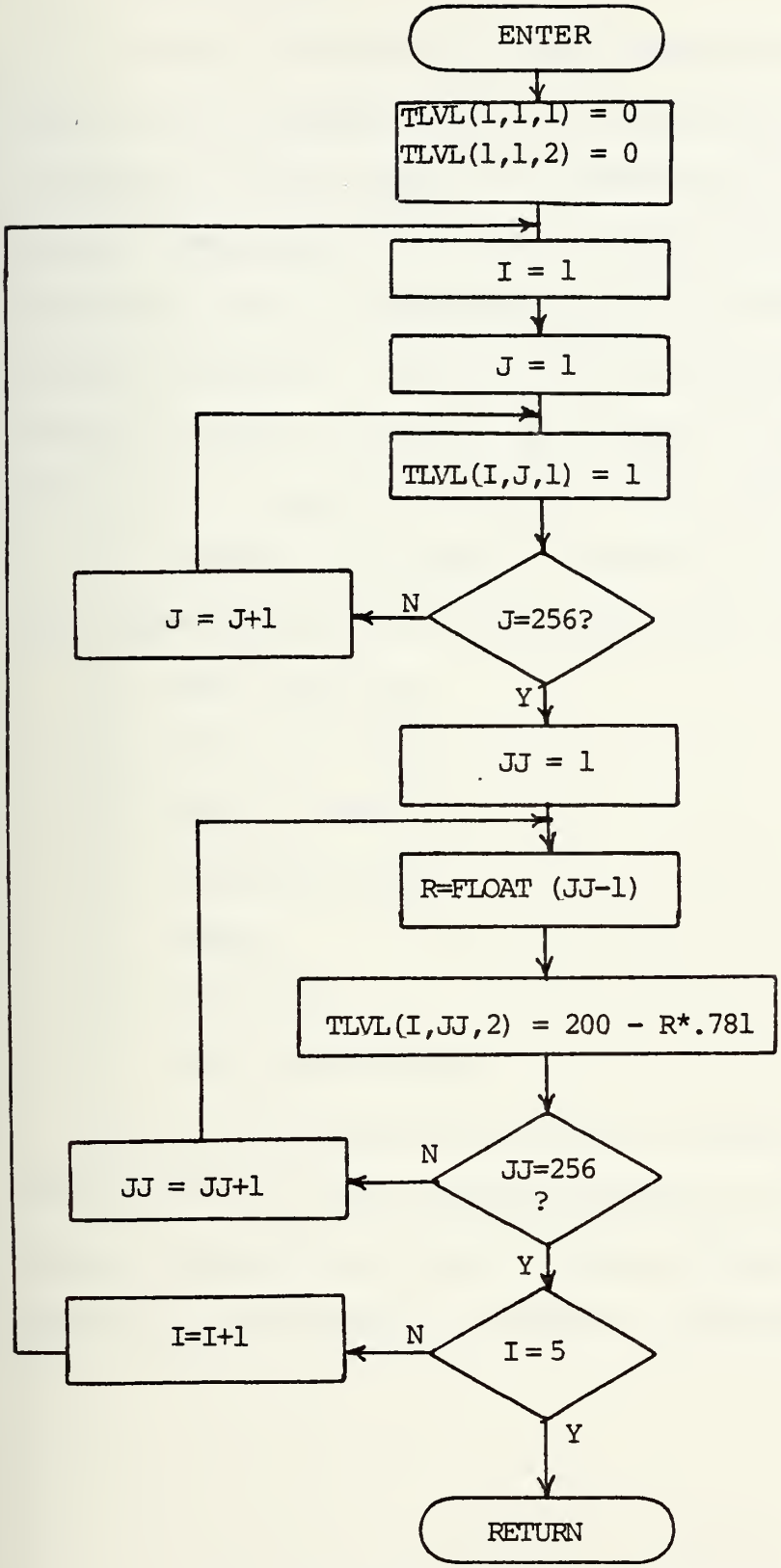
D. STORED PROGRAM TABLE GENERATOR MODULE 'FILLTLU'

Emulation of the system for debugging purposes using the 8002A requires the prestorage in memory of the tank level lookup tables. This subprogram is not required for an operational system whose tables are located in read only memory. The flowchart illustrates the sequence of events when FILLTLU is called. The routine is simply a nested set of loops which provide arbitrarily determined entries for the level and



21. Table Lookup Module Flowchart

gallons vectors for each tank hypothetically served by the system. The first vector of the first tank is filled, then the second vector is filled with scaled values corresponding to gallons. Upon completion of the first tank vector pair, the remaining tank vector pairs are defined in the same fashion. The advantage of using a large number of table entries for actual tanks is that inherent nonlinearities due to physical tank profiles may be overcome even though the interpolation routine between adjacent values is linear. This is accomplished by assigning a higher number of recorded levels to that area of the tank where a unit change in level produces a large change in gallons contained, such as near the bottom of a typical tank where the tank exterior tends to be rather more horizontal than vertical in most vessels. The higher region of the tank may be assigned a lower number of table entries spaced farther apart without excessive degradation in the interpolated results. Although development of such a set of table entries for each tank served would initially be tedious it need only be done once and then applied to corresponding tanks in other vessels of the class constructed from similar plans, with modifications required only when structural reconfiguration of the vessel so warrants. Appendix C contains the program listing.



22. Table Generator Module Flowchart

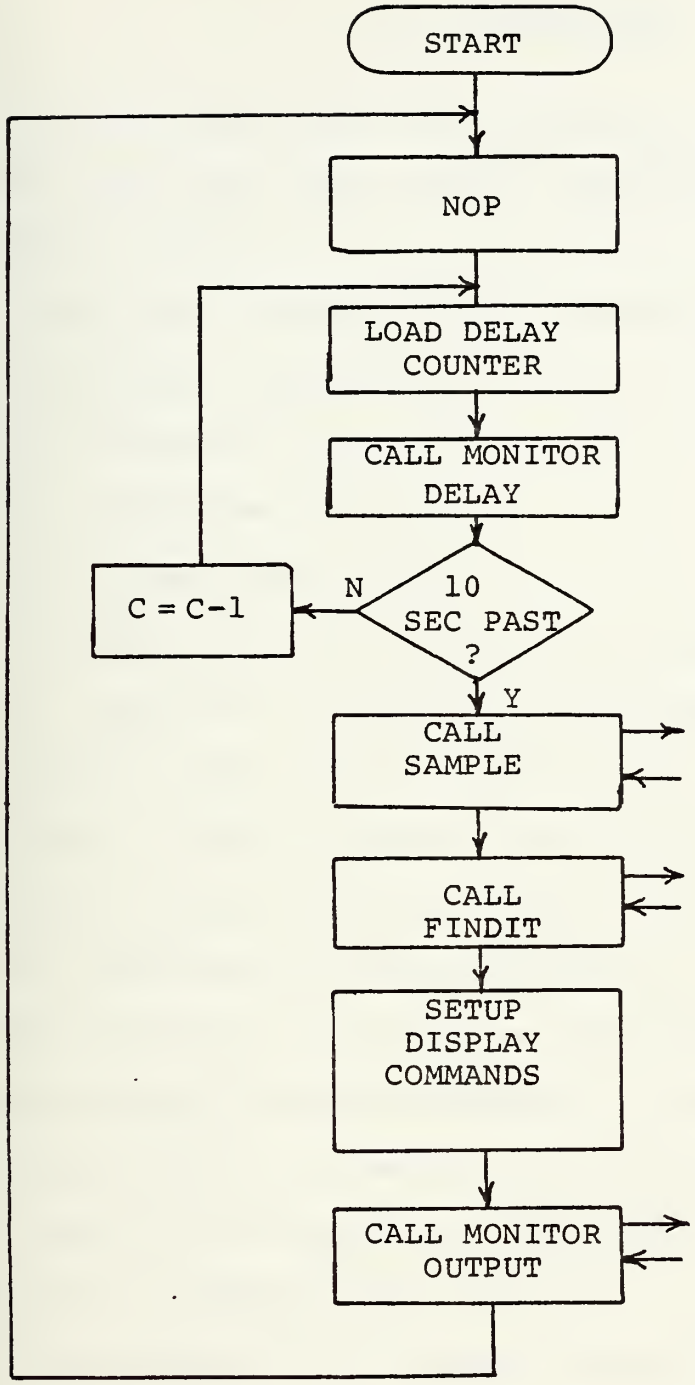
E. MAIN PROGRAM

The main program is a hand assembled management scheme which ties together the above subprograms and provides the necessary control words for activation of the data input system components. It also provides for output of the processed data by accessing the I/O routines of the SDK-85 monitor program. The flow chart illustrates the flow of events as each process is performed in sequence as an endless loop. Appendix D contains the program listing.

In the MDS environment, satisfactory operation of the individual modules described above was observed for:

1. Data sampling.
2. Time averaging.
3. Table lookup.
4. Interpolation.
5. Delay.
6. Display.
7. Table generation.

It is recommended that future efforts concentrate on manipulation of the defined variables in each module to permit proper interaction of the aggregate program while minimizing the amount of absolute addressing required.



23. Main Program Flowchart (Single Tank Operation)

IX. CONCLUSION

The prototype Tank Level Indicator system described herein was a dual path project consisting of hardware and software sections.

Development of the hardware section required:

1. Concept definition.
2. Component selection.
3. Subsystem design.
4. System construction.
5. Simulation and testing of subsystems.
6. Operation of combined subsystems.

Each of these project elements has been described above in detail. The logic paths for concept definition and component selection were reviewed, followed by evaluations of the performance of each subsystem. The proposed input system was shown to function as specified, within the limits of the sensor simulation employed. Further testing of the hardware system is dependent upon satisfactory reduction of the controlling algorithms to the point where they may be committed to EPROM memory storage.

Development of the software section required:

1. Identification of hardware processes receiving program control.
2. Identification of the supporting functions required to generate usable information from data.

3. Organization of algorithms to realize each of the supporting functions.
4. Coding of each algorithm into 8085A compatible language.
5. Validation of each coded algorithm to ensure proper operation.

Final development of the software section was necessarily limited by available time so that only the overall concept and module development were attempted. Each of the sub-program modules was shown to be operational in the MDS environment. Further development is required to combine the several modules and the SDK-85 monitor program into a fully functional entity.

X. RECOMMENDATIONS

Recommendations for further development effort address system complexity, subsystem performance, software refinement and a suggestion for prototype development.

A. SYSTEM COMPLEXITY

The rudimentary system as described herein is over complex for the limited task of sampling a single tank, however, the logical extension of the system to serve the large number of tanks in a typical system may be realized with very little additional complexity. With additional development of the control logic needed to bring these additional tanks into the system, the microcomputer TLI system becomes a cost effective and attractive alternative to the systems currently employed.

B. SUBSYSTEM PERFORMANCE

Each of the subsystems described above performed as intended after the initial setup and calibration were accomplished. The complete tank level indicator system was not, however, subjected to a rigorous testing program, due in part to delays in component procurement, software development and lack of a suitable test platform in which to install the prototype version of the TLI system. It is recommended that the single tank system be subjected to laboratory testing with emphasis on tank probe selection and display methods.

C. SOFTWARE

In addition to the requisite hand assembly described above, there exists a wide variety of improvements which might be appended to the basic algorithms proposed herein. Development of additional functional capabilities for the TLI microcomputer would certainly improve its usefulness and would more fully employ the capabilities inherent to the system. Addition of programming and display hardware to provide remote presentation of data at monitoring stations throughout the vessel is a desirable feature when viewed from the standpoint of damage control information flow. Software routines to accomplish accounting and bookkeeping functions related to liquid stores management may be added to automate the inventory control and consumption rate calculations now accomplished manually. Reference 6 provides several insights leading to compact realizations of the necessary algorithms. Memory expansion to accommodate these additional functions may be achieved without significant alteration to the hardware of the basic system, as outlined in Ref. 3.

After suitable laboratory verification it is recommended that a prototype system be constructed and packaged for at sea evaluation as a functioning unit aboard an active vessel or perhaps aboard the Naval Postgraduate School Research Vessel ACANIA.

APPENDIX A

INPUT MODULE PROGRAM LISTINGS

```
    SUBROUTINE SAMPLE
TITLE:  SAMPLE
 355+100DATA BYTES AS PRINTED HERE WITH COMMENTS.
WITHOUT VERBAGE LENGTH IS 291 PROGRAM + 72 DATA BYTES.
THIS SUBROUTINE DEVELOPS A 1 X J ARRAY OF TIME AVERAGED INPUTS.
THS ARRAY'S NAME IS AVG.  J IS NUMBER OF TANKS TO BE SAMPLED.
L IS NUMBER OF SAMPLES PER TANK, TO BE DETERMINED BASED
ON SYSTEM SERVICED BY MAIN. FOR TEST PURPOSES LET J=5 AND L=10.

INITIALIZE AND DIMENSION

TANKS ARE SAMPLED ROUND ROBIN
     MVI       A,02     ;
     OUT       20H      ;PROGRAM THE 8155A CSR
     MVI       A,01     ;SEND PULSE TO LSB OF 8155 PORT B
     OUT       22       ;THENCE TO AD570 BL/CONV NOT LINE
     XRA       A        ;KILL 2.6 USEC THEN
     NOP                ;
     OUT       22       ;RESET PULSE TO START CONVERSION
     LXI       D,6      ;SET UP FOR 30 SEC DELAY
     CALL      DELAY    ;USING MONITOR ROUTINE
                        ;AND PROCEED

     DIMENSION TEMP(5), PORT (5), AVG(5)
     INTEGER PORT
     L=10
     K=1
     J=5
     DO 10 I=1,5
     LXI       H,000A
     SHLDL
     LXI       H,0001
     SHLIK
     LXI       H,0005
     SHLIJ
     TEMP(I)=0.0
     LXI       H,0001
     SHLDI
10   AVG(I)=0.0
     LHLDI
     DAD       H
     DAD       H
     LXI       D,TEMP 0004
     DAD       D
     SHLDT:000000
```

```
      LXI       H ,[     00       00       00 ]
      CALL$L1
      LHLIT:000000
12    N=1
      LHLDI
      DAD       H
      DAD       H
      LXI       D,AVG-0004
      DAD       D
      SHLDT:000000
      LXI       H, [     00       00       00 ]
      CALL$L1
      LHLDT:000000
      CALL$T1
      LHLDI
      INX       H
      MVI       A,05
      SUB       L
      MVI       A,00
      SBB       H
      JP0015
THE DATA IS READ IN FROM LOW 8155 PORT A
AFTER CONVERSION HAS BEEN ORDERED AND 30 USEC PASS
14    READ(1,21)PORT(N)
      LXI       H,0001
      SHLIN
      LXI       D 21L
      LXI       H, [     01       00 ]
      CALL$R2
21    FORMAT(I3)
      LHLIN
      DAD       H
      LXI       D PORT-0002
      DAD       D
      SHLDT:000000
      LHLDT:000000
      XCHG
      LXI       H, [     01       00 ]
      MVI       A,02
      CALL$I0
      CALL$ND
ACCEPTABLE VALUES OF PORT(N) ARE 0 THRU 255
AS RECEIVED FROM THE 8 BIT ADC FROM PORT(N)
      TEMP(N)=TEMP(N)-PORT(N)
      AVG(N)=TEMP(N)/K
MIXED MODE ARITHMETIC INTENTIONAL
      N=N-1
      IF(N.LE.J) GO TO 14
      LHLDN
      DAD       H
      DAD       H
```

```
      SHLDT:000000
      LXI       D,TEMP-0004
      DAD       D
      SHLDT:010000
      LHLDN
      DAD       H
      LXI       D PORT-0002
      DAD       D
      MOV       A,M
      INX       H
      MOV       H,M
      MOV       L,A
      CALL$CA
      LHLDT:010000
      CALL$AB
      LHLDT:010000
      CALL$T1
      LHLDT:000000
      LXI       D, AVG-0004
      DAD       D
      SHLDT:020000
      LHLDT:010000
      CALL$D1
      LHLDK
      CALL$DA
      LHLDT:020000
      CALL$T1
      LHLDN
      INX       H
      SHLDN
      XCHG
      LHLDJ
      MOV       A,E
      SUB       L
      MOV       L,A
      MOV       A,D
      SBB       H
      MOV       H,A
      MOV       A,L
      RLC
      ORA       L
      ANI7F
      ORA       H
      ICR       A
      ADI81
      SBB       A
      STAT:000002
30    CONTINUE
      ORA       A
      JNZ14L
      F=K+1
```

```
      IF(K.GT.L) GO TO 40
      LHLDK
      INX       H
      SHLDK
      XCHG
      LHLDL
      MOV       A,E
      SUB       L
      MOV       L,A
      MOV       A,D
      SBB       H
      MOV       H,A
      MOV       A,D
      RLC
      ORA       L
      ANI7F
      ORA       H
      DCR       A
      SUI7F
      SBB       A
      STAT:000002
      GO TO 12
      ORA       A
      JNZ40L
 40   CONTINUE
      JMP12L
      RETURN
      RET
      END


     SUBROUTINE SAMPLE
      MVI       A,02      ;
      OUT       20H       ;
      MVI       A,01      ;
      OUT       22        ;
      XRA       A         ;
      NOP                 ;
      OUT       22        ;
      LXI       D,6       ;
      CALL      DELAY     ;
      L=10
      K=1
      J=0
      A=0.0
 14   READ(L,21)I
      LXI       H,000A
      SHLDL
      LXI       H,0001
      SHLIK
```

```
      LXI       H,0000
      SHLDJ
      LXI       H, [      00        00        00        00 ]
      CALL$L1
      LXI       H,A
      CALL$T1
      LXI       D,21L
      LXI       H, [      01        00 ]
      CALL$R2
21    FORMAT(I3)
      LXI       D,I
      LXI       H, [      01        00 ]
      MVI       A,02
      CALL$I0
      CALL$ND
      J=J+I
      A=FLOAT(J)/FLOAT(K)
      K=K+1
      IF(K.GT.L) GO TO 40
      LHLDI
      XCHG
      LHLDJ
      DAD       D
      SHLDJ
      LXI       H,K
      CALLFLOAT
      LXI       H,T:000001
      CALL$T1
      LXI       H,J
      CALLFLOAT
      LXI       H,T:000001
      CALL$DB
      LXI       H,A
      CALL$T1
      LHLDK
      INX       H
      SHLDK
      XCHG
      LHLDL
      MOV       A,E
      SUB       L
      MOV       L,A
      MOV       A,D
      SBB       H
      MOV       H,A
      MOV       A,L
      RLC
      ORA       L
      ANI7F
```

```
      ORA       H
      DCR       A
      SUI7F
      SBB       A
      STAT:000002
      GO TO 14
      ORA       A
      JNZ40L
40    CONTINUE
      JMP14L
      RETURN
      RET  —
      END
```

APPENDIX B

TABLE LOOKUP MODULE PROGRAM LISTINGS

```
TITLE:  FINDIT
TABLE LOOKUP AND LINEAR INTERPOLATION ROUTINE
AVG IS THE 1 BY J INPUT VECTOR WHERE J IS THE NUMBER OF
TANKS TO BE SAMPLES.  AVG IS DERIVED BY THE SAMPLE SUBROUTINE.
LET J=5 FOR TEST PURPOSES.  THE SECOND DIMENSION OF TLVL
IS THE NUMBER OF TABULATED LEVELS PER TANK IN MEMORY 256.
A DATA FILE MUST BE CREATED BEFORE RUNNING THIS MODULE
OR EXIST IN SYSTEM HIGH 8755 READ ONLY MEMORY
     DIMENSION TLVL (5 256,2), TGAL(5), AVG(5)
     LOGICAL FLAG(5)
     N=256
N IS NUMBER OF TAB  LEVELS PER TANK
     J=5
     DO 40 K=1,J
     LXI      H,0100
     SHLDN
     LXI      H,0005
     SHLDJ
     FLAG(K) .FALSE.
     LXI      H.0001
     SHLDK
     IF(AVG(K).LT.TLVL(K,1,1), OR.AVG(K).GT.TLVL(K,N,1))FLAG(K)=.TRUE.
     LHLDK
     LXI      D FLAG-0001
     DAD      D
     SHLDT:000000
     XRA      A
     LHLDT:000000
     MOV      M,A
     LHLDK
     DAD      H
     DAD      H
     SHLDT:010000
     LXI      D,AVG-0001
     DAD      D
     SHLDT:010000
     LXI      D,TLVL-0004
     DAD      D
     SHLDT:030000
     LHLIN
     XCHG
     LXI      H,0014
     CALL$M9
     XCHG
     LHLDT:010000
```

```
      DAD     D
      LXI     DMTLVL-0016
      DAD     D
      SHLDT:040000
      LHLDT:020000
      CALL$L1
      LHLDT:040000
      CALL$SB
      DCR     A
      SUI7F
      SBB     A
      STAT:000002
      LHLDT:020000
      CALL$L1
      LHLDT:030000
      CALL$SB
      RAL
      SBB     A
      LXI     H,T:00002
      ORA     M
      STAT:010002
      ORA     A
      JZ0000
      NN=N-1
      LHLDK
      LXI     D,FLAG-0001
      DAD     D
      SHLDT:000000
      MVI     A,FF
      LHLDG:000000
      MOV     M,A
      I=1
28    IP=I+1
      LHLDN
      DCX     H
      SHLDNN
      LXI     H,0001
      SHLDI
      IF AVG K .LT.TLVL(K,IP,1) .OR.I.GE.NN) GO TO 32
      LHLDI
      INX     H
      SHLDIP
      LHLDK
      DAD     H
      DAD     H
      SHLDT:000000
      LXI     D,AVG-0004
      DAD     D
      SHLDT:010000
      LHLDIP
      XCHG
      LXI     H,0014
```

```
     CALL$M9
     XCHG
     LHLDT:000000
     DAD      D
     LXI      D TLVL-0018
              DAD        D
     SHLDT:020000
     LHLDI
     XCHG
     LHLDNN
     MOV      A,E
     SUB      L
     MOV      L,A
     MOV      A,D
     SBB      H
     MOV      H,A
     MOV      A,L
     RLC
     ORA      L
     ANI7F
     ORA      H
     RAL
     CMC
     SBB      A
     STAT:000000
     LHLDT:010000
     CALL$L1
     LHLDT:020000
     CALL$SB
     RAL
     SBB      A
     LXI      H,T:000002
     ORA      M
     STA:010002
     I=IP
     ORA      A
     JNZ32L
     GO TO 28
     LHLDIP
     SHLDI
32   TINC=(AVG(K)-TLVL K,I 1 )/(TLVL K,IP 1)-TLVL K,I 1 )
     JMP28L
     TGAL(K)=TLVL(K,I,2)+TINC* TLVL(K IP,2)-TLVL K,I 2))

LINEAR INTERPOLATION

40   CONTINUE
     LHLDK
     DAD      H
     DAD      H
```

```
SHLDT:000000
LXI     D AVG-0004
DAD     D
SHLDT:010000
LHLDI
XCHG
LXI     H,0014
CALL$M9
XCHG
LHLDT:000000
DAD     D
SHLDT:020000
LXI     D TLVL -0018
DAD     D
SHLDT:030000
LHLDIP
XCHG
LXI     H,0014
CALL$M9
XCHG
LHLDT:000000
DAD     D
SHLDT:040000
LXI     D TLVL 0018
DAD     D
CALL$L1
LHLDL:030000
CALL$SB
LXI     H T:000001
CALL$T1
LHLDT: 030000
CALL$L1
LHLDT:010000
CALL$SB
LXI     H T:000001
CALL#SB
CALL$NB
LXI     H TINC
CALL$T1
LHLDT:000000
LXI     D TGAL 0004
DAD     D
SHLDT:050000
LHLDT:020000
LXI     D,TLVL+13E8
DAD     D
SHLDT:060000
LHLDT:040000
LXI     D,TLVL+13E8
DAD     D
```

```
      SHLDT:070000
      LHLDT:020000
      LXI     D,TLVL+13E8
      DAD     D
      SHLDT:070000
      LHLDT:020000
      LXI     D,TLVL+13E8
      DAD     D
      CALL$L1
      LHLDT:070000
      CALL$SB
      LXI     H,TINC
      CALL$MB
      LHLDT:060000
      CALL$SB
      CALL$NB
      LHLDT:050000
      CALL$T1
FLAG TRUE WARNS THAT TGAL WAS EXTRAPOLATED PAST TABLE LIMITS
TGAL IS TANK CONTENT IN HUNDREDS OF GALLONS.
ABBREVIATED FORM OF THIS SUBROUTINE WILL BE CALLED BY MAIN
TO OPERATE ON INPUT PROVIDED BY SAMPLE.
      RETURN I.HLDK
      INX     H
      XCHG
      LHLDJ
      XCHG
.     MOV     A,E
      SUB     L
      MOV     A,L
      SBB     H
      JP000F
      RET
      END
PROGRAM UNIT LENGTH 01BC   444   Bytes
DATA AREA LENGTH=2854 (10324) Bytes


SUBROUTINE FINDIT
 DIMENSION T(10,2)
      LOGICAL F
      F=.FALSE.
      IF(A.LT.T(1,1).)R.A.GT.T(10,1))F=.TRUE.
      XRA     A
      STAF
      LXI     H,A
      CALL$L1
      LXI     H,T+0024
      CALL$SB
      DCR     A
```

```
      SUI7F
      SBB     A
      STAT:000002
      LXI     H,A
      CALL$L1
      LXI     H,T
      CALL$SB
      RAL
      SBB     A
      LXI     H,T=000002
      ORA     M
      STAT:010002
      ORA     A
      JZ0000
      I=1
      MVI     A FF
      STAF
 28   IP=I+1
      LXI     H,0001
      SHLDI
      IF A.LT.T(IP,1).OR.I.GE.9) GO TO 32
      LHLDI
      INX     H
      SHLDIP
      DAD     H
      DAD     H
      LXI     L T-0004
      DAD     D
      SHLDT:000000
      LHLDI
      LXI     D,FFF7
      DAD     D
      MOV     A,L
      RLC
      ORA     L
      ANI7F
      ORA     H
      RAL
      CMC
      SBB     A
      STAT:000002
      LXI     H A
      CALL$L1
      LHLDT:000000
      CALL$SB
      RAL
      SBB     A
      LXI     H T:000002
      ORA     M
      STAT:010002
      I=IP
```

```
     ORA      A
     JNZ32L
     GO TO 28
     LHLDIP
     SHLDI
32   C=(A-T(I,1))/(T(IP,1))-T(I,1)
     JMP28L
     G=T(I,2)+C*(T(IP,2)-T(I,2))
     RETURN
     LHLDI
     DAD      H
     DAD      H
     SHLDT:000000
     LXI      D T-0004
     DAD      D
     SHLDT:010000
     LHLDIP
     DAD      H
     DAD      H
     SHLDT:020000
     LXI      D T-0004
     DAD      D
     CALL$L1
     LHLDT:010000
     CALL$SB
     LXI      H,T:000001
     CALL$T1
     LHLDT:010000
     CALL$L1
     LXI      H.A
     CALL$SB
     LXI      H,T:000001
     CALL$DB
     CALL$NB
     LXI      H,C
     CALL$T1
     LHLDT:000000
     LXI      D,T+0024
     DAD      D
     SHLDT:030000
     LHLDT:020000
     LXI      D,T+0024
     DAD      D
     SHLDT:040000
     LHLDT:000000
     LXI      D,T+0024
     DAD      D
     CALL$L1
     LHLDT:040000
     CALL$SB
```

```
      LXI     H,C
      CALL$MB
      LHLDT:030000
      CALL$SB
      CALL$NB
      LXI     H,G
      CALL$T1
      RET
      END

PROGRAM UNIT LENGTH=00FF  255  BYTES
DATA AREA LENGTH=0072 (114) BYTES
```

APPENDIX C

TABLE GENERATOR MODULE PROGRAM LISTING

```
TITLE:  FILLTLU
FILL THE TABLE FOR TANK #1 WITH A HYPOTHETICAL
SET OF VALUES AND THEN DUPLICATE FOR TANKS 2 THRU 5
TO GET A MEASURE OF MEMORY REQUIRED FOR LOOKUP TABLES
     DIMENSION TLVL(5,256,2)
     TLVL(I,J,1)=0.
     LXI     B,$$L
     JMP$INIT
     TLVL(1,1,2)=0.
     DO 30 I=1,5
     LXI     H,[       00        00        00        00 ]
     CALL$L1
     LXI     H, TLVL
     CALL$T1
     LXI     H,[       00        00        00        00 ]
     CALL$L1
     LXI     H TLVL 1400
     CALL$T1
     DO 10 J=1,256
     LXI     H 0001
     SHLDI
     TLVL(I,J,1)-J
     LXI     H 0001
     SHLDJ
10   CONTINUE
     LHLDI
     DAD     H
     DAD     H
     SHLDT:000000
     LHLDJ
     XCHG
     LXI     H,0014
     CALL$M9
     XCHG
     LHLDT:000000
     DAD     D
     LXI     D,TLVL-0018
     DAD     D
     SHLDT:010000
     LHLDJ
     CALL$CA
     LHLDT:010000
     CALL$T1
     DO 20 JJ=i,256
```

```
     LHLDJ
     INX     H
     MVI     A,00
     SUB     L
     MVI     A,01
     SBB     H
     JP0027
     R=FLOAT(JJ-1)
     LXI     H,0001
     SHLDJJ
     TLVL(I,JJ,2)=200.-R*0.781
NOMINAL 20KGAL TANK DB 256 DB 100 GIVES SCALE FACTOR  781
FILL COLUMN TWO WITH LARGEST VALUE FIRST THEN DECREASING
BECAUSE PROBE CAPACITANCE DECREASES AS LEVEL INCREASES.
20   CONTINUE
     LHLDJJ
     DCX     H
     SHLDT:000000
     LXI     H,T:000000
     CALLFLOAT
     LXI     H,R
     CALL$T1
     LHLDI
     DAD     H
     DAD     H
     SHLDT:010000
     LHLDJJ
     XCHG
     LXI     H,0014
     CALL$M9
     XCHG
     LHLDT:010000
     DAD     D
     LXI     D,TLVL=13E8
     DAD     D
     SHLDT:020000
     LXI     H, [       9D       FF       47       90 ]
     CALL$L1
     LXI     H R
     CALL$MB
     LXI     H, [       00       00       48       88 ]
     CALL$SB
     CALL$NB
     LHLDT;020000
     CALL$T1
30   CONTINUE
     LHLDJJ
     INX     H
     MVI     A,00
     SUB     L
```

```
     MVI     A 01
     SBB     H
     JP0064
THIS MODULE IS A TEST DEVICE ONLY AND WILL EVENTUALLY
BE REPLACED BY EPROM LOOKUP TABLE OF APPROPRIATE DIMENSION.
     STOP
     LHLDI
     INX     H
     MVI     A 05
     SUB     L
     MVI     A 00
     SBB     H
     JP0021
     CALL$ST
     END

PROGRAM UNIT LENGTH 00E2  226 BYTES
DATA AREA LENGTH 2811  10257  BYTES.
```

APPENDIX D

MAIN PROGRAM LISTING

```
        ;TANK LEVEL INDICATOR SYSTEM MAIN
        ;PROGRAM USES INPUT MODULE SAMPLE,
        ;TABLE LOOKUP MODULE FINDIT,SDK-85
        ;MONITOR ROUTINE DELAY AND MONITOR
        ;ROUTINE OUTPT.
MAIN    NOP                         ;
LOOP1   MVI     C.1DH               ;LOAD DELAY COUNTER FOR 29 ITERATIONS
LOOP2   LXI     D,0FFFFH            ;SET DELAY FOR MAX TIME
        CALL    DELAY               ;
        DCR     C                   ;
        CPI     C,0                 ;IF TEN SECONDS ELAPSE GO ON ELSE AGAIN
        JNZ     LOOP2               ;
        CALL    SAMPLE              ;GET A VALUE
        CALL    FINDIT              ;INTERPOLATE AFTER TABLE LOOKUP
        XRA     A                   ;SET UP FOR DISPLAY OF GALLONS X 100
        MOV     B,A                 ;
        LXI     H,DATA              ;DATA IS START OF TWO BYTE DATE AT TOP OF

        CALL    OUTPT               ;RAM MONITOR ROUTINE GETS IT TO SDK-85
        JMP     LOOP1               ;DISPLAY GO BACK FOR ENDLESS LOOP
                                    ;
DELAY   EQU     05F1H               ;ADDRESSES MUST BE COORDINATED WITH SUB
SAMPLE  EQU     0800H               ;ROUTINE ALLOCATIONS
FINDIT  EQU     0A00H               ;
DATA    EQU     28F0H               ;
        END
```

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Thesis
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A microprocessor managed shipboard tank level indicator system.