A VOLTAGE SQUARING CIRCUIT

and

ANALOG TO DIGITAL CONVERTER

for

PULSED SYSTEMS

by

LT. PAUL EDWARD PAKOS, USCG

S.M. THESIS   MAY, 1965

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S. B., U. S. Coast Guard Academy

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Submitted to the Department of Electrical Engineering on 26 May 1965 in partial fulfillment of the requirements for the degree of Master of Science.

ABSTRACT

An accurate, wideband, voltage squaring circuit suitable for use aboard a spacecraft has been designed, built, and evaluated. The device is based upon the theory of piecewise linear synthesis.

A relatively simple scheme for converting analog information to digital form has been fully developed and partially evaluated. It is particularly suited for pulsed systems where the duration between pulses is such that very rapid conversion is not necessary.

Thesis Supervisor: J. F. Reintjes

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I wish to express appreciation for the encouragement and
technical assistance afforded me by all of the group members of the
Venus Spacecraft Radar Project.

Paul E. Pakos

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CHAPTER I

Development of Specifications

I.A. Introduction

A spacecraft radar system is being developed to gather sufficient

information to construct a gross reflectivity map of a planet's surface.

In order to accomplish this goal, it is necessary to compare the energy

transmitted to the energy received. Because the energy in the received

voltage signal, e(t), is proportional to $\int_{-\infty}^{+\infty} e^2(t)\,dt$, it is necessary

to square the signal prior to the integration process. (2)

Since it is desirable to accomplish the data processing aboard

the spacecraft, it is also necessary to convert the information to

digital form in order to telemeter the data to ground control stations.

The body of this report deals with a squaring circuit which

satisfies the system requirements. It has been constructed and evalu-

ated, and performance data appear in Chapter IV. A detailed study of

the problem of conversion to digital form has also been made and appears

as an appendix. Included are circuit diagrams and data obtained from

prototype components.

I.B. System Requirements

The transmitted signals consist of a series of four bursts of r-f

pulses, 1 msec in duration and spaced 20 msec apart, the series of bursts

being separated by 15 seconds. Refer to Fig. I.1. This timing allows

the received echoes to arrive during the time interval between bursts.

Due to doppler shifts, frequency spreading, and pulse length

spreading, the echo resulting from any one of the series of bursts may

appear anywhere within a very wide spectrum and may be as long as 4 msec
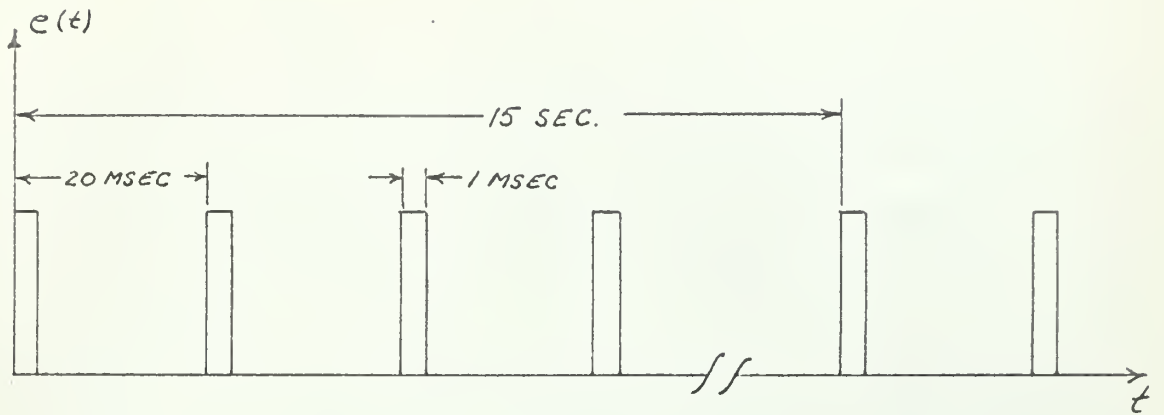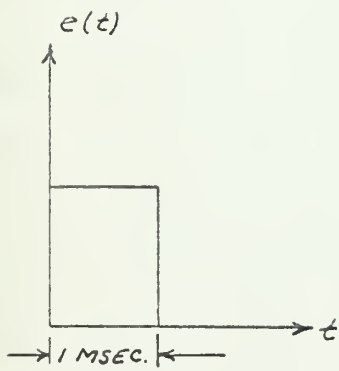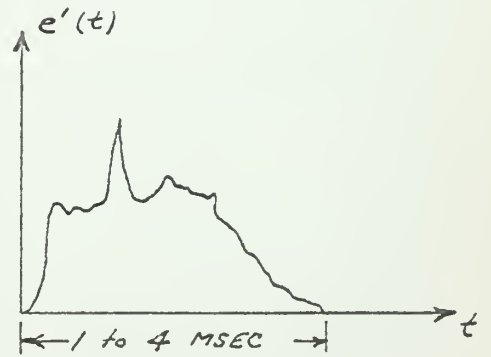
FIG. I.1. TRANSMITTED SIGNAL

a) TRANSMITTED PULSE

b) RECEIVED PULSE

FIG. I.2. COMPARISON OF TRANSMITTED AND
RECEIVED PULSE SHAPES

in duration. This signal will be processed through a set of band pass

filters which covers the appropriate frequency spectrum with overlapping

pass bands, each filter being 100 kc wide. After leaving the band pass

filter, the echo will be envelope detected, and it is this envelope

which will be squared and integrated to determine the energy in the

received signal.[2]

The signal to be squared will probably only vaguely resemble the

square pulse transmitted. See Fig. I.2. However, the actual shape of

the envelope of the received pulse is unimportant as long as the dura-

tion and frequency components are known. Referring to Fig. I.3, note

that the output of the filter bank will be a signal which has a band-

width of no more than 100 kc. Since an envelope detector is a non-

linear device, one cannot specify its characteristics in the frequency

domain, but it can be qualitatively stated that the effect of envelope

detection is to eliminate the carrier f_c' and to leave only the side-

bands centered about zero frequency. Hence, the envelope displayed in

Fig. I.2(b) will never contain components greater than 50 kc.

The input and output signal levels of the squaring circuit are

based upon the accuracy desired, the limitations of the components used,

and convenience. As discussed in Chapter II, an appropriate input signal

level is 0 to 10 volts with a function generation of $e_{out} = (1/10)e_{in}^2$.

It is obviously desirable to keep the errors as small as possible.

Specifically, it is desired to keep the errors down to 1% or less over

the major portion of the operational range of the circuit.

The fact that the entire device is to be placed in a spacecraft

imposes the additional requirements of low power, light weight, and
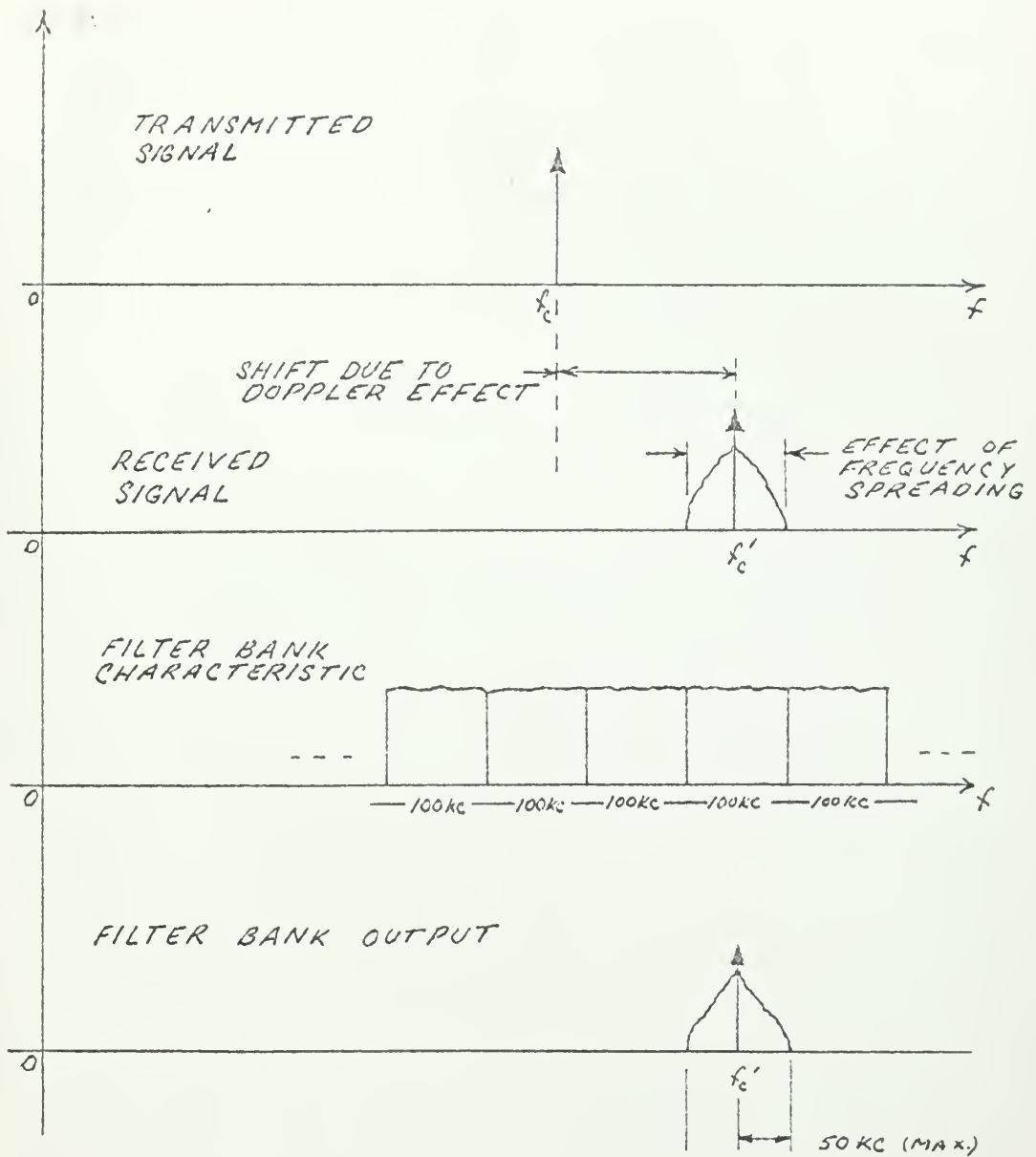
FIG.I.3. FREQUENCY DOMAIN REPRESENTATION OF SIGNAL PROCESSING

thermal insensitivity.

Summarizing, the problem is to build a squaring circuit which meets the following specifications:

(a) Input signal level: 0 to 10 volts

(b) Function generation: $e_{out} = (1/10) e_{in}^2$

(c) Allowable error: no more than 1% over major portion of the operational range

(d) Bandwidth: 0 to 50 kc

(e) Light Weight

(f) Low power consumption

(g) Thermal Insensitivity: Operational over a range of $-25^{\circ}C$ to $+75^{\circ}C$

CHAPTER II

Squaring Circuit Design

II.A. Theory of Piecewise Linear Synthesis

An examination of components and devices having a square law
characteristic showed all to be inadequate for this application. It
was therefore decided that the best way to generate the desired quad-
ratic was by piecewise linear circuit synthesis.

Numerical Analysis techniques indicate that any curve can be
approximated by piecewise linear methods. Refer to Fig. II.1.

The method of approximation shown is that which yields the least
mean square error. For a quadratic, the least mean square error exists
when:[3]

(1) Equal segments are taken along the x axis.

(2) The slope of the linear approximation equals the slope at
     the midpoint of the curve.

(3) Each linear approximation passes through a point $\Delta h^2/12$
     above the midpoint of the curve, where Δh equals the length
     of the segment on the x axis.

In order to have reasonable input and output values consistent
with high accuracy, it was decided to generate the function $y = 1/10\ x^2$,
where x will take on any value between 0 and 10 volts. It was decided
to use twelve segments to perform the approximation. This corresponds
to a theoretical maximum error of 0.07 volt and a theoretical rms error
of 0.027 volt. In consequence of applying the least mean square error
criteria to this specific problem, the resultant slopes and breakpoints
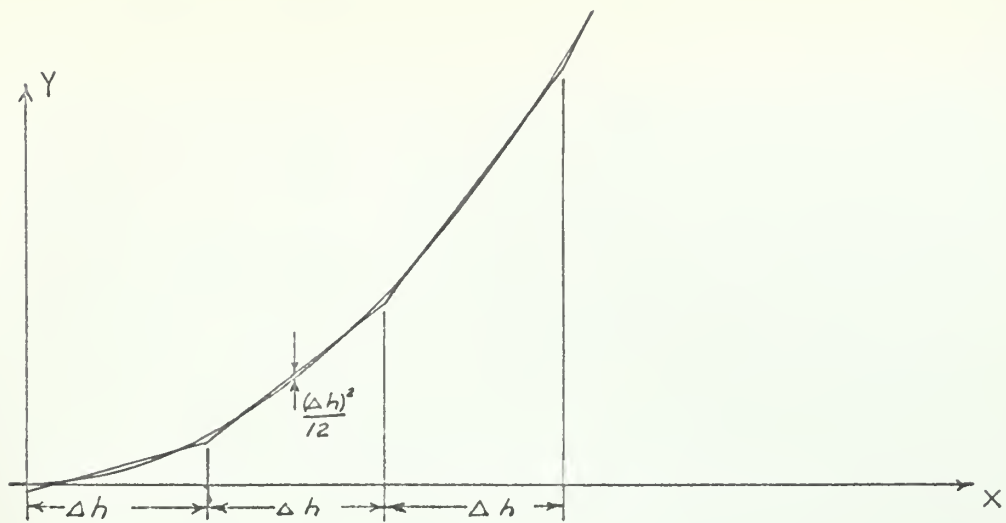have been tabulated in Fig. II.2.

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FIG. II.1. APPROXIMATING A CURVE BY LINEAR SEGMENTS

Segment	Input Range (Volts)	Slope of Curve at Midpoint	Output Range (Volts)	Optimum Midpoint of Output Voltage
1	0.000 - 0.833	0.083	0.000 - 0.069	0.023
2	0.833 - 1.667	0.250	0.069 - 0.278	0.162
3	1.667 - 2.500	0.416	0.278 - 0.625	0.440
4	2.500 - 3.333	0.583	0.625 - 1.111	0.856
5	3.333 - 4.167	0.750	1.111 - 1.736	1.412
6	4.167 - 5.000	0.916	1.736 - 2.500	2.106
7	5.000 - 5.833	1.083	2.500 - 3.402	2.939
8	5.833 - 6.667	1.250	3.402 - 4.444	3.912
9	6.667 - 7.500	1.416	4.444 - 5.625	5.023
10	7.500 - 8.333	1.583	5.625 - 6.944	6.273
11	8.333 - 9.167	1.750	6.944 - 8.403	7.662
12	9.167 - 10.000	1.916	8.403 - 10.000	9.190

FIG. II.2. REQUIRED SLOPES AND BREAKPOINTS TO APPROXIMATE $Y = (1/10) X^2$ WITH LINEAR SEGMENTS

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The rigid application of the table of Fig. II.2 to an actual circuit would require a small negative voltage at the output while the input was zero. (Refer again to Fig. II.1 to see this graphically.) This is undesirable, so the actual approximation used should start exactly at the origin. This small shift will naturally introduce a small error, but, as will be pointed out in Chapter IV, the non-ideal characteristics of the diodes employed in the final circuit are such that the actual error observed is still less than that predicted by the least mean square error criteria.

The slopes of the segments correspond to the desired circuit gains while the figures tabulated under "Input Range" give the values of the input voltages at which the circuit gain must change. Fig. II.3 displays the circuit gain as a function of the input voltage for both the true quadratic and the piecewise linear approximation.

II.B. System Configuration Considerations

A frequently employed technique for generating non-linear characteristics in Analog Computers employs an operational amplifier in the basic configuration shown in Fig. II.4.[3]

As will be shown later in this chapter, this circuit has a transfer function given by $e_{out}/e_{in} = -Z_{fb}/Z_i$. Therefore, a non-linear characteristic can be generated by making either Z_{fb} or Z_i a function of the input voltage. The former method was investigated and found impractical for this application. There are also several ways in which Z_i can be made to change with input voltage, but one method is particularly suitable and lends itself to ease of analysis. It is shown in Fig. II.5.

To clarify the following discussion, the resistors r_1, r_2,... will
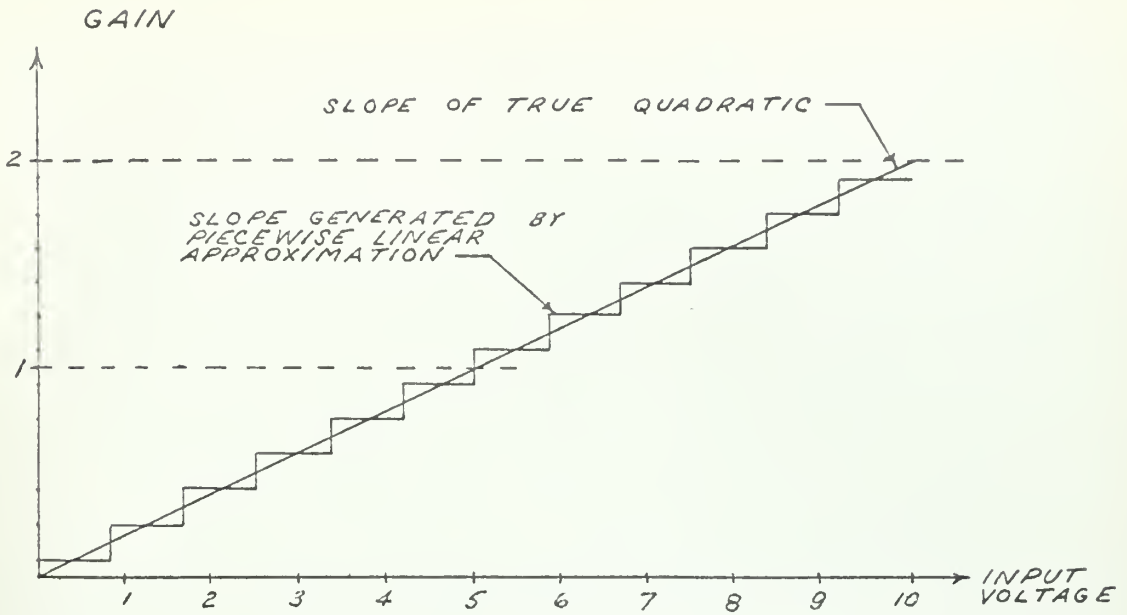
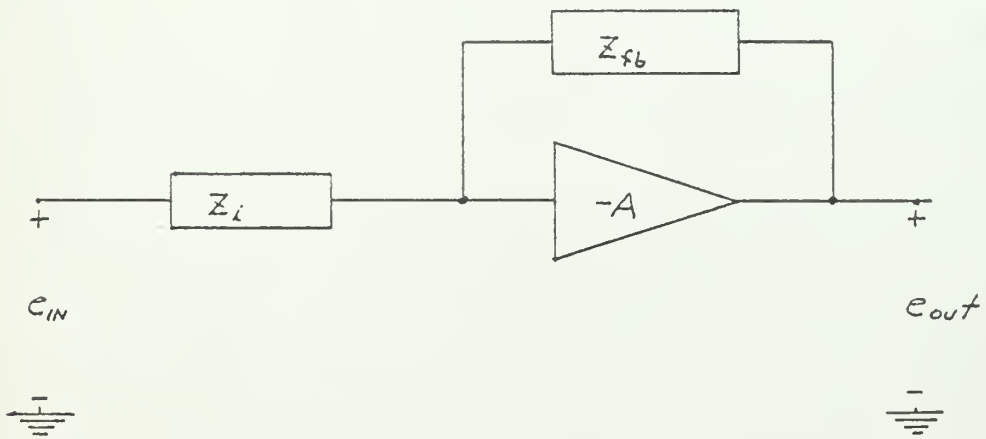FIG. II.3.   GAIN   AS A FUNCTION   OF INPUT VOLTAGE

FIG. II.4.   BASIC   CONFIGURATION   EMPLOYED
FOR   NON-LINEAR   FUNCTION   GENERATION

be termed the bias chain, and the resistors R_o, R_1,... will be termed
the segmented input impedance network.

This configuration enjoys several practical advantages which
will be brought out in the detailed analysis. However, one which is
not so apparent is the fact that quiescently, with zero input voltage,
all of the diodes in the segmented impedance network are back biased.
Therefore, the biasing voltage, $-E_b$, has no effect upon the output of
the circuit. This did not hold true in several other configurations
examined where the biasing voltage caused an offset voltage at the
output which could not be eliminated.

For the sake of simplicity, consider the situation depicted in
Fig. II.6, where only R_o, R_1, and R_2 are present in the input network.
The principles brought out in the analysis apply to all segments in the
same manner.

Assume $r_1 \ll R_1$, so $R_1 + \left(\sum\limits_{k=2}^{k=12} r_k \ \middle\| \ r_1 \right) \cong R_1$ where the symbol $\|$
means "in parallel with". Under this assumption, the bias network im-
pedances can be neglected.

The diode conducts when the voltage at point $B \geq 0$. By super-
position, the voltage at point B is given by $\dfrac{-R_2}{R_1 + R_2} E_1 + \dfrac{R_1}{R_1 + R_2} e_{in}$,
if e_g is assumed to be a virtual ground. This is true for an operational
amplifier and will be proven shortly. Under this assumption, the diode
will conduct when $e_{in} = \dfrac{R_2}{R_1} E_1$.

For convenience, let $R_1 = R_2$. Then the diode will start to con-
duct when the input voltage is of the same magnitude as the biasing voltage
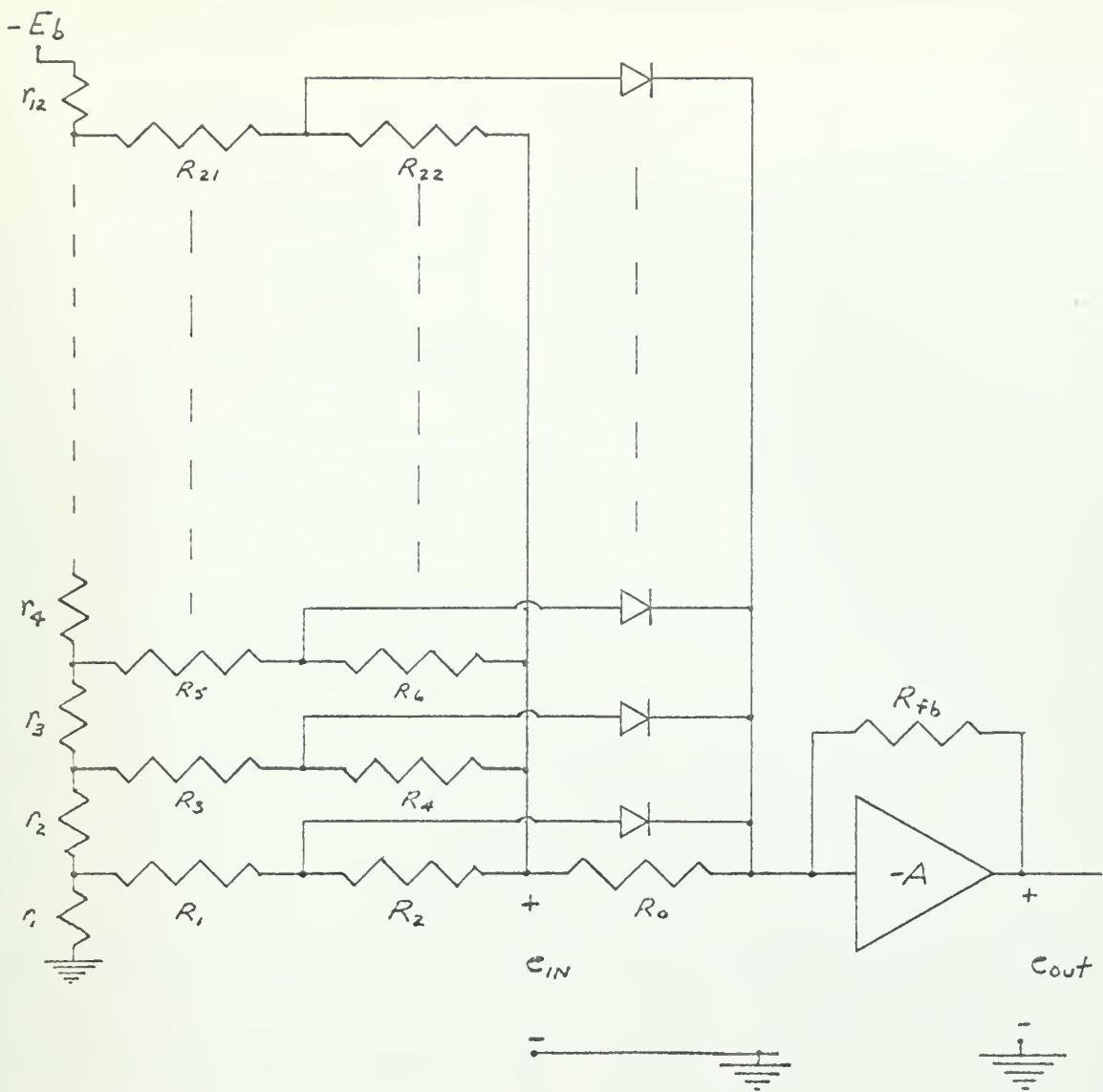of that particular segment.

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FIG. II.5. CONFIGURATION EMPLOYED TO CARRY OUT
QUADRATIC APPROXIMATION WITH TWELVE
SEGMENTS
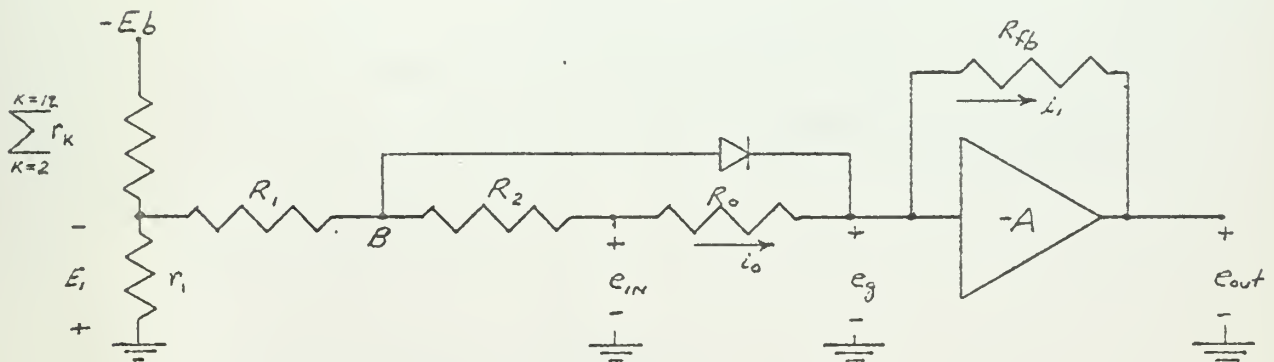

FIG. II.6. TWO SEGMENT APPROXIMATION TO DEMONSTRATE
ANALYSIS TECHNIQUE

For $0 < e_{in} < E_1$, we have:

$$i_o = \frac{e_{in} - e_g}{R_o}; \quad i_1 = i_o \text{ due to infinite input impedance of}$$

$$\text{Operational Amplifier}$$

$$i_1 = \frac{-e_{out} + e_g}{R_{fb}}; \quad e_{out} = -Ae_g$$

$$\therefore \quad \frac{e_{in} - e_g}{R_o} = \frac{-e_{out} + e_g}{R_{fb}}$$

$$\frac{e_{in}}{R_o} + \frac{e_{out}}{AR_o} = \frac{-e_{out}}{R_{fb}} - \frac{e_{out}}{AR_{FB}}$$

$$e_{in} (1/R_o) = -e_{out} \left(\frac{1}{R_{fb}} + \frac{1}{AR_{FB}} + \frac{1}{AR_o} \right)$$

$$e_{out}/e_{in} = \frac{-1/R_o}{1/R_{fb} + 1/AR_{FB} + 1/AR_o}$$

However, for an operational amplifier, A is very large, so AR_{FB} and AR_o

are $\gg R_{fb}$ so $\dfrac{e_{out}}{e_{in}} \cong \dfrac{-R_{fb}}{R_o}$

Under the same assumption of large gain:

$$e_g = \frac{-e_{out}}{A} \cong 0, \text{ confirming that the input is at a virtual}$$

$$\text{ground.}$$

For $e_{in} > E_1$, and under our previous assumption that $r_1 \ll R_1$, the

analysis for the case where the diode is forward biased proceeds as

follows: Refer to Fig. II.7.

Since $e_g \cong 0$; $i_1 \cong 0$

$$\text{so } i_{fb} = i_o + i_2 = \frac{e_{in}}{R_o \| R_2}$$

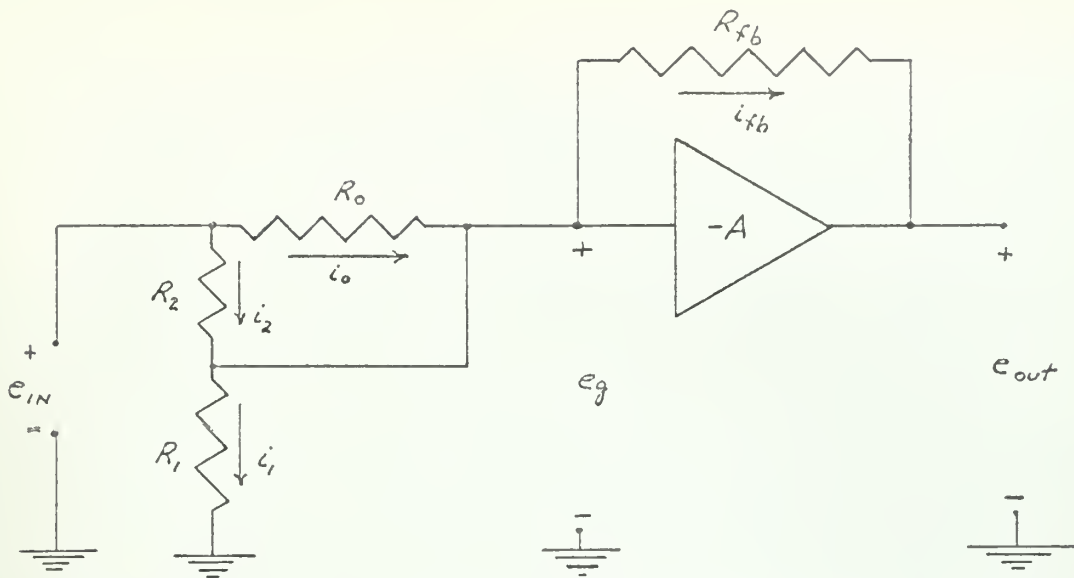FIG. II.7. SIMPLIFIED SCHEMATIC OF FIG. II.6
FOR $e_{IN} > E_1$.

$$R_{eq} = \left(\sum_{n=1}^{n=k} r_n \right) \middle\| \left(\sum_{n=k+1}^{n=12} r_n \right)$$

FIG. II.8 EQUIVALENT CIRCUIT OF BIAS
CHAIN AT kth BIAS POINT ABOVE
GROUND.

$$\text{and } e_{out} = -i_{fb}R_{fb} = \left(\frac{-e_{in}}{R_o \,||\, R_2}\right) R_{fb}$$

$$e_{out}/e_{in} = -R_{fb}/ \left(R_o \,||\, R_2\right)$$

Hence, the effect of the diode's conducting is simply to alter R_i by placing another resistance in parallel with it. This analysis can easily be extended to all other segments, the only difference being that the equivalent circuit of the biasing network changes as one moves up the chain. Specifically, at any point, the equivalent circuit of the biasing network can be represented by that shown in Fig. II.8, where k represents the kth biasing point on the 12 segment chain.

However, as long as the resistances in the segmented impedance network are much larger than the resistors in the bias chain, these effects can b^ neglected, and the resistance to ground through the biasing network can always be assumed to be zero.

The previous discussion has led to the adoption of the circuit configuration to be used, and armed with this information, it is now a not too formidable task to select component values for a 12 segment squaring circuit. However, the additional constraints of low power and 50 kc bandwidth require investigation before any choice of resistance values can be made.

II.C. The Frequency-Response Problem

The desired broadband response of the circuit shown in Fig. II.5 is limited by the frequency characteristics of the Operational Amplifier and by the self-capacitance of the switching diodes. The former limitation can be overcome by proper selection of the amplifier. The effect due to the latter can be reduced by using high-speed switching diodes

which have a very small capacitance. However, these actions in themselves do not guarantee broadband response, and in most cases, it is necessary to bypass all of the resistors with capacitors. Consider the schematic of Fig. II.9.

Recall that Gain $= -Z_{fb}/Z_i$

Hence, $e_{out}/e_{in} = -\left(\dfrac{R_{fb}}{1 + sR_{fb}C_{fb}}\right) \cdot \left(\dfrac{1 + sR_oC_o}{Ro}\right)$

$$\dfrac{e_{out}}{e_{in}} = -\dfrac{R_{fb}}{R_o}\left(\dfrac{1 + sR_oC_o}{1 + sR_{fb}C_{fb}}\right)$$

but if $R_oC_o = R_{fb}C_{fb}$, then $\dfrac{e_{out}}{e_{in}} = \dfrac{-R_{fb}}{R_o}$; independent of frequency.

There is another important factor to consider which prohibits arbitrary selection of the resistors in the segmented impedance chain and the capacitors across them. This factor can best be explained by considering the impulse response of Fig. II.10. This circuit is the segmented impedance network of Fig. II.7 in which R_o, R_1, and R_2 have been bypassed with capacitors and in which the diode and R_o are shown connected to an actual ground rather than the virtual ground of the Operational Amplifier. This latter change merely makes the following analysis easier to understand. It does not alter the validity of the argument and the fact that it does not affect what happens in the segmented input impedance network has been verified experimentally.

To proceed with the analysis, note that for a voltage impulse great enough to cause the diode to conduct, capacitors C_o and C_2 tend to charge almost immediately because they are directly across the input. R_1 and C_1 are shorted out. However, as soon as the input voltage drops
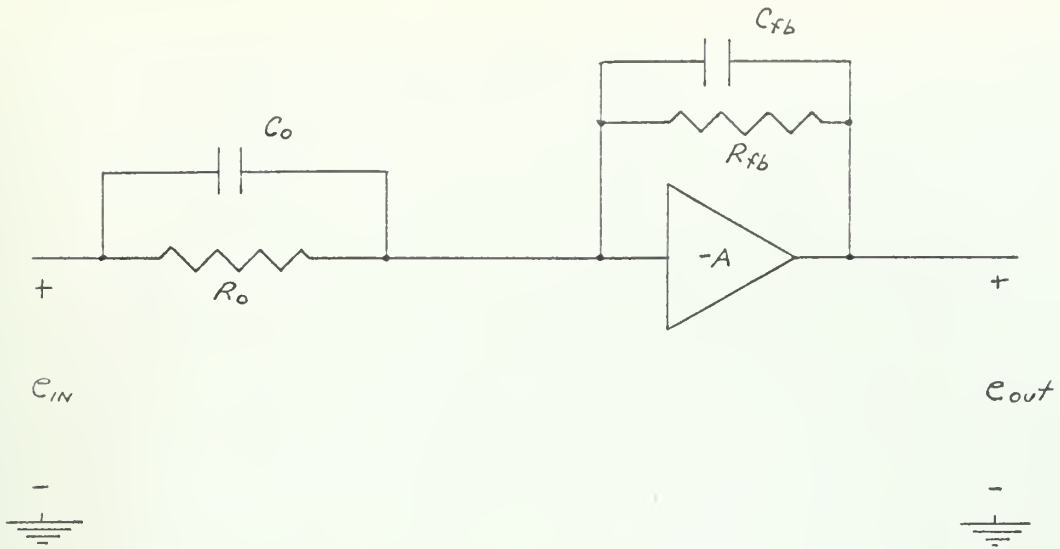
FIG. II.9   USE OF CAPACITORS TO IMPROVE
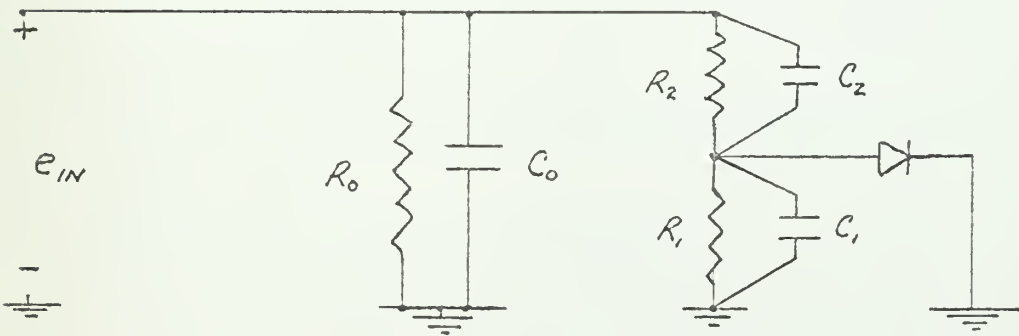FREQUENCY - RESPONSE

FIG. II.10   MODIFIED INPUT IMPEDANCE NETWORK
OF FIG. II.7.

to zero, the diode will have ceased conducting and capacitor C_2 must discharge through the parallel combination of R_1 and R_2. Using this example of the system's impulse response, an analogy can be drawn to the situation which exists when a high frequency voltage signal is present at the input. Clearly, unless the charge is removed from the capacitor C_2 before the next cycle appears, phase shifts will occur in the segmented impedance network and the entire circuit will not perform the squaring operation properly. It is therefore important that the RC products of the individual resistors and their bypass capacitors be kept as low as possible.

In order to ensure that the diode conducts at the same input voltage regardless of frequency, it is essential that the impedance of the parallel combination of R_1 and C_1 equal the impedance of the parallel combination of R_2 and C_2. This obviously must also hold for all other segments of the impedance chain.

These concepts form the basis for good frequency-response of the entire squaring circuit.

II.D. Selection of the Operational Amplifier

The Operational Amplifier was selected with the following major considerations in mind:

1. high gain bandwidth product

2. solid state construction

3. $\pm$ 10 volt output

4. good thermal stability

5. low power consumption

A review of commercial operational amplifiers led to the selection

of the TYPE FSL-6 manufactured by the Nexus Research Laboratory, Inc.
The FSL-6 has the characteristics exhibited in Fig. II.12 and Fig. II.13.
Since this is a model designed primarily for laboratory use, the premium
model FSL-12 should be used for actual flight applications. The FSL-12
has better thermal stability and in general is more suitable for critical
applications.

Storage temp:	-30°C to $+85^{\circ}$C
Operating temp:	-25°C to $+85^{\circ}$C
Supply Voltage:	$\pm$ 16 volts
Common Mode Input Voltage:	$\pm$ 11 volts
Diff. Input Voltage:	$\pm$ 15 volts
Input Overload Current:	$\pm$ 1 ma
Output Overload Current:	$\pm$ 30 ma

Fig. II.12   Absolute Maximum Ratings of FSL-6

II.E.   Component Selection

The preceding sections of this chapter have developed constraints
appropriate to the design of the circuit. Obviously, the selection of
component values involves necessary compromises in order to best satisfy
all of the requirements. As an example of the most obvious compromise,
recall from Section II.A that it was decided to use twelve segments to
perform the approximation and the circuit would be in the configuration
of Fig. II.5. Because total power consumption consists of the power
supplied to the amplifier and the power supplied to the bias chain, it is

SYMBOL	CHARACTERISTICS (at 25° C UNLESS NOTED)			UNITS
V_{cc}	Supply Voltage (3-wire D. C.)	±15	Design Center	volts D.C.
I_{cc}	Supply Current Quiescent / Full Output	±10 / ±30	Max.	ma
E_o	Output Voltage Range, $R_L = 500 \Omega$ Full Load	±10	Min.	volts P-P
I_o	Output Current Range	±20	Min.	ma P-P
E_{cm}	Input Common Mode Voltage Range	±3	Max.	volts P-P
E_{os}	Voltage Offset Stability at Constant Temperature (Long Term)	±100	Typical	μv
$\Delta E_{os}/\Delta V_{cc}$	Offset Voltage/Supply Voltage Stability Coefficient	200	Typical	μv/v
$\Delta E_{os}/\Delta T$	Offset Voltage Temperature Coefficient -25°C to +85°C	±12 / ±36	Typical / Max.	μv/°C
I_{os}	Input Offset Current	±10 / ±40	Typical / Max.	na
$\Delta I_{os}/\Delta T$	Offset Current Temperature Coefficient -25°C to +85°C	2.0	Max.	na/°C
A_o	Open Loop Gain at D.C. $R_L=500 \Omega$	100,000 / 50,000	Typical / Min.	-
f_t	Unity Gain Crossover Frequency	100	Typical	Mc
f_p	Frequency Limit Full Output (Unity Gain Inverter)	500	Typical	Kc
Z_d	Differential Input Impedance at D.C.	200,000	Typical	ohms
R_{os}	External Offset Voltage Zero Trim Potentiometer	100,000	-	ohms

FIG. II.13 FSL-6 Specifications

desirable to keep the bias chain resistors as high as possible. On the

other hand, all of the preceding analyses assumed that the bias chain

resistors were very much smaller than the resistors in the segmented

input impedance network. This therefore leads to the conclusion that

the resistors in the segmented network must be very large. However, it

is readily seen that this violates one of the frequency response con-

straints of keeping the individual RC products in the segmented network

very small.

The implications of all of these trade offs can best be determined

experimentally. This was in fact accomplished and the final circuit

reflects all of these compromises.

CHAPTER III

Circuit Construction and Adjustment

III.A. Adjustment Procedures

Based on the design concepts developed in Chapter II, a reasonable choice of component values was initially selected, and the values were subsequently altered to determine the best possible compromise.

Under conditions of low input signal frequency (100 cps or below), and an ambient temperature of $+25^{\circ}C$, the accuracy of the circuit is dependent upon two critical factors:

1) Proper adjustment of the breakpoints.

2) Proper circuit gain for the appropriate range of input voltage.

Once a bias voltage, $-E_b$, has been selected, all of the resistors in the bias chain can be fixed, but it is helpful to use potentiometers to adjust the first and last breakpoint, after which they too can be replaced by fixed resistors. It must be pointed out that each bias chain resistor must be selected very carefully because an error in the breakpoint of one segment affects the accuracy of the curve beyond that point. See Fig. III.1. Note how the error in the first breakpoint causes the approximation to be in error at all subsequent values of input voltage.

After the breakpoints have been adjusted, the slopes of the individual segments can be altered. This is a very straightforward method and needs no further explanation other than to point out that the slope adjustments should be made commencing with the lowest segment.

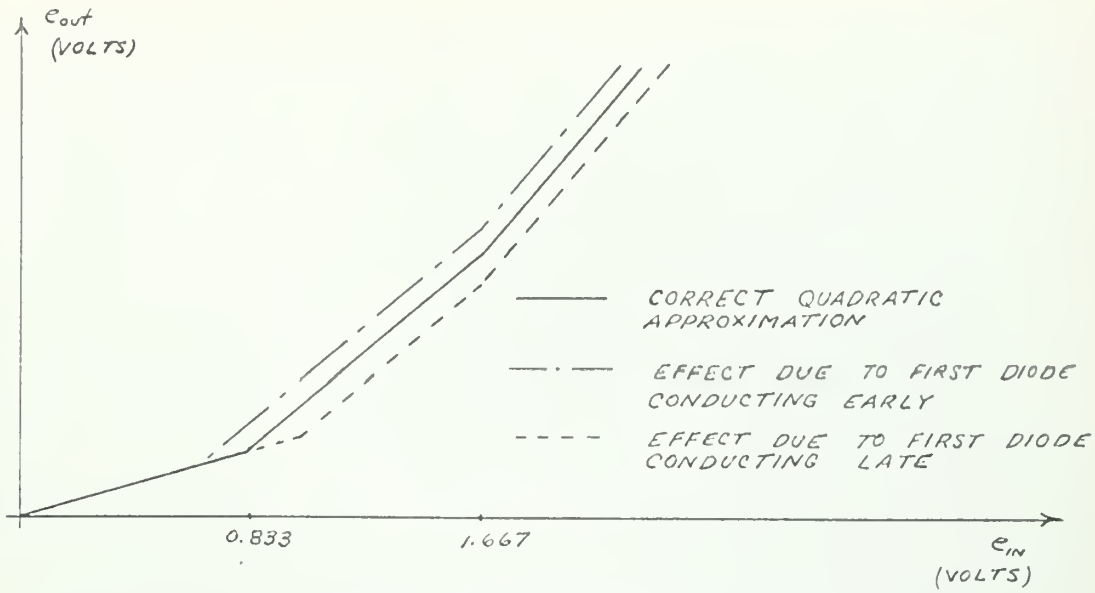It is also essential that the entire circuit be balanced, i.e.,
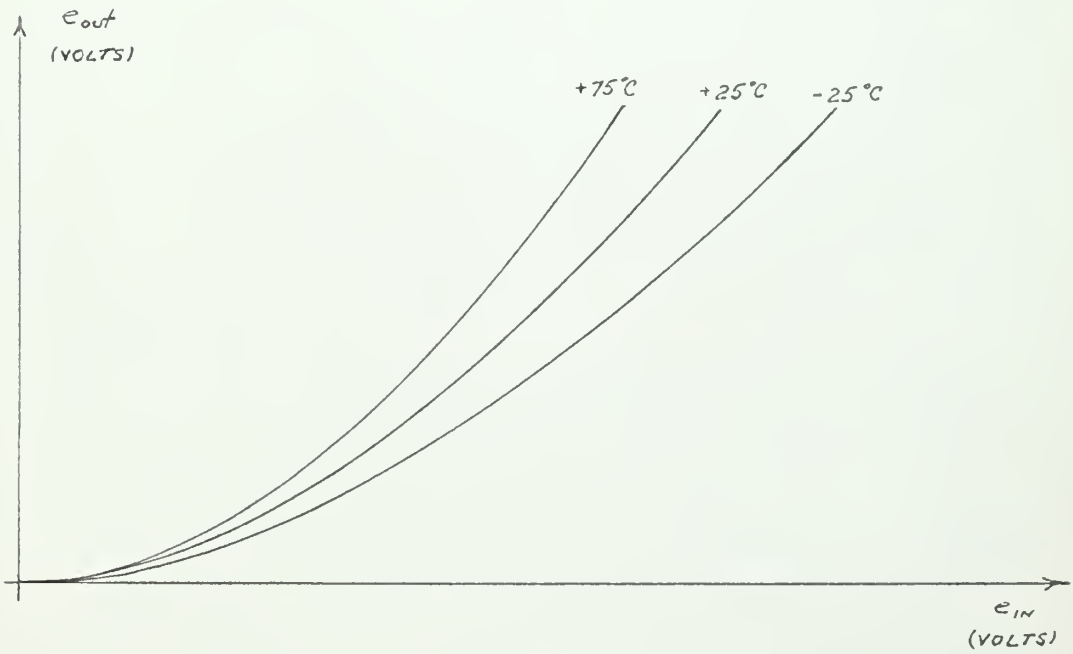
FIG. III.1.   EFFECT OF BREAKPOINT ERROR

Legend within figure:
CORRECT QUADRATIC APPROXIMATION
EFFECT DUE TO FIRST DIODE CONDUCTING EARLY
EFFECT DUE TO FIRST DIODE CONDUCTING LATE

Axis labels: e_{out} (VOLTS), e_{in} (VOLTS)
Values on axis: 0.833   1.667

FIG. III.2.   EFFECT OF TEMPERATURE   ON
CURVE GENERATED BY PIECEWISE
LINEAR METHOD

Axis labels: e_{out} (VOLTS), e_{in} (VOLTS)
Curve labels: +75°C   +25°C   -25°C

that the output voltage be zero when the input is grounded. This is accomplished by adjustment of a 100K external potentiometer in the operational amplifier circuitry. Instructions covering the supply voltage connections and external potentiometer arrangement accompany the amplifier. As in the case of those used for breakpoint adjustments, the balancing potentiometer may be replaced by a fixed resistance after balancing.

III.B. Testing Methods

1. Accuracy:

The best way to adjust the breakpoints and slopes referred to in the preceding section is to display the input-output characteristic on an oscilloscope while the circuit is operating with a low-frequency input (100 cps). However, scope calibration and resolution is insufficient for fine adjustment. It is therefore desirable to change from an oscilloscope to a digital voltmeter once the function generated is very close to that desired.

2. Frequency Response:

The ideal way to measure the frequency response of the circuit is to display the input-output curve on an oscilloscope, raise the frequency, and note any effect on the quadratic characteristic. However, the practical limitations of probe capacitance, oscilloscope input capacitance, and non-identical horizontal and vertical amplifiers in the scope render this method ineffective because the trace displayed reflects all of these external effects.

A suitable alternate method is to employ a dual trace oscilloscope and to measure the input and output voltages at different

frequencies. This is the manner in which all of the frequency response
data of Chapter IV was taken.

    3. Thermal Sensitivity:

    By placing the circuit in a hot/cold chamber and by making
input and output measurements with a digital voltmeter, the effect of
temperature upon circuit accuracy can be determined. Analysis of data
obtained in this manner leads to the appropriate temperature compensation
schemes which are discussed in the next section.

III.C. Temperature Compensation

    It is a well known fact that the voltage drop across a diode
decreases with increasing temperature. As far as the squaring circuit
is concerned, high temperatures cause the diodes to conduct sooner than
anticipated. Accordingly, they conduct later than anticipated at low
temperatures. As used herein, "sooner" means the diode conducts at an
input voltage lower than that desired, and "later" means the breakpoint
voltage is higher than desired. Fig. III.2 shows these effects on the
circuit's input-output characteristic. Because all adjustments to the
circuit are made at +25°C, it is desirable to have the curve generated
at +25°C hold over the entire temperature range.

    These temperature effects were observed experimentally and errors
ranged from as high as 16% of the desired value at low input voltages
to 4% at high input voltages. Compensation was therefore required.

    As discussed in preceding sections of this chapter, errors in
the breakpoints of lower segments cause substantial errors at higher
levels. The solution to the temperature compensation problem was there-
fore predicated upon the fact that compensation of the breakpoints which

are dependent upon the lower input voltages is most important. The effects at the higher voltages can then be examined to see if the unremoved error can be tolerated.

Consider the situation which exists at high temperatures. The diode in the first segment of the input impedance chain conducts early. The following analysis therefore applies to this situation:

Referring back to Fig. II.6 and considering the first breakpoint, recall that at $+25^{\circ}C$, the diode conducts when $e_{in} = \dfrac{R_2}{R_1} E_1$. Therefore for $R_2 = R_1$, $e_{in} = E_1$. At $75^{\circ}C$, the diode will conduct when $e_{in} = E_1 - \Delta e$, where Δe is due to the effect of the higher temperature. However, if the resistance of the first section of the bias chain could be increased such that the bias voltage across it was raised to $E_1 + \Delta e$ at $+75^{\circ}C$, then the diode would conduct when $e_{in} = (E_1 + \Delta e) - \Delta e = E_1$ as desired.

Alternately, if R_1 could be lowered such that at $+75^{\circ}C$, $\left(\dfrac{R_2}{R_1 - \Delta r}\right) E_1 = E_1 + \Delta e$, then at $+75^{\circ}C$: $\quad e_{in} = \dfrac{R_2}{R_1 - \Delta r} (E_1) - \Delta e$

$$e_{in} = (E_1 + \Delta e) - \Delta e = E_1 \text{ as desired.}$$

The same analysis will hold for lower temperatures.

Two common devices used to solve temperature compensation problems are the thermistor and the sensistor. Both have established temperature coefficients which enable one to predict its resistance at a specific temperature, the basic difference between the two being that the thermistor resistance decreases with temperature while the sensistor resistance increases with temperature.

From the preceding analysis, it is clear that if compensation is to be made by changing the impedance in the bias chain, a sensistor should

be used. Alternately, if it is more desirable to lower the resistor in the segmented input impedance chain, a thermistor should be used.

It must be understood that rarely does the exact temperature coefficient desired for a specific application coincide with that of a thermistor or sensistor. Hence, it is necessary to "pad" these temperature sensitive elements by either a series or a parallel resistance or both. Elementary circuit theory can be employed to determine the padding necessary to yield the desired temperature coefficient desired.

These techniques were employed in the squaring circuit compensation problem. It was only necessary to adequately compensate the first two segments of the input impedance chain to reduce the error to a tolerable level.

As an example of the application of these principles, consider the analysis which led to the compensating elements in the bias chain and segmented inpedance network of Fig. III.3.

Case 1. Use of a Thermistor to compensate the first breakpoint:

As stated earlier, it is necessary to lower R_1 at $+75^{\circ}$C and to raise R_1 at -25°C to achieve the compensation desired. At $+25^{\circ}$C, the input voltage at which the diode conducts is given by $e_{in} = \dfrac{R_2}{R_1} E_1$. Suppose that at -25°C, the diode is conducting 0.25 volt too late; therefore, at -25°C, we would like the diode to conduct when $e_{in} = \left(\dfrac{R_2}{R_1}\right)\left(E_1\right) - 0.25$. This is to be accomplished by a change in R_1; hence we desire

$$\left(\frac{R_2}{R_1}\right)\left(E_1\right) - 0.25 = \frac{R_2}{R_1'} E_1$$ where R_1' is the new value of R_1 at -25°C. R_1' is the only unknown and can therefore be solved for.

At $+75^{\circ}$C, if the diode is conducting 0.25 volt too early, we would like it to conduct when $e_{in} = \left(\dfrac{R_2}{R_1}\right)\left(E_1\right) + 0.25$. As before,

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$$\left(\frac{R_2}{R_1}\right)\left(E_1\right) + 0.25 = \frac{R_2}{R_1''} E_1 \text{ where } R_1'' \text{ is the new value of } R_1 \text{ at } +75^\circ C. \text{ In}$$

the actual calculation for the first breakpoint, the results implied

that:

at $-25^\circ C$, R_1 should take on the value 112K.

at $+25^\circ C$, R_1 should take on the value 75K.

at $+75^\circ C$, R_1 should take on the value 56K.

A 15K Thermistor was employed which displayed the following

characteristics:

at $-25^\circ C$, resistance = 207K.

at $+25^\circ C$, resistance = 15K.

at $+75^\circ C$, resistance = 2.25K.

Placing a resistor, x, in parallel with the Thermistor, and a

resistor, y, in series with that parallel combination, we have the follow-

ing requirements:

at $-25^\circ C$: $y + \left(207 \parallel x\right) = 112K.$

at $+25^\circ C$: $y + \left(15 \parallel x\right) = 75K.$

at $+75^\circ C$: $y + \left(2.25 \parallel x\right) = 56K.$

The problem is obviously overspecified, but using the constraint

at $+25^\circ C$ and one other usually provides a solution which yields adequate

compensation. In this particular case, x = 82K and y = 56K.

Case 2. Use of a Sensistor to compensate the second breakpoint:

The Thermistor adequately compensated the first breakpoint. To

compensate the second breakpoint, a Sensistor was used in the second

bias chain segment. Using the notation of Fig. II.5 and Fig. II.6, let

the biasing voltage of this segment be termed E_2. At $+25^\circ C$, the second

diode will conduct when $e_{in} = \frac{R_4}{R_3} E_2$. Suppose the diode conducts 0.2 volt

too early at $+75^\circ$C and 0.2 volt too late at -25°C. We would then desire that at -25°C, the diode conduct when $e_{in} = \left(\dfrac{R_4}{R_3}\right)\left(E_2\right) - 0.2$ and at $+75^\circ$C, when $e_{in} = \left(\dfrac{R_4}{R_3}\right)\left(E_2\right) + 0.2$.

In this case, we are attempting to change the bias voltage with temperature, so at -25°C, $\left(\dfrac{R_4}{R_3}\right)\left(E_2\right) - 0.2 = \dfrac{R_4}{R_3} E_2'$ where E_2' is the desired biasing voltage at -25°C. Likewise, at $+75^\circ$C, $\left(\dfrac{R_4}{R_3}\right)\left(E_2\right) + 0.2 = \dfrac{R_4}{R_3} E_2''$ where E_2'' is the desired biasing voltage at $+75^\circ$C. E_2' and E_2'' are the only unknown quantities and can be solved for easily. Suppose a 1K Sensistor was available with the following specifications:

at -25°C, resistance $= 700 \ \Omega$

at $+25^\circ$C, resistance $= $ 1K.

at $+75^\circ$C, resistance $= 1350 \ \Omega$

Using a series parallel arrangement again, with x the resistor in parallel with the Sensistor and y the resistor in series with that parallel combination, the following relationships exist because of the voltage divider in the bias chain:

at -25°C: $\dfrac{(y + (700 \parallel x) + {}^r1)}{\displaystyle\sum_{k=1}^{k=12} r_k} \left(E_b\right) = E_2'$

at $+25^\circ$C: $\dfrac{(y + (1000 \parallel x) + {}^r1)}{\displaystyle\sum_{k=1}^{k=12} r_k} \left(E_b\right) = E_2$

at $+75^\circ$C: $\dfrac{(\dot{y} + (1350 \parallel x) + {}^r1)}{\displaystyle\sum_{k=1}^{k=12} r_k} \left(E_b\right) = E_2''$

Again, the problem is overspecified, but employing the same

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technique of using the constraint at $+25^{\circ}C$ and one other results in good

compensation.   In the actual circuit, the results were: x = 7.2K and

y = 100 ohms.

III.D.   The Final Circuit

The result of the design criteria, experimental compromises, and

compensation schemes is depicted in Fig. III.3.   This is the circuit on

which all of the performance data of Chapter IV is based.

Note that it is necessary to select all of the resistors to be

the value indicated in order to achieve the high accuracy desired.   The

principal reason adjustments in the resistance values of the segmented

impedance chain were necessary is because the bias chain resistors were

kept as large as possible to reduce power consumption.   It should also

be pointed out that the second segment of the bias chain, containing

the sensistor, must be chosen so that the entire series parallel combi-

nation is equivalent to 1K as in the other branches.
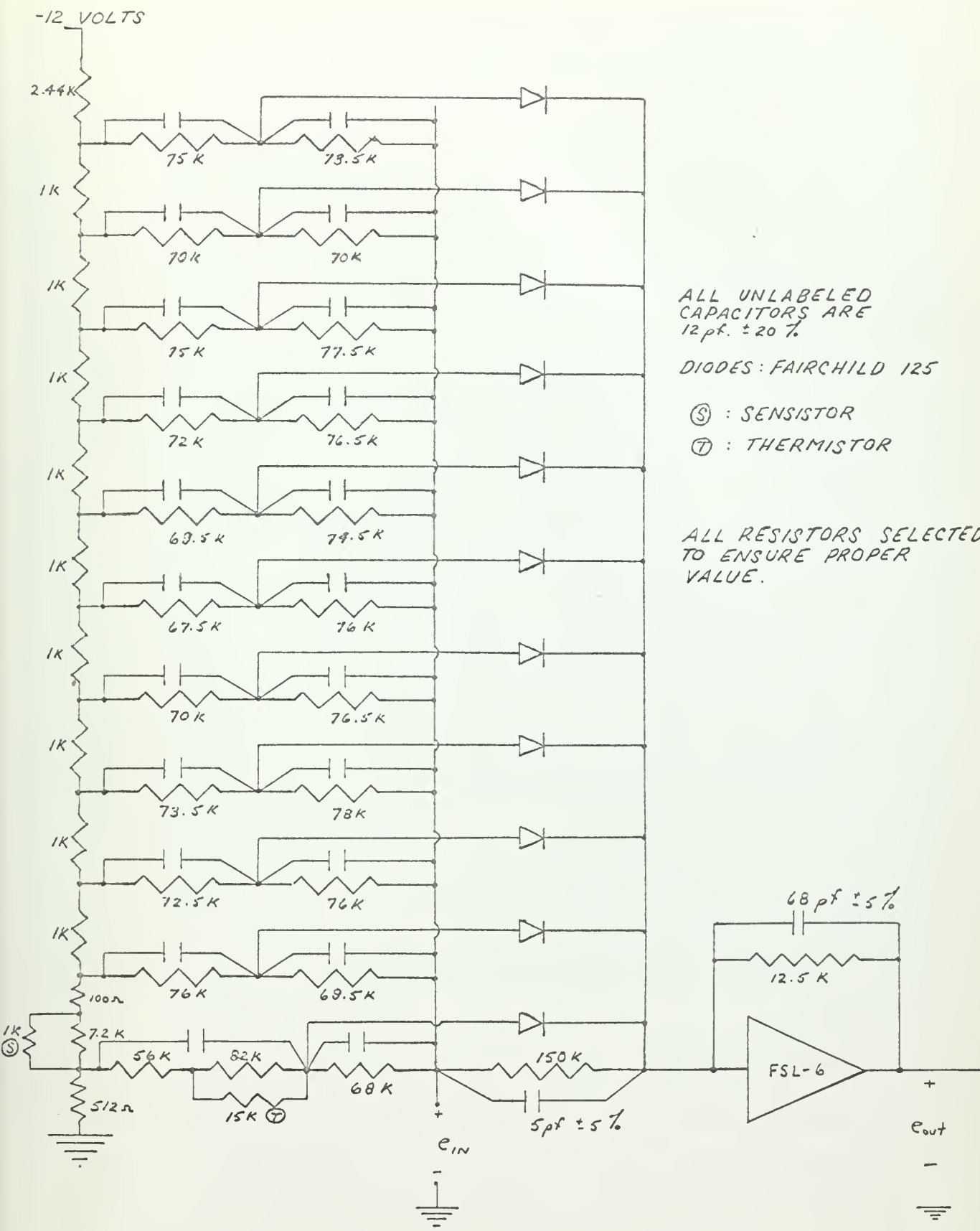
FIG. III. 3. FINAL DESIGN OF SQUARING CIRCUIT

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CHAPTER IV

Performance

IV.A. Circuit Accuracy

The table shown in Fig. IV.1 indicates the system error at various input voltages. These are no load d.c. measurements made at +25°C using a digital voltmeter. The % error is based upon the desired output; therefore, for low input voltages, a small error may yield a high error percentage. It must be borne in mind that the twelve segment approximation scheme inherently means that the quadratic is being approximated by a straight line for an input signal of 0.833 volt or less. Obviously, this will result in large errors at the low end of the input voltage scale. The tabulated results bear this out. However, the maximum error observed was 0.046 volt and the rms error is 0.021 volt, as opposed to the theoretical maximum error of 0.07 volt and theoretical rms error of 0.027 volt. Thus, the actual circuit exceeds the performance predicted by theory. This is true because the non-ideal characteristics of the diodes employed serves to round off the corners of the breakpoints.

The input-output characteristic of the circuit is shown in Fig. IV.2. The photograph was taken while the circuit operated at an input frequency of 100 cycles/sec and an ambient temperature of +25°C.

IV.B. Thermal Sensitivity

A plot of % error versus input voltage at various temperatures appears in Fig. IV.3. The curves show the result of compensating the first and second breakpoints of the twelve segment approximation. As was explained in Chapter III, temperature variations cause the diodes

INPUT (VOLTS)	DESIRED OUTPUT (VOLTS)	CIRCUIT OUTPUT (VOLTS)	% ERROR
0.500	0.025	0.041	+64.0
0.750	0.056	0.064	+14.3
1.000	0.100	0.100	0.00
1.200	0.144	0.136	-5.51
1.400	0.196	0.185	-5.61
1.600	0.256	0.245	-4.30
1.800	0.324	0.319	-1.54
2.000	0.400	0.396	-1.00
2.250	0.506	0.502	-0.83
2.500	0.625	0.622	-0.48
2.750	0.756	0.756	0.00
3.000	0.900	0.902	+0.22
3.500	1.225	1.239	+1.14
4.000	1.600	1.619	+1.17
4.500	2.025	2.051	+1.28
5.000	2.500	2.521	+0.84
5.500	3.025	3.051	+0.86
6.000	3.600	3.625	+0.69
6.500	4.225	4.255	+0.71
7.000	4.900	4.932	+0.65
7.500	5.625	5.657	+0.57
8.000	6.400	6.446	+0.72
8.500	7.225	7.265	+0.54
9.000	8.100	8.133	+0.41
9.500	9.025	9.042	+0.19
10.000	10.000	10.007	+0.07

FIG. IV.1. D.C. PERFORMANCE at 25°C
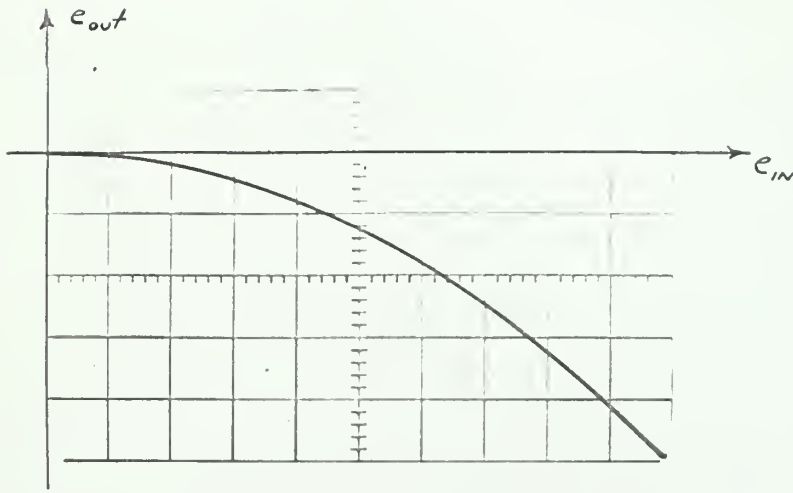
FIG. IV.2 Input-Output Characteristic at 25°C, 100 cycles/sec

      Vert. Scale: 2 volts/div.

      Horiz. Scale: 1 volt/div.

to conduct either too soon or too late, and the lower breakpoints are the most critical. From Fig. IV.3, it can be seen that compensation reduced the errors to less than 2% at -25°C and to 5% or less at $+75^{\circ}$C. If these errors still cannot be tolerated, the other breakpoints can also be compensated. The technique employed is identical to that used in Chapter III to illustrate compensation of the first two.

IV.C. Effect of Supply Voltage Variation

Fig. IV.4 displays a table of input and output values for various input signal levels. All indications are that as long as the supply voltages are kept to within $\pm$ 1 volt, the effect on the output can be neglected. This is true because variations in the supply voltage only change the gain of the Operational Amplifier. As long as the gain remains sufficiently high to support the previously developed approximations that the gain is infinite, no change in circuit operation should be expected.

IV.D. Power Consumption

Fig. IV.5 shows the power consumption measured at various temperatures under no load conditions for both high and low input signal levels.

IV.E. Frequency Response

Fig. IV.6 displays the frequency response of the squaring circuit. This response is obviously a function of the input signal level because of the segmented input impedance network. To properly interpret the Figure, it is important to realize that the circuit gain is different for different input voltages. This was discussed fully in Chapter II. Therefore, the important consideration to be kept in mind in examining
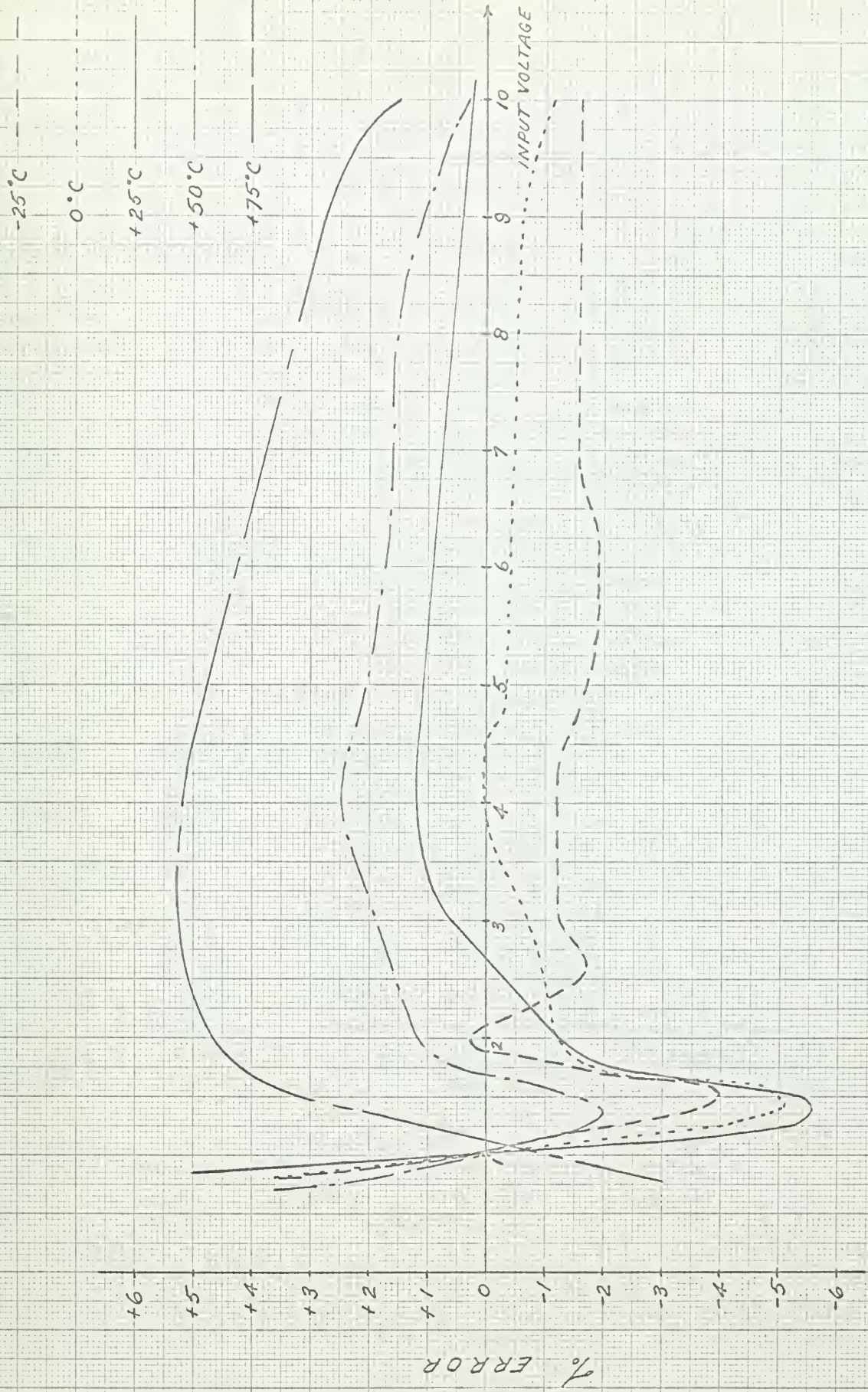
FIG. IV. 3 % ERROR VS. INPUT VOLTAGE FOR VARIOUS TEMPERATURES

INPUT (VOLTS)	SUPPLY VOLTAGE				
	± 14.0	± 14.5	± 15.0	± 15.5	± 15.9
	OUTPUT VOLTAGE				
1.000	0.100	0.100	0.100	0.100	0.100
3.000	0.901	·0.901	0.902	0.901	0.901
5.000	2.519	2.519	2.521	2.519	2.521
8.000	6.441	6.433	6.446	6.441	6.436
10.000	9.985	10.001	10.007	10.006	10.008

FIG.IV.4.   EFFECTS OF SUPPLY VOLTAGE VARIATIONS

TEMP.	INPUT VOLTAGE	POWER CONSUMPTION (MILLIWATTS)		
		AMPLIFIER	BIAS CHAIN	TOTAL
-25°C	1.000	94.4	13.8	108.2
	10.000	102.8	15.7	118.5
+25°C	1.000	101.0	13.8	114.8
	10.000	108.6	15.7	124.3
+75°C	1.000	103.8	13.8	117.6
	10.000	110.8	15.7	126.5

FIG.IV.5   POWER CONSUMPTION DATA
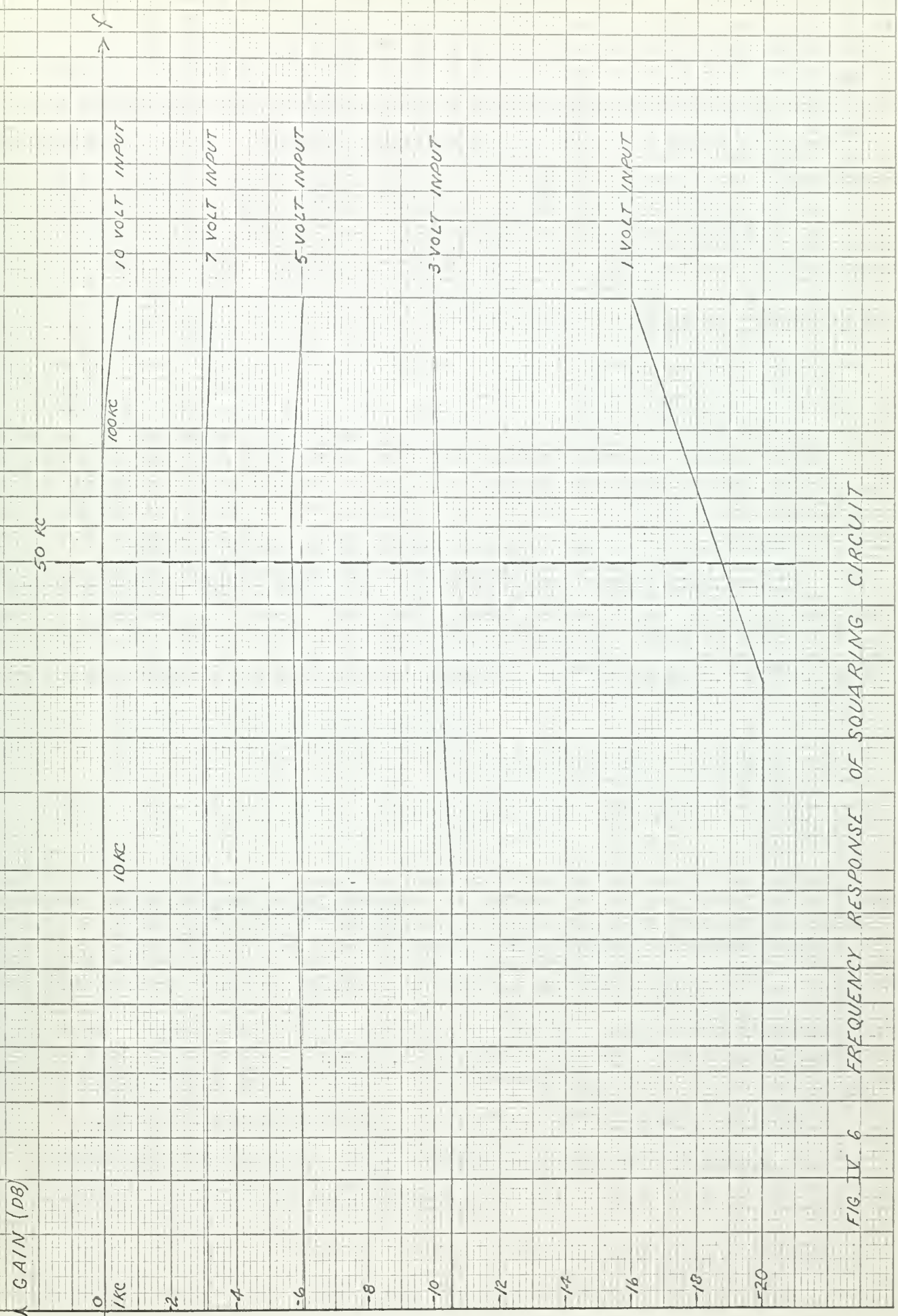
FIG. IV. 6   FREQUENCY RESPONSE OF SQUARING CIRCUIT

Fig. IV.6 is not what the gain in db is for a particular input voltage, but whether or not it stays the same as the frequency is increased. Although variations in the frequency response curves are slight for most input voltages, these variations could be eliminated completely by adjusting tuned capacitors across the resistors in the input impedance chain in lieu of using the 12 pf $\pm$ 20% presently employed.

Measurements were also made of the frequency response at $+75^{\circ}C$ and at $-25^{\circ}C$. There was an indication that the frequency response improved at lower temperatures and became worse at higher temperatures, but both of these effects were so slight that they are considered negligible.

A graphic illustration of the frequency response of the circuit can be obtained by examining Fig. IV.7(a) and (b) which show how the circuit squared the upper half of a 1kc and 50 kc sine wave respectively. Note the slight distortion and phase shift in the 50kc case.

IV.F.   Effect of Bias Voltage Variations

Because changes in the bias voltage directly affect the breakpoints of the linear segments, this voltage is much more critical than the supply voltages. See Fig. IV.8.

IV.G.   Step Response of the System

The inputs to the squaring circuit will resemble the transmitted pulses; it is therefore desirable to examing the step response of the system. Figures IV.9, IV.10 and IV.11 display both the input and output for signal levels of 1, 5, and 10 volts respectively.

Note the overshoot in the 1 volt case. It is strongly felt that this is caused by excessive stray capacitance in the circuit wiring which is comparable to the 5 pf across R_o.
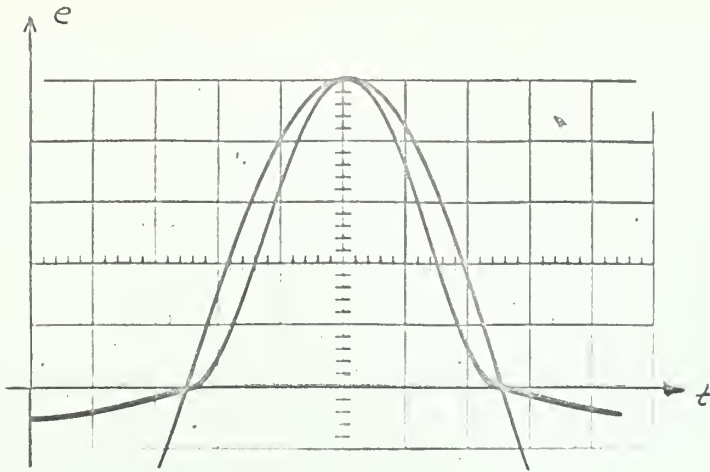
a) 1 kc.
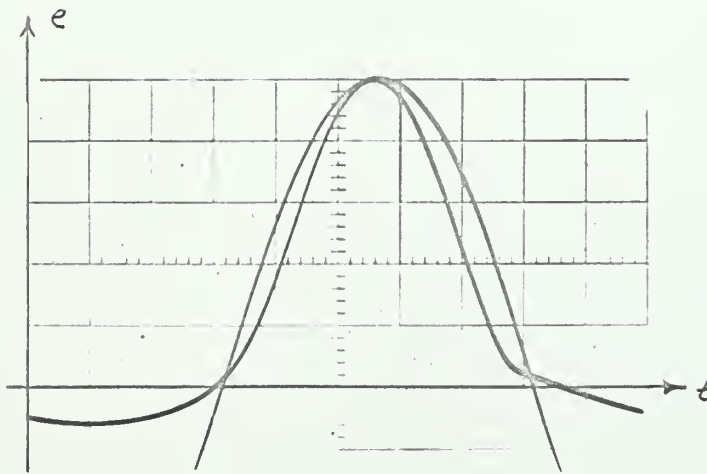
b) 50 kc.

FIG. IV.7. Response to a Sine Wave Input
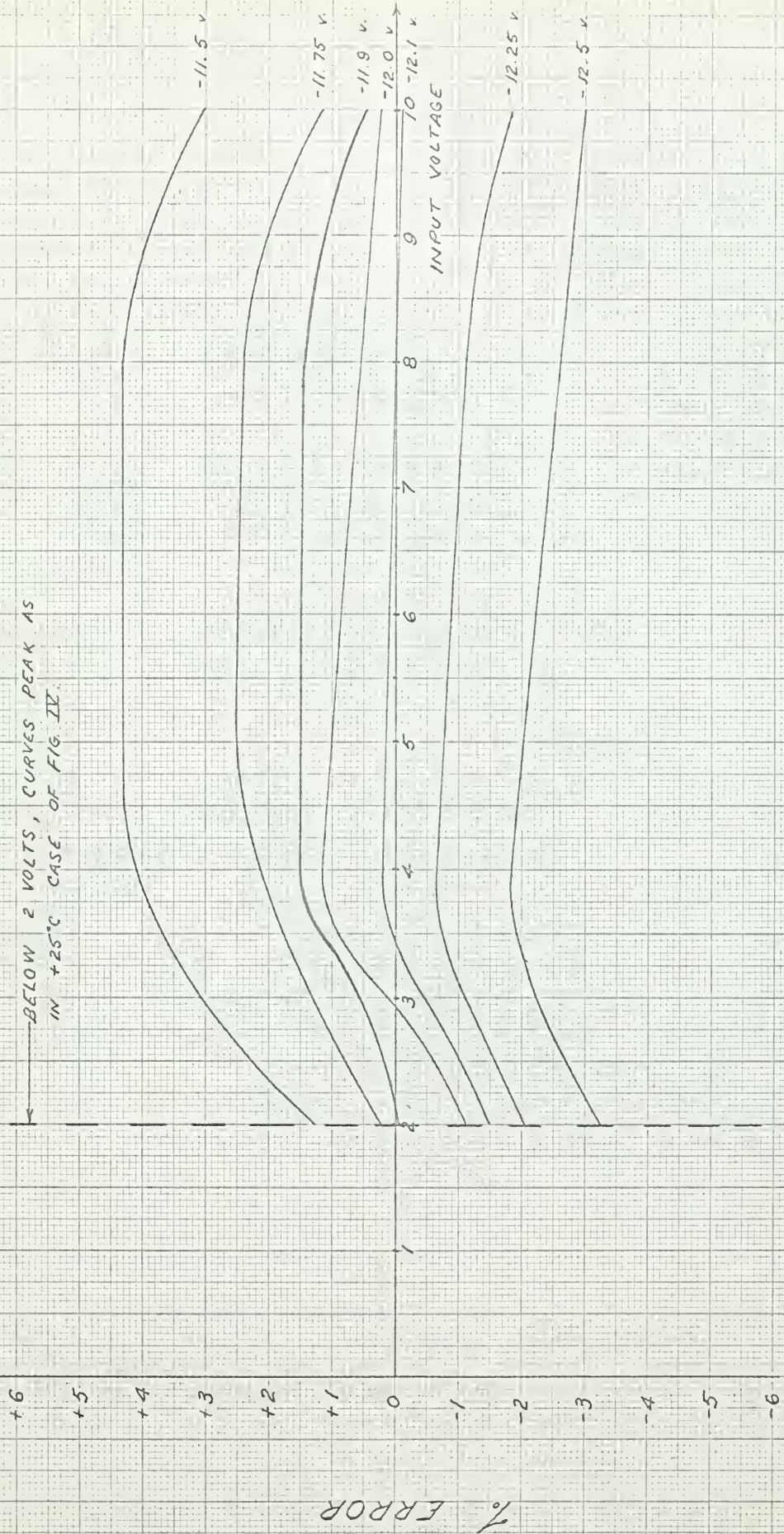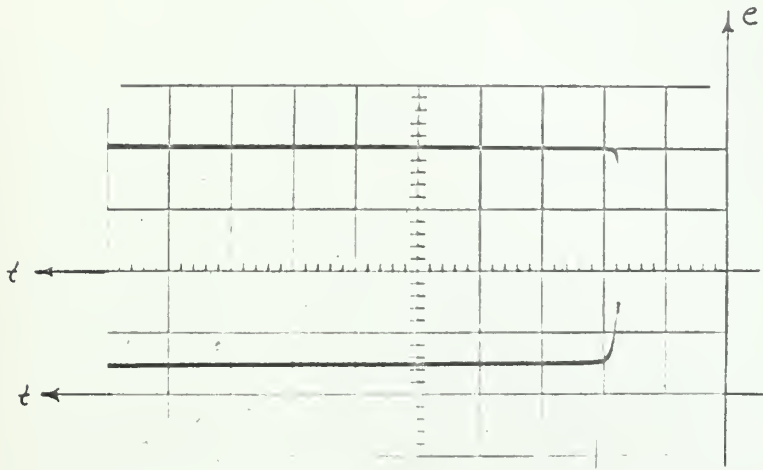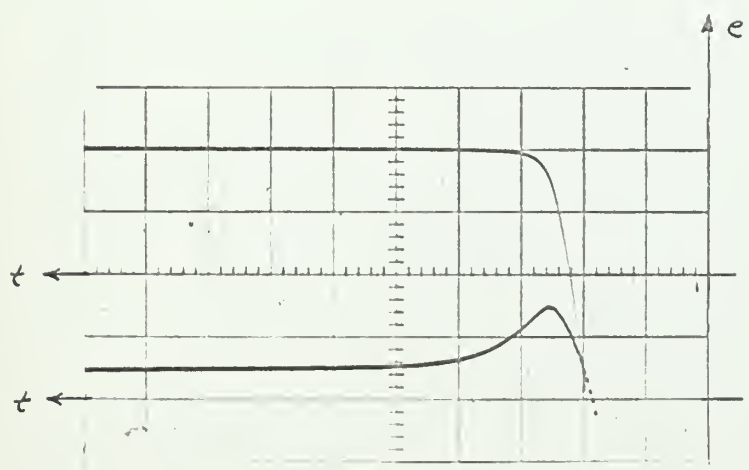
Upper Curve: Input

Lower Curve: Output

Vert. Scale: 2 volts/div.

FIG. IV. 8. % ERROR VS. INPUT VOLTAGE FOR VARIOUS BIAS VOLTAGES

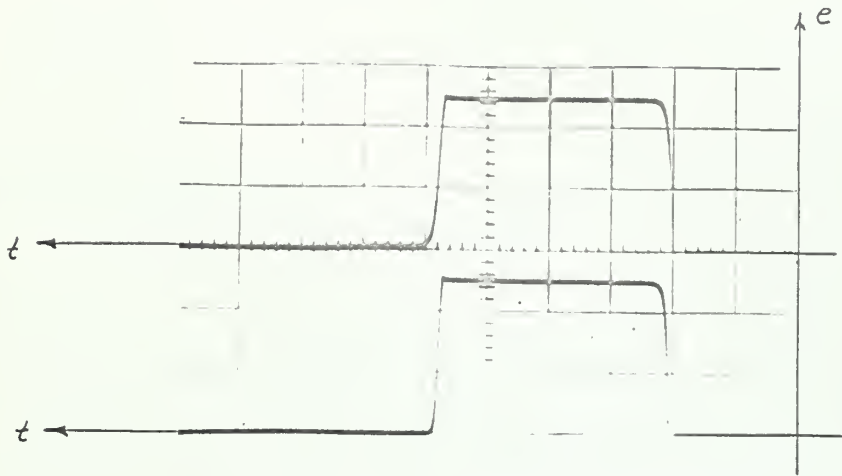a) Horiz. Scale: 20 μsec/div.

b) Horiz. Scale: 2 μsec/div.
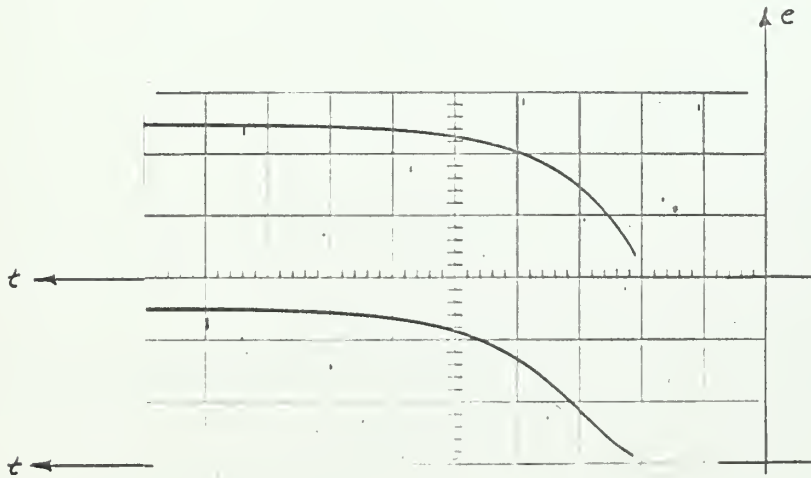
FIG. IV.9. Response to a 1 Volt Step

Top Trace: Input
                    Vert. Scale: 0.5v./div.

Bottom Trace: Output
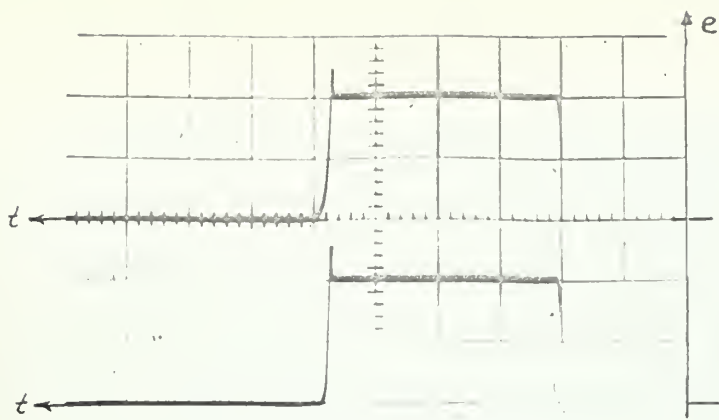   Vert. Scale: 0.2v./div.

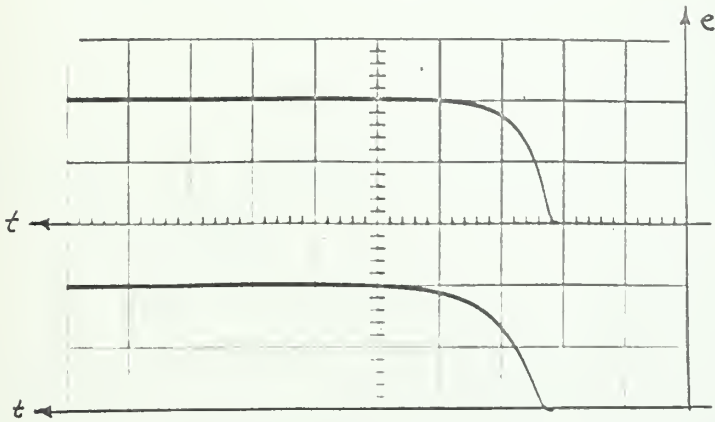a) Horiz. Scale: 50 μsec/div.

b) Horiz. Scale: 2 μsec/div.

FIG. IV.10. Response to a 5 Volt Step

Top Trace: Input
                     Vert. Scale: 2 volts/div.
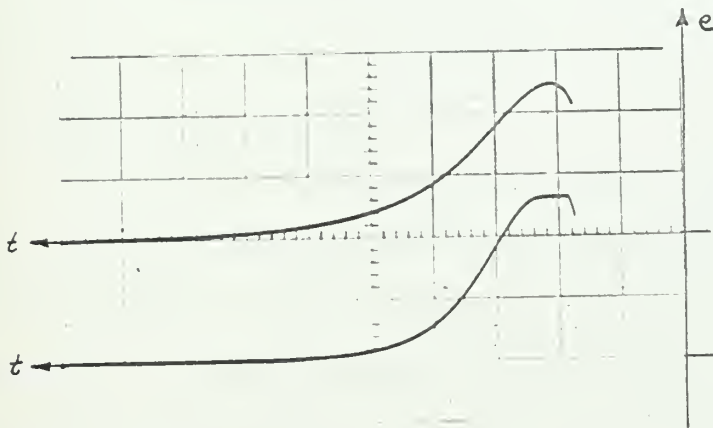
Bottom Trace: Output
                     Vert. Scale: 1 volt/div.

a) Horiz. Scale: 50 μsec/div.

b) Leading Edge; Horiz. Scale: 1 μsec/div.

c) Trailing Edge; Horiz. Scale: 2 μsec/div.

FIG. IV.11. Response to a 10 Volt Step

Top Trace: Input
                Vert. Scale: 5 volts/div.

Bottom Trace: Output
                Vert. Scale: 5 volts/div.

In examining the rise times of the squaring circuit it must be kept in mind that the circuit is in fact attempting to square the input pulse. Therefore, what may at first appear to be a lag in the response is, upon closer examination, revealed to be the squaring operation taking place. This is more clearly displayed in Fig. IV.10(c) which gives an expanded view of the sharp pulse on the trailing edge of the input, and the squaring circuit's response to this pulse. Note how the circuit starts to follow, saturates at about 13 volts, and then, except for a slight lag, squares the trailing edge on its way down to zero.

IV.H. Input Impedance

The input impedance is clearly a function of the input voltage. For inputs below 0.833 volt, the impedance is 150K. With the maximum voltage of 10 volts present at the input, the impedance has been measured at 6.5K. This is relatively low, but will not present any problems if the preceding circuit is designed with a very low output impedance.

IV.I. Discussion of Results

The preceding sections of this chapter indicate that the circuit of Fig. III.3 performs the desired squaring operation in a highly satisfactory manner. Specifically, in a thermostatically controlled environment of approximately 0°C to $+25^{\circ}$C, the errors are kept to approximately 1% or less for all input signal levels greater than 2 volts. If, however, it is necessary that this low error percentage be maintained over a wider temperature range (-25°C to $+75^{\circ}$C), additional temperature compensation can be accomplished by employing the same type of techniques which were demonstrated by the analyses of Chapter III.

It is important to note the effects of variations in the power

supplies upon circuit performance. It has been found that optimum performance is highly dependent upon a well regulated bias voltage. Fig. IV.8 indicates that this voltage should be maintained at -12 volts $\pm$ 1%. On the other hand, regulation of the power supply of the operational amplifier can be relaxed to $\pm$ 1 volt without any adverse effects.

A noteworthy limitation of the circuit is the relatively low input impedance of 6.5K when a 10 volt signal is applied at the input. However, this will not be a problem as long as the preceding circuit is designed with this limitation in mind.

The initial specifications of low power consumption and wide bandwidth have been met. In regard to the latter, it has been shown that at the middle and high ranges of input voltage, the frequency response curves show practically no variation of the input-output characteristic all the way out to 100 kc. It is these characteristics which contribute to the circuit's fine performance when a voltage step is applied at the input.

Summarizing, it has been shown that in its present form, the squaring circuit of Fig. III.3 is excellent for the intended application as long as the input voltage is kept above 2 volts, the entire circuit is placed in a temperature controlled environment, and the biasing voltage is maintained within 1% of -12 volts.

APPENDIX A

The Analog to Digital Converter

A.I.   Basic Conversion System

A detailed study has been made of the problem of converting to
digital form the signal which is proportional to the energy in the
received pulse.

After passing through the squaring circuit, the signal will be
integrated with a standard integrator circuit and the result will be
stored on a capacitor. Conversion of this capacitor voltage to digital
form will be accomplished by a scheme suggested by James K. Roberge,
which is depicted in Fig. A.1-1. Note that the And gate has three in-
puts. One is termed a "convert" pulse and is a signal received from
other circuitry which tells the converter to carry out the conversion
process. This pulse could be generated by a threshold detector which
triggers when the received signal falls below a certain level, that
level being the same as that established above the ambient noise to
determine the presence of an echo. The convert pulse should be of a
duration greater than the maximum amount of time required to carry out
the conversion process.

Another input to the gate is that from the zero crossing detector,
whose function is to keep a sustained pulse into the gate whenever the
voltage across the capacitor is greater than zero and to remove it
otherwise.

The last input is a series of clock pulses of a predetermined
frequency and duration. With both the convert pulse and detector pulse
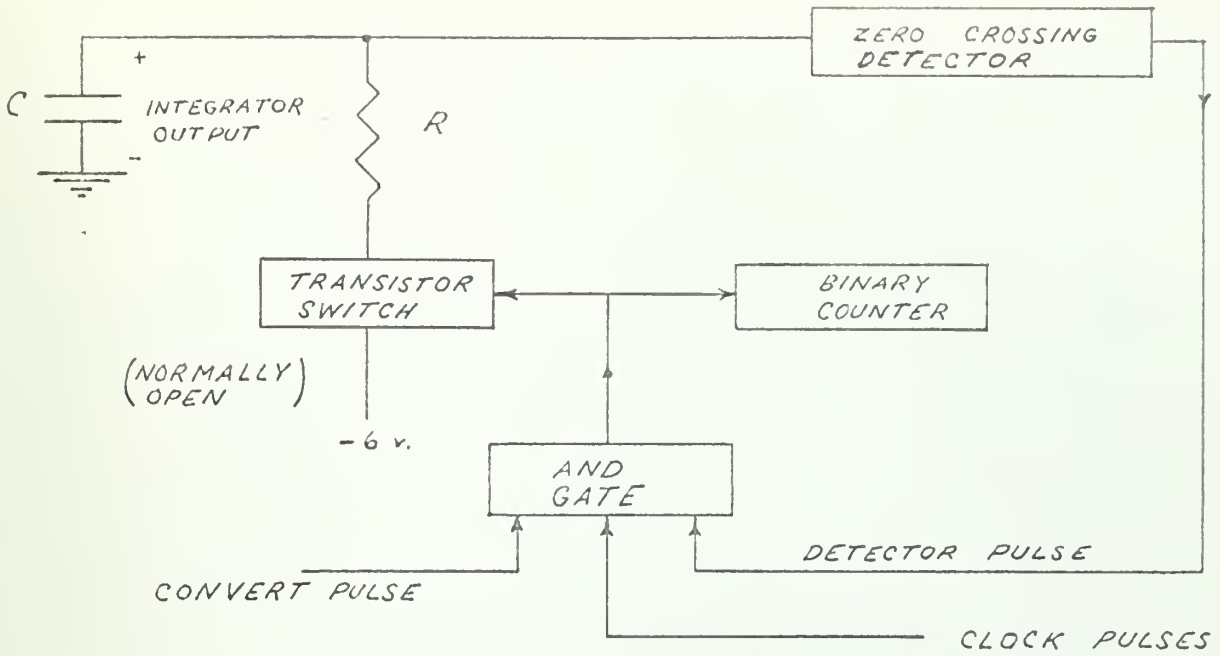present the clock pulses pass through the And gate and alternately turn
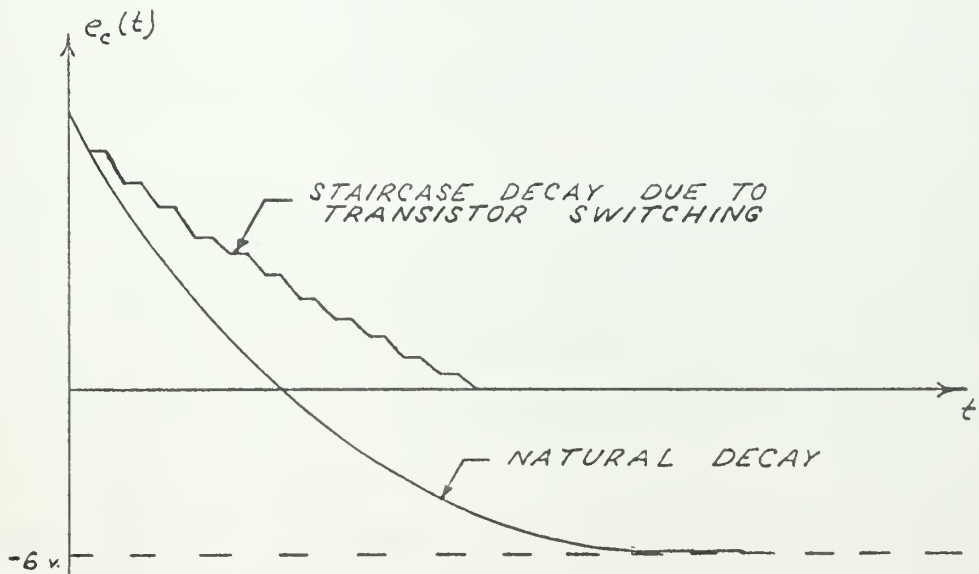
FIG. A.1-1 ANALOG TO DIGITAL CONVERSION SYSTEM

FIG. A.1-2 EFFECT OF TRANSISTOR SWITCHING ON CAPACITOR VOLTAGE

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the transistor switch off and on. The off-on switching of the tran-
sistor causes the capacitor voltage to decay through resistor R in the
manner shown in Fig. A. 1-2.

When the capacitor voltage reaches zero, the detector signal
disappears, the And gate "closes", and the clock pulses are no longer
allowed through. Thus, the number of clock pulses passing through the
gate is uniquely related to the initial voltage on the capacitor and
therefore provides information in digital form as to the magnitude of
that voltage. For testing purposes, a binary counter is used to count
these pulses. In the final data conversion system, the pulses can be
used as a digital input to the telemetry circuitry, which will modify
and code them prior to actual transmission of the information to ground
control stations.

A. II. Integration Circuitry

In order to obtain meaningful specifications for the A/D con-
verter, it is necessary to examine the integrator which will operate
on the output of the squaring circuit and provide the input to the con-
verter.

The maximum voltage appearing at the integrator output will be
proportional to the maximum output of the squaring circuit. Specifically,
if we allow that the maximum received pulse width due to spreading is
4 msec, then the maximum input to the integrator will be a 10 volt pulse
lasting for 4 msec.

Using an integrator as shown in Fig. A. 2-1, and recalling that
for A very large $e_{out}/e_{in} = -Z_{fb}/Z_i$, we can see that

$$e_{out}(s) = \frac{-1}{sRC} \; e_{in}(s)$$

$$\text{or} \quad e_{out}(t) = \frac{-1}{RC} \int_{-\infty}^{+\infty} e_{in}(t) \; dt$$

Recalling that the voltage output of the squaring circuit is negative, the integrator output will have the polarity shown in Fig. A. 2-1. The gain of the circuit can be adjusted by a suitable choice of R and C. To see exactly what gain is required, it is necessary to consider not only the maximum input, but also the minimum useful input which may exist. The minimum useful input level to the squaring circuit is approximately 1 volt; therefore, the minimum useful input to the integrator circuit will be a pulse of 0.1 volt, 1 msec in duration. It follows from the preceding discussion that

$$e_{out \; min} = \frac{-1}{RC} \; (0.1v) \; (1 \; msec)$$

$$e_{out \; max} = \frac{-1}{RC} \; (10 \; v) \; (4 \; msec)$$

In selecting the time constant RC, the choice is governed by these factors:

1. Selection of a resistance R high enough to prevent loading down the output of the squaring circuit.

2. Selection of a capacitor C consistent with the requirements of the Analog to Digital Converter.

3. An RC product which will yield reasonable integrator output magnitudes.

The squaring circuit operational amplifier is designed to deliver the full output voltage range with a load of 500 ohms. However, power
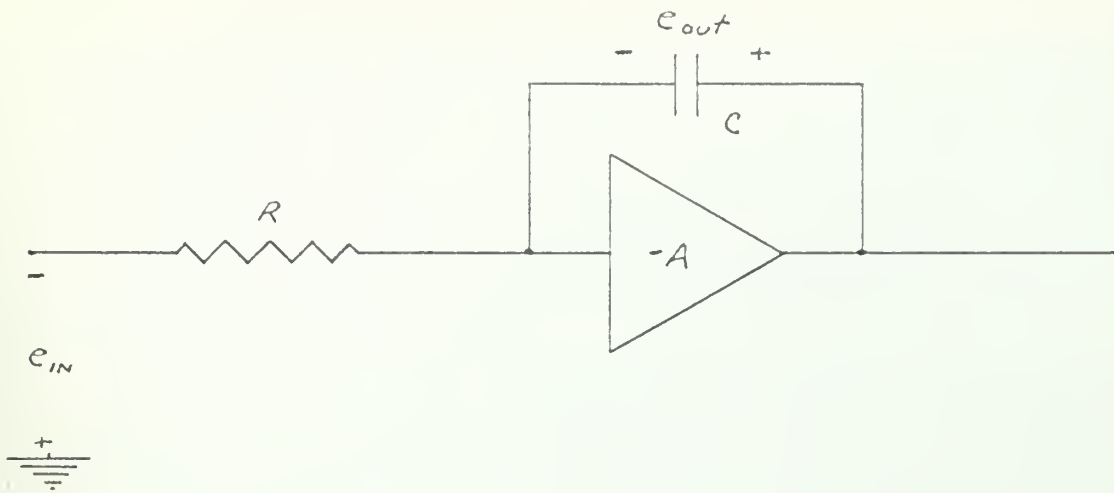
- 54 -

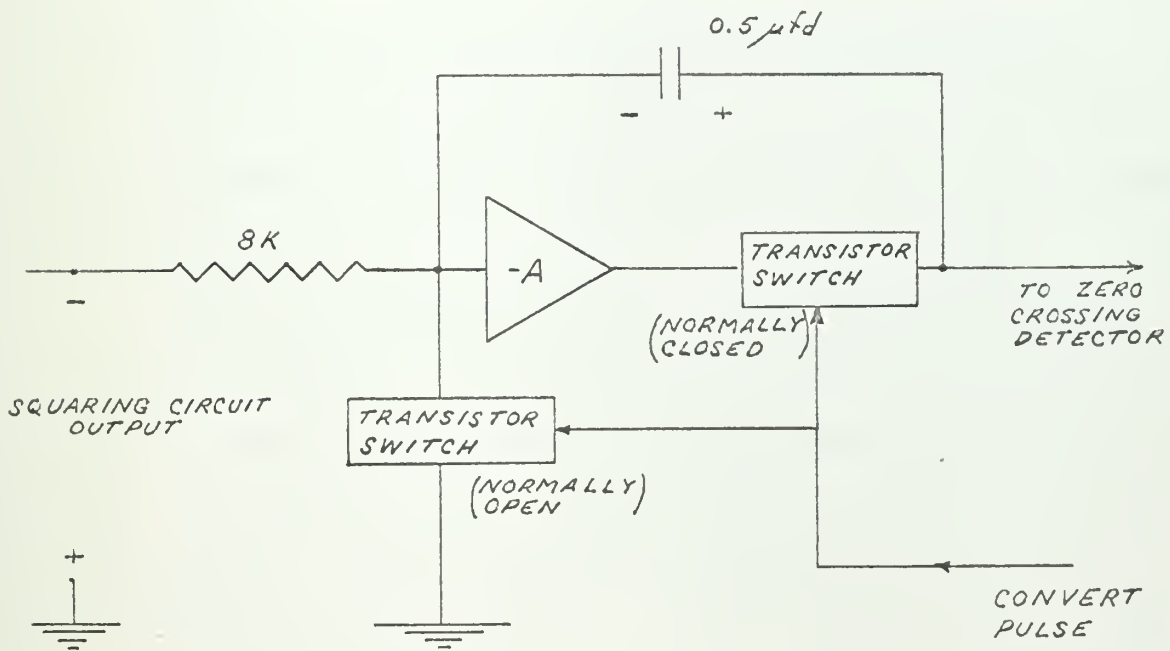FIG. A. 2-1   INTEGRATOR   CIRCUIT

FIG. A. 2-2   INTEGRATOR TO BE USED   IN DATA
              PROCESSING   SYSTEM

consumption is highest under this condition and it is desirable to make the load resistance greater. As will be shown in the discussion of the converter circuitry, a C of 0.5 μfd is preferred. Therefore, selecting an R of 8K, the integrator minimum and maximum magnitudes are given by 25 mv and 10 volts, respectively.

The conversion scheme is dependent upon the fact that one end of the capacitor holding the integrator output voltage is grounded. The floating ground existing in the integrator of Fig. A. 2-1 is insufficient. It will therefore be necessary to free the capacitor from the integrator after integration and prior to conversion. See Fig. A. 2-2.

The signal which accomplishes this switching can be actuated from the same threshold circuitry which transmits the convert pulse to the And gate.

A.III. Development of Constraints for the A/D Conversion Process

The problem of conversion can best be attacked by considering both the maximum and minimum voltages to be converted and by considering the maximum amount of time allowed for the conversion process.

Fig. A. 3-1 shows the relative timing of signals at various places in the system. The distance to the planet's surface will be such that the received echoes arrive during the 15 second period between bursts. Each one of the four received pulses will contain useful information and it is therefore desirable to process the information from one pulse before the next pulse arrives. We have seen that there is effectively no delay in squaring, nor should there be any delay involved in the integration process.

Examination of Fig. A. 3-1 indicates that the conversion to digital form must take place in no more than 16 msec. Our system constraints
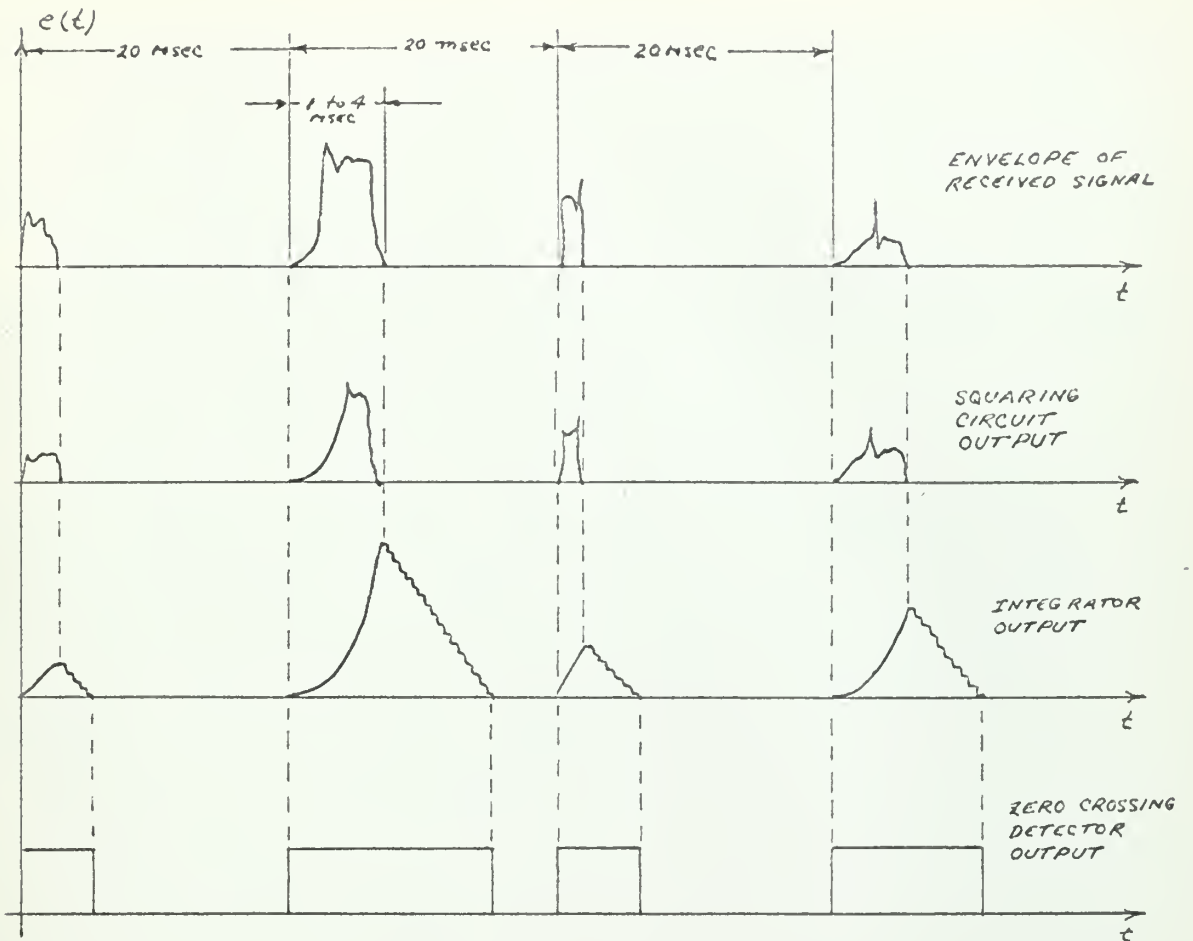
e(t)

20 msec ── 20 msec ── 20 msec

1 to 4 msec

ENVELOPE OF
RECEIVED SIGNAL

t

SQUARING
CIRCUIT
OUTPUT

t

INTEGRATOR
OUTPUT

t

ZERO CROSSING
DETECTOR
OUTPUT

t

FIG. A.3-1   TIMING   DIAGRAM

R

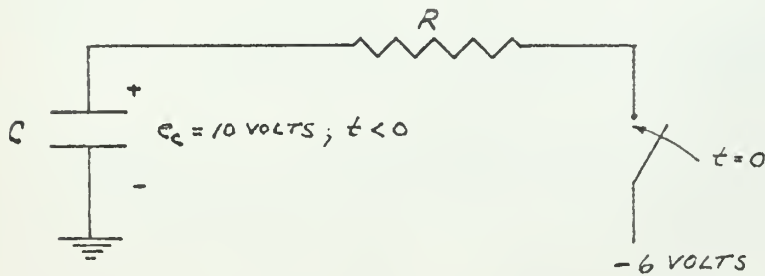C $e_c = 10$ VOLTS ; $t < 0$

$t = 0$

- 6 VOLTS

FIG. A.3-2   RC CIRCUIT WITH INITIAL CONDITIONS

- 57 -

are therefore twofold: 1) The conversion must take place in less than 16 msec. 2) The clock pulses must have a frequency and duration such that a 25 mv change of capacitor voltage is detected.

Maximum allowable conversion time is obviously related to the maximum voltage to be converted. Consider the RC circuit of Fig. A. 3-2 with an initial voltage of 10 volts on the capacitor.

Clearly, $e_c = -6 + (10 + 6) e^{-t/\tau}$ describes the natural decay of capacitor voltage at any time t. To be safe, let us demand that the conversion be completed in 10 msec. By making the off-on times of the clock pulses equal, this in effect requires that the voltage decay naturally to 0 volts in 5 msec. Hence:

$$0 = -6 + 16 \ e^{-5 \ msec/\tau}$$

$$\tau = 5.1 \ msec = RC$$

so let RC = 5 msec.

The requirement that the small signal level of 25 mv be detected and converted is important when considering the slope of the decaying capacitor voltage as it passes through zero.

Consider the following:

$$e_c = E_f + (E_i - E_f) \ e^{-t/\tau} \quad \text{where } E_f = E_{final} \text{ and } E_i = E_{initial}$$

$$\left. \frac{de_c}{dt} \right|_{e_c = 0} = 0 - \left(\frac{E_i - E_f}{\tau} \right) e^{-t/\tau} \Bigg|_{e_c = 0}$$

but at $e_c = 0$, $e^{-t/\tau} = \dfrac{-E_f}{E_i - E_f}$

so $\left. \dfrac{de_c}{dt} \right|_{e_c = 0} = + \dfrac{E_f}{\tau}$

It is important to note that this slope is independent of the initial
voltage on the capacitor. Therefore, near zero:

$$\Delta e = \frac{-6}{5.0 \text{ msec}} \Delta t$$ where Δe is the amount of voltage change
on C during a time interval Δt, which is the duration of one clock pulse.
Obviously, if it is desired to detect a useful signal level of 25 mv,
Δe must be no greater than 25 mv. On the other hand, the larger Δe is,
the greater the error which will exist if an extra clock pulse is
allowed through the And gate. Consider the situation where 25 mv exists
on the capacitor, and for some reason two pulses rather than one come
through the gate. This will allow e_c to decay to approximately -25 mv
rather than zero and will therefore cause an offset error in the next
integration. It is therefore better to have greater resolution near
zero. The following sections will show that 6 mv can be achieved in
practice.

There, allowing Δe = 6 mv

$$6 \text{ mv} = \frac{-6}{5.0 \text{ msec}} \Delta t$$

$$\Delta t = \frac{(6 \text{ mv}) (5.0 \text{ msec})}{6 \text{ volts}} = 5 \text{ } \mu\text{sec duration of clock pulses}$$

Allowing the on-off times of the pulses to be equal, this require-
ment will be satisfied by a 100 kc pulse generator.

Summarizing the constraints on the switching circuit:

1) RC = 5.0 msec

2) Pulse generator frequency = 100 KC

3) Clock pulse duration = 5 μsec

A.IV. The Zero Crossing Detector

The operational constraints imposed upon the zero crossing

detector circuitry are as follows:

a) It must have a very high input impedance to prevent the charged capacitor from leaking any charge to ground during periods when the transistor switch is open.

b) It must be able to detect as small an input as 25 mv on the capacitor, and transmit a constant signal into the And gate until the capacitor voltage drops below zero.

c) The delay between the time the detector recognizes the fact the capacitor voltage is less than zero and the time the pulse to the And gate is discontinued must be short to prevent additional clock pulses from passing through the gate and being counted in the binary counter. To be uncompromising and demand no error in this respect would require that this delay be less than 5 μsec, the time interval between clock pulses.

A prototype of the zero crossing detector has been designed and built. It consists of a differential amplifier with one input grounded, the output of which feeds a Schmitt Trigger. See Fig. A. 4-1. The differential amplifier is a modification of one designed by Joseph A. Bosco.

The circuit must handle an input of up to 10 volts, and therefore the Differential Amplifier will saturate. However, this should not cause any special problems since the diode in the collector of T_1 prevents current flow from base to collector when the input reaches that maximum level. The input impedance will drop from 1 Megohm to about 830 K during saturation, but this effect is negligible. Saturation has

- 60 -
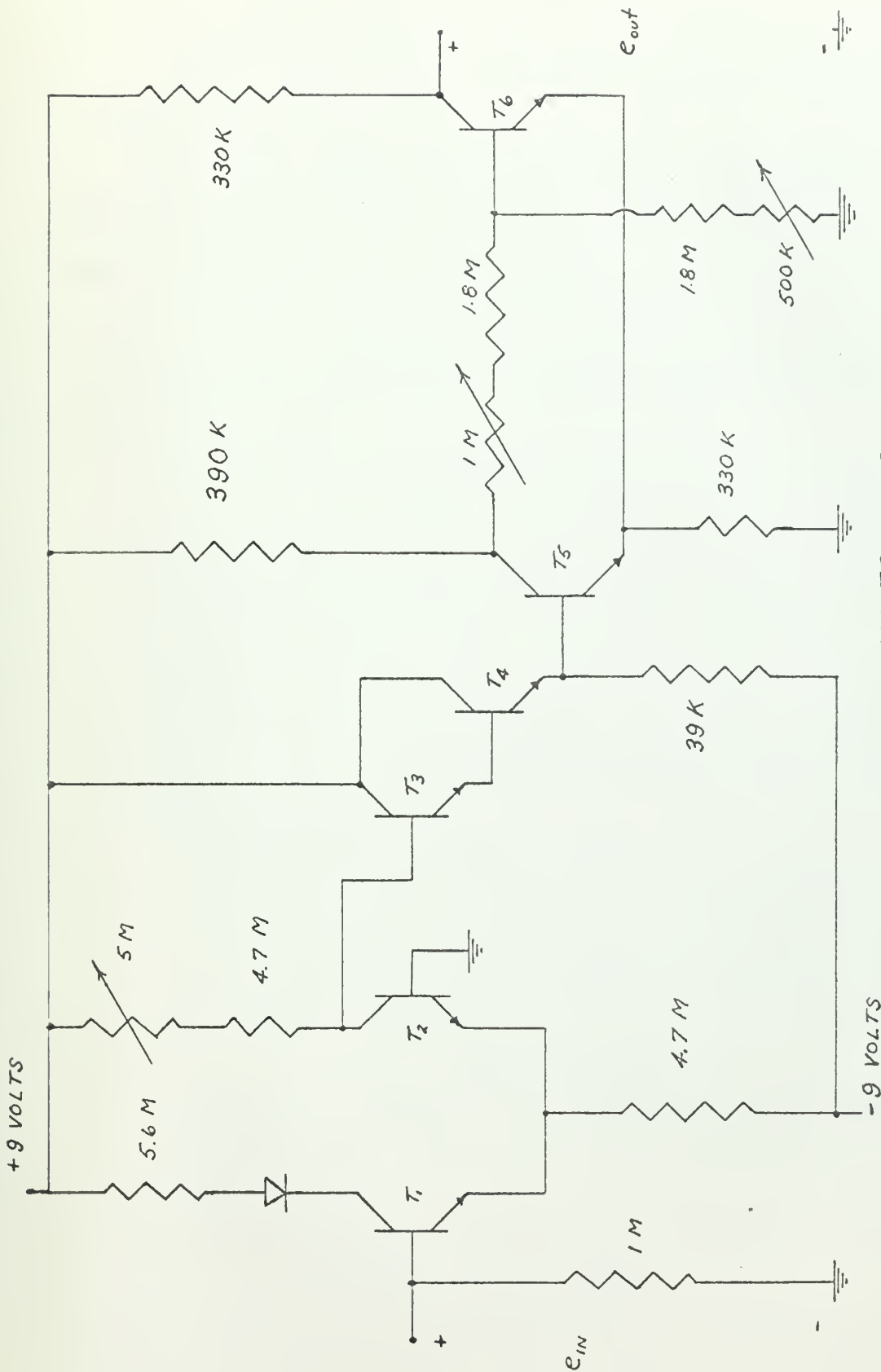
FIG. A. 4-1   ZERO CROSSING DETECTOR

absolutely no effect on the output pulse.

The input-output characteristic of the entire detector circuit is shown in Fig. A. 4-2.

The Schmitt trigger has been designed so that triggering can be made to occur from state OA (off and active for transistors T_5 and T_6 respectively) to state AO. This concept of triggering while a transistor is in an active state rather than a saturated state allows faster switching speeds because there is no excess charge to be removed from the base region.[8]

It is useful at this point to examine the error introduced by the finite input impedance of the circuit. Recall that the whole conversion scheme is based upon the assumption that the only capacitor voltage decay which exists is that through the resistor which is alternately being switched in and out by the clock pulses. In reality, with a maximum of 10 volts on the capacitor and an input impedance of 1 Megohm at the zero crossing detector:

Total conversion time: 10 msec

Time transistor switch is open = Time capacitor decays into input impedance of zero crossing   detector = 5 msec

hence, $e_c = -6 + 16 e^{-t/\tau}$

and t = 5 msec

where $\tau = 1$ Megohm$\cdot$C; it is obvious that the larger the C, the better;

set C = 0.5 µfd

$$\tau = (10^6)(0.5 \times 10^{-6}) = 0.5 \text{ sec}$$

and $e_c = -6 + 16 e^{-5 \text{ msec}/.5 \text{ sec}} = -6 + (16)(0.99) = 9.84 \text{ v.}$

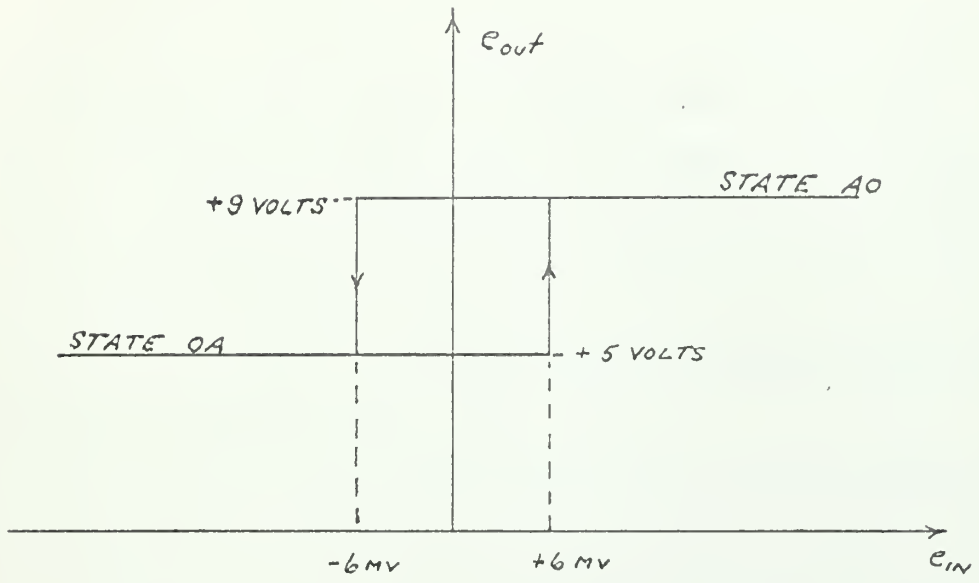FIG. A. 4-2   INPUT OUTPUT CHARACTERISTIC   OF ZERO
               CROSSING DETECTOR OF FIG. A.4-1.

so leakage error = 10v - 9.84v = 0.16v = 1.6%

This error is lower for all lower initial voltages on C since the time the capacitor faces the zero crossing detector is lowered accordingly. Calculations indicate that at mid range (e_c = +5 volts) the error due to leakage is 1.2% and at an initial capacitor voltage of 1 volt, the error is 0.3%.

The circuitry of Fig. A. 3-1 has not been optimized in any sense and the following comments apply:

1. A 40 μsec time delay exists between the time the input drops below -6 mv and the time the output changes state. This corresponds to a counting error of 4 pulses with a subsequent offset error on the next integration. It is not known at present if this can be tolerated; if not, the delay can be reduced by using smaller resistance values at the expense of greater power consumption.

2. It is likely that the 1 Megohm resistance at the input can be increased without affecting the circuit's operation. This will have the effect of reducing the leakage error.

3. The circuit has not been tested under a wide range of temperatures and most likely will require some compensation.

4. The output transition from +5 to +9 volts should be converted to a 0 to +2 volt step before it reaches the And gate.

A.V. The And Gate and Switching Circuit

Fig. A. 5-1 shows a preliminary design of this component, but the circuit has not been tested. It accepts a 0-2 volt pulse on each of its three inputs and should accomplish the necessary on-off switching
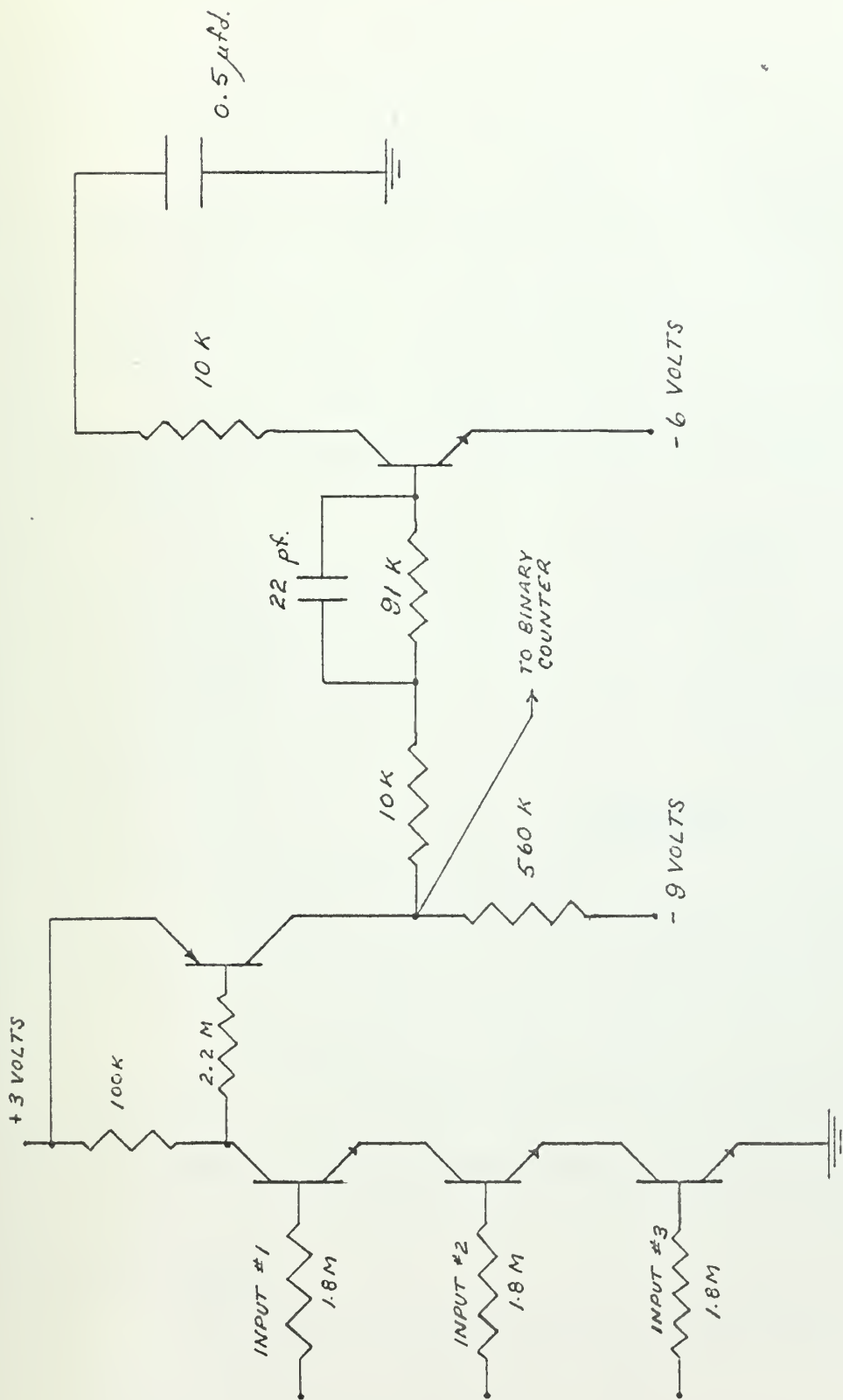
FIG. A.5-1. AND GATE AND SWITCHING CIRCUIT

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of the transistor in the capacitor decay circuit. Note that the previously developed constraints of $C = 0.5$ µfd and $\tau = 5$ msec demand that the resistance in the switching circuit be 10K.

For testing purposes, the input to the binary counter may be chosen any place beyond the And Gate and where sudden voltage transitions occur as a result of the clock pulses. The location indicated in the schematic is probably the most convenient.

To illustrate the manner in which the initial capacitor voltage is uniquely determined by the number of pulses counted, consider the following:

$$e_c = E_{final} + (E_{initial} - E_{final})e^{-t/\tau}$$

where $E_{final} = -6$ volts and $\tau = 5$ msec.

When the counter stops counting and the capacitor voltage is zero:

$$0 = -6 + (E_{initial} + 6)e^{\frac{-(x)(5 \text{ µsec})}{5 \text{ msec}}}$$

where x = number of pulses counted and 5 µsec = pulse duration hence:

$$E_{initial} = 6e^{+x/1000} - 6$$

This function can be plotted to give a curve of initial capacitor voltage versus number of pulses counted, thereby providing an easy way to test the circuitry.

A.VI. <u>Summary</u>

Summarizing the most important constraints developed in the preceding analysis:

<u>Integrator</u>:

$RC = 4$ msec; $C = 0.5$ µfd, $R = 8K$

Switching Circuit:

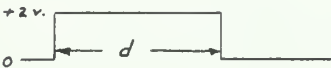RC = 5 msec; C = 0.5 µfd, R = 10K

Clock Pulses: f = 100 kc, pulse length = 5 µsec.

And Gate:

Input levels:

Convert Pulse:

Pulse Shape:

where 10 msec < d < 16 msec.

A suitable pulse length is 14 msec.

Figure A. 6-1 depicts the entire data processing system from the output of the squaring circuit to the input of the binary counter. It is emphasized that the zero crossing detector is the only circuit which has been tested, and as mentioned previously, it has not been optimized.

Nevertheless, the entire scheme as shown is a theoretically sound and practically feasible manner of accomplishing the analog to digital conversion.
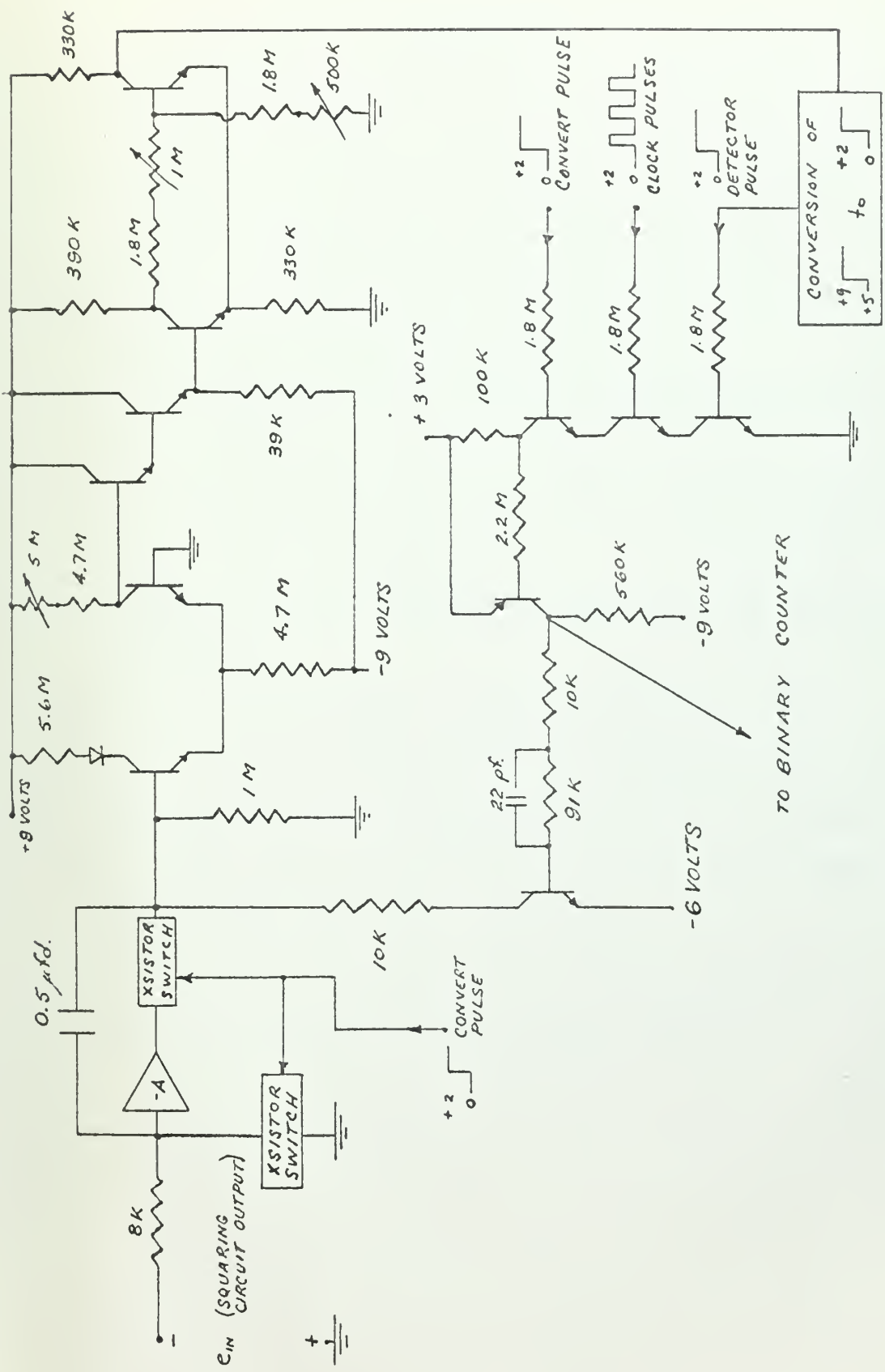
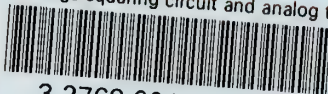FIG. A.6-1. INTEGRATOR AND ANALOG TO DIGITAL CONVERTER

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