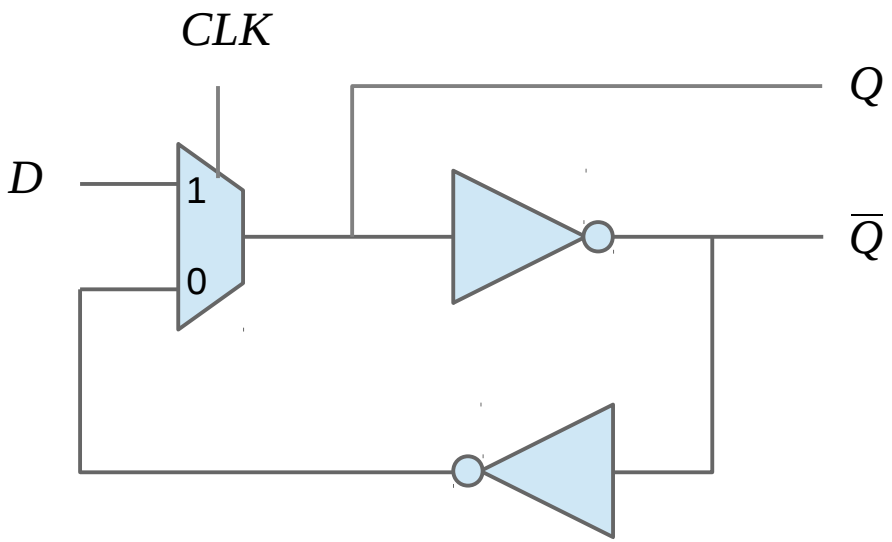
Sequential Gates

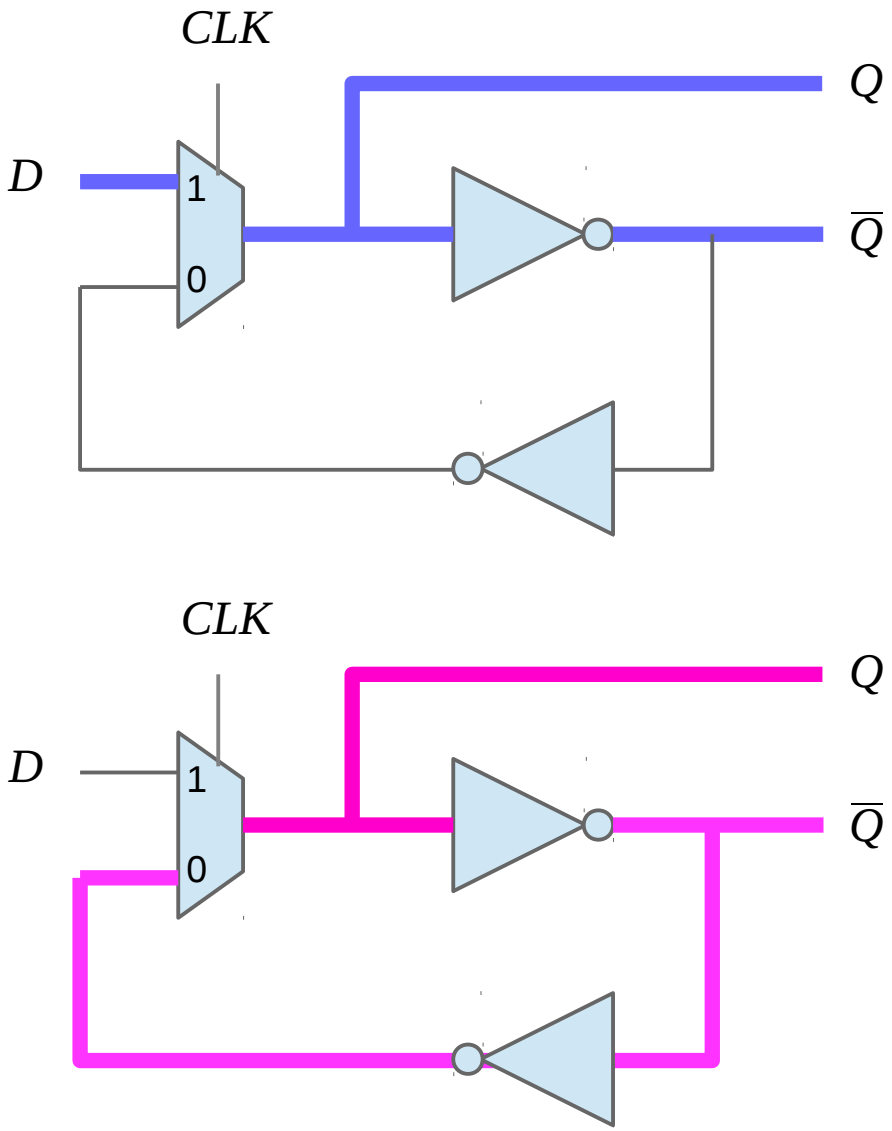
Please send corrections (or suggestions) to youngwlim@hotmail.com.

This document was produced by using OpenOffice and Octave.

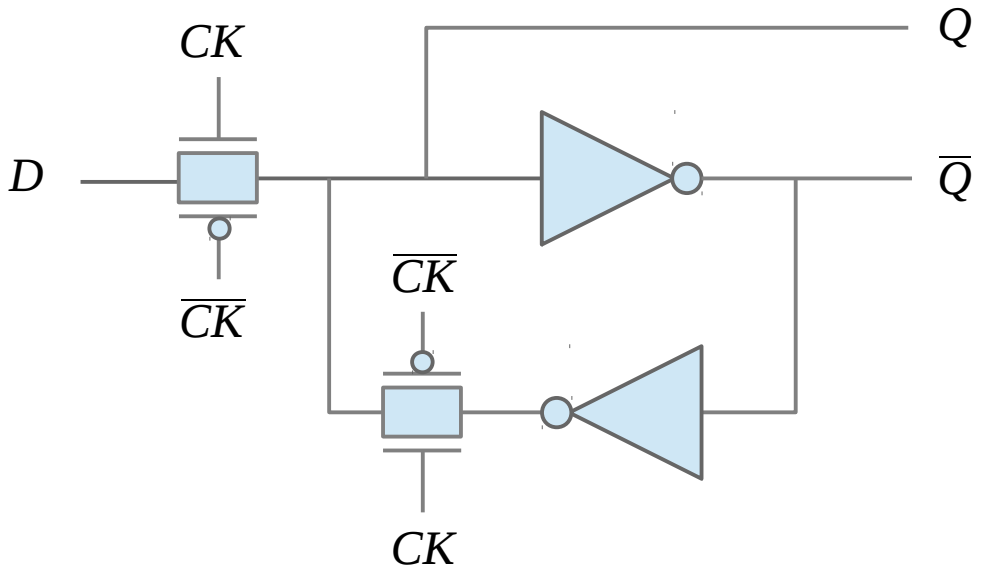
D Latch with Mux (1)



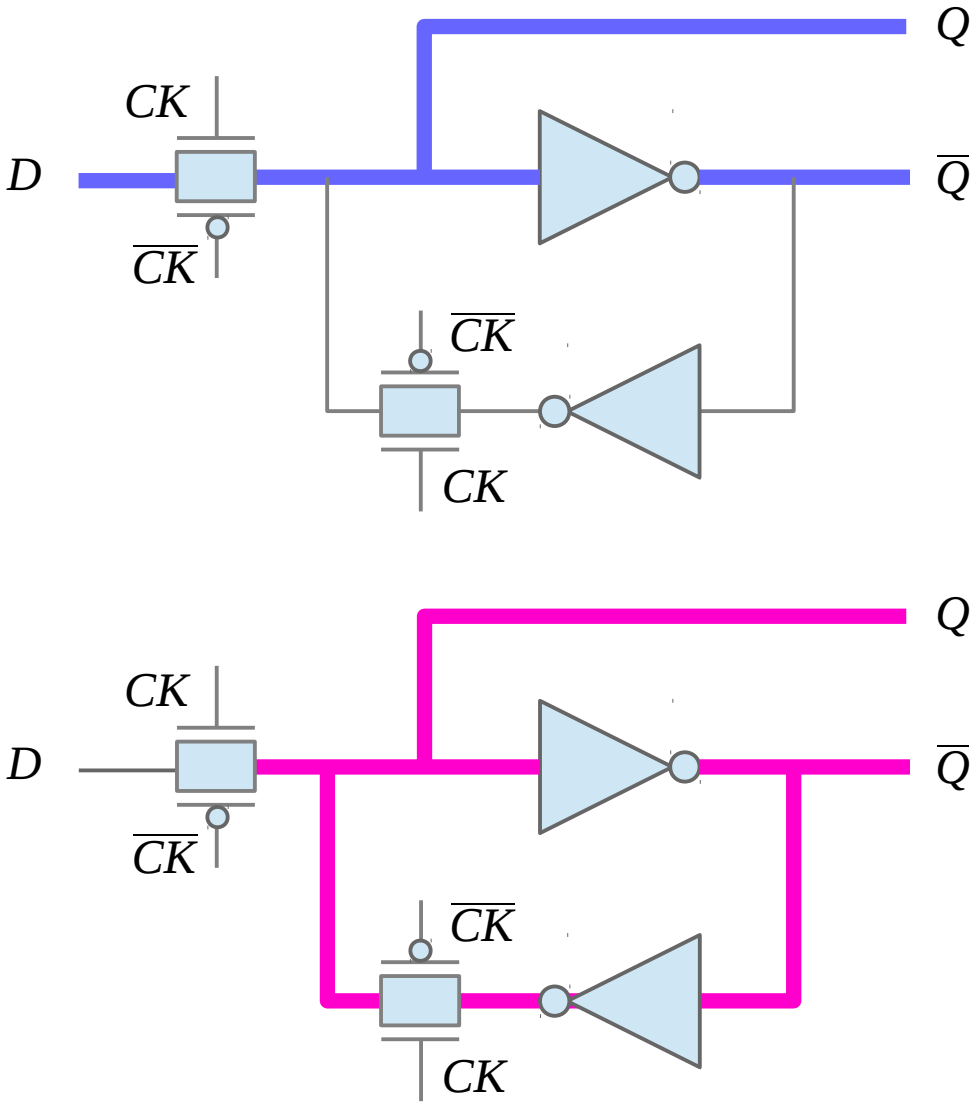
D Latch with Mux (2)



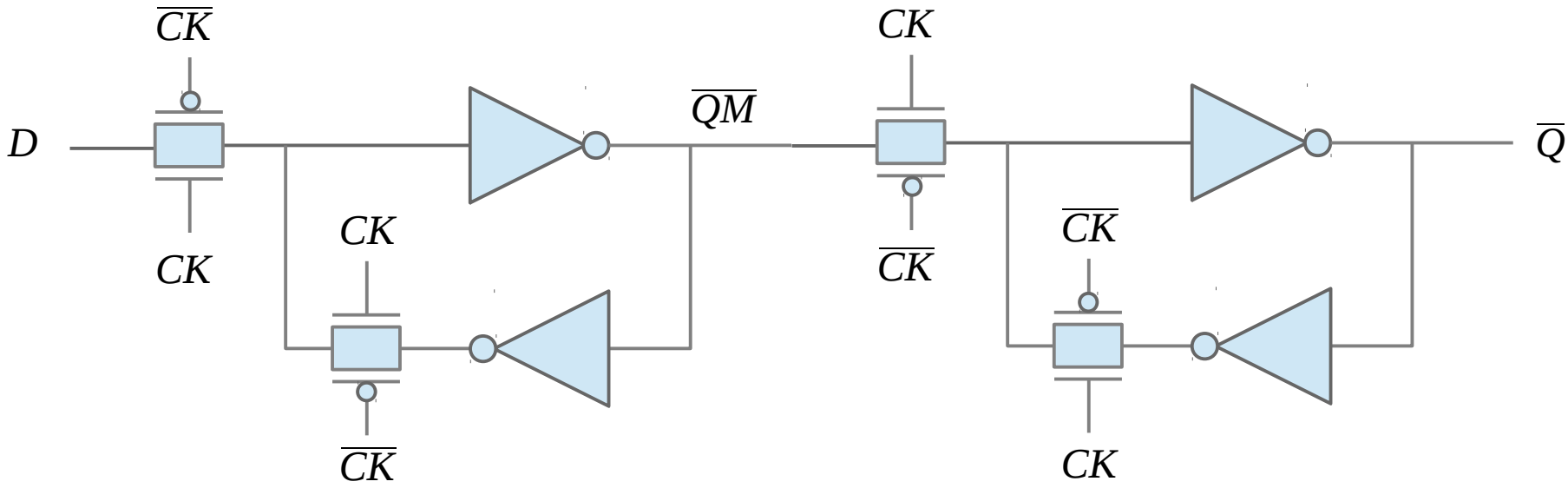
D Latch with Pass Gate (1)



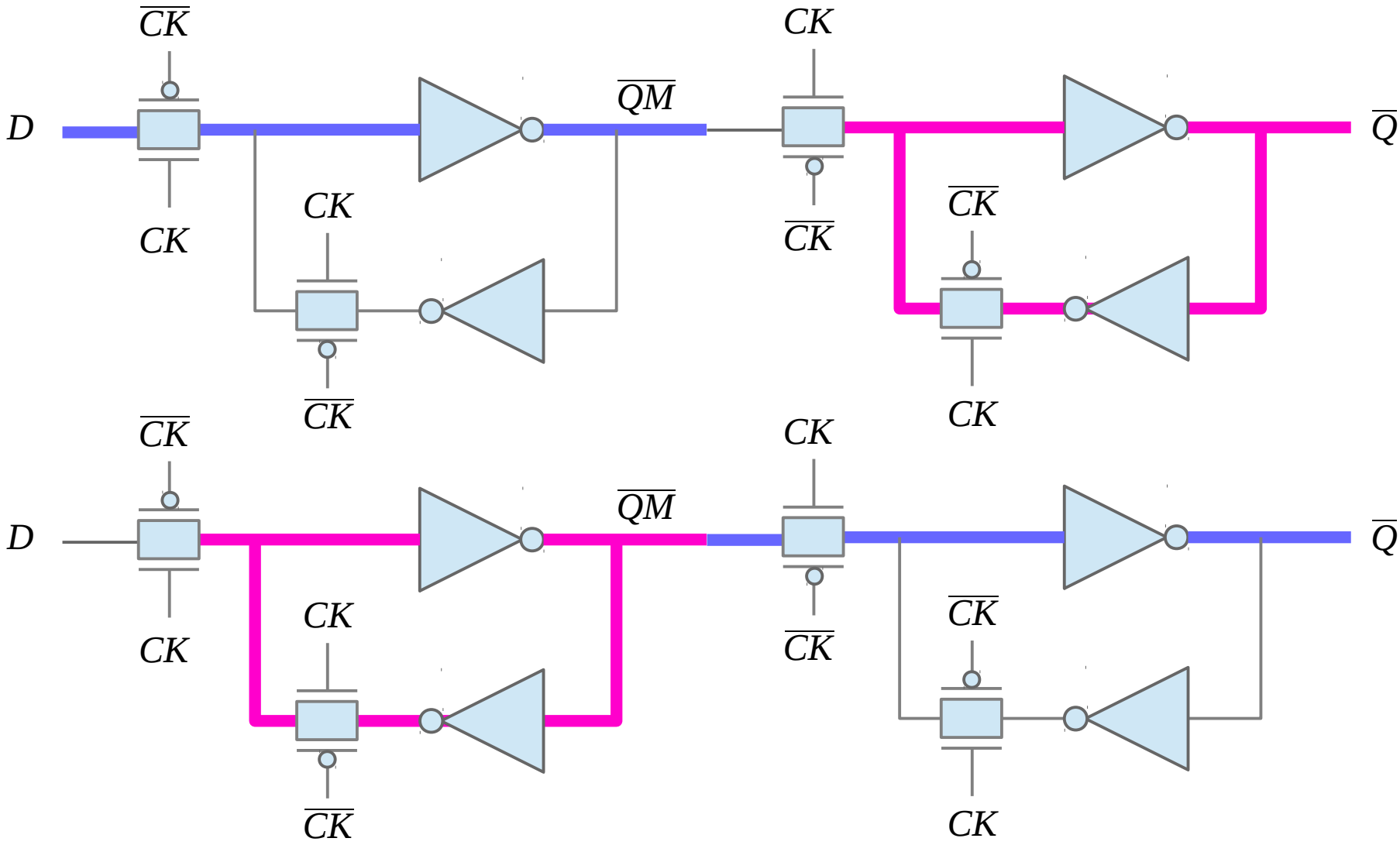
D Latch with Pass Gate (2)



D Flip Flop with Pass Gate (1)



D Flip Flop with Pass Gate (2)



Sequential Element Types

CMOS Latches
CMOS FlipFlops
Pulsed Latches
Latches and FlipFlops with a Reset
Latches and FlipFlops with an Enable

References

[1] http://en.wikipedia.org/
[2] http://www.allaboutcircuits.com/
[3] W. Wolf, “Modern VLSI Design : Systems on Silicon
[4] N. Weste, D. Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”
[5] J. P. Uyemura, “Introduction to VLSI Circuits and Systems”