aging procedure and the ensuing limitation of the frequency bandwidth have to be determined.

4) By modification of the equivalent bit test procedure a "maximum error" plot can be construed which allows for the specification of the digital filter.

5) The bandwidth of the digital filter compares favorably with that of an analog impulse oscilloscope designed for HV impulse test monitoring. This indicates the feasibility of the adaptation of presently available digitizers for monitoring impulse tests on non-self-restoring insulation such as power transformers.

ACKNOWLEDGMENT

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They are also obliged to B. Poulin and D. Gervais who performed the modified equivalent bit test on an actual digitizer.

REFERENCES

[1] *Techniques for High Voltage Testing*, IEC Pub. 60.
[2] T. M. Souders and D. R. Flach, "An automated test set for high resolution analog-to-digital and digital-to-analog converters," *IEEE Trans. Instrum. Meas.*, vol. IM-28, no. 4, pp. 239-244, Dec. 1979.
[3] R. Malewski, "Digital techniques in high-voltage measurements," Paper 82 WM254-1, presented at the IEEE PES Winter Meeting, 1982.
[4] T. M. Souders, "A dynamic test method for high resolution A/D converters," *IEEE Trans. Instrum. Meas.*, vol. IM-31, no. 1, pp. 3-5, Mar. 1982.
[5] N. A. Robin and B. Ramirez, "Capture fast waveforms accurately with a 2-channel programmable digitizer," *Electron. Des.*, no. 3, pp. 50-53, Feb. 1980.
[6] M. Neil and A. Muto, "Tests unearth a-d converter's real-world performance," *Electronics*, vol. 55, no. 4, pp. 127-132, Feb. 24, 1982.

High-Accuracy Settling Time Measurements

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***Abstract*—Methods are described for measuring the settling times and other dynamic characteristics of voltage and current output D/A converters (DAC's), operational amplifiers, and precision voltage step generators. Circuits are described for measuring voltage-output device settling times as short as 1 μs to within a settling error of ± 2 ppm, and current-output device settling times as short as 40 ns to within a settling error of ± 0.012 percent.**

I. INTRODUCTION

SETTLING TIME is an important measure of the dynamic performance of D/A converters (DAC's), operational amplifiers, and precision voltage step generators. Settling time for these devices can be defined as follows (see Fig. 1): Following a prescribed input change, usually full-scale range (FSR), the settling time of the device is the time required for the output to reach and remain within a given error band whose center coincides with the final value. Settling error is $\pm\frac{1}{2}$ the error band. For DAC's, the error band is usually $\pm\frac{1}{2}$ least significant bit (LSB). Note that part of the settling time is time interval $t_2 - t_1$, the delay of the output relative to the input. This definition is also applicable to voltage step generators, triggered at time t_1.

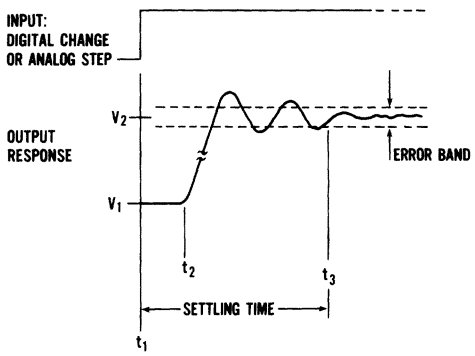

Fig. 1. Definition of settling time. Also applicable to voltage step generators, triggered at time t_1.

An additional measure of the dynamic performance of these devices is the offsets, thermal transients, and other recovery time effects caused by changes in repetition (or switching) rate, duty cycle, and output amplitude. These effects, as well as settling time, cause the device accuracy to be different under severe dynamic conditions than under, say, quasi-static con-

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ditions. Therefore, it is useful to have test methods for making accurate relative measurements as the device is exercised over a range of operating conditions.

This paper describes two circuits for measuring the settling time of voltage-output devices to within a settling error of ±2 ppm of FSR, and a circuit for measuring the settling time of fast current-output devices to within a settling error of ±0.012 percent of FSR. These circuits are generally suitable for comparing a device's voltage or current output immediately after a transition with the output at times up to at least a second after the transition, where essentially static conditions prevail.

II. Measurement Methods

A. Choice of Oscilloscope

The most detailed examination of voltage steps can be made using a wide-band oscilloscope with a sensitive vertical amplifier. Oscilloscopes designed for "real-time" measurements are available with maximum vertical deflection sensitivities ranging from 10 μV/cm to 2 mV/cm. Corresponding bandwidths are typically 1 and 200 MHz. Deflection sensitivies as high as 20 or 50 μV/cm are useful for settling time measurements. Since the voltage step illustrated in Fig. 1 can be as large as 20 V, devices for measuring settling time often employ a biased voltage divider to shift level V_2 to near zero potential and use various circuits to limit the output signal prior to the voltage transition. This shifting and limiting permits accurate measurement of voltage variations near the V_2 level and avoids overdrive of the oscilloscope prior to the transition [1], [2]. However, the effect of the transient that results during the transition V_1 to V_2 must be carefully evaluated.

Sampling oscilloscopes, which display the input signal in "equivalent time," have a maximum vertical sensitivity of approximately 2 mV/cm and a bandwidth of at least 1 GHz [3]. Since the minimum sampling period is sufficient to allow an overdriven vertical amplifier to recover between samples, the problem of overdrive is minimal for sampling oscilloscopes. Therefore, very fast voltage steps as large as (approximately) 2 V can be examined without limiting [4]. To prevent loading of the signal source by the low input impedance (50 Ω) of these units, an interfacing field-effect transistor (FET) probe or specially designed amplifier with high input impedance and 50-Ω output impedance is usually used. However, either a probe or amplifier may be susceptible to overdrive and adds noise and instability to the measurement system. Also, since sampling oscilloscopes are not suitable for observing low-frequency data, they cannot be used to compare the dynamic performance of a device with its quasi-static performance.

For the applications described in this paper, real-time (conventional) oscilloscopes have the advantages of high sensitivity, low noise, and excellent dc stability. Also, they can operate at very slow as well as fast sweep speeds. Their chief disadvantage is their susceptibility to overdrive from test circuit transients. A real-time oscilloscope was used in each of the settling time circuits to be described; however, for comparison, a sampling oscilloscope was also used with the fastest test circuit.

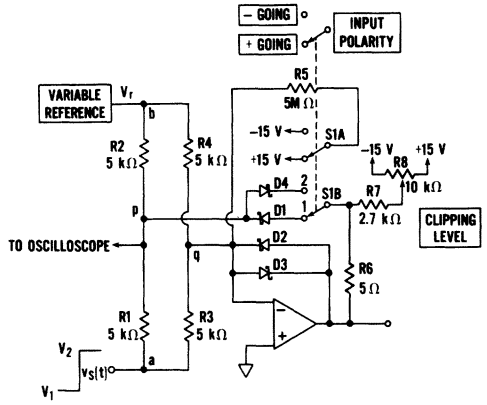

Fig. 2. Circuit for measuring settling times as small as 5 μs to a settling error of ±2 ppm. Circuit is insensitive to changes in switching rate, duty cycle, and amplitude of the input signal.

B. Voltage-Output Settling Time Test Circuits

Two circuits were developed for measuring settling times of voltage steps. The first circuit, shown in Fig. 2, can measure settling times as small as 5 μs to a settling error of ±2 ppm of 20-V FSR. The amplifier is used to limit the signal to the oscilloscope during these time intervals when the signal is not being viewed, but is effectively isolated from the signal when the voltage step is being viewed. If the settling time following the DAC voltage transition from V_1 to V_2 is to be examined, switch $S1$ is placed in position 1 and reference voltage V_r (opposite in polarity to V_2) is adjusted so that $|V_2|$ is slightly larger than $|V_r|$. The circuit operation is then as follows: Prior to the positive voltage step, $D1$ and $D2$ conduct. Diode $D2$ holds note q within microvolts of ground potential, and $D1$ holds node p within a few millivolts of ground. (The clipping level is adjustable by $R8$.) After $V_s(t)$ makes the transition to V_2, the output of the amplifier swings negative to about −0.3 V, reverse biasing $D1$ and $D2$. Thus node p is isolated from the amplifier circuit, leaving only resistance in the signal path to the oscilloscope. The bias current supplied to node q via $R5$ serves to shorten the amplifier switching time when voltage $V_s(t)$ approaches V_2. Also, Schottky-type diodes are employed to yield fast switching. To view negative-going steps, the switch is put in position 2. The oscilloscope used with this circuit was characterized by low noise (~8 μV rms), a bandwidth of 1 MHz, and a sensitivity of 100 μV/cm. This deflection sensitivity corresponds to 0.4 cm/LSB when testing an 18-bit DAC with a 20-V full-scale range (FSR).

The above test circuit was used to measure the settling time and recovery time effects of the NBS DAC-18 (18-bit D/A converter standard), now used as a check standard for the NBS Data Converter Test Facility [5]. The circuit has also been used to test a number of commercial 16- and 18-bit DAC's. (See Section II-C for performance verification of this test circuit.)

Other techniques for measuring the settling time of voltage-output DAC's are described in [2], [6], and [7].

A second, faster circuit shown in Fig. 3 was designed to measure DAC settling times in the 1–5-μs range to within a settling error of ±2 ppm of 20-V FSR. This circuit was also required for measuring the settling time of the voltage step

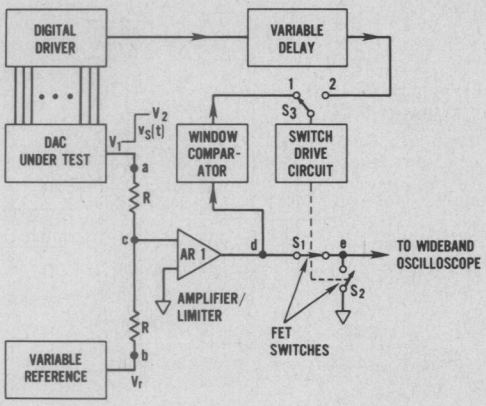

Fig. 3. Circuit for measuring settling times in the 1–5-μs range to a settling error of ±2 ppm.

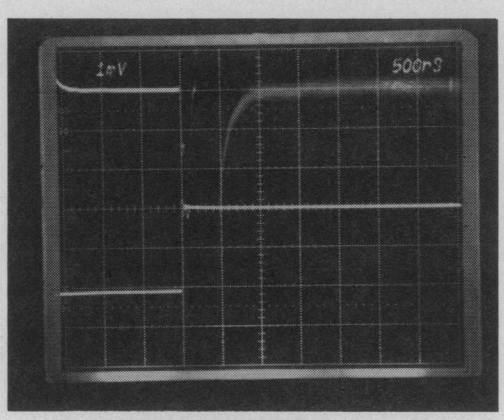

Fig. 4. Voltage response at node e, Fig. 3, to 10-V step applied to nodes a and b (DAC and reference disconnected). Settling time T_t is ~0.9 μs to a settling error of ±2 ppm.

generator employed in the NBS Data Converter Test Facility to dynamically test A/D converters [8]. The circuit basically consists of the following: 1) a precision voltage divider for comparing input signal levels, V_2, up to ±10 V with reference voltages, V_r, of the same nominal magnitude but of opposite polarity; 2) a wide-band amplifier ($AR1$) for amplifying the signal output from the divider center tap, which has a gain of 10 for very small values of $|V_s(t) + V_r|$; and 3) transistorized series and shunt switches (S_1 and S_2), which connect the oscilloscope to either the amplifier output or signal ground (0 V), respectively. These switches are controlled by a window comparator which senses the magnitude of the output voltage from the amplifier, thus avoiding overdrive of the measuring device by excessively large signals. Switch $S1$ closes and $S2$ opens when the magnitude of the voltage at node d decreases to ~10 mV. If control of the switching time is desired, the switch drive circuit can also be triggered (via switch $S3$, position 2) by the digital driver through a variable delay circuit. This configuration permits the settling waveform to be observed at selectable points in time. Use of $AR1$ permits a lower sensitivity (1-mV/cm), wider bandwidth (100-MHz) oscilloscope to be used than was employed in the circuit shown in Fig. 2.

To minimize the settling time of the amplifier and switch circuits, Schottky clipping diodes (not shown) are employed to limit the input and output signals of the amplifier at nodes c and d, as well as its gain, when $|V_s(t) + V_r|$ is large. As with most operational amplifiers with a gain–bandwidth product larger than about 500 MHz, amplifier $AR1$ (and, therefore, the test set) experiences significant recovery time effects when exercised over a wide range of operating conditions. Therefore, the test circuit shown in Fig. 2 is preferred over the above circuit for recovery time measurements on voltage-output devices.

C. Performance Verification

The flat pulse generator described in the Appendix was used to determine the settling time (T_t) of several test circuits. For the circuit in Fig. 2, T_t is 3.5 μs to within a settling error of ±2 ppm, using an oscilloscope with 1-MHz bandwidth, 100-μV/cm sensitivity, and 50-pF input capacitance (including connecting cable). This circuit is useful for estimating device

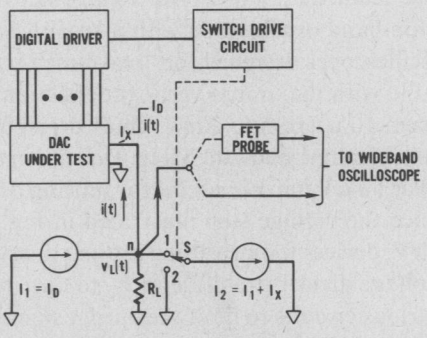

Fig. 5. Test circuit for measuring current-output DAC settling times as small as 40 ns to within ±0.012 percent.

settling time (T_d) as small as ~5 μs; however, if the observed settling time (T_m) is less than 10 μs, a more accurate estimate of T_d can be obtained from the approximation, $T_d \simeq \sqrt{T_m^2 - T_t^2}$ (see Appendix). Recovery time effects in this circuit were measured for switching rates ranging from 1 Hz to 100 kHz and duty cycles ranging from ~0.1 to ~0.9, using voltage steps from the flat pulse generator (with V_m = 10 V and C = 0). No shift in the output greater than ±20 μV (±2 ppm) was observed during these tests.

The settling time T_t was determined for the circuit configuration shown in Fig. 3 and $S3$ in position 1. The upper trace of Fig. 4 shows the voltage at node e following an input transition (lower trace) from −10 to 0 V. Since $AR1$ has a small-signal gain of 10, the effective deflection sensitivity for the upper trace is 100 μV/cm and one small division corresponds to 2 ppm of 10-V FSR. Hence, $T_t \simeq 0.9$ μs. When this circuit is used to estimate the settling time T_d of a device, $T_d \simeq T_m - T_t$, where T_m is the observed settling time (see Appendix).

D. Current-Output Settling Time Test Circuit

The circuit shown in Fig. 5 was developed to measure the settling time of high-speed current-output DAC's. Upon command, the digital driver switches the DAC under test from an output current of I_x to a current level of I_D. At the same time, the switch drive circuits change switch S from position 1 to position 2. When $i(t) = I_D$, current I_1 is set equal to I_D by adjusting I_1, for zero-output voltage. Prior to the transition to

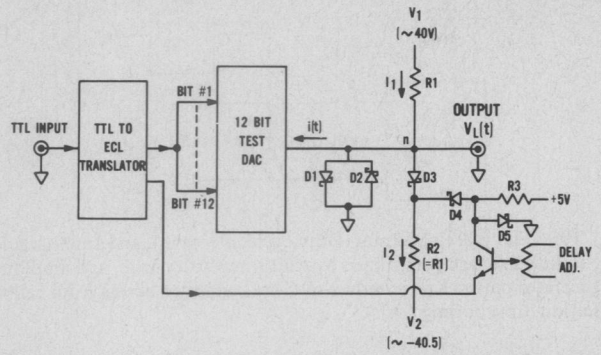

Fig. 6. Detailed diagram of test circuit shown in Fig. 5 for the special case of switching the test DAC between all bits off and all bits on. Current I_2 is switched from $D3$ to $D4$ when the DAC current is turned on.

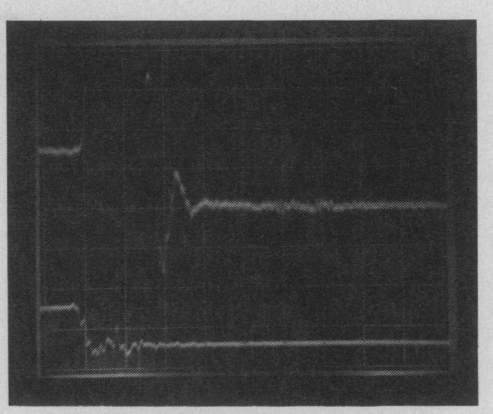

Fig. 7. Oscilloscope photograph showing output settling of commercial DAC. Vertical sensitivity is 2 mV/cm (~4 LSB's/cm). Horizontal time base is 20 ns/cm. Upper trace shows settling of $V_L(t)$ for an FSR change in DAC current. Voltage $V_L(t)$ is delayed 9 ns relative to ECL signal (lower trace).

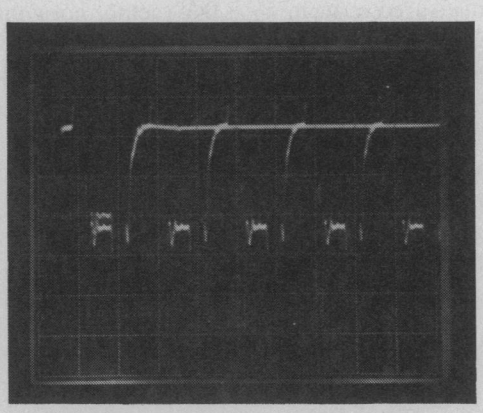

Fig. 8. Oscilloscope photograph showing offset in DAC output, with bits on, caused by change in switching rate. Measured $V_L(t)$ is 0 V (center horizontal graticle line) for 160-kHz switching rate and −1.2 LSB's when rate is 10 MHz. Bit ON time is constant at 100 ns. No FET probe was used.

I_D, when $i(t)$ is equal to I_x, I_2 is adjusted so that $I_2 = I_1 + I_x$. For example, if the test DAC is connected for bipolar operation and switches from $-I_D$ to $+I_D$, I_2 should be set to approximately $2I_D$. The oscilloscope used with this test set was characterized by low noise (~0.1 mV rms), a bandwidth of 200 MHz, and an input capacitance of 20 pF. The unity-gain FET probe has a bandwidth of 900 MHz, and was used to reduce the capacitive loading of the oscilloscope to 3 pF. The vertical deflection sensitivity used for all of the measurements was 2 mV/cm. A socket was used in the test set to facilitate substitution of DAC's.

A detailed diagram of this test circuit is shown in Fig. 6 for the special case of switching the test DAC between all bits off and all bits on. The TTL-to-ECL translator is used to drive the emitter-coupled logic employed in most very fast DAC's. The translator also supplies the drive current for transistor Q, which is turned off when the DAC bits are turned on. Turning Q off transfers I_2 from $D3$ to $D4$. Since the current switching in the DAC may be slower than the switching of I_2 from $D3$ to $D4$, the latter may be delayed up to 3 or 4 ns by the delay (bias) adjustment to minimize the switching transient at the output. A small trimmer capacitor (not shown) connected between the collector of Q and ground may also be used for this purpose. Diode $D5$ is used to limit the reverse voltage applied to $D3$ by limiting the positive voltage excursion at the collector of the transistor. Diodes $D1$ and $D2$ serve to protect the DAC from transients at node n when applying V_1 and V_2. Since the nominal value of $V_L(t)$ at the output is approximately 0 V before and after switching I_2 and the intervening switching transient can be adjusted for a small average value by the delay adjustment, overdrive of the FET probe and oscilloscope vertical amplifier are minimized.

Fig. 7 is an oscilloscope photograph which shows the response of a commercial state-of-the-art 12-bit current-output DAC for an FSR change (sweep speed is 20 ns/cm). The FSR was 10 mA and the 200-Ω output resistance of the DAC served as the load resistance R_L. Therefore, a 1 LSB change in DAC current (0.024 percent of FSR) causes an output voltage change of 0.48 mV, or a deflection change of 0.24 cm. Using the 50-percent amplitude point of the ECL input signal to the DAC (lower trace) as the zero time reference, the output voltage (upper trace) appears to settle to within $\pm\frac{1}{2}$ LSB of the final value approximately 50 ns later. Since the ECL signal was delayed ~2 ns by a connecting cable to the oscilloscope and the specified delay of the FET probe is 11 ns, the net delay of $V_L(t)$ relative to the ECL signal was ~9 ns. Therefore, the measured settling time of the test DAC is ~41 ns.

The same DAC, soldered directly into a printed circuit board, may have a slightly smaller settling time because of shorter input and output lead lengths. Also, measurements indicate that the settling time decreases from 41 ns to about 38 ns as R_L is decreased from 200 to 50 Ω. The 38–41-ns range of settling times measured with this technique is in good agreement with the manufacturer's specification.

The measurement shown in Fig. 7 was repeated, substituting a sampling oscilloscope for the conventional oscilloscope (see Fig. 5), to determine whether the latter instrument was being overdriven. The settling transient and settling time were essentially the same as shown in Fig. 7; hence, it appears that the conventional oscilloscope was not overdriven.

The test circuit shown in Fig. 6 is also well suited for measuring offsets, thermal transients, and other recovery time effects as the test DAC is exercised over a wide range of operating conditions. For example, Fig. 8 shows the offset in $V_L(t)$ caused by changing the DAC switching rate from 160 kHz to 10 MHz. For this test, the bit ON time was held con-

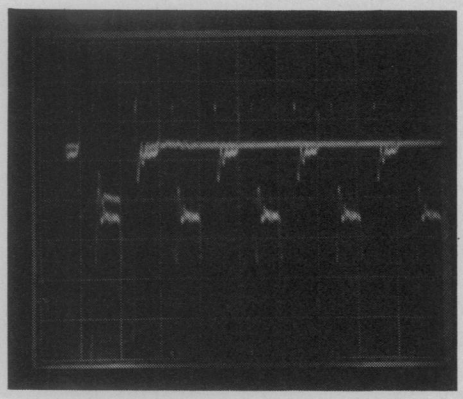

Fig. 9. Measurements shown in Fig. 9 repeated using FET probe. Change in DAC switching rate causes offset in probe (present during both bit ON and OFF times) as well as in DAC.

stant at 100 ns and the OFF time was varied from 6.2 μs to 100 ns. The measured value of V_L is 0 V (center horizontal graticule line) when the switching rate is 160 kHz and is approximately -1.2 LSB's when the rate is 10 MHz. This offset is attributed to the DAC, and not the oscilloscope (used without a FET probe), since no offset change is perceptible during the time intervals when the DAC bits are off. The offset decreases with lower switching rates and is negligible below 2 MHz. These measurements were repeated using an FET probe (Fig. 9). It is seen that the offset contributed by the probe (present during both bit ON and OFF times) is about 0.8 LSB.

Other techniques for measuring the settling time of current output DACs are described in [9]–[11].

III. Conclusion

Circuits have been described for measuring voltage-output device settling times as short as 1 μs to within a settling error of ± 2 ppm of FSR and current-output device setting times as short as 40 ns to within a settling error of ± 0.012 percent of FSR. When a device under test (DUT) is measured for settling time, the output may exhibit offsets, thermal transients, and other recovery time effects when the DUT is exercised over a wide range of operating conditions. These recovery time effects on the DUT are not easily quantified unless the settling time measuring circuit itself (including the oscilloscope) is essentially free of these defects. These defects have been minimized with the measurement methods described in this paper and appear to be less than $\pm\frac{1}{2}$ LSB for the test circuits shown in Figs. 2 and 5 (used without a probe) corresponding to ± 2 and ± 120 ppm, respectively. Both of these circuits are used with an oscilloscope which was selected for low noise and minimal susceptibility to overdrive. The low-noise oscilloscope makes it feasible to measure small voltage changes using a relatively small deflection sensitivity. Reducing the oscilloscope sensitivity, in turn, minimizes the overdrive from test circuit transients. Also, no preamplification was used in either test set to minimize settling time effects in the test circuit itself when exercised over a wide range of operating conditions.

Appendix

Schottky diodes have been used in conjunction with both voltage and current pulse generators [12], [13] to generate fast, high-quality voltage steps which are needed to accurately measure the settling times of amplifiers and other circuits. A version of this type of "flat pulse generator" is shown in Fig. 10. In this circuit, a commercial pulse generator (rise and fall times: ~3 ns) with adjustable high and low voltage levels is used in conjunction with a Schottky diode (D) to generate a voltage step from level $+V_m$ to 0 V, where V_m is adjustable up to 10 V. The diode serves to "disconnect" the pulse generator from resistor R when the generator output is approximately 0 V, so that $V_0(t)$ is a flat, well defined voltage level of 0 V during time interval b. The pulse applied to the diode is adjusted to return to a slightly negative value during time interval b to ensure that small pulse generator voltage variations do not cause forward conduction in D. Also, five parallel diodes were actually used for D to minimize diode heating and consequent reverse conduction under conditions of large V_m and large duty cycle (duty cycle = $a/(a+b)$). Reversed diode polarity and voltage levels complementary to those just described are used to generate a voltage step from $-V_m$ to 0 V.

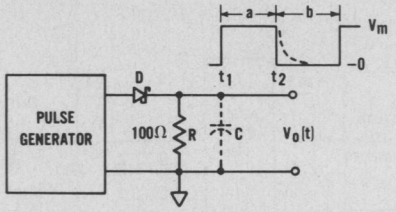

Fig. 10. Flat pulse generator. Duty cycle, $a/(a+b)$, and amplitude V_m of output pulses are determined by width, repetition rate, and amplitude of generator pulses. Known values of C are connected across R for calibrated settling time at time $t = t_2$.

The settling time of the voltage transition at time T_2 can be adjusted by shunting R with known values of C. Using pulses with a range of known settling times, this flat pulse generator was used to determine the responses of the test circuits shown in Figs. 2 and 3. (The variable reference and device being tested are disconnected and the flat pulse generator output is connected to nodes a and b.) For the circuit shown in Fig. 2, the response is given approximately by

$$T_m \simeq \sqrt{T_d^2 + T_t^2}$$

or

$$T_d \simeq \sqrt{T_m^2 - T_t^2}$$

where T_m is the observed settling time when measuring a settling time T_d, and T_t is the settling time of the test circuit. Settling time T_t is defined as the limiting value of T_m as T_d approaches zero. A sufficiently accurate value of T_t is obtained if T_d is less than 50 ns. Correspondingly, for the circuit shown in Fig. 3, the response is, approximately,

$$T_m \simeq T_d + T_t$$

or

$$T_d \simeq T_m - T_t.$$

Thus a device settling time T_d is determined from the measured (observed) settling time, corrected for the settling time of the test circuit itself.

When measuring settling times to a settling error of ± 2 ppm of FSR, considerable care must be taken to avoid unwanted ground currents between the instruments and circuits used in

a test setup. Ground currents can slow the settling time of voltage steps applied to a test circuit or the output voltage to be measured.

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REFERENCES

[1] A. G. Perrey and H. K. Schoenwetter, "A Schottky diode bridge sampling gate," Nat. Bur. Stand (U.S.) Tech. Note 1121, May 1980.
[2] J. A. Whealler, "A new technique for testing settling time in a production environment," in *Dig. 1981 Int. Test Conf.* (Philadelphia, PA, Oct. 1981).
[3] Tektronix, Inc., Instruction manual for "7S14 Dual Trace Delayed Sweep Sampler" (Beaverton, OR, 1973).
[4] Tektronix, Inc., "DAC measurements: The sampling oscilloscope approach," Sampling Appl. Note 42K1.0 (Beaverton, OR, 1977).
[5] T. M. Souders, D. R. Flach, and B. A. Bell, "A calibration service for analog-to-digital and digial-to-analog converters," Nat. Bur. Stand. (U.S.) Tech. Note 1145, July 1981.
[6] Teledyne Philbrick, "Specifying and testing digital-to-analog converters," Bull. AN-25 (Dedham, MA 1976).
[7] D. H. Sheingold, Ed., *Analog—Digital Conversion Notes.* Norwood, MA: Analog Devices, Inc., 1980, pp. 207–211.
[8] T. M. Souders, D. R. Flach, and T. C. Wong, "An automatic test set for the dynamic characterization of A/D converters," this issue, pp. 180–186.
[9] Burr-Brown, "DAC 63, ultra-high speed digital-to-analog converter," specifications and applications information (Tucson, AZ., 1981).
[10] D. B. Bruck, *Data Conversion Handbook.* Burlington, MA: 1974, pp. 2-51, 2-52.
[11] Precision Monolithics, Inc., "DAC-10, 10-bit high speed multiplying D/A converter," specifications and applications information (Santa Clara, CA, 1980).
[12] J. R. Andrews *et al.* "Survey of present waveform sampling system limitations," NBS Rep. 10731, Feb. 1972.
[13] J. R. Andrews, B. A. Bell, N. S. Nahman, and E. E. Baldwin, "Reference waveform flat pulse generator," this issue, pp. 27–32.

Reference Waveform Flat Pulse Generator

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***Abstract*—The NBS Reference Flat Pulse Generator (RFPG) is used to transfer dc voltage and resistance standards to the nanosecond domain. It provides a step amplitude of 1.000 V (open circuit) from a source impedance of 50.0 Ω. The transition duration is 600 ps, and all perturbations are damped out to less than ±10 mV within 5 ns. It can also be used as a time interval transfer standard.**

INTRODUCTION

THE NEED FOR a reference step-like generator has become increasingly important for accurately characterizing the step response of oscilloscopes, transient recorders, and fast sampling channels of digital measurement instruments and automatic test equipment (ATE). By comparing the measurement waveforms and/or data with those of a reference waveform, the fidelity with which the measurement system can acquire the waveform can be determined. The dynamic performance of a measurement system is often desired, together with its ability to measure dc or steady-state quantities.

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From a practical point of view, it is often desirable to be able to calibrate the dc voltage levels of the measurement system, as well as any time-dependent parameters. For this reason a voltage step function, whose beginning and ending dc levels are calibratable, has considerable merit as a reference standard, particularly if the transition between these two levels is also well behaved and predictable. Such was the purpose for developing the Reference Flat Pulse Generator (RFPG) at NBS.

AVAILABLE WAVEFORM

In theoretical time-domain studies the ideal unit step generator is commonly used as a driving source. However, in experimental work the ideal generator must be replaced by a physically realizable one, i.e., a step-like transition generator.

The voltage step-like transition generator produces a noninstantaneous voltage transition from an initial voltage level to a final one. An equivalent circuit for the voltage transition generator may be characterized in terms of the step response $E_g(s)$ of a four-terminal network having a voltage transfer