MICROCOMPUTER BASED
SOLID STATE CRASH DATA RECORDER
FOR MILITARY AIRCRAFT

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THESIS

MICROCOMPUTER BASED
SOLID STATE CRASH DATA RECORDER
FOR MILITARY AIRCRAFT

by

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Thesis Advisor: U. R. Kodres

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The microcomputer provides an expansion capability for future applications of the flight recorder. Research and development, structural history, maintenance analysis, and training are areas where the Crash Data Recorder can also serve as an analytical tool.

Continued research in this subject is highly recommended.

Microcomputer Based Solid State Crash Data Recorder For Military Aircraft

by

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Lieutenant, United States Navy
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requirements for the degree of

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The design, breadboard implementation, and functional testing of a Crash Data Recorder for military aircraft is reported. A microcomputer is used to analyze the flight parameters, reduce redundant data, and record only significant information to be used in post-crash analysis. Non-volatile solid state memory is used as the recording medium. Functional tests indicate that the solid state recorder's reliability is higher than that of mechanical magnetic tape recorders while cost, weight, size, and required maintenance are greatly reduced.

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LIST OF ACRONYMS

AIRS	Accident Investigation Retrieval System
BITS	Binary Digits
BORAM	Block Oriented Random Access Memory
CDR	Crash Data Recorder
CPI	Crash Position Indicator
EARAM	Electrically Alterable Random Access Memory
FDR	Flight Data Recorder
FIR	Flight Incident Recorder
GDRU	Ground Data Reduction Unit
IGFET	Insulated Gate Field Effect Transistor
MBR	Memory Buffer Register
MIL STD	Military Standard
MNOS	Metal Nitride Oxide Semiconductor
MOS	Metal Oxide Semiconductor
PL/M	Programming Language for Microcomputers
RAM	Random Access Memory
ROM	Read Only Memory
TTL	Transistor-Transistor Logic
UL	Universal Locator
ULAIDS	Universal Locator-Airborne Integrated Data System
VINRAM	Virtually Nonvolatile Random Access Memory

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I. INTRODUCTION

The continual growth of military aviation has resulted in the design of aircraft which are safer and far more reliable than those of the past. Unfortunately, aviation accidents continue to occur in the military community. The United States Navy loses an average of 80 aircraft per year whose cost exceeds 120 million dollars.

During a period of three years, 1973 to 1975, 42 Naval aircraft were lost as a result of an identical malfunction. These losses represent approximately four operational squadrons and a cost of 65 million dollars. Since most of the aircraft involved in these accidents were completely destroyed, little knowledge could be gained from the wreckage to identify the causal factors. A flight data recorder aboard these aircraft could have provided sufficient information to prescribe the necessary improvements required to prevent accident repetition.

The loss of high value aircraft and the priceless loss of aircrew life involved in accidents continues, while a reliable source of accident information is still not available. The last communications received, and the recovered wreckage, no longer produce sufficient information to determine the accident causes of modern, high performance, military aircraft.

Unlike the commercial airlines, few military aircraft

have a flight recording system installed. Commercially available systems are not adaptable to general military use.

Recent advances in electronics include microcomputers and nonvolatile solid state memories. These state-of-the-art components make it possible to incorporate new technology in the design of an advanced recording system suitable for military use. This thesis consists of the design, breadboard implementation, and functional testing of a Crash Data Recorder which employs a microcomputer and nonvolatile solid state storage to provide an economic and technically feasible solution to existing systems' constraints. Section II contains background information on recording systems used in military aircraft, including existing equipment and future design trends. The general description of the Crash Data Recorder is presented in Section III. Section IV describes the breadboard implementation and testing of the system. The conclusions and recommendations of this research effort are presented in Section V. Appendix A contains a description of the Metal Nitride Oxide Semiconductor Memory technology and of the various memories examined. Appendices B and C include the computer programs of the system and the listings and plots obtained during testing. Construction details of the memory module are presented in Appendix D.

II. CRASH DATA RECORDERS FOR MILITARY AIRCRAFT

A. REQUIREMENTS

In 1972 the Chief of Naval Operations established a general policy for the incorporation of Crash Position Indicators (CPI) and Flight Data Recorders (FDR) systems in all new aircraft designs [Ref. 1]. This general policy was later expanded to include the evaluation of present technology for the purpose of determining the cost effectiveness of retrofitting existing inventory aircraft with Flight Data Recorder systems. As a result of the increasing need to improve aviation safety and the absence of an efficient post-crash analysis capability, the above requirement was subsequently added to the Navy's General Aircraft Specification. Deviations from this specification requires specific approval by the Chief of Naval Operations.

The United States Air Force's policy of incorporating CPI and FDR systems in specified cargo and transport aircraft dates back to 1966. The C-130, C-133, and C-141 type aircraft were retrofitted with a system that would aid in locating the aircraft accident scene. Recorder and locator systems were part of the original aircraft design in the C-5 and B-1 aircraft. In 1973 the Chief of Staff, USAF established a mandatory requirement to include Flight Data Recorders in all aircraft which enter initial production after 1 July 1974 [Ref. 2].

Studies performed by the Directorate of Aerospace Safety have concluded that installation of recoverable Flight Data Recorders and Crash Position Indicators is a cost effective measure. The benefits of improved accident investigation capability, reduced cost of aircraft losses, and decreased aircraft down time far outweigh the cost of these systems.

Recommendations of a study conducted by the Aviation Safety Programs, Naval Postgraduate School, indicate that crash-protected digital flight recorders should be installed in all high value military aircraft [Ref. 3]. The information recorded at the time immediately preceding the accident could later be used to re-create the accident conditions in flight simulators.

A state-of-the-art survey of Flight Data Recorders was the subject of a thesis recently completed at the Naval Postgraduate School [Ref. 4]. This work includes a detailed analysis of commercially available recording systems, primarily those used by the airlines, and their possible adaptation to meet the military requirements. The author concludes that existing systems are based on outdated technology and are unfit for most military applications.

The requirements for Crash Data Recorders in military aircraft are well established. Recorded flight data used as a tool in the area of crash investigation can represent an annual cost savings to the Department of Defense of several

million dollars and, most important, a considerable reduction of the priceless loss of aircrew life involved in aviation accidents. Unfortunately most military aircraft still do not have any onboard recording systems. The requirement to incorporate this type of equipment in new aircraft design has been waived for some recently acquired military aircraft. The S-3 Viking, F-14 Tomcat, and the new F-18 are representative examples of new Naval aircraft that do not have CPI/FDR equipment due to the unavailability of small, reliable, and cost effective systems adaptable for general military use.

B. EXISTING SYSTEMS

A survey of existing military flight data recorders indicated that most systems were designed to be used in transport, cargo, and patrol type aircraft. This equipment is generally large and heavy and is not suitable for use in smaller tactical aircraft where size and weight are critically restricted. Although the mass production of an existing system for use in all military aircraft would bring down the high unit cost, retrofit installation and maintenance costs involved with currently available equipment would be far from optimum.

The most failure prone component of the existing systems is the digital magnetic tape recorder. The tape recorder is a mechanical device with many moving parts requiring lubrication and maintenance. The recording heads

need to be periodically cleaned and realigned. The volatility encountered in mechanical devices is not desirable in an environment of high gravitational forces and accelerations typically found in tactical aircraft operations. Arrested landings, catapult launchings, and air to air combat are maneuvers in which a mechanical tape recorder is found to be very susceptible to failure.

The following is a brief description of two similar CPI/FDR systems used in military aircraft. Both systems provide a recoverable package that contains a magnetic tape recorder and an emergency radio beacon transmitter.

1. AN/ASH-20 (v)

The AN/ASH-20(v) Flight Recorder-Locator System [Ref. 5] was developed by Leigh Instruments Limited, a Canadian company, in conjunction with the Naval Air System Command. This system is installed in the USN P-3 anti-submarine warfare aircraft. It consists of a performance monitoring system which collects flight information from aircraft instruments and records it together with crew intercom voices on a magnetic tape. Thirty-two flight parameters are continuously recorded in a bi-directional tape cassette that stores an updated record of the last 30 minutes of flight.

The recorder tape deck is housed with the emergency radio beacon transmitter in a deployable airfoil package. Crash sensors, located throughout the aircraft, can detect the aircraft structural deformation and will activate the mechanism that commands airfoil separation. The airfoil

is an aerodynamically designed component that generates lift allowing it to fly away in a predetermined separation trajectory that enhances its survivability. The radio beacon is activated by airfoil separation and emits an emergency distress signal that aids search and rescue operations in locating the crash. The weight of the entire system exceeds 100 pounds.

A ground based installation is required to process the information contained in the magnetic tape for its subsequent use by crash investigation personnel. The Signal-Data Sound Reproducer consists of a Digital Equipment Corporation Model PDP-8 computer and an extensive list of expensive peripheral equipment. Consequently only one ground installation has been purchased by the Navy to support this system.

2. AN/ASH-31 (v)

The AN/ASH-31(v) Flight Data Recorder/Emergency Locator Transmitter [Ref. 6] was developed by the Collins Radio group of Rockwell International for the Air Force's B-1 Strategic Bomber aircraft. The system consists of an ejectable package containing a magnetic tape recorder and a survivable radio beacon transmitter, a base assembly containing the recorder electronics and ejection mechanism, and a number of crash sensors, located throughout the aircraft, that provide the stimulus for system ejection upon aircraft structural deformation.

Digital data to be recorded are received from the aircraft's central computer via a central multiplex data bus as defined in Military Standard 1553A [Ref. 7]. Voice signals transmitted and received by radio and aircraft performance data are recorded continuously with the oldest information being erased as current information is recorded. The system, as used in the B-1 aircraft, records over 64 flight parameters and keeps a current history of the last 30 minutes of the flight.

A thruster system is used to insure that the recorder is ejected and clears the aircraft impact area with a maximum probability of survival. A parachute is deployed soon after system ejection to slow the rate of descent of the package and provide a surface landing velocity no greater than 40 feet per second. The beacon transmitter is activated upon system separation and facilitates the prompt recovery of aircraft and recorder after an accident. The weight of all airborne components is approximately 50 pounds.

Ground processing equipment consists of a Data Transcription Unit used to convert the recorder's 4-channel magnetic tape to a standard 9-channel computer format. Flight data analysis is to be conducted at a conventional Electronic Data Processing Center.

C. FUTURE DEVELOPMENTS

The introduction of recoverable flight data recorders

into some military aircraft has provided a valuable source of additional information for accident investigating authorities. The incorporation of an effective Crash Data Recorder in modern, more complex, and extremely expensive tactical military aircraft would be an invaluable contribution to flight safety as well as a means to improve aircraft availability and mission effectiveness. The Department of Defense needs an improved CPI/FDR system using modern electronic components which provides a high degree of reliability as well as a substantial reduction in weight, volume, maintenance, and unit cost. Both the industrial and the military community continue to search for improved technological developments applicable to Crash Data Recorders.

The Hamilton Standard Division of United Technologies recently conducted a design study for the U.S. Army involving an Accident Investigation Retrieval System (AIRS) [Ref. 8]. The proposed system is to be used in Army helicopters. They plan to use either solid state or magnetic bubble memories instead of magnetic tape, and a microprocessor to selectively record flight parameters. Because the system is designed to employ state of the art electronic components, projected costs are considerably lower than existing systems and a significant weight and volume reduction will be achieved. Since the project was still in early design stage, much of the information could not be disclosed as it is of a proprietary nature.

The United States Navy is currently involved in the development of a Universal Locator-Airborne Integrated Data System (ULAIDS) [Ref. 9]. The goal of this project is to systematically integrate the common functions of aircraft subsystems into a prototype system interfaced with on-board computers. Figure 1 depicts the general integration scheme to be followed in ULAIDS. Signal data acquisition, multiplexing, conversion, and distribution will be under the control of a central computer. Digital interconnections between the subsystems will be accomplished via the Military Standard 1553A Multiplex Data Bus [Ref. 7]. The program requires that a prototype system be installed in an A-7E aircraft in order to conduct ground and flight functional tests.

The incorporation of a recoverable Flight Incident Recorder and Universal Locator (FIR/UL) system is a major component of project ULAIDS. The purpose of the FIR/UL system is to record selected flight parameters for in-flight incident and post-crash analysis as well as to provide an effective means to quickly locate downed aircraft.

The implementation of the ULAIDS project will be a significant step towards the Navy goals of improving aircraft flight safety, increase mission effectiveness, and reduce maintenance costs. Unfortunately the major design restriction of ULAIDS is that the project is to be accomplished with existing, off-the-shelf available hardware. Since the commercially available recording systems are

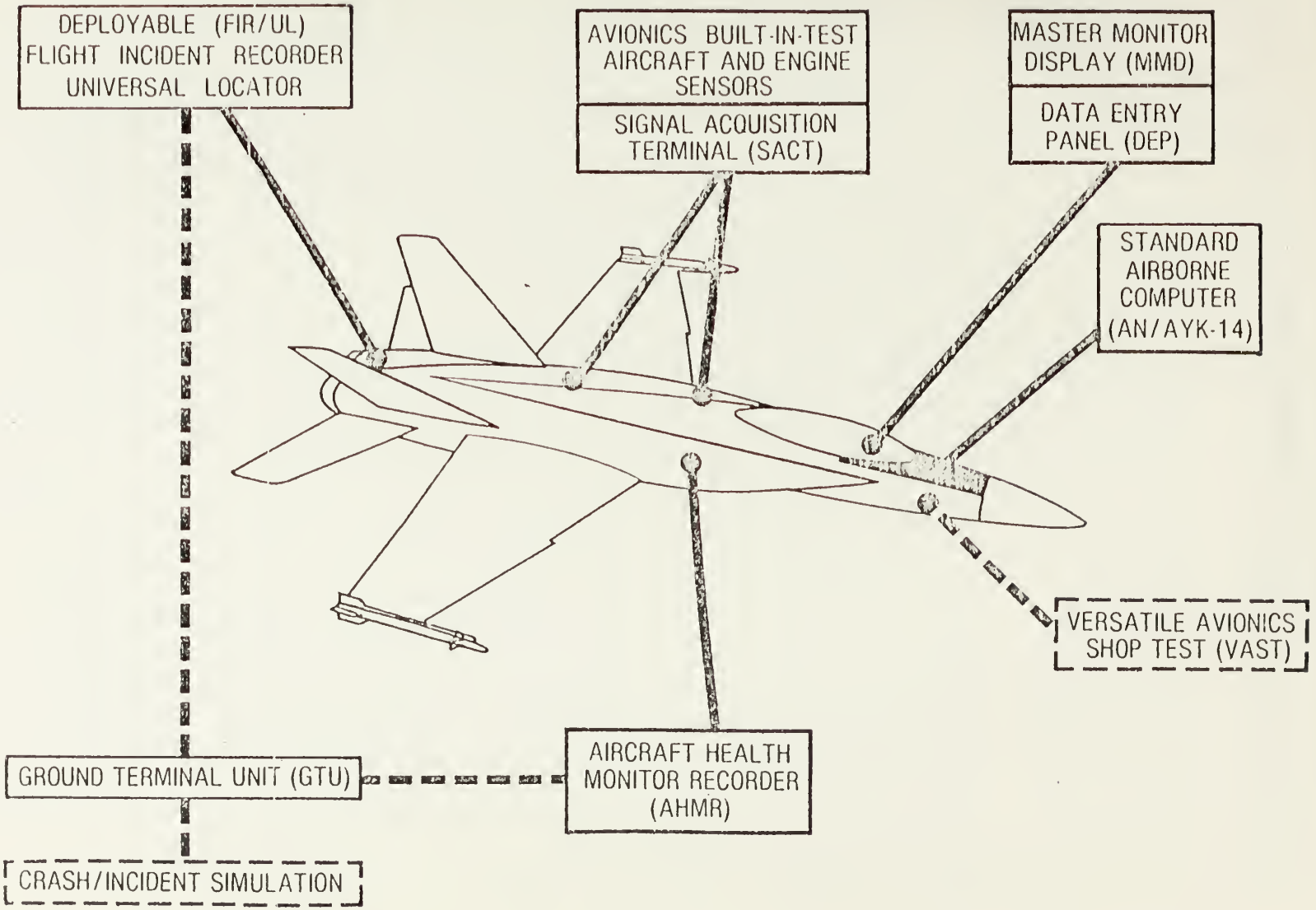


Figure 1. UNIVERSAL LOCATOR-AIRBORNE INTEGRATED DATA SYSTEM

based on magnetic tape, the ULAIDS FIR/UL subsystem will contain a failure prone mechanical magnetic tape recorder.

III. SYSTEM DESCRIPTION

A. GENERAL

The microcomputer based Crash Data Recorder system incorporates the latest advances in computer and nonvolatile solid state memory technologies. A functional block diagram of the system is shown in Figure 2.

Primary design goals were to improve the reliability and reduce the maintenance requirements of existing systems while obtaining an acceptable compromise between the number of parameters to record and the system's cost, weight, and size which are critical in military applications.

A major consideration in the design was to provide an alternate to the Flight Incident Recorder subsystem of the ULAIDS project described in Section II. Therefore the FIR/UL Experimental and Developmental Specifications [Ref. 10] were used as general guidelines.

The heart of the system is a microcomputer that selectively records flight data into a fixed number of nonvolatile solid state memory elements. Performance parameters and elapsed flight time are recorded only when parameters exceed a pre-specified incremental tolerance. The recording is sequential and continuous. When the memory is full, the oldest information is erased as current information is recorded. The length of flight data that can be stored is a function of the rate of change of the flight parameters.

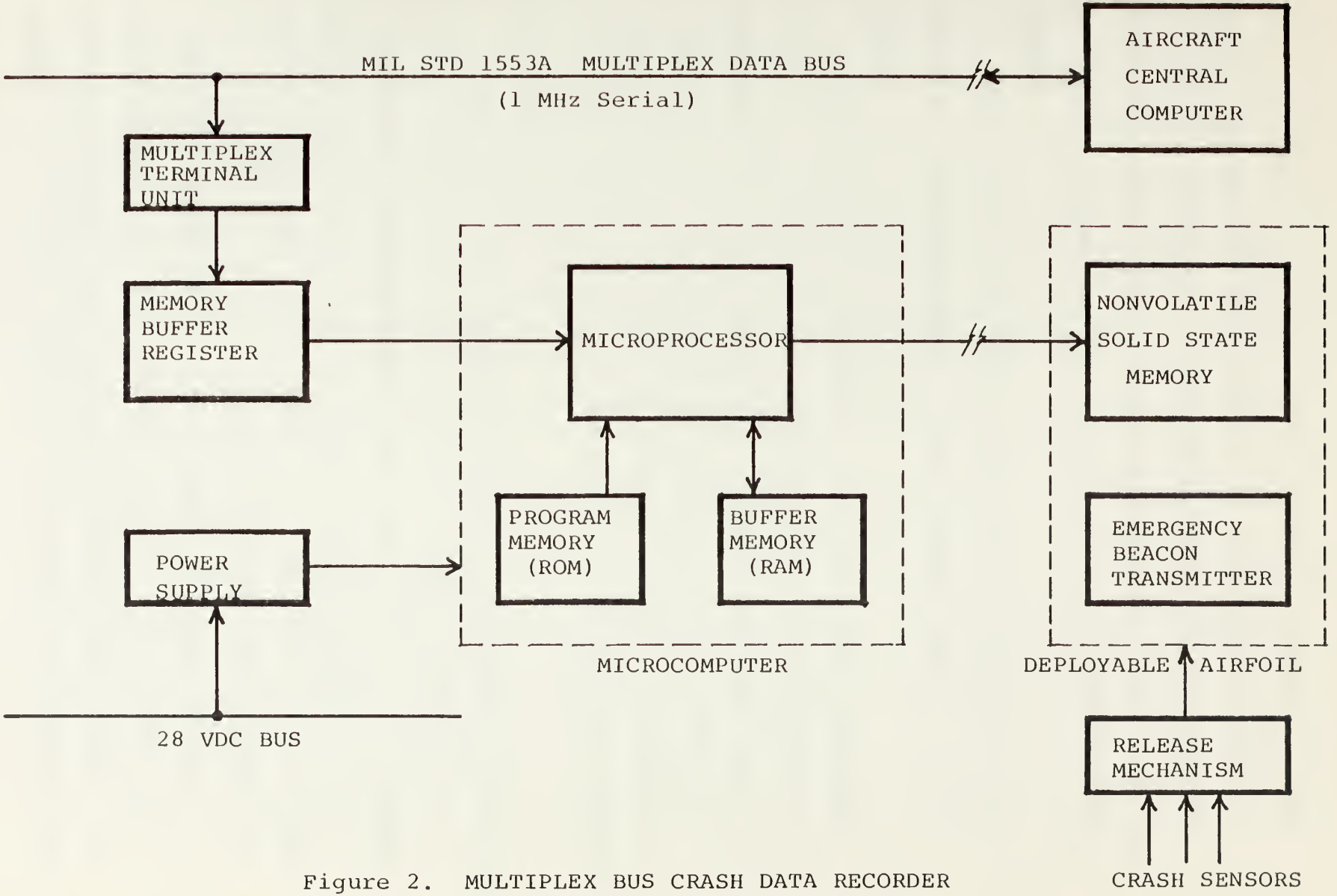


Figure 2. MULTIPLEX BUS CRASH DATA RECORDER

The solid state memory bank and the emergency radio beacon transmitter are enclosed in a separable airfoil. Frangible, hydrostatic, and thermostatic probes located in critical areas of the aircraft provide the electrical signal to command system separation upon pilot ejection or actual crash.

No provision for voice recording is incorporated because of the large amount of solid state memory that is needed to store digitized audio data.

Post-accident expansion of the recovered compressed data and analysis of the accident conditions recorded are performed using an inexpensive Ground Data Reduction Unit. Continuity of overall system architecture and software utilization are provided by using a similar microcomputer for data reduction as the one used in the airborne component.

B. INTERFACE

The Crash Data Recorder receives the digital information to be analyzed from the aircraft's central processor via the MIL STD 1553A Multiplex Data Bus [Ref. 7]. The system interfaces directly to the Memory Buffer Register (MBR) which is attached to the data bus. The purpose of the MBR is to receive the digital message at the bus frequency of 1 MHz and temporarily store it while the microcomputer analyzes the data at a slower frequency. A message consists of 32 words, each 16 binary digits (BITS) long. The number of messages received by the MBR each second depends

on the number of parameters to be recorded. For instance, if 64 different parameters were to be processed each second the central processor would send 2 messages, each one half second apart, to the MBR.

Figure 3 depicts the alternate interface required for systems that will be used in aircraft without a Multiplex Data Bus. By using the aircraft sensors and a signal conditioning and digitizing module, the system becomes independent of the multiplex data bus.

C. MICROCOMPUTER PREPROCESSING

The system is based on the principle of processing the parameters prior to recording. This eliminates redundant information and reduces the storage requirements of solid state memory.

When the Memory Buffer Register has received a digital message, it will signal the microcomputer to begin the execution of an algorithmic routine. The computer program analyzes each individual parameter and determines whether or not its particular tolerance has been exceeded. If the necessary conditions are met, the flight parameter and the time of occurrence are recorded.

The tolerances for the various parameters are prespecified according to the mission requirements and the type of aircraft in which the system is to be used. The Crash Data Recorder is very versatile since only the software modules need to be changed for different fleet aircraft. The computer program is stored in a separate Read Only Memory.

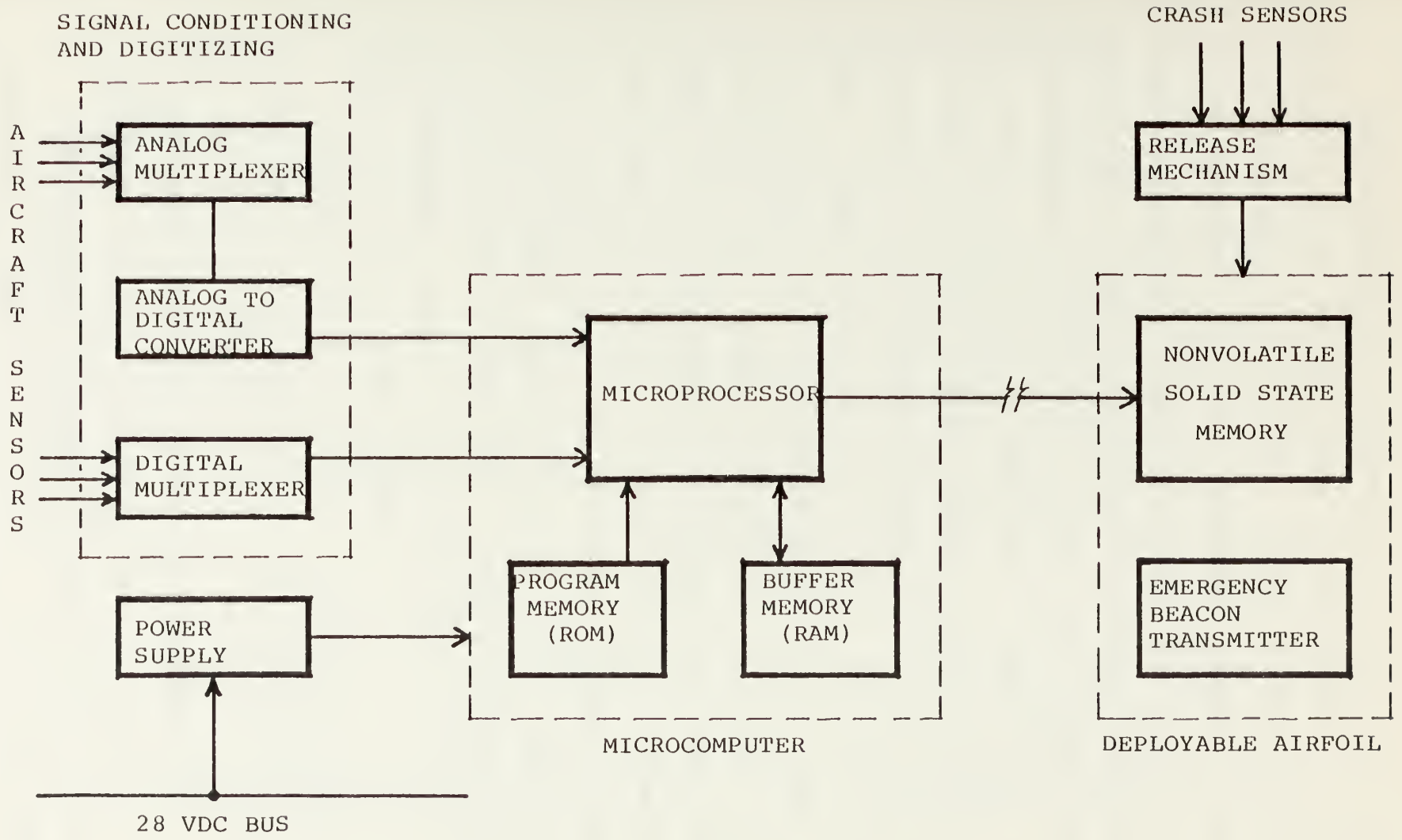


Figure 3. SELF-CONTAINED CRASH DATA RECORDER

The microcomputer automatically changes the tolerances depending on the flight regime of the aircraft. The airspeed tolerance, for instance, varies according to the actual airspeed. One knot incremental values will be recorded whenever the airspeed is within 10 knots of aircraft stall speed. Higher incremental tolerances are used when the airspeed is beyond the aircraft stall speed, which is internally computed using the angle of attack input. The altitude tolerance changes, using a similar routine, according to the present barometric altitude of the aircraft. Greater altitude resolution is provided when closer to the ground than at intermediate levels of 10,000, 25,000, and 35,000 feet. Ground proximity is calculated from the radar altitude input which is recorded only when within effective radar range. Some less critical parameters are only recorded during local maxima and minima or when outside their normal operating limits. This "smart" processing allows greater definition of data at critical points and decreases the storage requirements to within acceptable levels for a solid state medium.

Another feature of having a microcomputer selectively record the flight parameters is that the system is not restricted to fixed sampling rates. Particular parameters can be sampled as often as desired since the actual recording occurs only when the controlling tolerance is exceeded.

The suggested parameters to be analyzed and recorded are shown in Table I and Table II. These lists comprise a subset of the parameters required by the ULAIDS Flight

TABLE I.

Aircraft Parameters and Corresponding Recording Tolerances.

AIRCRAFT PARAMETER	RATE OF SAMPLING	SENSOR ACCURACY	RECORDING TOLERANCE
1. Time (elapsed)	*Recorded when any parameter exceeds its tolerance*		
2. Airspeed	1 sec.	± 10 kts.	1 kt., ± 10 kts of stall 5 kts. above 10,000 ft. 10 kts. above 15,000 ft. 15 kts. above 25,000 ft. 20 kts. above 35,000 ft.
3. Heading	1 sec.	± 2 deg.	1 deg., bank less than 20 deg. 2 deg. elsewhere
4. Altitude (baro)	1 sec.	± 100 ft. ± 150 ft. ± 200 ft ± 250 ft.	1 ft. below 5,000 ft. 2 ft. below 10,000 ft. 10 ft. below 25,000 ft. 50 ft. below 35,000 ft.
5. Altitude (radar)	1 sec.	± 10 ft.	1 ft. below 2,000 ft. AGL
6. Vertical Accel.	1/4 sec.	± 0.2 g	0.5 g,+1.0 to + 3.0 g 0.1 g,-3.0 to + 1.0 g 0.1 g,+3.0 to + 5.0 g 0.01g elsewhere
7. Pitch Attitude	1 sec.	± 2 deg.	2 deg., ± 10 deg from level 1 deg. elsewhere
8. Roll Attitude	1 sec.	± 2 deg.	Same as Pitch
9. Yaw Attitude	1 sec.	± 2 deg.	Same as Pitch

TABLE I. (Cont'd)

AIRCRAFT PARAMETER	RATE OF SAMPLING	SENSOR ACCURACY	RECORDING TOLERANCE
10. Angle of Attack	1 sec.	± 1 unit	1/2 unit, ± 2 units from stall 1 unit elsewhere
11. Air Temp.	2 sec.	± 1 deg. C	1 deg. C
12. Aileron Position	1 sec.	± 2 deg.	Tolerances
13. Elevator Position	1 sec.	± 2 deg.	Determined by
14. Rudder Position	1 sec.	± 2 deg.	Aircraft type

TABLE II.

Engine parameters and discrete inputs.

PARAMETER (ENGINE)	RATE OF SAMPLING	RECORDING TOLERANCE
1. Oil Pressure	1 sec.	Only Recorded if Outside
2. Turbine Inlet Temp.	½ sec.	Normal Operating Limits
3. Turbine Outlet Temp.	½ sec.	Tolerance Determined
4. Fuel Flow	1 sec.	By Engine Type
5. Oil Temp.	1 sec.	
6. RPM	1 sec.	10% within normal limits 1% elsewhere

DISCRETE-LANDING	DISCRETE-SYSTEMS
1. Flaps (leading edge)	1. Air Data Computer
2. Flaps (trailing edge)	2. Navigation System
3. Landing Gear	3. Primary UHF
4. Speed Brakes	4. Secondary UHF (guard)
5. Arresting Hook	5. Hud Fail

DISCRETE-ENGINE	DISCRETE-PILOT ACTION
1. Fuel Pressure	1. Fire Warning
2. Fuel Select	2. Fuel Warning
3. Chip Detect	3. Oxygen Warning
4. Anti-Ice	4. Rain Removal
5. Oil Warning	5. Microphone Keying

Incident Recorder specification. They are presented as a suggested compromise between the original requirement of 85 parameters and the present economic constraints of nonvolatile solid state memory. A very large memory storage is required to record all the parameters specified for the FIR system. Since a main objective of the Crash Data Recorder is to provide a small, light, and inexpensive source of information for accident investigation, there must be a balance between the number of parameters to record and the size of the nonvolatile solid state storage. For a given size of memory, the trade-offs are:

1) Less recorded parameters (eliminate dependent parameters without losing information).
2) Larger tolerances.
3) Less flight time retained prior to crash.
4) Sample parameters, but record only if outside normal limits.

The suggested parameters were chosen to provide sufficient pre-accident information while maintaining an acceptable storage requirement.

Fourteen individual flight parameters are listed in Table I with their corresponding sampling rates. Also shown are the particular incremental tolerances and the references used by the microcomputer in automatically changing these tolerances. Table II lists the engine parameters and discrete inputs. Since discrete inputs can be digitally

represented by an ON or OFF condition, packing of the discrete parameters was accomplished in 2 words. Each word consists of 10 BITS and is recorded whenever any one of the parameters in the word changes state.

In existing recording systems all flight parameters are continuously recorded regardless of their real value to accident investigation. Generally the number of significant digits of the recorded information exceeds the accuracy of the sensor providing the information. In contrast, onboard analysis allows logical decision making of what and when to record. The overall effect of the microcomputer preprocessing is not to blindly sample and record parameters but to analyze and save only that information that is pertinent to accident cause determination.

D. NONVOLATILE SOLID STATE MEMORY

A nonvolatile solid state recording medium replaces the mechanical magnetic tape recorder found in existing systems. Solid state storage is significantly more reliable than magnetic tape as there are no tape transport mechanisms or other moving parts to jam or fail while subjected to the high gravitational forces encountered in a tactical environment. Electromechanical devices have limited data transfer rates due to their relatively long start and stop cycles. Consequently, existing systems are operated in a continuous recording mode with constant head to tape contact that causes progressive wear. Periodic head cleaning and

replacement of failed components are responsible for the high maintenance overhead associated with magnetic tape recorders. Data transfer rate of solid state memory is only limited by memory access time. Present technology provides a memory access cycle time of only 500 nanoseconds. The much longer life expectancy and the maintenance-free quality of a solid state recording medium are essential characteristics in a state of the art design. The reduction of man-hours in maintenance alone is a significant contribution towards the overall cost effectiveness of the Crash Data Recorder system.

Reference 4 provides a detailed description and the advantages and limitations of the various solid state memory technologies available. Metal Nitride Oxide Semiconductor (MNOS) memories were chosen for the Crash Data Recorder. High density MNOS memory elements are now commercially available due to recent advances in this technology. The MNOS memory types that were considered for application in the Crash Data Recorder are:

1) Block Oriented Random Access Memory (BORAM) [Ref. 11],

2) Virtually Nonvolatile Random Access Memory (VINRAM) [Ref. 12],

3) Electrically Alterable Random Access Memory (EARAM) [Ref. 13].

A description of the MNOS technology and of the 3 memory types examined in contained in Appendix A.

The size of the memory storage required is a function

of the number of parameters to be recorded and the minimun acceptable length of recorded flight. An extrapolation of the results obtained (SECTION IV) indicates that 7680 words of 16 BITS each would be sufficient to retain a 30 minute record of the parameters listed in Tables I and II. This can be accomplished with a module of only 30 memory elements since present manufacturing methods can produce a density of 4096 BITS per element. Approximately 80 memory elements would be required for the case in which all the parameters continuously surpass their recording tolerances during a 30 minute period.

The solid state memory module is enclosed within the separable airfoil package. Data and control lines to the memory are connected via a breakaway plug mounted on the surface of the airfoil. Since digital information is directly recorded into solid state memory there is no need for the extra step of a Harvard Bi-Phase or Non Return to zero formatting found in magnetic tape systems.

E. GROUND DATA REDUCTION UNIT

The average cost of ground processing units required for existing systems is near $200,000 dollars. A typical unit consists of a minicomputer, a tape interface, mass memory storage, an input-output device, high speed line printers, and analog plotters. Additional hardware and software programs are required because the magnetic tape format from the recorders are usually not compatible with the minicomputers and must be transcribed.

The Ground Data Reduction Unit (GDRU) used for the Crash Data Recorder was selected keeping the economic goal in perspective. A relatively inexpensive microcomputer developmental system is used whose microprocessor is identical to the one used in the airborne system. This entirely compatible architecture allows continuity of software utilization and simplicity of operation during data reduction.

The recovered memory module interfaces directly to the ground based microcomputer unit. (Figure 4). The GDRU extracts the compressed recorded information from the memory and expands it creating a second by second listing of all the parameters. If a parameter was not recorded in a particular second, indicating that its tolerance was not exceeded, the last known value of the parameter is inserted, thereby creating a continuous record. This information can then be used for further analysis during the investigation process. The expanded flight can be reproduced graphically and numerically using standard digital peripherals.

The cost of a GDRU consisting of the microcomputer, a cathode ray tube input-output console, a line printer, and a digital strip chart recorder ranges from $12,000 to $20,000 dollars. This low cost, as compared with existing systems, is representative of a Crash Data Recorder system based in latest available technology. The economical characteristics of the Ground Data Reduction Unit will make it possible for cognizant investigating authorities to have several units

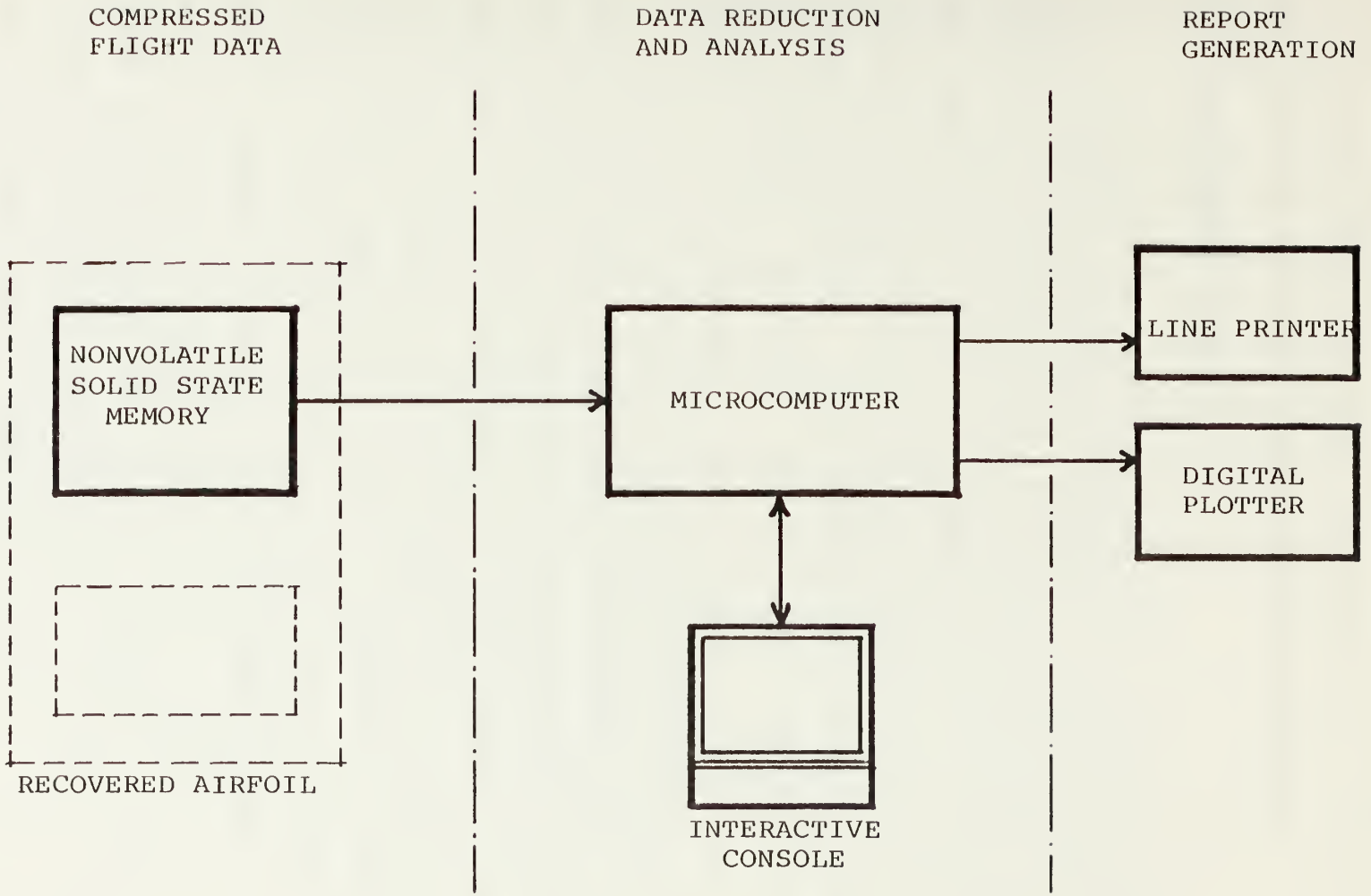


Figure 4. GROUND DATA REDUCTION UNIT

distributed among aviation activities. A simple memory-computer interface unit can be provided for installations with existing Automatic Data Processing Centers.

F. RECOVERABLE MODULE

No attempt was made to design this component because of its specialized nature. Instead, a study of existing systems' recoverable modules and their separation techniques was conducted in order to determine the feasibility of adapting a commercially available component to use in the Crash Data Recorder. Both systems described in Section II were carefully reviewed. Reference 14 contains a comparative analysis of high energy versus airfoil delivery techniques.

The airfoil package designed by Leigh Instrument Limited was chosen as the recoverable module for the Crash Data Recorder. A test copy of the aerodynamic airfoil was obtained from the manufacturer for the purpose of analyzing the proper accommodation of the solid state memory modules. The airfoil, depicted in Figure 5, measured 24 inches by 30 inches and was found to be too large for use in most tactical aircraft. However, Leigh also manufactures a smaller airfoil which is readily adaptable for application in the Crash Data Recorder. The airfoil separation system is already in military inventories, as it is used in conjunction with the Crash Position Indicator in several cargo and patrol aircrafts.

The airfoil is designed to be flush mounted in the empennage of the aircraft and is constructed of a fiberglass encased plastic foam. This construction provides good thermal insulation, protection from impact damage, and excellent floatation characteristics. The airfoil's aerodynamic shape generates lift that carries it in a predetermined, speed-reducing trajectory to the surface outside the periphery of the impact area. An emergency radio beacon transmitter (AN/URT-26 (v)) begins operation automatically upon separation and produces a distress signal that aids in locating the aircraft crash site. A more complete description and theory of operation of this component is contained in Ref. 5.

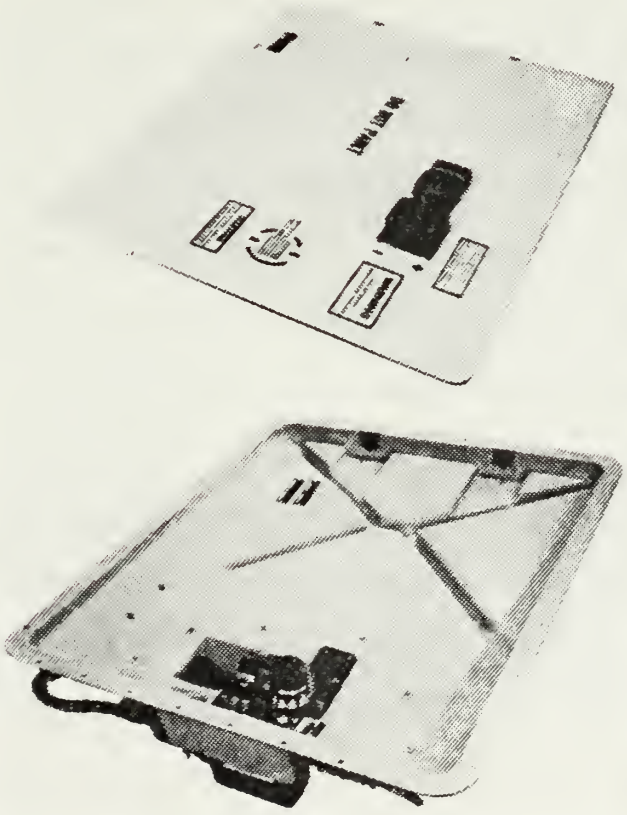


Figure 5. Recoverable Airfoil Module

IV. SYSTEM IMPLEMENTATION AND TESTING

A. MICROCOMPUTER DEVELOPMENTAL SYSTEM

The hardware implementation and the software development of the Crash Data Recorder were conducted using an Intellec 8 Microcomputer Developmental System (Fig. 6), made by Intel Corporation. The system was interconnected to a Datamedia Corporation video terminal and an Addmaster high-speed paper tape reader used as developmental peripherals.

The Intellec 8 system is based on the Intel 8008-1, 8 BIT, second generation microprocessor [Ref. 15]. Intel also manufactures a similar, but more advanced, third generation microprocessor; the 8080-A. Besides being faster and more powerful, the 8080-A microprocessor is presently available in a military specification version and would be used in actual airborne equipment. This microprocessor has become widely used in industry. It is already incorporated in several military systems, is multiple sourced, and is well supported by peripheral microcircuits and a high level language.

All software development was done in Programming Language for Microcomputers (PL/M); a high level computer language specially designed to support Intel's microprocessors [Ref. 16]. The use of PL/M provides direct transportability of software between the 8008-1 and the 8080-A microprocessors. PL/M is a block structured language that serves as an

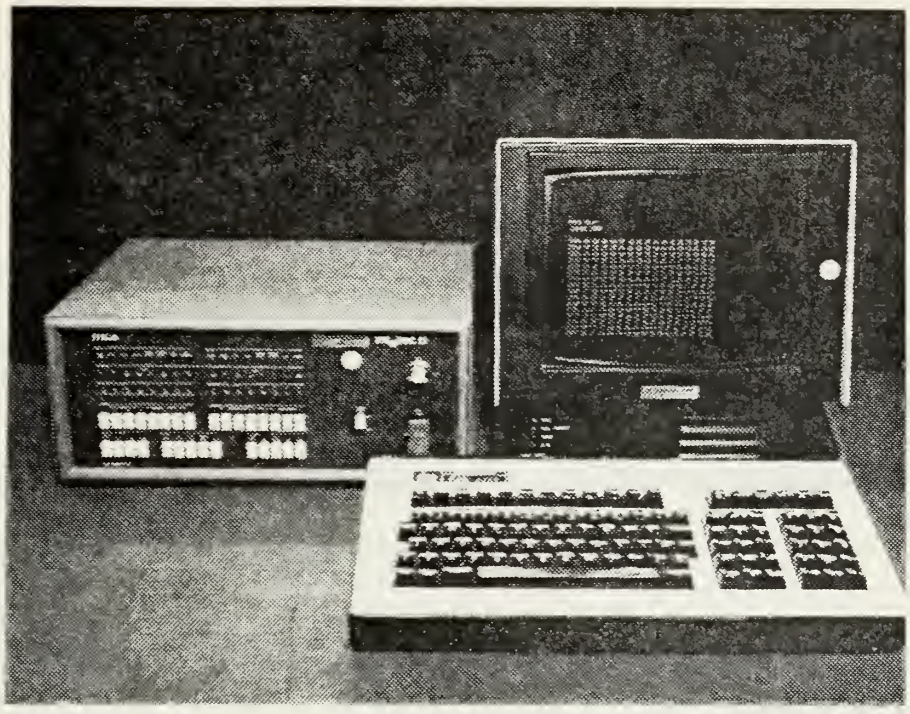


Figure 6. MICROCOMPUTER DEVELOPMENTAL SYSTEM

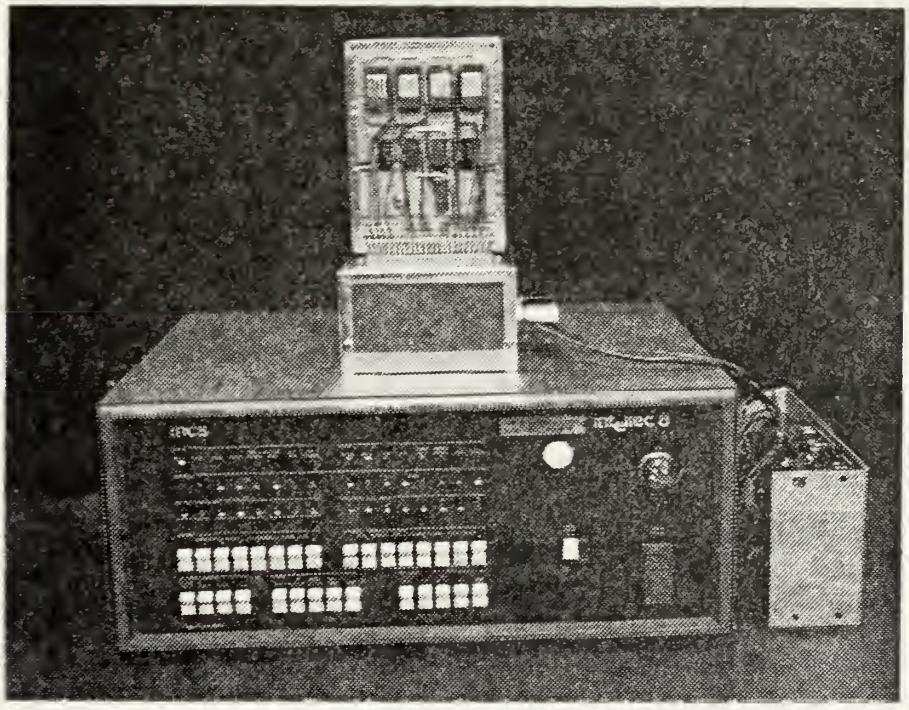


Figure 7. MICROCOMPUTER-MEMORY INTERFACE

excellent tool for rapid program development. It's simple primitives allows the computer program to be almost self documented, when compared to Assembly Language Level.

The PL/M programs included in Appendix B were compiled into machine executable code using the Naval Postgraduate School IBM 360/67 computer facilities. The output from this process could then be loaded into the Microcomputer Developmental System and subsequently executed.

B. TEST DATA

Flight data from a commercial airliner was obtained from the National Transportation Safety Board. This data was recorded in a 9-track magnetic tape using a serial format. Because this source was not directly compatible with the Microcomputer Developmental System its use was discontinued. Since the search for recorded data from a military flight proved unsuccessful, it was decided to create an artificial flight to use as a test bed in the development of the Crash Data Recorder.

A three minute record of a representative, highly maneuverable, tactical flight was created. The rapidly changing parameters gave a better indication of the memory density required to store enough data to accurately recreate the flight. Table III shows the flight parameters and their corresponding mnemonic labels used in the computer programs. This table also shows the parameter's range, recording accuracy, and sampling rate. Appendix C contains a second by second

TABLE III.

Parameters and Labels Used in Test Data.

PARAMETERS	MNEMONIC LABEL	HEX LABEL	SAMPLE RATE	RANGE	RECORDING ACCURACY
1. TIME (minutes)	MINS	00	1 sec	0-720 min	1 min.
2. TIME (seconds)	SECS	01	1 sec.	0-60 sec	1 sec.
3. VERTICAL ACCEL.	VG-1	02	1/4 sec.	-3 to + 7 g	0.01 g
	VG-2	05	1/4 sec.	-3 to + 7 g	0.01 g
	VG-3	08	1/4 sec.	-3 to + 7 g	0.01 g
	VG-4	0B	1/4 sec.	-3 to + 7 g	0.01 g
4. ALTITUDE COURSE	ALTC	03	1 sec.	256-65,000 ft	256 ft
5. ALTITUDE FINE	ALTF	04	1 sec.	0-255 ft	1 ft
6. AIRSPEED	KCAS	06	1 sec.	0-1023 kts	1 kt
7. HEADING	HEAD	07	1 sec	0-360 deg	0.5 deg
8 DISCRETE (Landing)	DP-1	09	1 sec.	-	ON/OFF
9. DISCRETE (Systems)	DP-2	0A	1 sec.	-	ON/OFF

listing of the parameters in the original flight as well as plots of the parameters versus time, depicting their rapid rate of change.

The parameters chosen for the test flight are representative of the different types of parameters specified for the ULAIDS Flight Incident Recorder. Altitude, for instance, is a type of parameter whose value is subdivided into course and fine sections. Since course parameters change less frequently, this division provides additional memory savings while it still retains good parameter resolution. Vertical Acceleration represents those parameters that are rapidly changing and need to be sampled several times each second. Discrete parameters depict how to process several parameters in one data word.

Each data word consists of 16 binary digits as specified in Military Standard 1553-A. The 6 most significant BITS are reserved for the parameter's label and the 10 lower BITS are the parameter's binary value. Sixty-four parameters can be individually identified using this format.

C. DATA PROCESSING TRIALS

Several data processing trials were conducted to determine the amount of nonvolatile memory required to record significant data from the test flight. The flight data was loaded into the microcomputer's memory in the same sequence that it would arrive to the Memory Buffer Register. It was assumed that this data would be delivered by the aircraft's

central processor in a pre-determined orderly sequence of 16 BIT words without any labels.

The computing algorithm is contained in the PROCESS PLM program shown in Appendix B. The microcomputer retrieves one data word at a time from the MBR and compares it with the previous value of that particular parameter. If the absolute value of the difference between the new and old words exceeds the controlling tolerance, the new data value is recorded. The time of occurrence of the events is recorded only once for each second of data along with the new values of all the parameters that have exceeded their tolerance in that particular second. The latest recorded value of each parameter is retained in a buffer and is used as reference to compare subsequent information. A label indicating the parameter's name is added in the six most significant BITS of the data word prior to recording. Using this labeling method, information can be recorded at random and accurately identified when recovered.

The original processing algorithm tested would record the actual value of all parameters once every 30 seconds. Only new, significant, information was recorded in between the 30 second intervals. This method provided a convenient reference from which the entire flight could be reconstructed. However, the periodic recording of all parameters was found to be too memory consuming and was discontinued. The final algorithm only records the parameters once their tolerances

are exceeded. This method provides sufficient information to reconstruct the flight since all the parameters would normally change, at least once, in the 30 minute history provided by the Crash Data Recorder. Significant memory reduction was obtained using the later algorithm.

The flight data was processed using different tolerance values. A memory reduction factor was determined by comparing the amount of data obtained from the processed flight with the original flight data. Table IV shows the reduction factors obtained during this test. It is worth noting that, although the data represented a highly maneuverable flight the memory requirements were reduced by half by removing only repeated information (TEST NO. 1.). Much higher memory reduction factors than those shown in Table IV can be obtained from cruise flight conditions. Extrapolation of these results indicate that a Crash Data Recorder used to record the parameters listed in Section III, and using the variable tolerances previously described would require a 30 element memory module to retain the last 30 minutes of flight.

The recorded processed data was expanded using the same Microcomputer Developmental System. The RECOVER PLM computer program used is shown in Appendix B. The expansion process consists of reading the sparcely recorded parameters from a one second period and recreating that second of flight with all the parameters filled in. If a parameter was absent during this period, its previously recorded value

TABLE IV.

Tolerance

Results of Memory Required Versus Tolerance Tests.

TEST	ACCELER-ATION	ALTITUDE	AIR-SPEED	HEAD-ING	REDUCTION FACTOR	STORAGE REQ'D
1.	0.00 g	0 ft	0 kts	0 deg	1.8	2400
2.	0.05 g	2 ft	2 kts	2 deg	4.5	960
3.	0.05 g	5 ft	2 kts	2 deg	5.0	864
4.	0.10 g	5 ft	5 kts	2 deg	6.0	720
5.	0.10 g	10 ft	5 kts	3 deg	7.2	610
6.	0.10 g	20 ft	10 kts	5 deg	8.1	540

Original flight storage required = 4320 bytes.

is inserted creating a continuous record. Each word is sequentially read, its label removed, and its value placed in a buffer dedicated to that particular parameter. Once all the recovered data has been processed in this manner the values are converted to engineering units and are ready for output. The listing of the expanded data is accomplished via the interactive console or via a digital line printer. Examples of the recovered flight listings are included in Appendix C.

The relevancy of the data obtained from the processed flight could not readily be compared with the original flight by observing the recovered and original output listings. A series of parameter versus time plots were obtained from both the original and the recovered flight data. These plots, contained in Appendix C, give an indication of the correspondence between original values and values obtained by using selective recording. All plots were obtained using the Naval Postgraduate School's central computer facilities since a digital plotter that could interface directly with the microcomputer was not readily available. The computer program used to obtain these plots, PLOT FORTRAN, is included in Appendix B.

D. MEMORY MODULE TESTING

The VINRAM memories developed by Westinghouse, described in Appendix A, were determined to be best suited for application in the Crash Data Recorder. Their higher density

and unlimited erase-cycle properties are essential in a small volume, low maintenance system. However, because these memories were still undergoing production tests they were not available for evaluation. Therefore, the non-volatile memory module was constructed using Nitron Corporation NCM7050 MNOS memories. Figure 8 shows the memory module and its supporting assembly. A detail of the memories and associated circuitry is depicted in Figure 9.

Two NCM 7050 engineering samples were obtained from the manufacturer early in the development phase to determine the memories' reliability and evaluate their timing and interface requirements. The particular characteristics of the NCM7050 memory are described in Appendix A.

Successful writing, erasing, and reading from these memories were accomplished in a laboratory environment. Data was retained in the memories for a period of 14 days with only one isolated binary digit failure. A brief temperature retention test was conducted. Data was written in selected locations of both memories and then subjected to temperatures of 50°C, 75°C, and 100°C for a period of 12 hours each time. Favorable results were obtained with the exception of the same binary digit failure previously described. This failure occurred during the 100°C test. Discussions held with Nitron's application engineers disclosed that the particular lot that these samples were obtained from had experienced an unusually high failure rate.

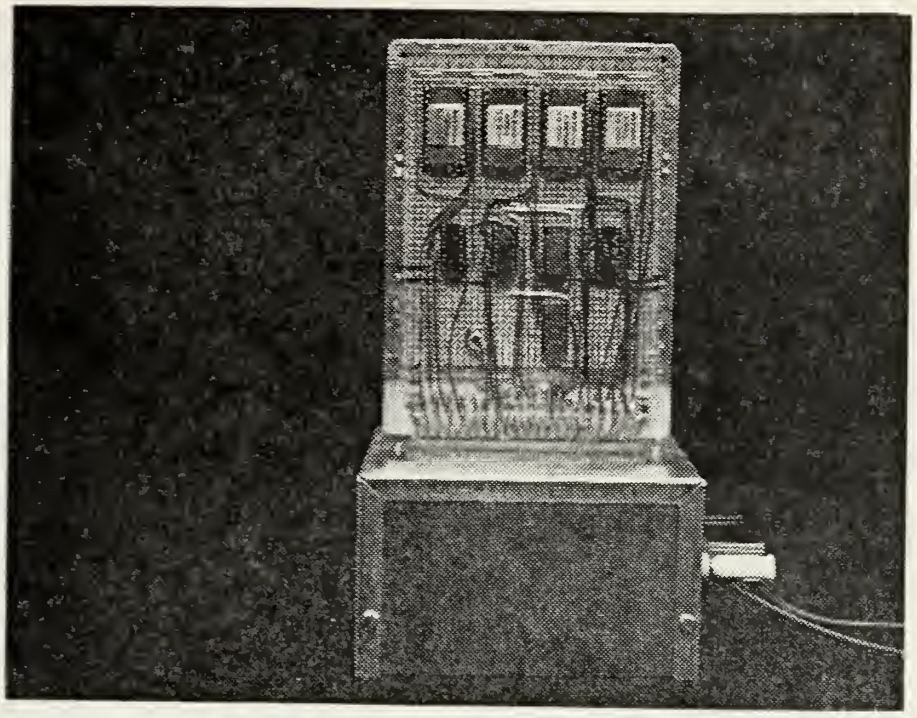


Figure 8. MODULE AND SUPPORTING ASSEMBLY

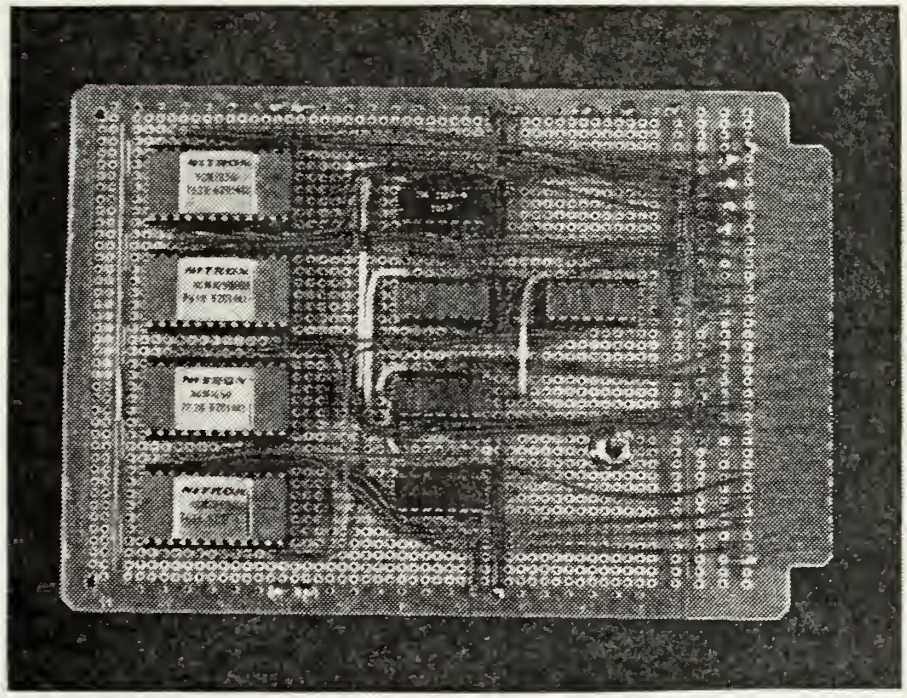


Figure 9. NONVOLATILE MEMORY MODULE

Therefore, the results obtained from the laboratory tests were considered to be satisfactory.

The memory module was constructed to provide a test bed that could be interfaced directly to the microcomputer. The module consists of four NCM7050 memory elements, TTL to MOS buffers, and a memory address decoder. A schematic of the circuit is shown in Figure 10 and construction details are included in Appendix D. This configuration provided a memory capacity of 256 - 16 BIT words which was enough to record partial test flight data in order to determine retention rates. Address, data, and control lines were connected to the microcomputer via the system's input and output ports. Additional software development was required to write, read, and control these separate memories. The software routines are included in the PROCESS PLM and RECOVER PLM computer programs.

The same test flight was used as input data to the processing algorithm, with the output recorded directly into the nonvolatile memory module. The first test consisted of processing the 3 minute flight once, with the last 256 words of information retained in the memories. Power was disconnected and the module was removed from its base for a period of one hour. Upon completion of the isolation period the module was re-connected and the RECOVER PLM program executed. The data retention rate was excellent with no failures observed. Several other short period isolation tests

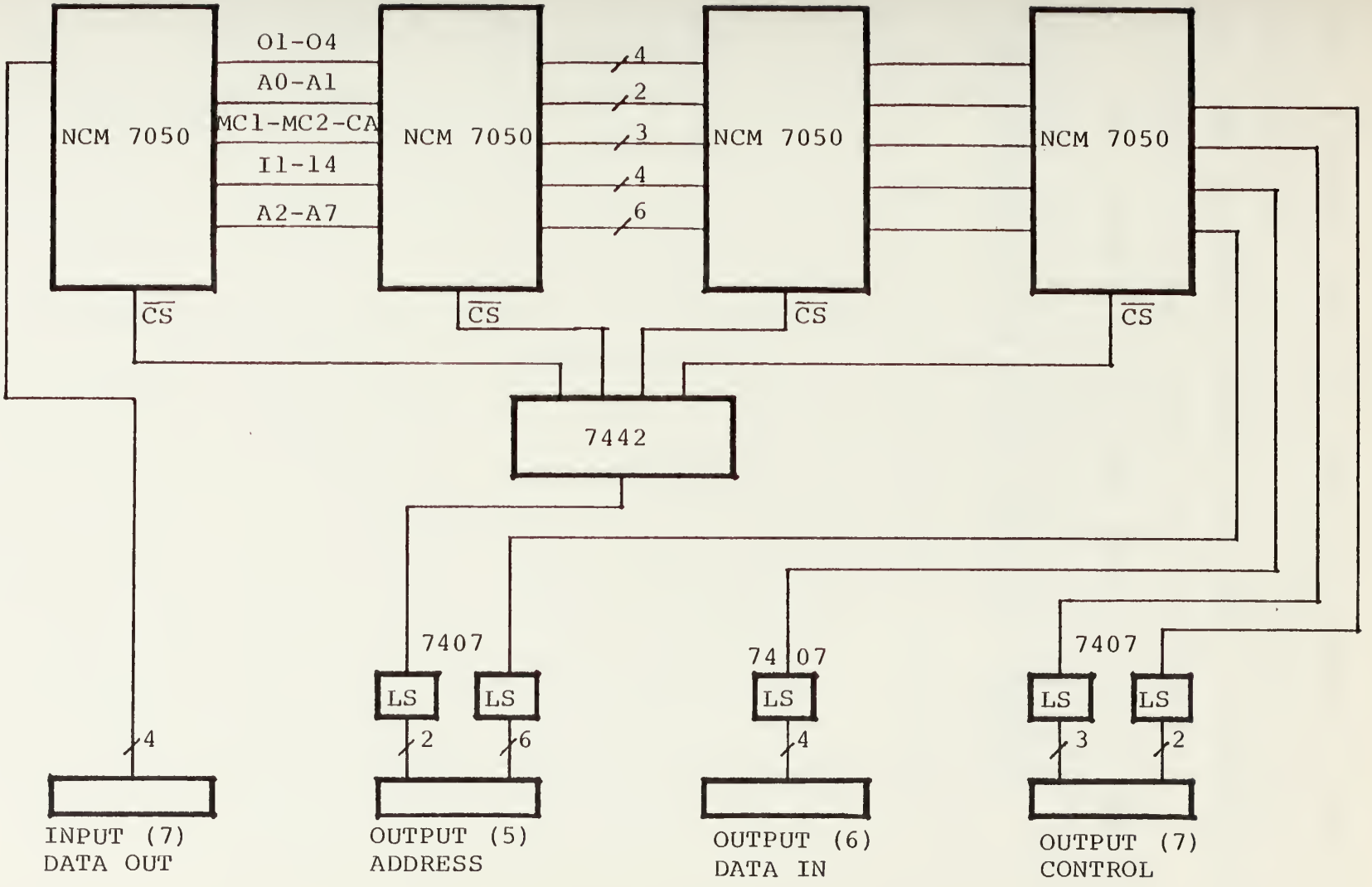


Figure 10. MEMORY CIRCUIT SCHEMATIC

were conducted, each time retaining different areas of the processed data, with similar full retention results. The last test conducted retained 256 words of information for a period of one week, again with no failures.

The results of the tests indicate that commercially available nonvolatile solid state devices can be used as the recording medium in the Crash Data Recorder.

V. CONCLUSIONS AND RECOMMENDATIONS

The developmental efforts described in this report indicate that the technology is now available to allow the design and implementation of a state-of-the-art recording system that is well suited for military applications. With increased reliability, reduced size and weight and, most important, low total cost, the Crash Data Recorder will improve operational safety by enhancing the probability of uncovering the accident's cause.

Discussions held with professional aviation accident investigators concluded that the information provided by the Crash Data Recorder would have been instrumental in determining the causes of the 42 accidents described in Section I. In retrospect, the recovered data would have been sufficient to prescribe the necessary improvements to prevent repeated accident occurrences.

The higher densities obtained in newer memories and the decreasing cost of solid state mass production will be contributory factors in the implementation of a Crash Data Recorder with sufficient storage to record additional flight parameters.

The presence of a microcomputer dedicated to the flight recorder provides a powerful tool whose full capabilities warrant further study directed towards other applications. Structural history, maintenance analysis, aircrew training, and tactical mission debriefing are areas where the Crash Data Recorder can also serve as an analytical tool.

The absence of a voice recording capability in the Crash Data Recorder may be questionable for certain applications. Electromechanical devices are still the only practical method of recording voice or audio information. However, some solid state data storage techniques, currently in advanced development stages, show promise of being able to store enough BITS in a given volume to make solid state storage of audio feasible in the near future [Ref. 17 and 18].

For installations which have a flight simulator, the development of an interface between the Crash Data Recorder and the simulator would provide a convenient wav of reconstructing the aircraft flight either for accident investigation or training.

Inertial navigation systems, installed in conventional tactical aircraft, provide an excellent source of highly accurate flight parameters. Further research should be conducted to determine the feasibility of interfacing the Crash Data Recorder directly to the inertial navigation system in order to eliminate the cost of sensor installation.

The design of the Crash Data Recorder is presented as an alternate to the Flight Incident Recorder subsystem of the ULAIDS project. It is therefore recommended that a full scale system be developed as soon as possible so that airborne functional testing can be conducted in the ULAIDS prototype aircraft.

APPENDIX A

MNOS MEMORY TECHNOLOGY

A. GENERAL

Semiconductor memories are extensively used in advanced airborne computing systems. One of the problems of semiconductor memories has been the complete loss of data when power is shut down or interrupted. This problem was overcome by the introduction of the Metal Nitride Oxide Semiconductor (MNOS) memory which retains data after power is removed.

The MNOS technology has been advancing rapidly during recent years and many MNOS memories have been developed under government contracts. These memories are manufactured using an extension of the MOS technology. An additional mask level, made of nitride, is used to produce the non-volatile elements. Unlike conventional random access memories, MNOS memories must be erased before data is re-written. Their ability to retain information results in lower power consumption since the memories need to be powered only during data transactions. In addition, memory cells can be made extremely small because the storage component consists of a single transistor. MNOS chips with 100,000 BITS of memory, instead of the current 2,000 BITS, are projected for future development [Ref. 19]. The production of low-cost, high density MNOS memories is improving

as new photolithographic techniques are developed. However, some of these devices have limitations in their applicability to systems because of their long write time (1 millisecond) and their limited endurance (10^6 write/erase cycles). The VINRAM memory described in this appendix was developed to overcome the speed and endurance constraints of MNOS memories.

B. MNOS MEMORY TRANSISTOR

Metal Nitride Oxide Semiconductor (MNOS) memories are based on the MNOS transistor which is a device similar to other Insulated Gate Field Effect Transistors (IGFET) [Ref. 11]. The gate insulator is composed of two layers. The first layer, at the silicon interface, consists of a thin oxide film. The second insulator layer, on top of the oxide, is a thick silicon-nitride film. A simplified cross section of a MNOS transistor is shown in Figure 11. The flow of current between the source and the drain is controlled by the gate electrode. When a high positive voltage is applied to the gate a negative charge is trapped in the nitride-oxide interface. A relatively large amount of energy is required to lift the charge out of the trap. The period of the charge retention at the interface has been measured to be longer than 4,000 hours.

The basic method of reading the cell is to measure the threshold of current flow between the source and the drain. A small negative voltage is applied to the gate until a

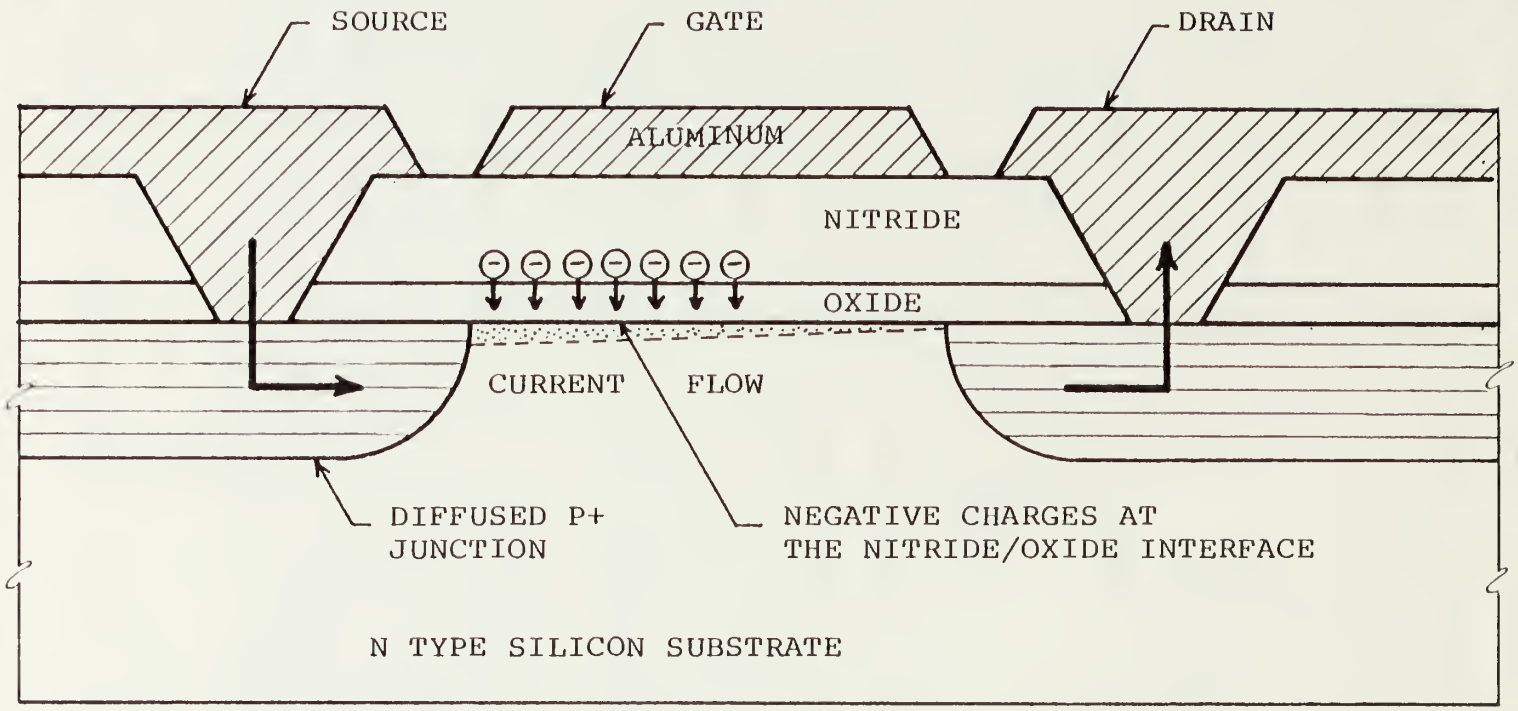


Figure 11. CROSS SECTION OF MNOS TRANSISTOR

small drain current is sensed. The interrogation voltage can be sensed only when the interface is negatively charged.

To erase the cell, a high negative voltage is applied to the gate which traps positive charges at the interface. This reverses the threshold effect and causes the cell to remain off when interrogated by a low voltage.

Nonvolatility of the memory cell is achieved because the read voltage amplitude is low compared to the amplitude required to change the trapped charges.

C. BLOCK ORIENTED RANDOM ACCESS MEMORY

The Block Oriented Random Access Memory (BORAM) [Ref. 11] was developed by the Westinghouse Defense and Electronic Systems Center through joint Army/Navy funding. The goal of this solid state memory is to eventually replace electro-mechanical secondary memory storage currently used in military applications.

The basic storage element is a MNOS transistor. Large-scale integration yields a memory density of 2048 BITS in a single chip measuring 161 mils by 169 mils. High density components are produced by packaging 16 memory chips into a hybrid microcircuit. Figure 12 depicts a BORAM memory card which contains 19 microcircuits. This card measures approximately 9 inches by 12 inches and has a total capacity of 622,600 BITS.

The characteristics of the BORAM memory are:

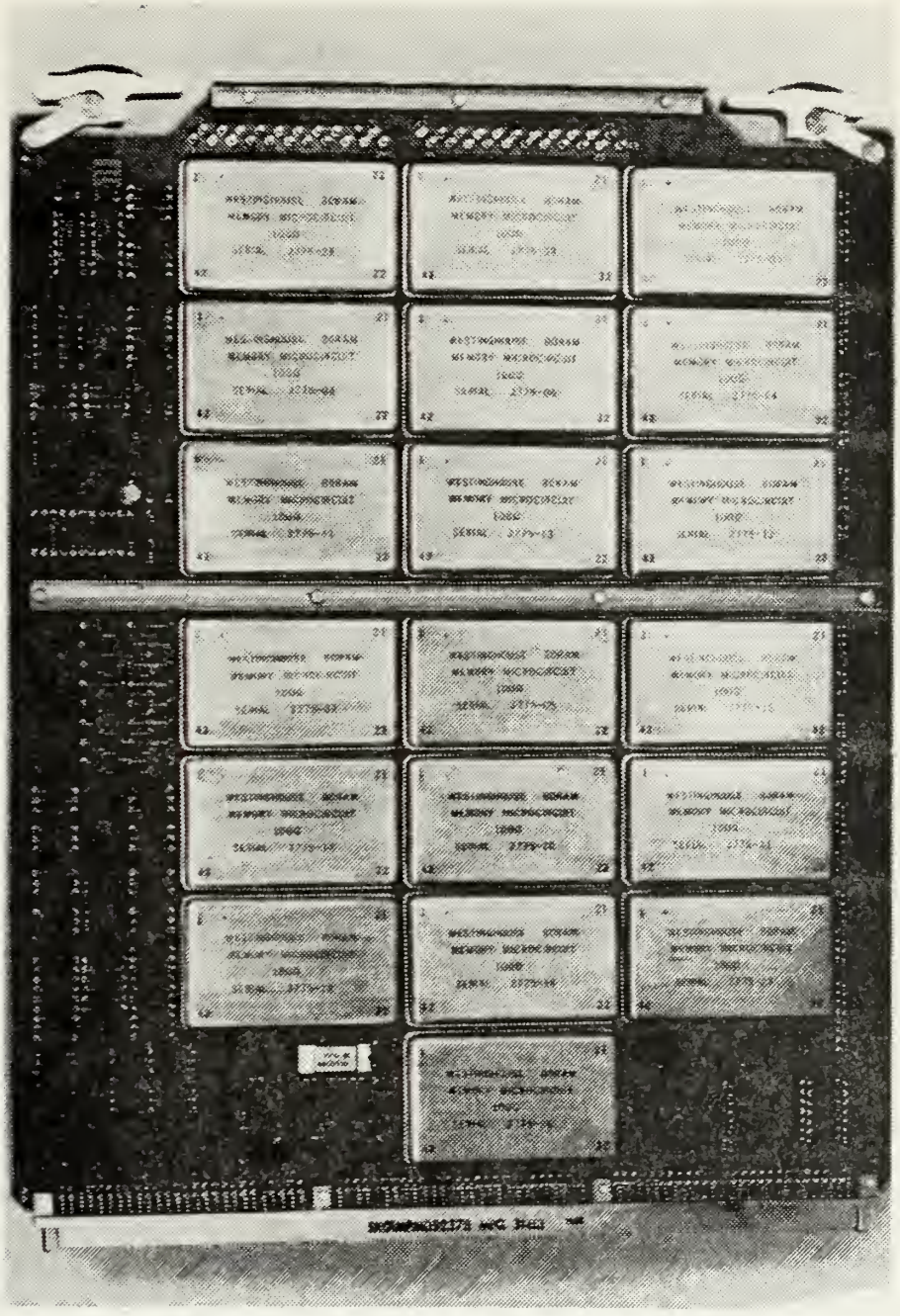


Figure 12. BORAM MEMORY CARD

1) Read access time...60 microseconds

2) Write cycle time...120 microseconds

3) Erase cycle time...200 microseconds

4) Temperature range..-55 to +125 deg C

5) Endurance.....10^{10} write/erase cycles

6) Retention.....4000 hours

7) Density.....2048 BITS (161x169 mils)

D. VIRTUALLY NONVOLATILE RANDOM ACCESS MEMORY

The Virtually Nonvolatile Random Access Memory (VINRAM) [Ref. 12] was developed jointly by the Westinghouse Defense and Electronic Systems Center and the Aeronautical Systems Division of the U.S. Air Force.

The basic storage element of the VINRAM memory cell contains a volatile and a nonvolatile memory site. The volatile site consists of a MOS transistor while the nonvolatile site consists of a MNOS transistor. This configuration allows the memory to be used mainly in the volatile mode. When power is removed or upon external command the information is transferred in parallel from the volatile sites to the MNOS elements. When power is regained the data in the nonvolatile sites is written into the volatile sites and the MNOS elements are erased. The endurance of the memory is improved by decreasing the number of required MNOS write/erase cycles. Since the volatile memory structures are used most the time, the read and write cycle times are similar to those of volatile semiconductor memories.

The characteristics of the VINRAM memory are:

1) Read access time...500 nanoseconds

2) Write cycle time...700 nonoseconds

3) Erase cycle time...10 microseconds

4) Temperature range..-55 to +125 deg C

5) Endurance.....Depends on MNOS write/erase cycles.

6) Retention.....2,000 hours (10 microseconds MNOS write cycle)

7) Density.....2,048 BITS (154 x 170 mils) Present

4,096 BITS (200 x 200 mils) Under Development

E. ELECTRICALLY ALTERABLE RANDOM ACCESS MEMORY

The Nitron Division of McDonnell Douglas Corporation manufactures the NCM7050 Electrically Alterable Random Access memory (EARAM) [Ref. 13]. This commercially available memory is a 1,024 BIT, fully decoded, nonvolatile MNOS memory designed for use in systems requiring permanent data storage without power consumption.

The characteristics of the NCM 7050 memory are:

1) Read access time...1.5 microseconds

2) Write cycle time...1.5 milliseconds

3) Erase cycle time...1.2 seconds

4) Temperature range..0 to + 70 deg C

5) Endurance.....10^6 write/erase cycles

6) Retention.....10,000 hours

7) Density.....1024 BITS (24 pin package)

APPENDIX B

COMPUTER PROGRAMS

This appendix contains the computer programs used in the development and testing of the Crash Data Recorder.

The first program, PROCESS PLM, performs the analysis and the recording of the parameters by the airborne component of the system. This routine was written in PL/M and consists of 6 procedures and the main program. The procedure ALGO contains the algorithm which decides when to record the parameters. If a parameter is to be recorded, the RECORD procedure writes the information in the solid state memory. The other procedures are used to support the main program and to control the memory module. The main program consists of a sequential analysis of each of the parameters in the order received by the Memory Buffer Register.

The RECOVER PLM program, written in PL/M, was designed to expand an display the compressed data in a standard format. The recovered information is first read into the microcomputer's memory by the MEMORY READ procedure. The main program separates the parameters into individual buffers, completes the missing information, and converts the values to engineering units. The reconstructed flight is displayed via the input-output terminal by the PRINT procedure.

The last program, PLOT FORTRAN, was designed to plot

the data from the original and the recovered flight on a Calcomp plotter. The routine was written in Fortran to make it compatible with the operating system used to drive the plotter. The parameter values are plotted versus time using the Naval Postgraduate School's subroutine DRAWP. The plots made using this program are included in Appendix C.

```
PROCESS PLM


  /* DECLARATION STATEMENTS */

DECLARE DCL LITERALLY 'DECLARE',
        LIT LITERALLY 'LITERALLY';
DCL TRUE LIT '0FFH',
   FALSE LIT '0';
DCL (LIMIT2,LIMIT4,LIMIT6,LIMIT7) BYTE,
    (MINFLAG,SECFLAG) BYTE,
    (I,M) BYTE;
DCL (OLDMIN,NEWMIN,NEWSEC) ADDRESS,
    (ALTC,ALTF,KCAS,HEAD,DP$1,DP$2,VG) ADDRESS,
    (INPUTBASE, OUTPUTBASE) ADDRESS,
    (INPUTBUFF BASED INPUTBASE) (720) ADDRESS,
    (OUTPUTBUFF BASED OUTPUTBASE) (720) ADDRESS,
    (J,K) ADDRESS;

  /* PROCEDURES */

CONVERT:  PROCEDURE (VALUE) ADDRESS;
DCL VALUE ADDRESS;
RETURN SHL(VALUE,8) + HIGH(VALUE);
END CONVERT;

NEXTPARAM:  PROCEDURE ADDRESSS;
DCL ITEM ADDRESS;
ITEM=CONVERT(INPUTBUFF(J));
J=J+1;
RETURN ITEM;
END NEXTPARAM;

RECORD:  PROCEDURE (ITEM,NAME);
DCL ITEM ADDRESS;
DCL NAME BYTE;
IF SECFLAG THEN DO;
                OUTPUTBUFF(K)=CONVERT(NEWSEC+1000H);
                SECFLAG=FALSE;
                K=K+1;
                END;
IF MINFLAG THEN DO;
                OUTPUTBUFF(K)=CONVERT(NEWMIN);
                MINFLAG=FALSE;
                K=K+1;
                END;
OUTPUTBUFF(K)=CONVERT(ITEM+SHL(DOUBLE(NAME),12));
K=K+1;
RETURN;
END RECORD;
```

```
ALGO:  PROCEDURE (OLD,THRESH,NAME) ADDRESS;
DCL (OLD,NEW,DIFF) ADDRESS;
DCL (THRESH,NAME) BYTE;
NEW=NEXTPARAM;
IF NEW > OLD THEN DIFF=NEW-OLD;
             ELSE DIFF=OLD-NEW;
IF LOW(DIFF) > THRESH THEN DO;
                           CALL RECORD(NEW,NAME);
                           RETURN NEW;
                           END;
                      ELSE RETURN OLD;
END ALGO;

VERTG:  PROCEDURE (NAME);
DCL NAME BYTE;
VG=ALGO(VG,LIMIT2,NAME);
RETURN;
END VERTG;

  /* MAIN PROGRAM */

MINFLAG,SECFLAG=FALSE;
ALTC,ALTF,KCAS,HEAD,VG = FALSE;
DP$1,DP$2=0FFH;
OLDMIN,J,K=0;
INPUTBASE=1000H;
OUTPUTBASE=2000H;
DO I = 0 TO 59;
 NEWMIN=NEXTPARAM;
 IF OLDMIN <> NEWMIN THEN DO;
                          OLDMIN=NEWMIN;
                          MINFLAG=TRUE;
                          END;
 NEWSEC=NEXTPARAM;
 SECFLAG=TRUE;
 CALL VERTG(2);
 ALTC=ALGO(ALTC,0,3);
 ALTF=ALGO(ALTF,LIMIT4,4);
 CALL VERTG(5);
 KCAS=ALGO(KCAS,LIMIT6,6);
 HEAD=ALGO(HEAD,LIMIT7,7);
 CALL VERTG(8);
 DP$1=ALGO(DP$1,0,9);
 DP$2=ALGO(DP$2,0,10);
 CALL VERTG(11);
END;
OUTPUTBUFF(K)=0FFFFH;
GO TO 3800H;
```

```
  /* MEMORY RECORDING PROCEDURE */

DCL(DESTI,CONTROL,MESS) BYTE;
DCL INFO ADDRESS;
DESTI = 0;
DO I = 0 TO 3;
 OUTPUT(5)=NOT DESTI;
 CONTROL=10H;
 OUTPUT(7)=NOT CONTROL;
 CONTROL=50H;
 OUTPUT(7)=NOT CONTROL;
   DO M = 1 TO 40;
   CALL TIME(250);
   END;
 CONTROL=10H;
 OUTPUT(7)=NOT CONTROL;
 DESTI=DESTI+40H;
END;
DESTI=0;
DO K = 0 TO 255;
 INFO=OUTPUTBUFF(K);
 OUTPUT(5)=NOT DESTI;
 CONTROL=0;
 OUTPUT(7)=NOT CONTROL;
 MESS=HIGH(INFO);
 OUTPUT(6)=MESS;
 CONTROL=1;
 OUTPUT(7)=NOT CONTROL;
 MESS=SHR(MESS,4);
 OUTPUT(6)=MESS;
 CONTROL=2;
 OUTPUT(7)=NOT CONTROL;
 MESS=LOW(INFO);
 OUTPUT(6)=MESS;
 CONTROL=3H;
 OUTPUT(7)=NOT CONTROL;
 MESS=SHR(MESS,4);
 OUTPUT(6)=MESS;
 CONTROL=CONTROL+40H;
 OUTPUT(7)=NOT CONTROL;
 CALL TIME(20);
 CONTROL=0;
 OUTPUT(7)=NOT CONTROL;
 DESTI=DESTI+1;
END;
EOF
```

```
  /* DECLARATION STATEMENTS */

DECLARE DCL LITERALLY 'DECLARE',
        LIT LITERALLY 'LITERALLY';
DCL (INPUTBASE,OUTPUTBASE) ADDRESS,
    (INPUTBUFF BASED INPUTBASE) (720) ADDRESS,
    (OUTPUTBUFF BASED OUTPUTBASE) (2880) BYTE;
DCL (MINS,SECS,ALTC,ALTF) (60) ADDRESS,
    (KCAS,HEAD,DP$1,DP$2) (60) ADDRESS,
    (VG$1,VG$2,VG$3,VG$4) (60) ADDRESS;
DCL CR LIT '0DH',
    LF LIT '0AH',
    SP LIT '20H';
DCL (TEMP,NUMB1,NUMB2,I,J) ADDRESS,
    (NAME,K,M,N,L) BYTE,
    RESULT (4) BYTE;
DCL TITLE DATA ('MINS SECS ALTC ALTF KCAS HEAD
                 DP-1 DP-2 VG-1 VG-2 VG-3 VG-4');

  /* PROCEDURES */

PRINT:  PROCEDURE (CHAR);
DCL CHAR BYTE;
GO TO 3809H;
END PRINT;

CRLF:  PROCEDURE;
CALL PRINT (CR);
CALL PRINT (LF);
RETURN;
END CRLF;

  /* MAIN PROGRAM */

INPUT BASE=2000H;
OUTPUTBASE=1000H;
DO M = 0 TO 59;
   MINS(M),DP$1(M),DP$2(M)=0AAAAH;
   ALTC(M),ALTF(M),KCAS(M),HEAD(M)=0AAAAH;
   VG$1(M),VG$2(M),VG$3(M),VG$4(M)=0AAAAH;
   SECS(M)=DOUBLE(M);
END;
I=0;
DO WHILE (TEMP:=INPUTBUFF(I))<>0FFFFH;
   TEMP=SHL(TEMP,8)+HIGH(TEMP);
   NAME=SHR(HIGH(TEMP),4);
   IF NAME=1 THEN M=LOW(TEMP);
```

```
   TEMP=TEMP AND 0FFFH;
     DO CASE NAME;
        MINS(M)=TEMP;
        SECS(M)=SECS(M);
        VG$1(M)=TEMP;
        ALTC(M)=TEMP;
        ALTF(M)=TEMP;
        VG$2(M)=TEMP;
        KCAS(M)=TEMP;
        HEAD(M)=TEMP;
        VG$3(M)=TEMP;
        DP$1(M)=TEMP;
        DP$2(M)=TEMP;
        VG$4(M)=TEMP;
     END;
   I=I+1;
END;
DO M = 0 TO 59;
   IF MINS(M)=0AAAAH THEN MINS(M)=MINS(M-1);
   IF VG$1(M)=0AAAAH THEN VG$1(M)=VG$4(M-1);
   IF ALTC(M)=0AAAAH THEN ALTC(M)=ALTC(M-1);
   IF ALTF(M)=0AAAAH THEN ALTF(M)=ALTF(M-1);
   IF VG$2(M)=0AAAAH THEN VG$2(M)=VG$1(M);
   IF KCAS(M)=0AAAAH THEN KCAS(M)=KCAS(M-1);
   IF HEAD(M)=0AAAAH THEN HEAD(M)=HEAD(M-1);
   IF VG$3(M)=0AAAAH THEN VG$3(M)=VG$2(M);
   IF DP$1(M)=0AAAAH THEN DP$1(M)=DP$1(M-1);
   IF DP$2(M)=0AAAAH THEN DP$2(M)=DP$2(M-1);
   IF VG$4(M)=0AAAAH THEN VG$4(M)=VG$3(M);
END;
DO M = 0 TO 59;
   ALTC(M)=SHL(ALTC(M),8);
END;
I=0;
DO M = 0 TO 59;
   INPUTBUFF(I)=MINS(M); I=I+1;
   INPUTBUFF(I)=SECS(M); I=I+1;
   INPUTBUFF(I)=ALTC(M); I=I+1;
   INPUTBUFF(I)=ALTF(M); I=I+1;
   INPUTBUFF(I)=KCAS(M); I=I+1;
   INPUTBUFF(I)=HEAD(M); I=I+1;
   INPUTBUFF(I)=DP$1(M); I=I+1;
   INPUTBUFF(I)=DP$2(M); I=I+1;
   INPUTBUFF(I)=VG$1(M); I=I+1;
   INPUTBUFF(I)=VG$2(M); I=I+1;
   INPUTBUFF(I)=VG$3(M); I=I+1;
   INPUTBUFF(I)=VG$4(M); I=I+1;
END;
J=0;
DO I = 0 TO 719;
   NUMB1=INPUTBUFF(I);
   M=3;
```

```
   DO N = 0 TO 3;
      RESULT(M)=(NUMB1-(NUMB2:=NUMB1/10)*10)+'0';
      NUMB1=NUMB2;
      M=M-1;
   END;
   DO M = 0 TO 3;
      OUTPUTBUFF(J)=RESULT(M);
      J=J+1;
   END;
END;
I=0;
DO M = 0 TO 2;
   CALL CRLF;
   DO N = 0 TO 58;
      CALL PRINT(TITLE(N));
   END;
   CALL CRLF;
   DO K = 0 TO 19;
      DO N = 0 TO 11;
         DO L = 0 TO 3;
            CALL PRINT(OUTPUTBUFF(I));
            I=I+1;
         END;
         CALL PRINT(SP);
      END;
      CALL CRLF;
   END;
END;
GO TO 3800H;

 /* MEMORY READING PROCEDURE */

DCL(DESTI,CONTROL,HIGHVAL,LOWVAL) BYTE;
DESTI=0;
DO I = 0 TO 255;
   OUTPUT(5)=NOT DESTI;
   CONTROL=30H;
   OUTPUT(7)=NOT CONTROL;
   CONTROL=70H;
   OUTPUT(7)=NOT CONTROL;
   HIGHVAL=INPUT(7) AND 0FH;
   CONTROL=31H;
   OUTPUT(7)=NOT CONTROL;
   CONTROL=71H;
   OUTPUT(7)=NOT CONTROL;
   HIGHVAL=HIGHVAL+SHL(INPUT(7),4);
   CONTROL=32H;
   OUTPUT(7)=NOT CONTROL;
   CONTROL=72H;
   OUTPUT(7)=NOT CONTROL;
   LOWVAL=INPUT(7) AND 0FH;
   CONTROL=33H;
```

```
    OUTPUT(7)=NOT CONTROL;
    CONTROL=73H;
    OUTPUT(7)=NOT CONTROL;
    LOWVAL=LOWVAL+SHL(INPUT(7),4);
    CONTROL=30H;
    OUTPUT(7)=NOT CONTROL;
    INPUTBUFF(I)=SHL(DOUBLE(HIGHVAL),8)+LOWVAL;
    DESTI=DESTI+1;
END;
EOF
```

```
      INTEGER*4 MINS(180),SECS(180),ITB(12)/12*0/
      REAL*4 ALT(180),KCAS(180),HEAD(180),VERG(720),TIMEX(720)
      REAL*4 RTB(28)/28*0.0/
      EQUIVALENCE (TITLE,RTB(5))
      REAL*8 TITLE(12)
      C
      DO 10 I=1,720
      TIMEX(I)=I-1
   10 CONTINUE
      C
      J=1
      DO 20 I=1,180
      READ(5,100) MINS(I),SECS(I),ALT(I),KCAS(I),HEAD(I),
      VERG(J),VERG(J+1),VERG(J+2),VERG(J+3)
      J=J+4
   20 CONTINUE
      C
      DO 30 I=1,720
      VERG(I)=VERG(I)/100.0
   30 CONTINUE
      WRITE (6,200)
      C
      J=1
      DO 40 I=1,180
      WRITE(6,300) MINS(I),SECS(I),ALT(I),KCAS(I),HEAD(I),
      VERG(J),VERG(J+1),VERG(J+2),VERG(J+3)
      J=J+4
   40 CONTINUE
      C
      DO 50 I=1,180
      ALT(I)=ALT(I)-15000.0
      KCAS(I)=KCAS(I)-240.0
   50 CONTINUE
      C
      DO 60 I=1,720
      VERG(I)=VERG(I)*100.0
   60 CONTINUE
      C
      ITB(3)=9
      ITB(4)=6
      RTB(1)=20.0
      RTB(2)=100.0
      READ(5,400) TITLE
      CALL DRAWP(180,TIMEX,ALT,ITB,RTB)
      ITB(4)=4
      RTB(2)=20.0
      READ(5,400) TITLE
```

```
CALL DRAWP(180,TIMEX,KCAS,ITB,RTB)
ITB(4)=9
RTB(2)=40.0
READ(5,400) TITLE
CALL DRAWP(180,TIMEX,HEAD,ITB,RTB)
ITB(4)=5
RTB(1)=80.0
RTB(2)=50.0
READ(5,400) TITLE
CALL DRAWP(720,TIMEX,VERG,ITB,RTB)
STOP
END
```

APPENDIX C

FLIGHT PARAMETERS LISTINGS AND PLOTS

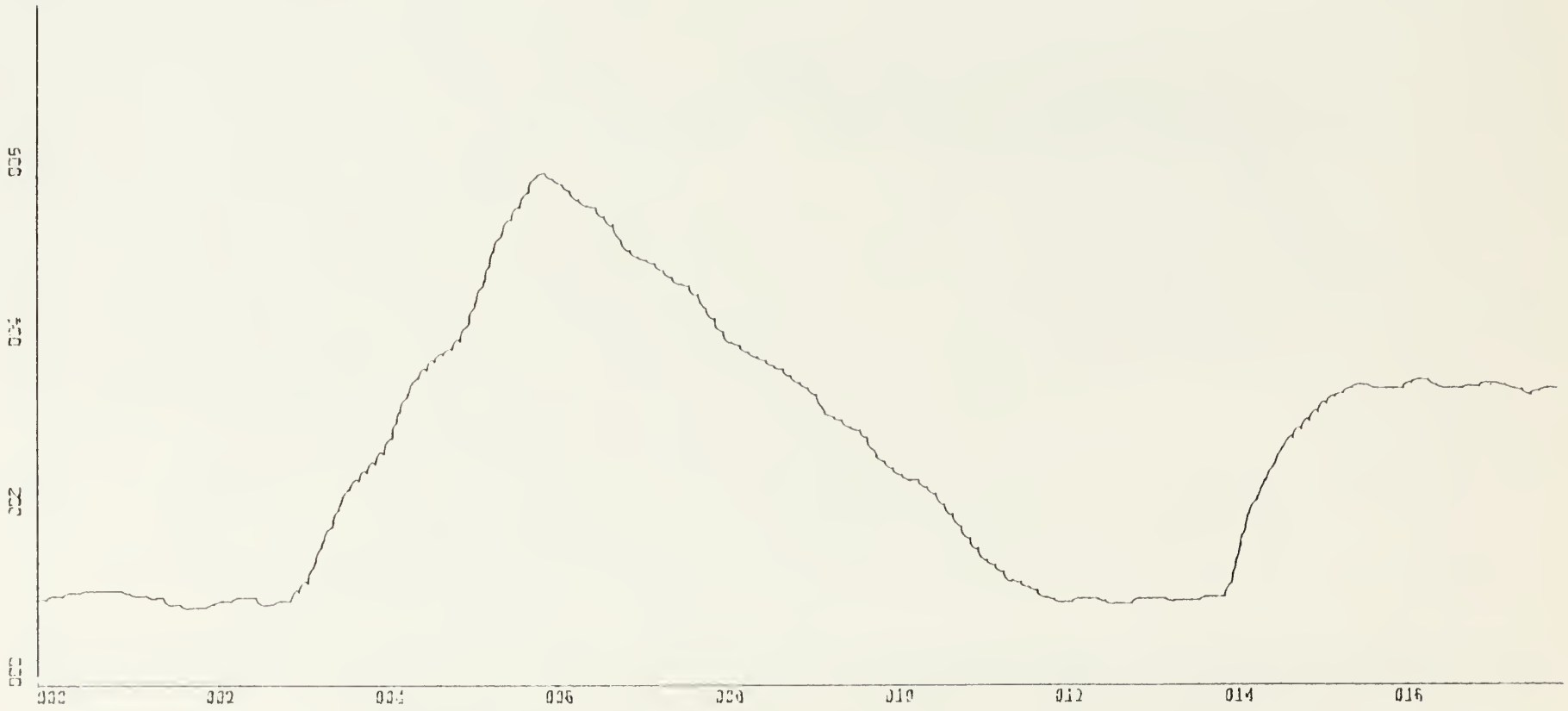
This appendix contains examples of the listings produced by the RECOVER PLM program and the Calcomp plots obtained using the PLOT FORTRAN routine.

Altitude, Computed Air Speed, Magnetic Heading, and Vertical Acceleration are plotted. Each parameter is plotted versus time from the original and the recovered data. The time axis expands the entire 3 minutes of the test flight. The original data plot of each parameter is followed by the corresponding recovered data plot for easy comparison.

The listed data represents the first minute of data depicted in the plots. Each section of 20 seconds from the original flight is followed by the corresponding section of the recovered flight.

ALTITUDE (Original)

Horizontal Scale = 20 seconds/inch
Vertical Scale = 200 feet/inch

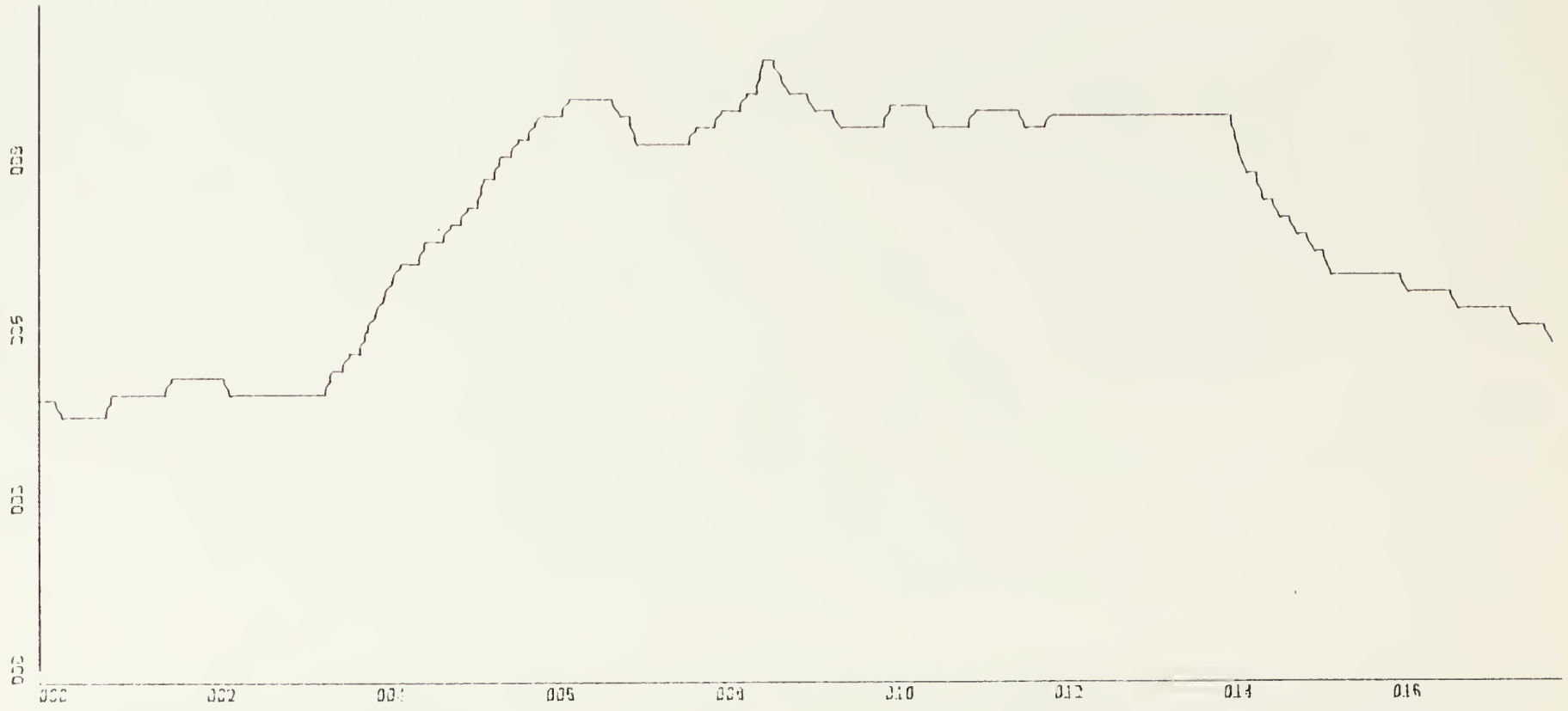


ALTITUDE (Recovered)

Horizontal Scale = 2- seconds/inch
Vertical Scale = 200 feet/inch

COMPUTED AIR SPEED (Original)

Horizontal Scale = 20 seconds/inch
Vertical Scale = 30 knots/inch

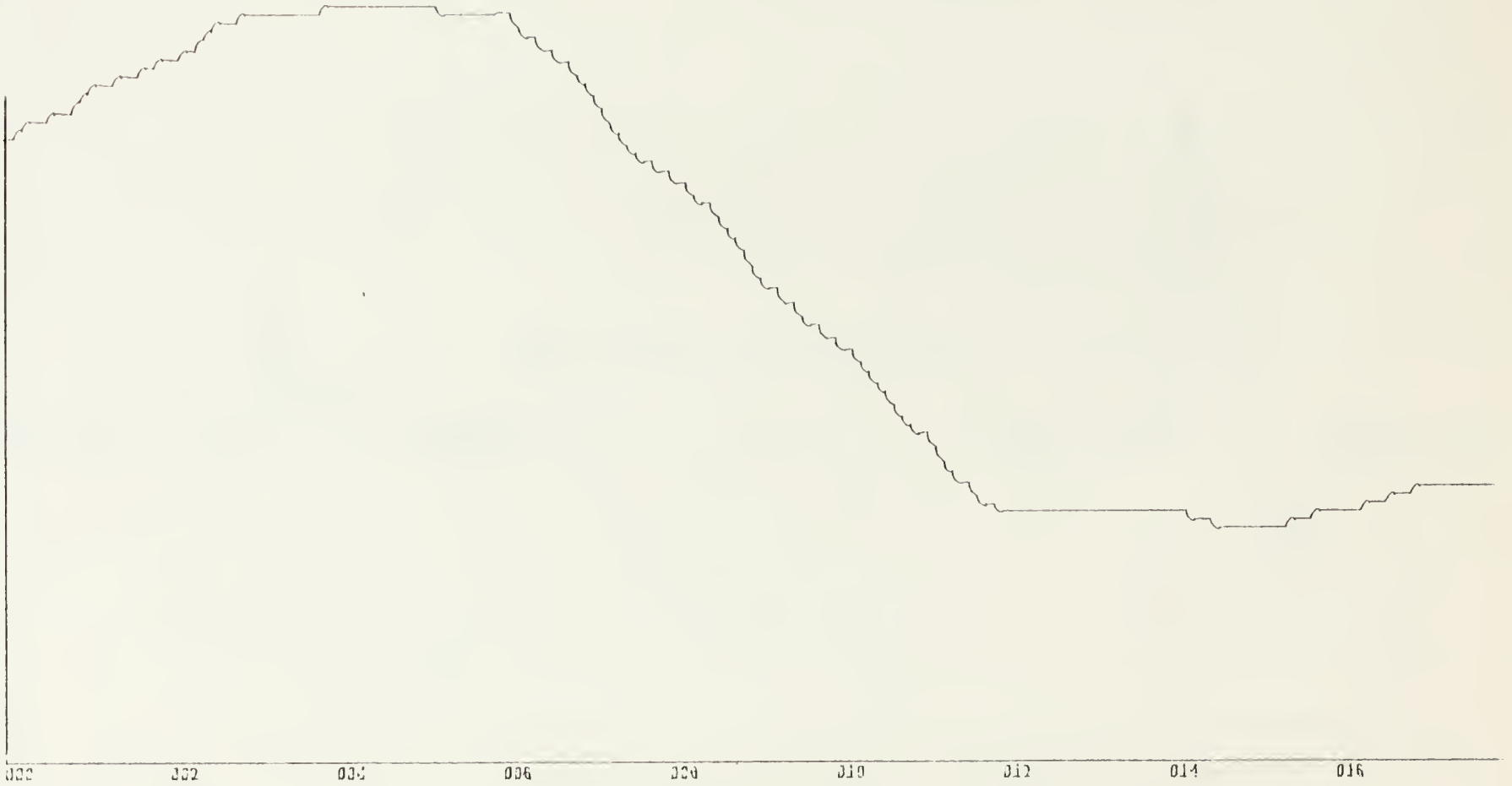


COMPUTED AIR SPEED (Recovered)

Horizontal Scale = 20 seconds/inch
Vertical Scale = 30 knots/inch

MAGNETIC HEADING (Original)

Horizontal Scale = 20 seconds/inch
Vertical Scale = 60 degrees/inch



MAGNETIC HEADING (Recovered)

Horizontal Scale = 20 seconds/inch
Vertical Scale = 60 degrees/inch

VERTICAL ACCELERATION (Original)

Horizontal Scale = 20 seconds/inch
Vertical Scale = 0.5 g/inch

VERTICAL ACCELERATION (Recovered)

Horizontal Scale = 20 seconds/inch
Vertical Scale = 0.5 g/inch

MINS	SECS	ALTC	ALTF	KCAS	HEAD	DP-1	DP-2	VG-1	VG-2	VG-3	VG-4
0028	0000	8960	0140	0250	0225	0000	0000	0100	0101	0101	0102
0028	0001	8960	0142	0249	0226	0000	0000	0102	0102	0103	0104
0028	0002	8960	0144	0248	0228	0000	0000	0105	0106	0106	0105
0028	0003	8960	0146	0247	0231	0000	0000	0106	0107	0107	0106
0028	0004	8960	0148	0246	0232	0000	0000	0106	0106	0105	0104
0028	0005	8960	0150	0245	0233	0000	0000	0105	0106	0106	0105
0028	0006	8960	0151	0246	0234	0000	0000	0106	0106	0105	0105
0028	0007	8960	0152	0247	0235	0000	0000	0106	0107	0105	0100
0028	0008	8960	0151	0248	0236	0000	0000	0103	0105	0107	0106
0028	0009	8960	0151	0251	0238	0000	0000	0106	0105	0106	0106
0028	0010	8960	0150	0252	0241	0000	0000	0105	0107	0109	0110
0028	0011	8960	0148	0251	0244	0000	0000	0107	0106	0104	0106
0028	0012	8960	0145	0250	0245	0000	0000	0106	0105	0106	0106
0028	0013	8960	0143	0251	0246	0000	0000	0105	0104	0105	0105
0028	0014	8960	0142	0252	0247	0000	0000	0105	0106	0106	0106
0028	0015	8960	0140	0253	0248	0000	0000	0107	0106	0108	0102
0028	0016	8960	0135	0254	0249	0000	0000	0102	0106	0104	0105
0028	0017	8960	0133	0254	0250	0000	0000	0105	0107	0106	0106
0028	0018	8960	0130	0255	0251	0000	0000	0106	0107	0106	0106
0028	0019	8960	0128	0256	0253	0000	0000	0107	0109	0108	0107

SECTION NO. 1 FIRST MINUTE - ORIGINAL DATA

MINS	SECS	ALTC	ALTF	KCAS	HEAD	DP-1	DP-2	VG-1	VG-2	VG-3	VG-4
0023	0000	8960	0140	0250	0225	0000	0000	0100	0100	0100	0100
0028	0001	8960	0140	0250	0225	0000	0000	0100	0100	0100	0100
0028	0002	8960	0144	0250	0228	0000	0000	0100	0106	0106	0106
0028	0003	8960	0144	0247	0231	0000	0000	0106	0106	0106	0106
0028	0004	8960	0148	0247	0231	0000	0000	0106	0106	0106	0106
0028	0005	8960	0148	0247	0231	0000	0000	0106	0106	0106	0106
0028	0006	8960	0151	0247	0234	0000	0000	0106	0106	0106	0106
0028	0007	8960	0151	0247	0234	0000	0000	0106	0106	0106	0100
0028	0008	8960	0151	0247	0234	0000	0000	0100	0100	0107	0107
0028	0009	8960	0151	0251	0238	0000	0000	0107	0107	0107	0107
0028	0010	8960	0151	0251	0241	0000	0000	0107	0107	0107	0107
0028	0011	8960	0148	0251	0244	0000	0000	0107	0107	0107	0107
0028	0012	8960	0145	0251	0244	0000	0000	0107	0107	0107	0107
0028	0013	8960	0145	0251	0244	0000	0000	0107	0107	0107	0107
0028	0014	8960	0142	0251	0247	0000	0000	0107	0107	0107	0107
0028	0015	8960	0142	0251	0247	0000	0000	0107	0107	0107	0107
0028	0016	8960	0135	0254	0247	0000	0000	0107	0107	0107	0107
0028	0017	8960	0135	0254	0250	0000	0000	0107	0107	0107	0107
0028	0018	8960	0130	0254	0250	0000	0000	0107	0107	0107	0107
0028	0019	8960	0130	0254	0253	0000	0000	0107	0107	0107	0107

SECTION NO. 1 FIRST MINUTE - RECOVERED DATA

MINS	SECS	ALTC	ALTF	KCAS	HEAD	DP-1	DP-2	VG-1	VG-2	VG-3	VG-4
0028	0020	8960	0128	0254	0254	0000	0000	0107	0106	0106	0106
0028	0021	8960	0135	0253	0255	0000	0000	0106	0107	0107	0107
0028	0022	8960	0139	0252	0256	0000	0000	0107	0105	0104	0105
0028	0023	8960	0141	0251	0258	0000	0000	0105	0105	0105	0105
0028	0024	8960	0143	0251	0260	0000	0000	0105	0106	0106	0106
0028	0025	8960	0145	0253	0263	0000	0000	0106	0107	0105	0103
0028	0026	8960	0141	0252	0266	0000	0000	0104	0105	0106	0106
0028	0027	8960	0135	0251	0267	0000	0000	0106	0107	0108	0106
0028	0028	8960	0135	0250	0268	0000	0000	0105	0103	0105	0103
0028	0029	8960	0138	0249	0269	0000	0000	0102	0100	0100	0100
0028	0030	8960	0140	0250	0270	0000	0000	0100	0104	0108	0110
0028	0031	8960	0150	0250	0270	0000	0000	0115	0125	0140	0150
0028	0032	8960	0160	0250	0270	0000	0000	0140	0130	0125	0118
0028	0033	8960	0182	0251	0270	0000	0000	0120	0123	0120	0118
0028	0034	8960	0208	0253	0269	0000	0000	0120	0125	0121	0120
0028	0035	8960	0226	0255	0269	0000	0000	0118	0117	0115	0115
0028	0036	8960	0252	0256	0270	0000	0000	0116	0115	0115	0114
0028	0037	9216	0014	0258	0270	0000	0000	0112	0104	0110	0109
0028	0038	9216	0024	0260	0271	0000	0000	0110	0115	0111	0110
0028	0039	9216	0034	0262	0272	0000	0000	0110	0111	0110	0110

SECTION NO. 2 FIRST MINUTE - ORIGINAL DATA

MINS	SECS	ALTC	ALTF	KCAS	HEAD	DP-1	DP-2	VG-1	VG-2	VG-3	VG-4
0028	0020	8960	0130	0254	0253	0000	0000	0107	0107	0107	0107
0028	0021	8960	0135	0254	0253	0000	0000	0107	0107	0107	0107
0028	0022	8960	0139	0254	0256	0000	0000	0107	0107	0107	0107
0028	0023	8960	0139	0251	0256	0000	0000	0107	0107	0107	0107
0028	0024	8960	0143	0251	0260	0000	0000	0107	0107	0107	0107
0028	0025	8960	0143	0251	0263	0000	0000	0107	0107	0107	0107
0028	0026	8960	0143	0251	0266	0000	0000	0107	0107	0107	0107
0028	0027	8960	0135	0251	0266	0000	0000	0107	0107	0107	0107
0028	0028	8960	0135	0251	0266	0000	0000	0107	0107	0107	0107
0028	0029	8960	0138	0251	0269	0000	0000	0107	0100	0100	0100
0028	0030	8960	0138	0251	0269	0000	0000	0100	0100	0108	0108
0028	0031	8960	0150	0251	0269	0000	0000	0115	0125	0140	0150
0028	0032	8960	0160	0251	0269	0000	0000	0140	0130	0130	0118
0028	0033	8960	0182	0251	0269	0000	0000	0118	0118	0118	0118
0028	0034	8960	0208	0251	0269	0000	0000	0118	0125	0125	0125
0028	0035	8960	0226	0255	0269	0000	0000	0118	0118	0118	0118
0028	0036	8960	0252	0255	0269	0000	0000	0118	0118	0118	0118
0028	0037	9216	0014	0258	0269	0000	0000	0112	0104	0110	0110
0028	0038	9216	0024	0258	0269	0000	0000	0110	0110	0110	0110
0028	0039	9216	0034	0262	0272	0000	0000	0110	0110	0110	0110

SECTION NO. 2 FIRST MINUTE - RECOVERED DATA

MINS	SECS	ALTC	ALTF	KCAS	HEAD	DP-1	DP-2	VG-1	VG-2	VG-3	VG-4
0028	0040	9216	0044	0265	0272	0000	0000	0112	0110	0110	0110
0028	0041	9216	0056	0268	0273	0000	0000	0111	0109	0111	0104
0028	0042	9216	0074	0271	0273	0000	0000	0112	0112	0110	0110
0028	0043	9216	0105	0274	0273	0000	0000	0109	0107	0109	0102
0028	0044	9216	0127	0275	0273	0000	0000	0110	0112	0101	0110
0028	0045	9216	0144	0276	0273	0000	0000	0110	0109	0108	0107
0028	0046	9216	0154	0278	0272	0000	0000	0107	0106	0105	0105
0028	0047	9216	0165	0279	0272	0000	0000	0106	0105	0105	0104
0028	0048	9216	0173	0280	0272	0000	0000	0104	0105	0104	0103
0028	0049	9216	0179	0281	0272	0000	0000	0103	0101	0101	0101
0028	0050	9216	0189	0282	0271	0000	0000	0100	0098	0097	0096
0028	0051	9216	0209	0284	0270	0000	0000	0098	0100	0101	0099
0028	0052	9216	0234	0286	0270	0000	0000	0100	0103	0102	0101
0028	0053	9472	0003	0289	0269	0000	0000	0103	0105	0100	0098
0028	0054	9472	0036	0291	0268	0000	0000	0099	0100	0103	0101
0028	0055	9472	0058	0293	0269	0000	0000	0103	0105	0101	0100
0028	0056	9472	0075	0294	0270	0000	0000	0099	0101	0102	0102
0028	0057	9472	0088	0296	0270	0000	0000	0103	0101	0100	0100
0028	0058	9472	0106	0298	0270	0000	0000	0097	0095	0096	0097
0028	0059	9472	0124	0299	0270	0000	0000	0095	0097	0099	0100

SECTION NO. 3 FIRST MINUTE - ORIGINAL DATA

MINS	SECS	ALTC	ALTF	KCAS	HEAD	DP-1	DP-2	VG-1	VG-2	VG-3	VG-4
0028	0040	9216	0044	0265	0272	0000	0000	0110	0110	0110	0110
0028	0041	9216	0056	0268	0272	0000	0000	0110	0110	0110	0104
0028	0042	9216	0074	0271	0272	0000	0000	0112	0112	0112	0112
0028	0043	9216	0105	0274	0272	0000	0000	0112	0112	0112	0102
0028	0044	9216	0127	0274	0272	0000	0000	0110	0110	0101	0110
0028	0045	9216	0144	0274	0272	0000	0000	0110	0110	0110	0110
0028	0046	9216	0154	0278	0272	0000	0000	0110	0110	0110	0110
0028	0047	9216	0165	0278	0272	0000	0000	0110	0110	0110	0104
0028	0048	9216	0173	0278	0272	0000	0000	0104	0104	0104	0104
0028	0049	9216	0179	0281	0272	0000	0000	0104	0104	0104	0104
0028	0050	9216	0189	0281	0272	0000	0000	0104	0098	0098	0098
0028	0051	9216	0209	0284	0272	0000	0000	0098	0098	0098	0098
0028	0052	9216	0234	0284	0272	0000	0000	0098	0098	0098	0098
0028	0053	9472	0003	0289	0269	0000	0000	0098	0105	0105	0098
0028	0054	9472	0036	0289	0269	0000	0000	0098	0098	0098	0098
0028	0055	9472	0058	0293	0269	0000	0000	0098	0105	0105	0105
0028	0056	9472	0075	0293	0269	0000	0000	0099	0099	0099	0099
0028	0057	9472	0088	0296	0269	0000	0000	0099	0099	0099	0099
0028	0058	9472	0106	0296	0269	0000	0000	0099	0099	0099	0099
0028	0059	9472	0124	0299	0269	0000	0000	0099	0099	0099	0099

SECTION NO. 3 FIRST MINUTE - RECOVERED DATA

APPENDIX D

MEMORY MODULE WIRING LISTS

The following are detailed wiring lists of the constructed nonvolatile memory module. The relative placement of the components in the module is shown in Figure 9. For purposes of identification the following conventions apply:

A1-XX	NITRON NCM7050 MEMORY 1 - PIN XX
A2-XX	NITRON NCM7050 MEMORY 2 - PIN XX
A3-XX	NITRON NCM7050 MEMORY 3 - PIN XX
A4-XX	NITRON NCM7050 MEMORY 4 - PIN XX
B1-XX	SIGNETICS 7407 BUFFER 1 - PIN XX
B2-XX	SIGNETICS 7407 BUFFER 2 - PIN XX
B3-XX	SIGNETICS 7407 BUFFER 3 - PIN XX
B4-XX	SIGNETICS 7407 BUFFER 4 - PIN XX
C1-XX	SIGNETICS 7442 BCD TO DECIMAL DECODER - PIN XX
IN7-X	INPUT PORT 7 - BIT X
OUT5-X	OUTPUT PORT 5- BIT X
OUT6-X	OUTPUT PORT 6- BIT X
OUT7-X	OUTPUT PORT 7- BIT X

MEMORIES (NCM 7050)

A1-01-------+15V	A4-01--------+15V
A1-02-------*	A4-02--------B4-02
A1-03-------*	A4-03--------B4-04
A1-04-------*	A4-04--------B4-06
A1-05-------*	A4-05--------B4-08
A1-06-------*	A4-06--------B4-10
A1-07-------*	A4-07--------B4-12
A1-08-------*	A4-08--------B2-10
A1-09-------*	A4-09--------B2-8
A1-10-------*	A4-10--------B2-6
A1-11----B3-02	A4-11--------B3-8
A1-12----GRND	A4-12--------GRND
A1-13-----15V	A4-13---------15V
A1-14-------*	A4-14--------B2-02
A1-15-------*	A4-15--------B2-04
A1-16-------*	A4-16--------B1-02
A1-17-------*	A4-17--------IN7-1
A1-18-------*	A4-18--------B1-04
A1-19-------*	A4-19--------IN7-2
A1-20-------*	A4-20--------B1-06
A1-21-------*	A4-21--------IN7-3
A1-22-------*	A4-22--------B1-08
A1-23-------*	A4-23--------IN7-4
A1-24-----+5V	A4-24--------+5V

*These pins are connected in series with corresponding pins of memories A2,A3, and A4.

BUFFERS (7407)

B1-01-------OUT6-1
B1-02-------A4-16 AND PU
B1-03-------OUT6-2
B1-04-------A4-18 AND PU
B1-05-------OUT6-3
B1-06-------A4-20 AND PU
B1-07-------GRND
B1-08-------A4-22 AND PU
B1-09-------OUT6-4
B1-10-------N/C
B1-11-------N/C
B1-12-------N/C
B1-13-------N/C
B1-14--------+5V

B2-01--------OUT7-7
B2-02--------A4-14 AND PU
B2-03--------OUT7-6
B2-04--------A4-15 AND PU
B2-05--------OUT7-5
B2-06--------A4-10 AND PU
B2-07--------GRND
B2-08--------A4-9 AND PU
B2-09--------OUT7-1
B2-10--------A4-8 AND PU
B2-11--------OUT7-2
B2-12--------N/C
B2-13--------N/C
B2-14--------+5V

B3-01-------C1-01
B3-02-------A1-11 AND PU
B3-03-------C1-02
B3-04-------A2-11 AND PU
B3-05-------C1-03
B3-06-------A3-11 AND PU
B3-07-------GRND
B3-08-------A4-11 AND PU
B3-09-------C1-04
B3-10-------N/C
B3-11-------N/C
B3-12-------N/C
B3-13-------N/C
B3-14--------+5V

B4-01--------OUT5-6
B4-02--------A4-02 AND PU
B4-03--------OUT5-5
B4-04--------A4-03 AND PU
B4-05--------OUT5-4
B4-06--------A4-04 AND PU
B4-07--------GRND
B4-08--------A4-05 AND PU
B4-09--------OUT5-3
B4-10--------A4-06 AND PU
B4-11--------OUT5-2
B4-12--------A4-07 AND PU
B4-13--------OUT5-1
B4-14--------+5V

PU-Connected to 1000 OHMS pull up resistor to +15 volts. See Figure 10.

DECODER (7442)

C1-01--------B3-01
C1-02--------B3-03
C1-03--------B3-05
C1-04--------B3-09
C1-05--------N/C
C1-06--------N/C
C1-07--------N/C
C1-08--------GRND
C1-09--------N/C
C1-10--------N/C
C1-11--------N/C
C1-12--------SWITCH-ON(GRND)-OFF(+5V)
C1-13--------GRND
C1-14--------OUT5-8
C1-15--------OUT5-7
C1-16--------+5V

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