

Latches and Flip-flops (3A)

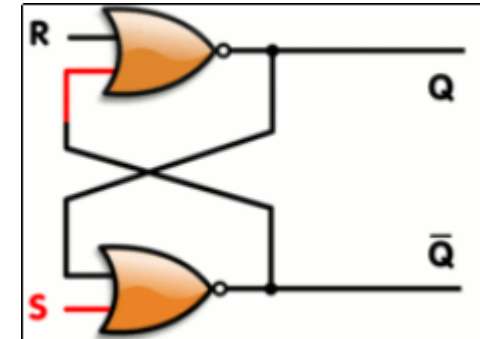
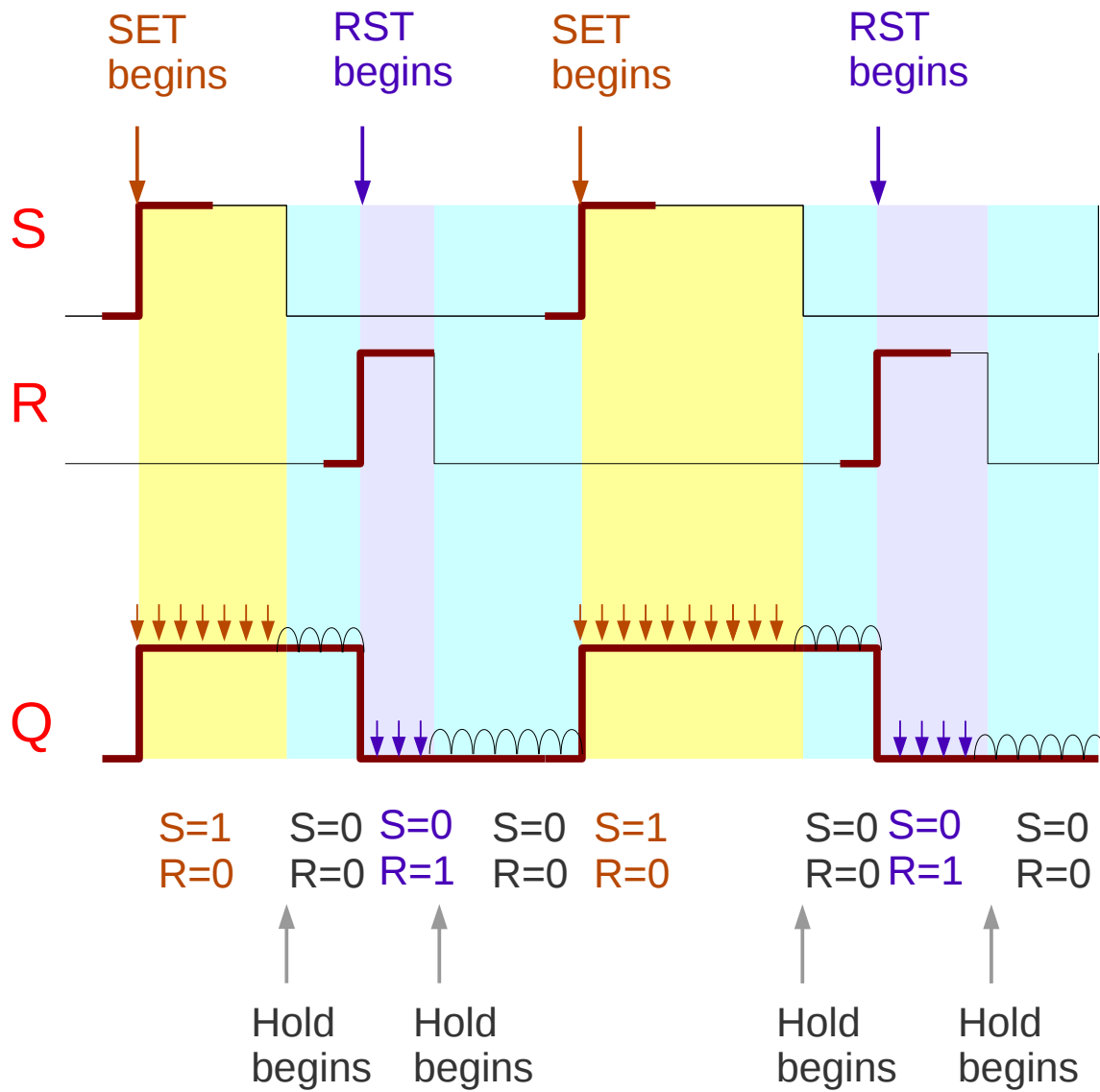
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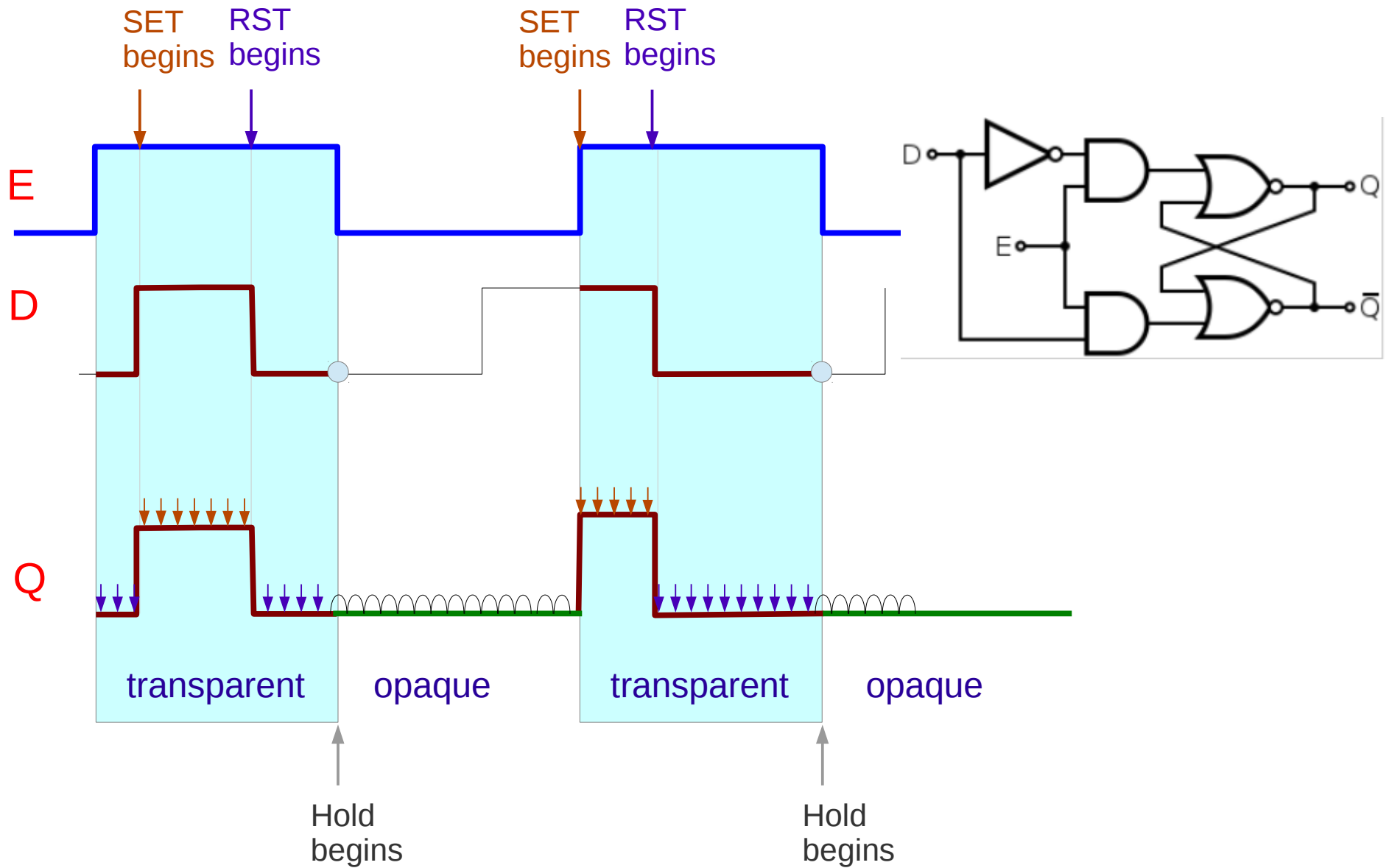
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NOR-based SR Latch

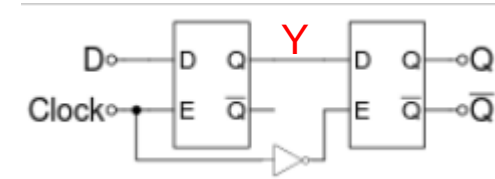
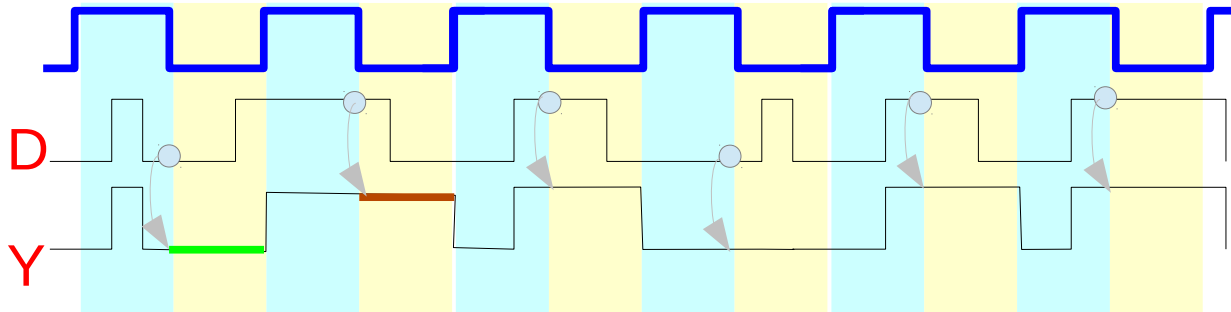


NOR-based D Latch

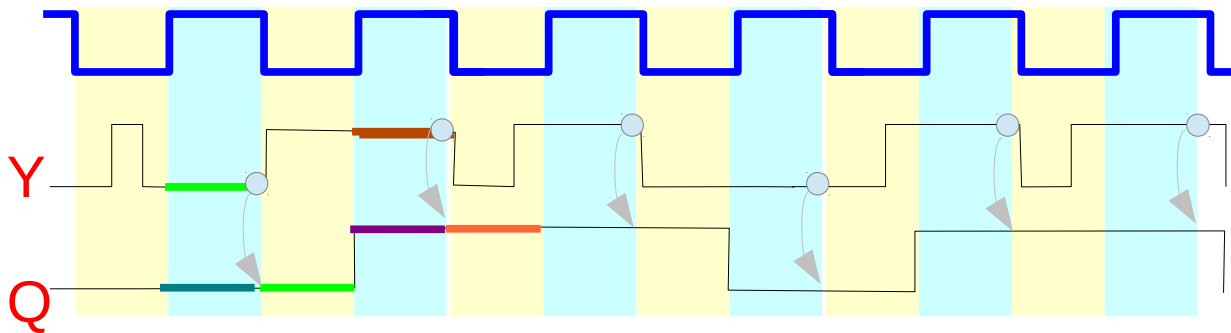


Master-Slave D FlipFlop

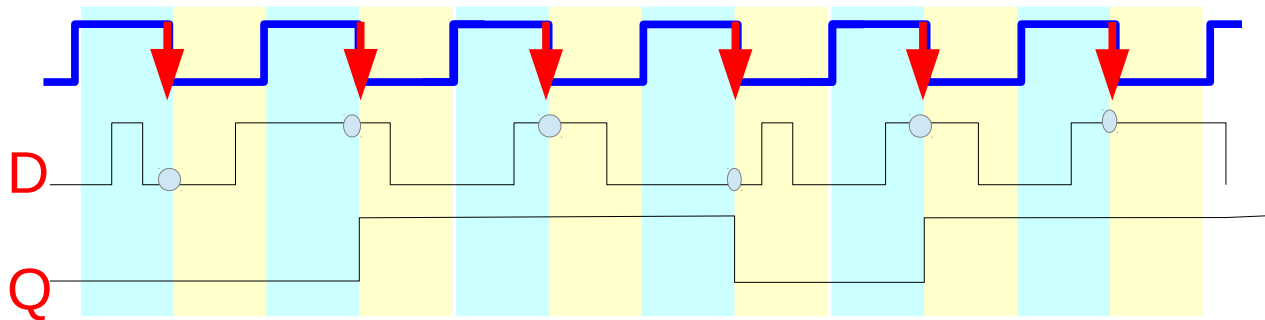
Master D Latch



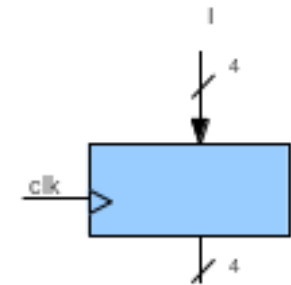
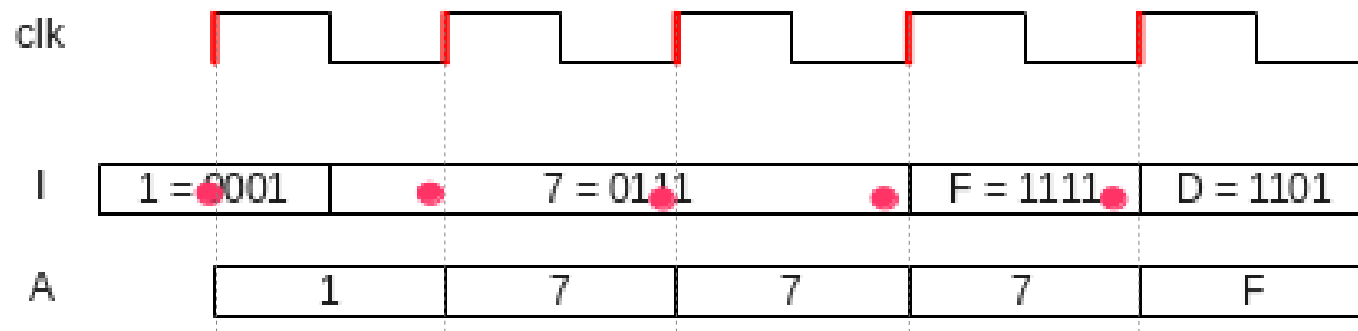
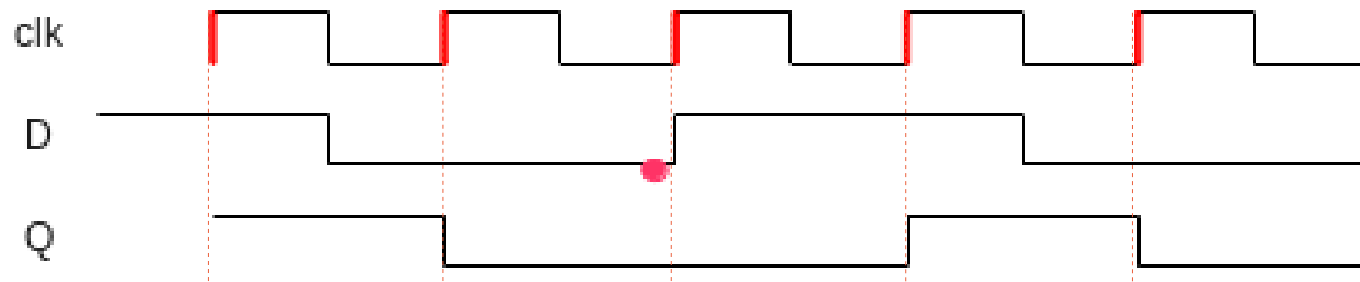
Slave D Latch



Master-Slave D F/F

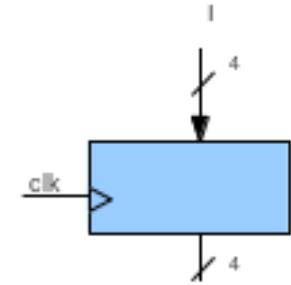
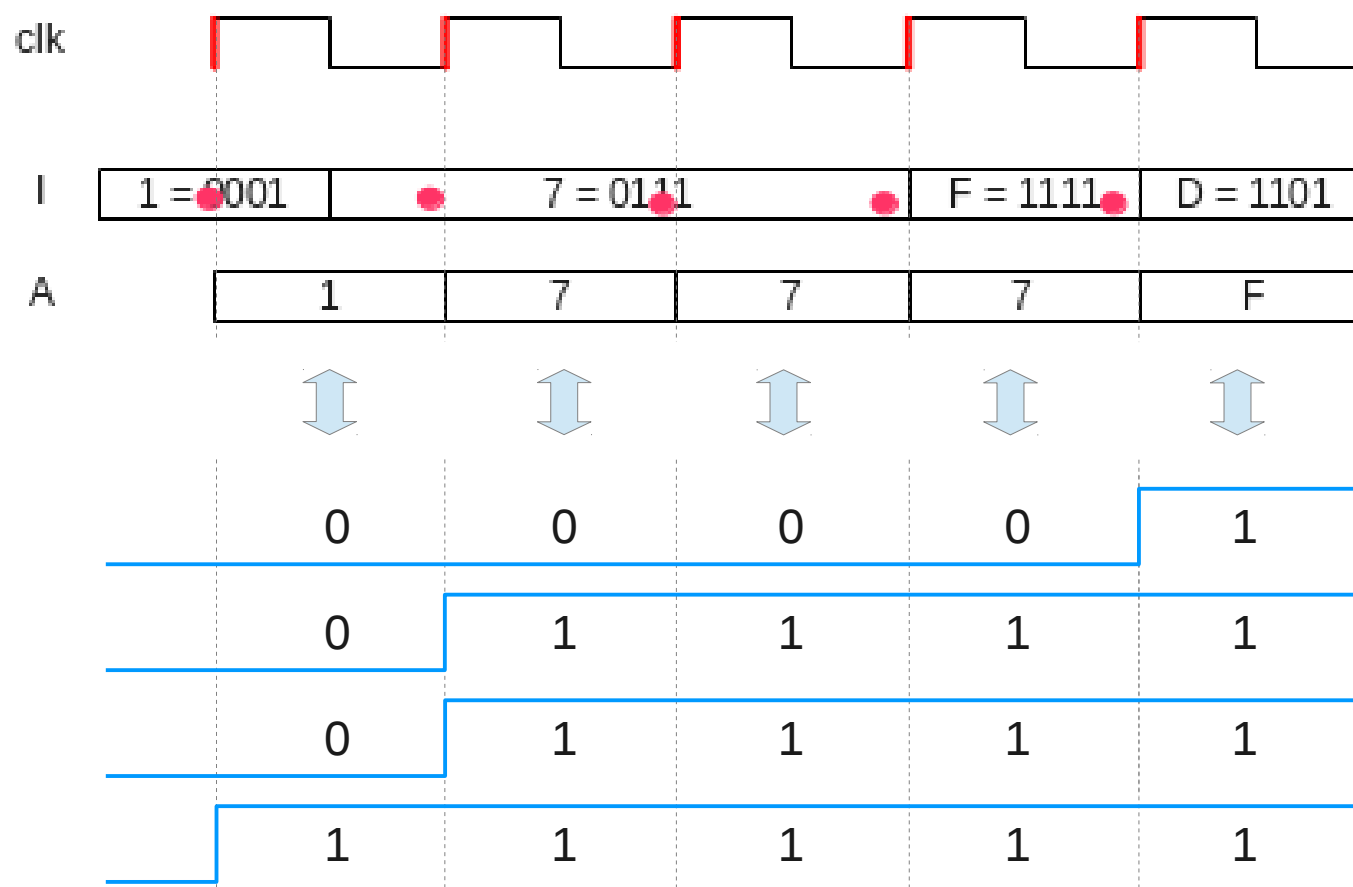


FF and Register Timing



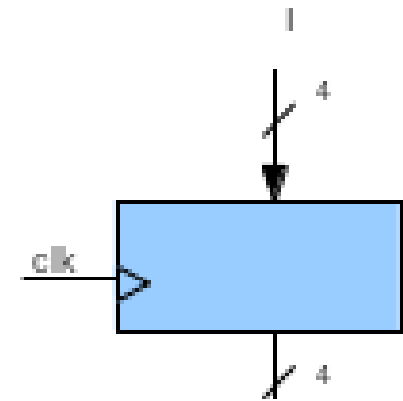
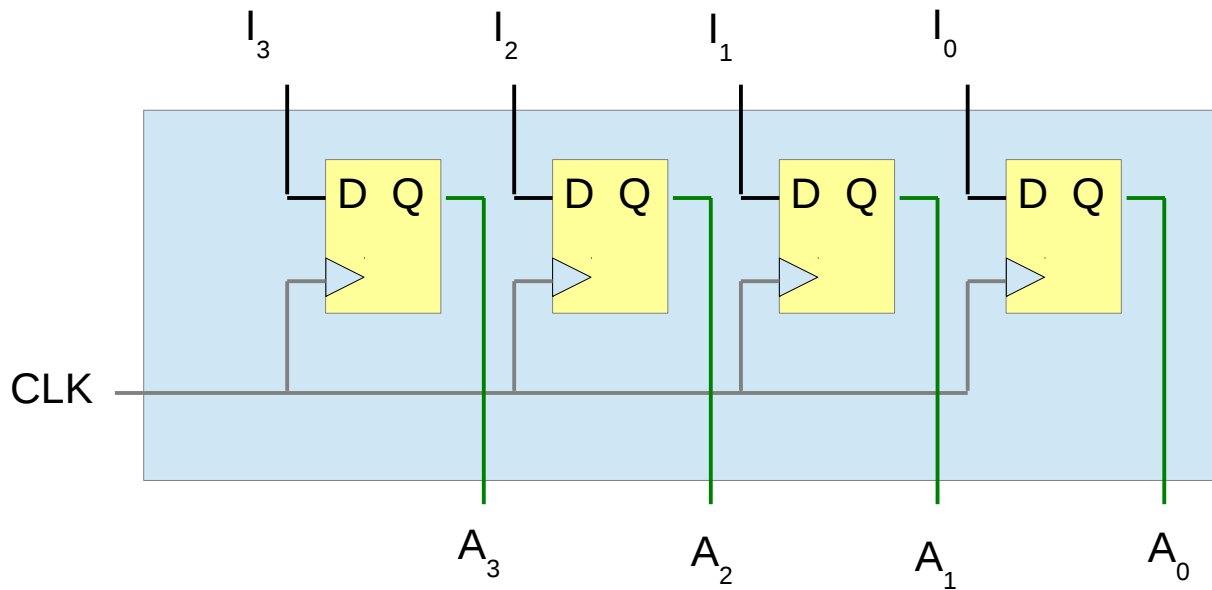
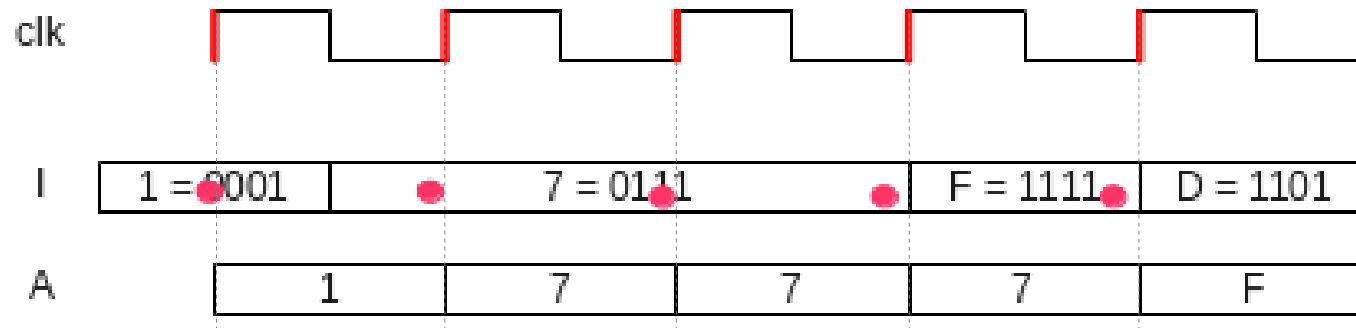
Decimal

Bus Notation



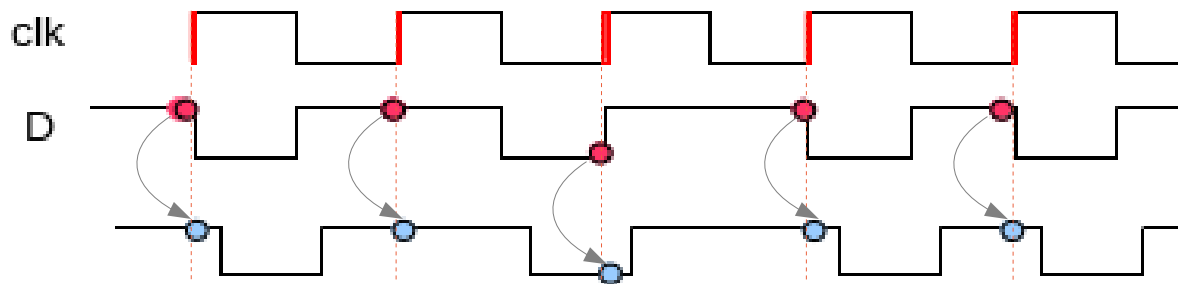
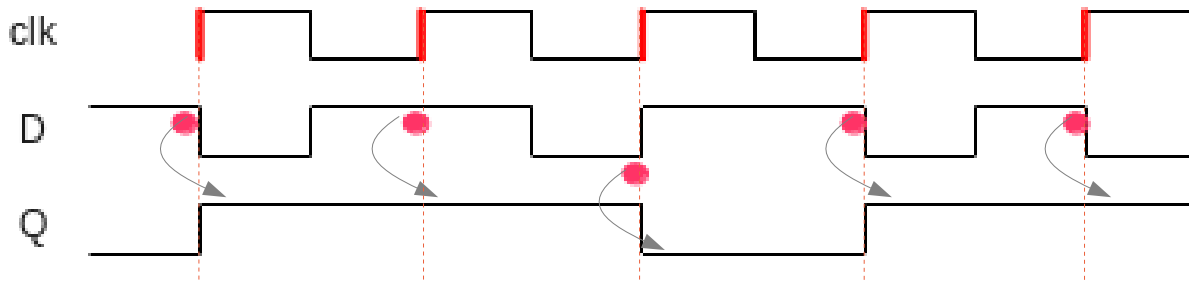
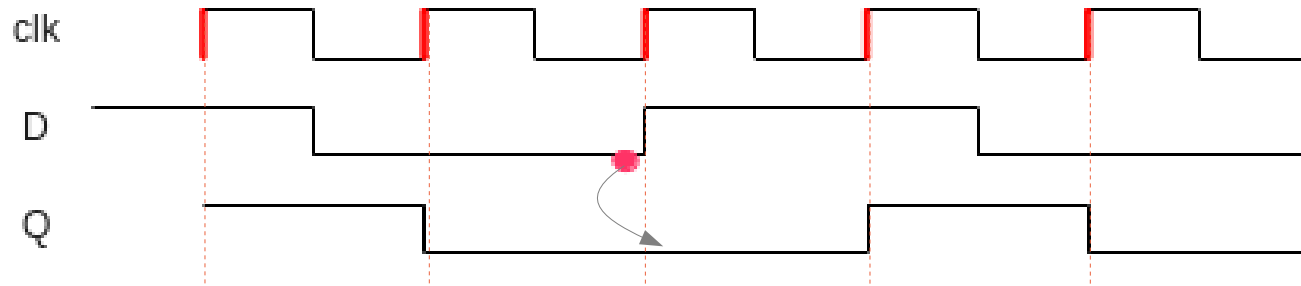
Decimal

Register



Decimal

FF Timing

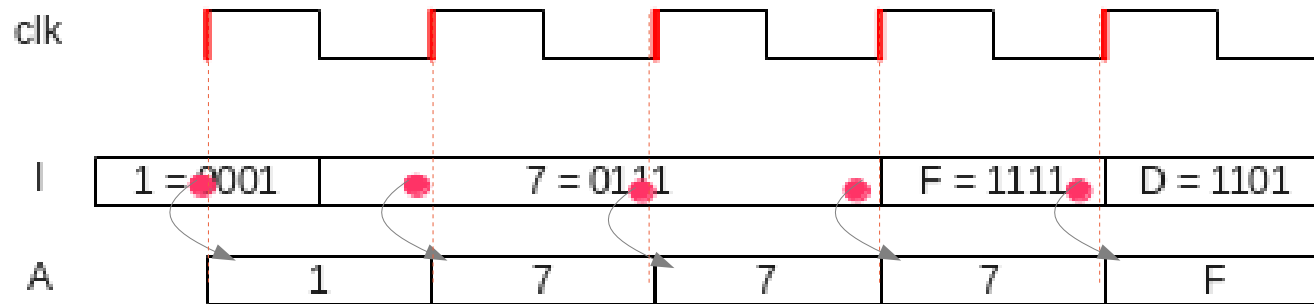


input signal with a delay ignored (ideal case)

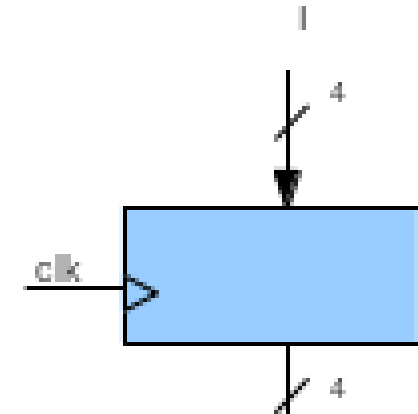
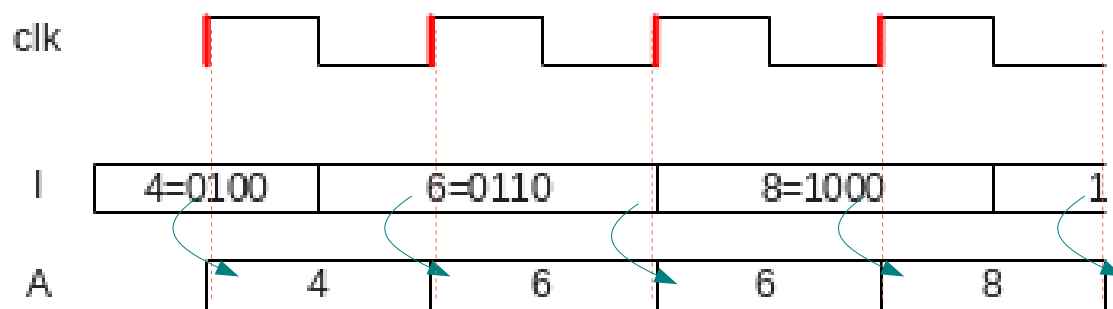
input signal with a delay explicitly shown

Register Timing

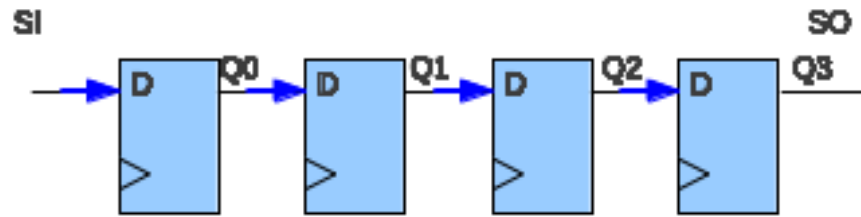
input signal with a delay explicitly shown



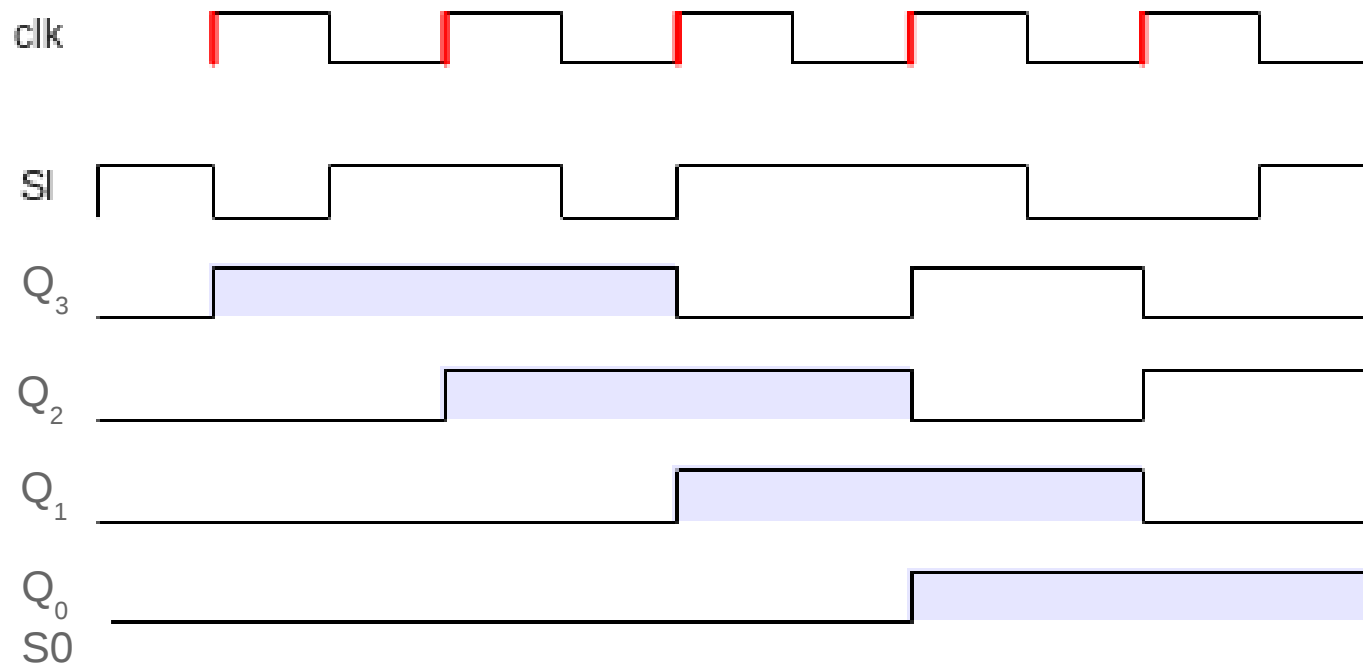
input signal with a delay explicitly shown



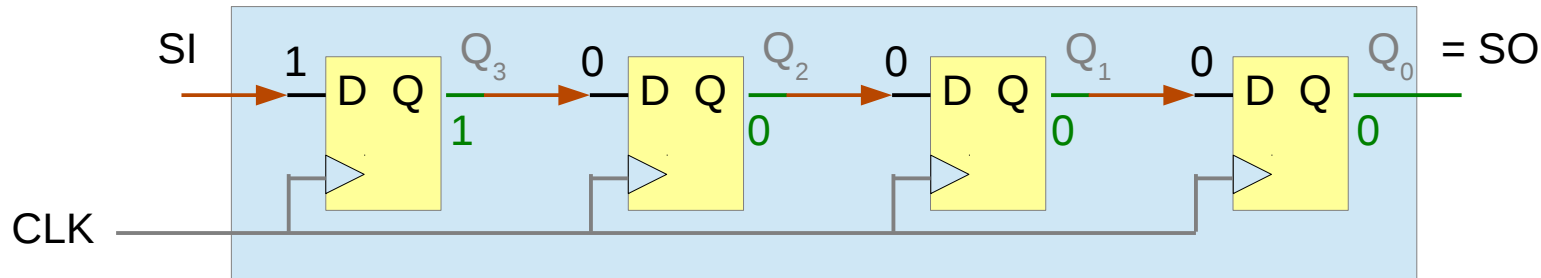
Shift Register Timing



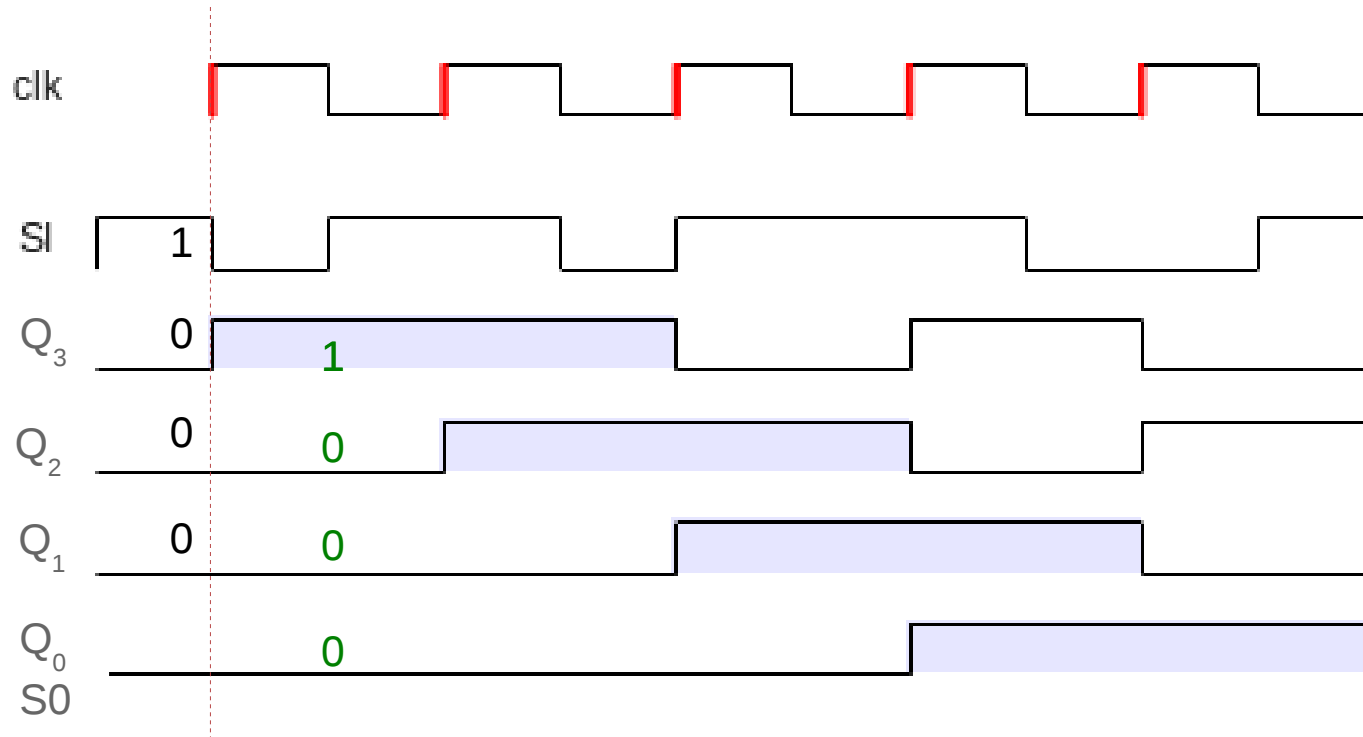
Connected in serial,
but parallel assignments



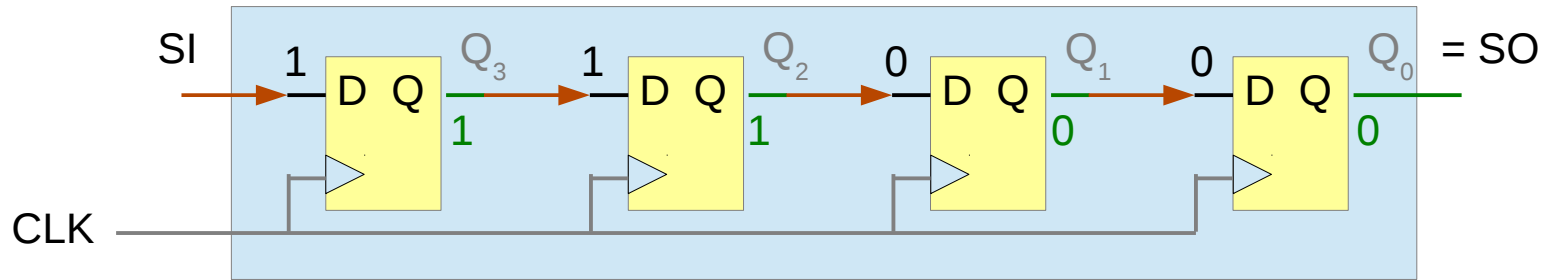
Shift Register Timing - Cycle 1



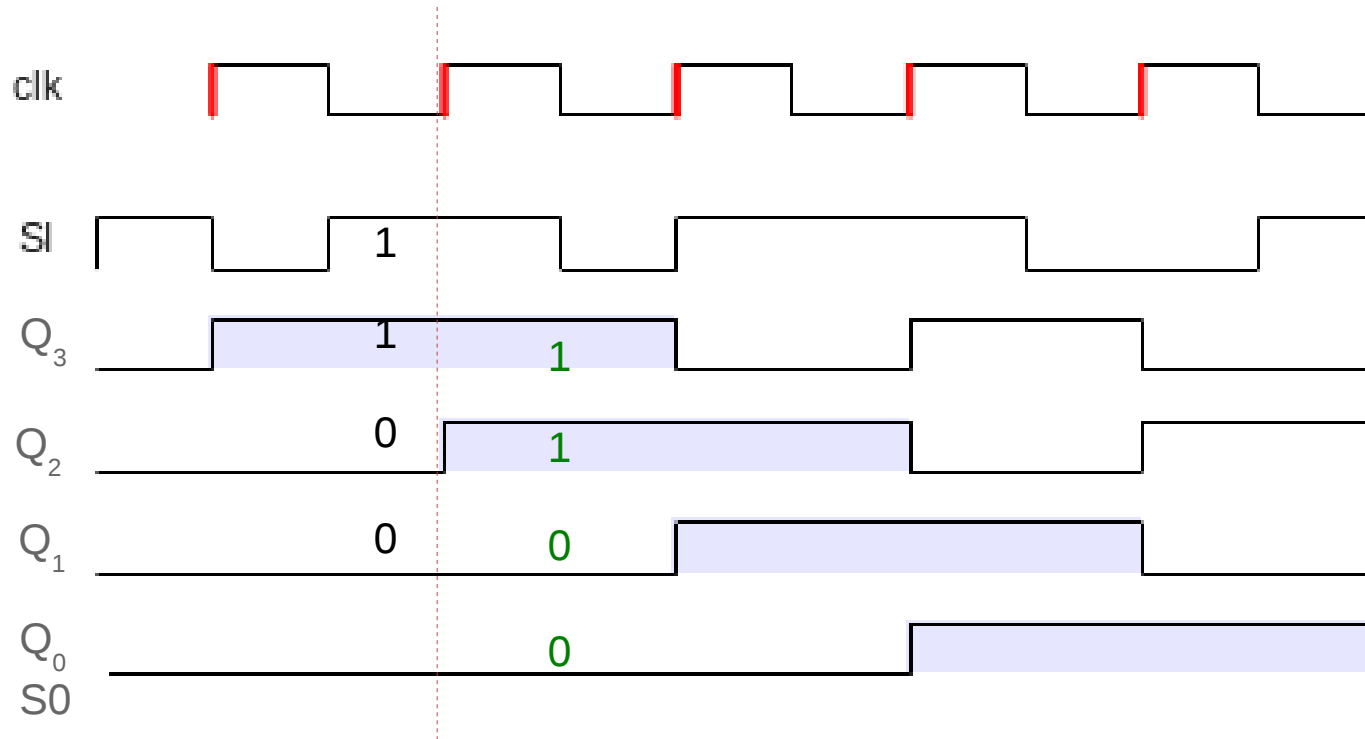
Connected in serial,
but parallel assignments



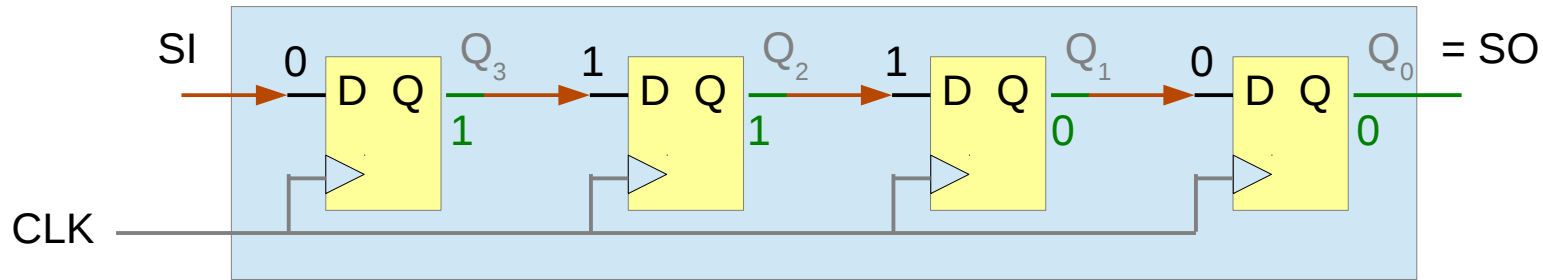
Shift Register Timing - Cycle 2



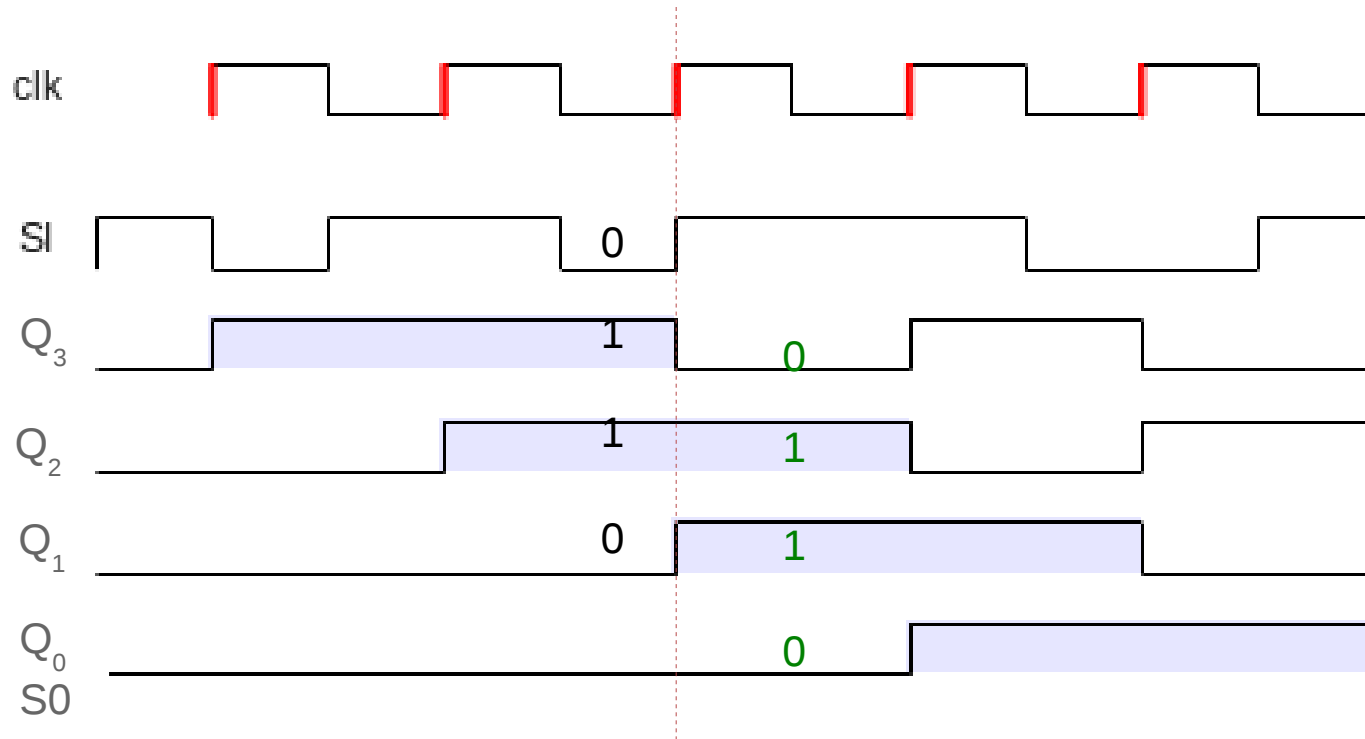
Connected in serial,
but parallel assignments



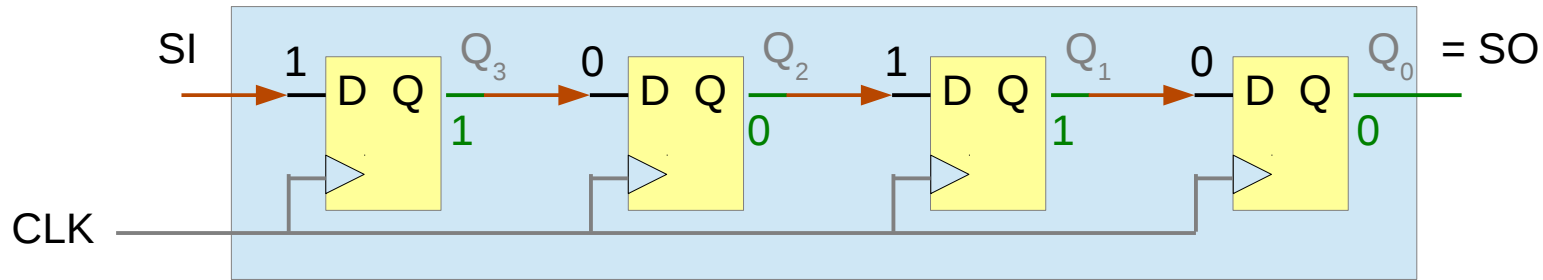
Shift Register Timing - Cycle 3



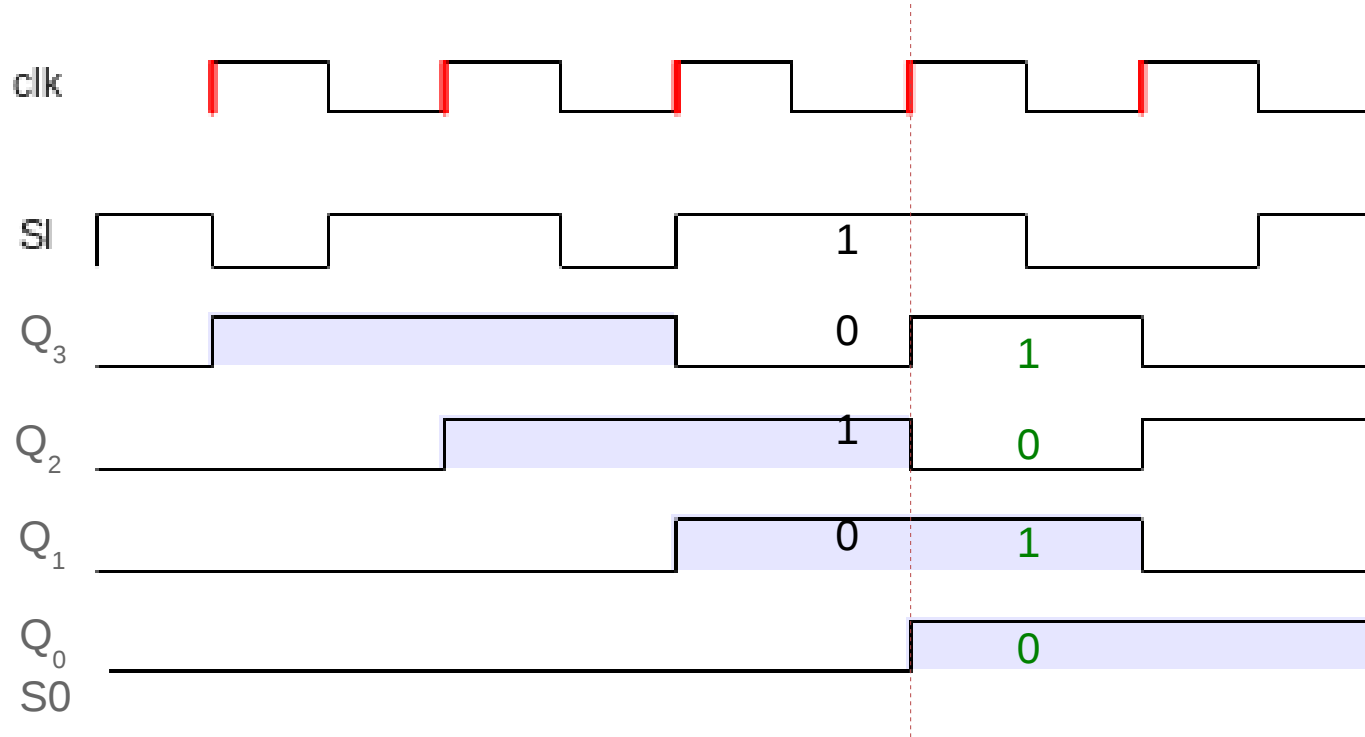
Connected in serial,
but parallel assignments



Shift Register Timing - Cycle 4



Connected in serial,
but parallel assignments



References

- [1] <http://en.wikipedia.org/>
- [2] <http://planetmath.org/>
- [3] M.L. Boas, "Mathematical Methods in the Physical Sciences"