Cache Design (H1)

20160530

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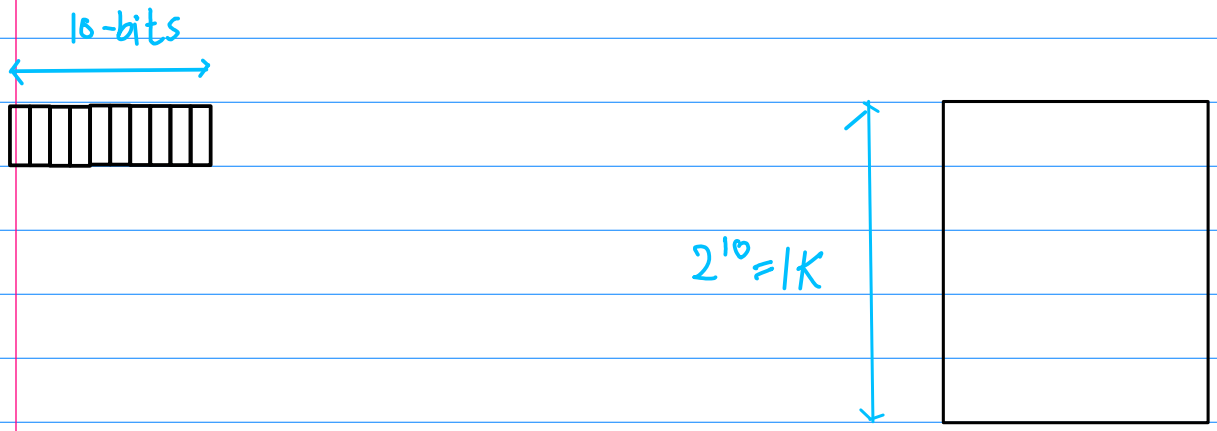
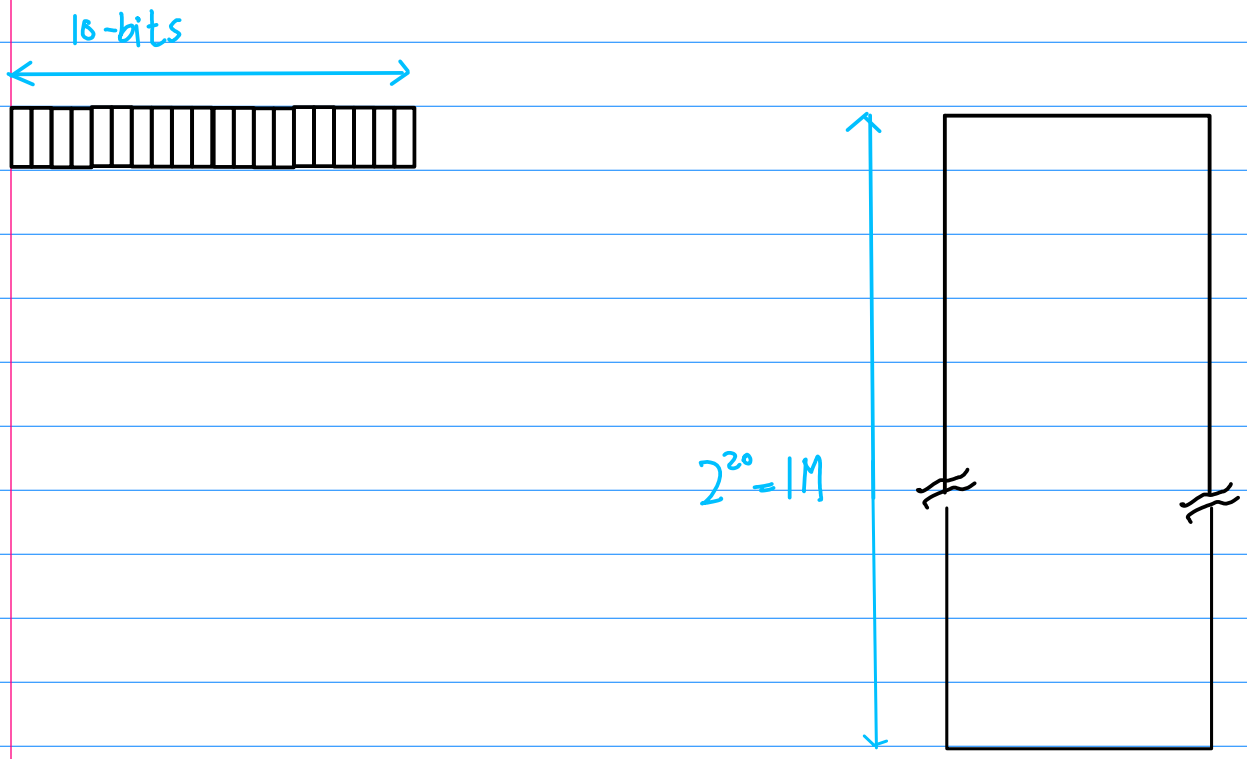
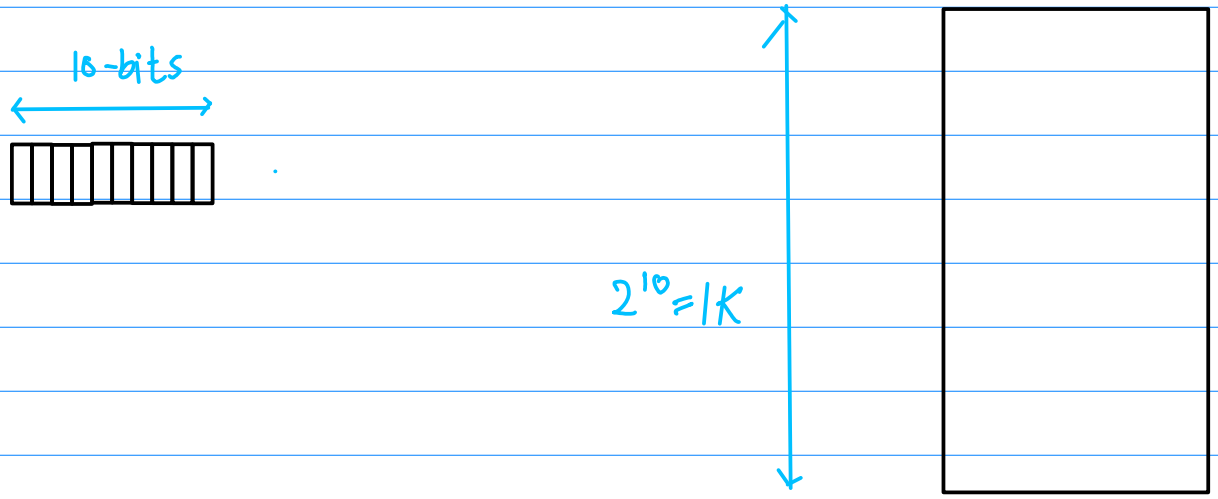
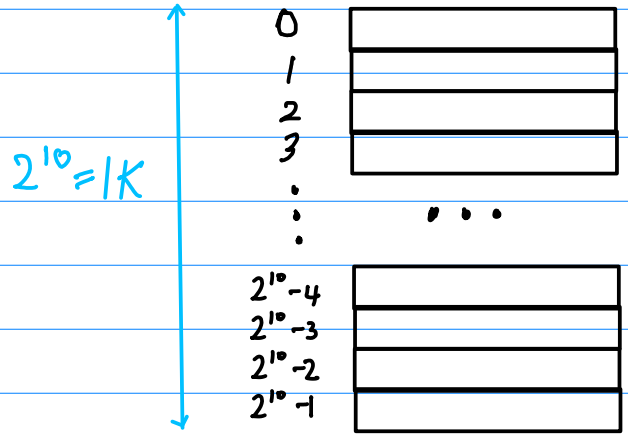
Based on

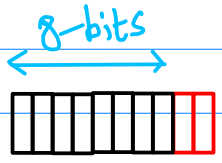
M.J. Flynn & W. Luk
Computer System Design
System-on-Chip


10-bits
$2^{10}=1K$

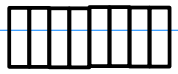

10-bits
$2^{20}=1M$

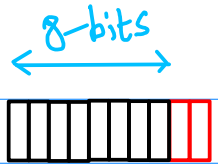




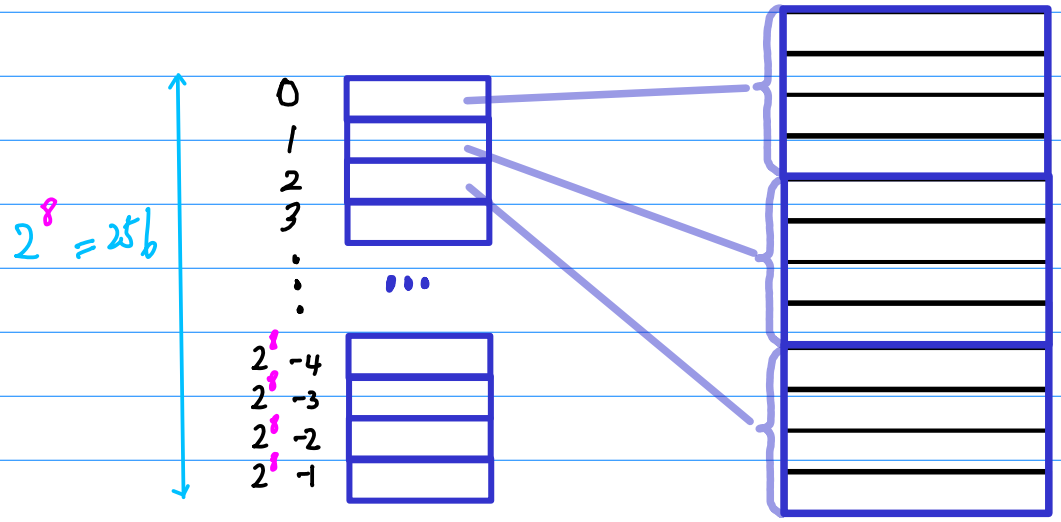


$$2^{10} = 2^{8+2} = 2^8 \cdot 2^2$$





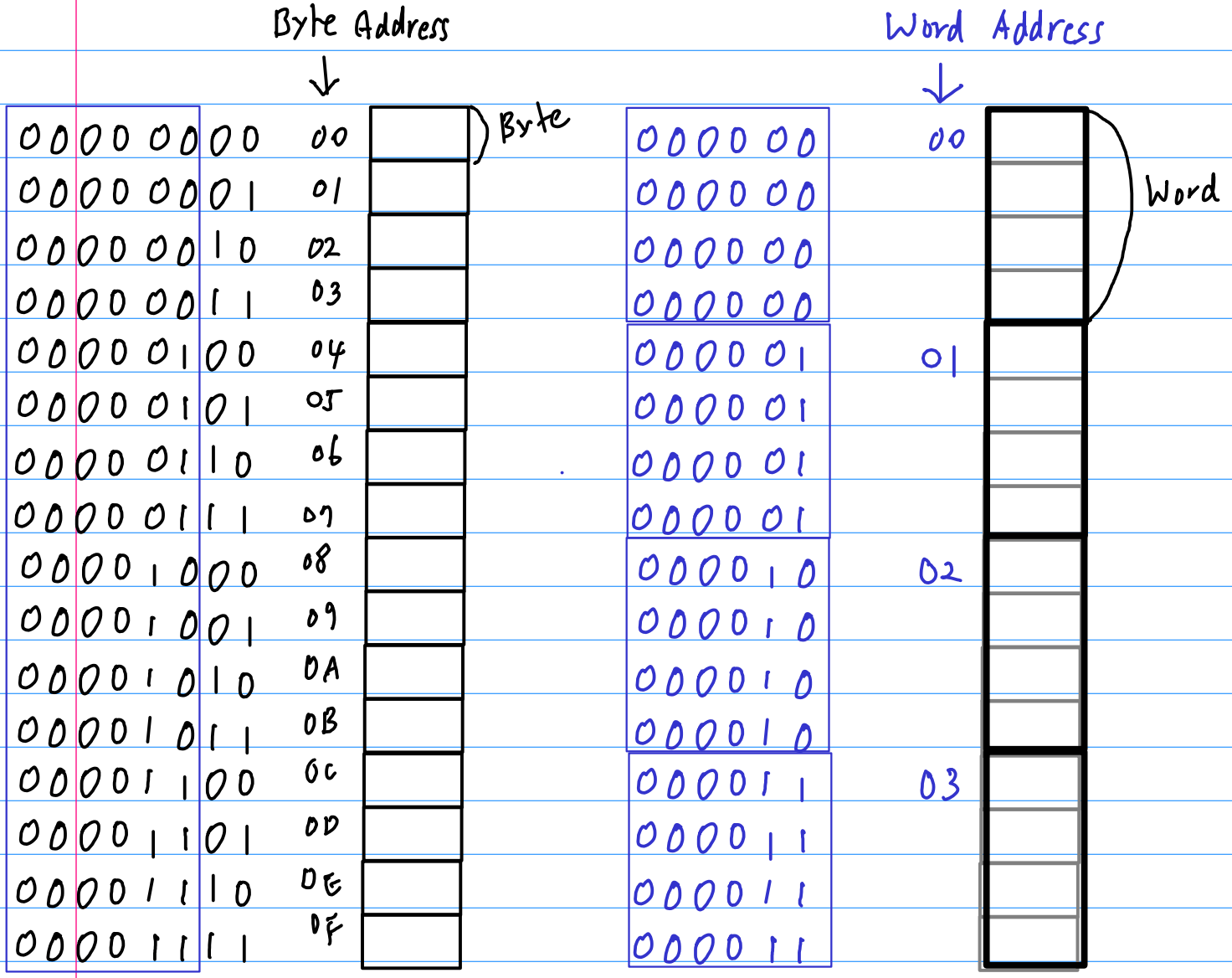
$2^{10} = 2^{8+2} = 2^8 \cdot 2^2$

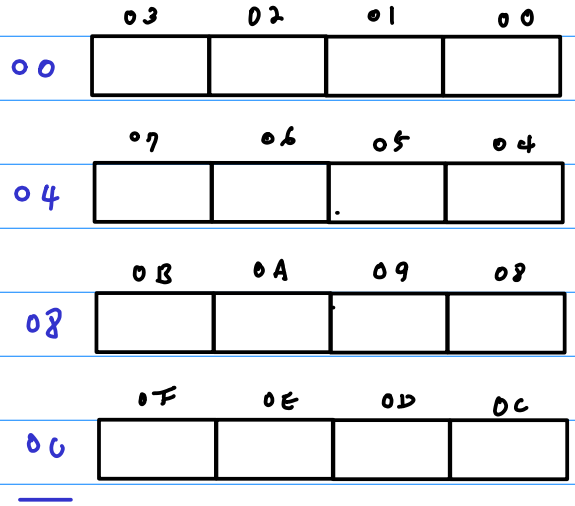


the total # of ▭'s : $2^8 = 256$

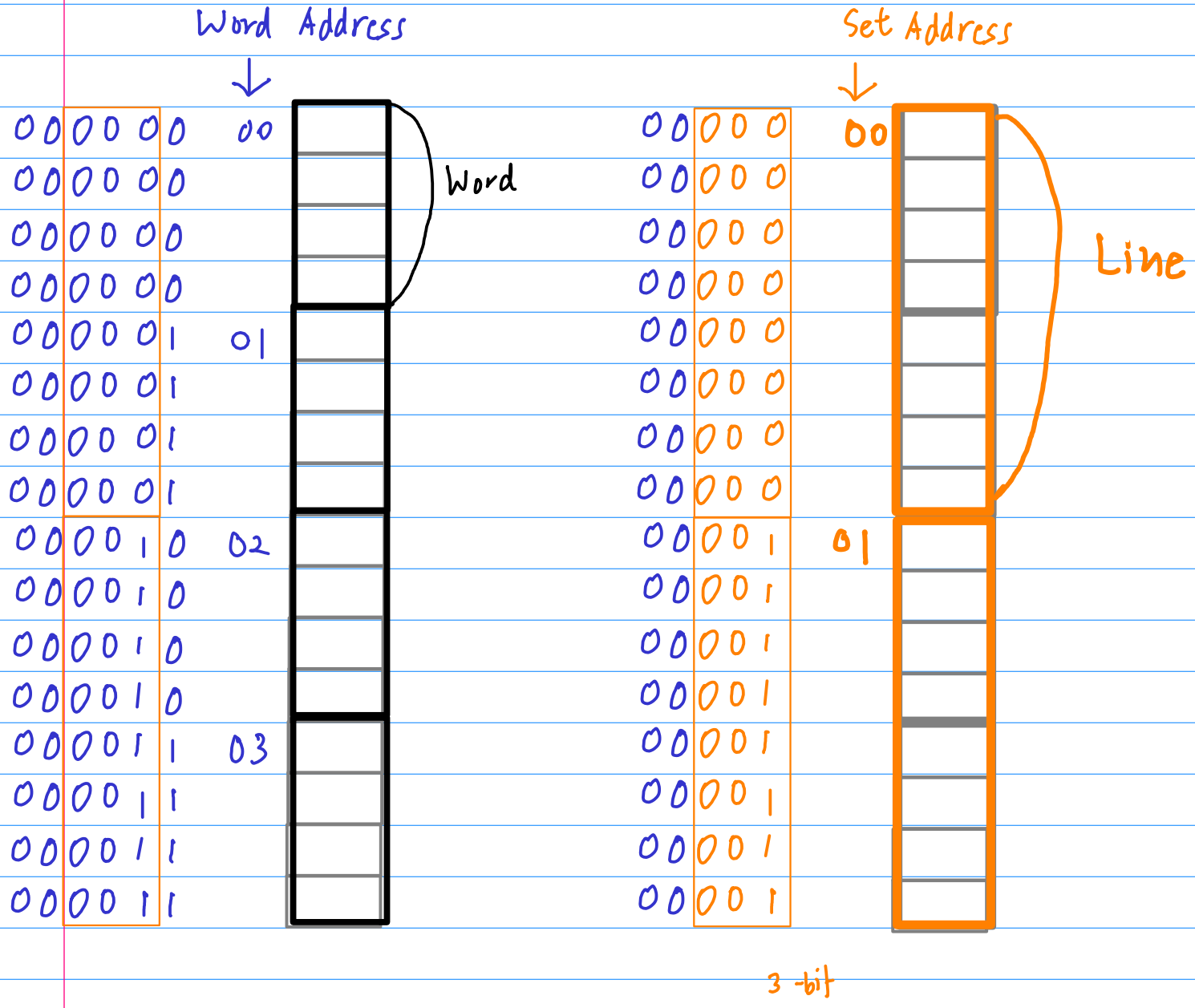
each ▭ has 2^2 ▭'s

Byte Address & Word Address





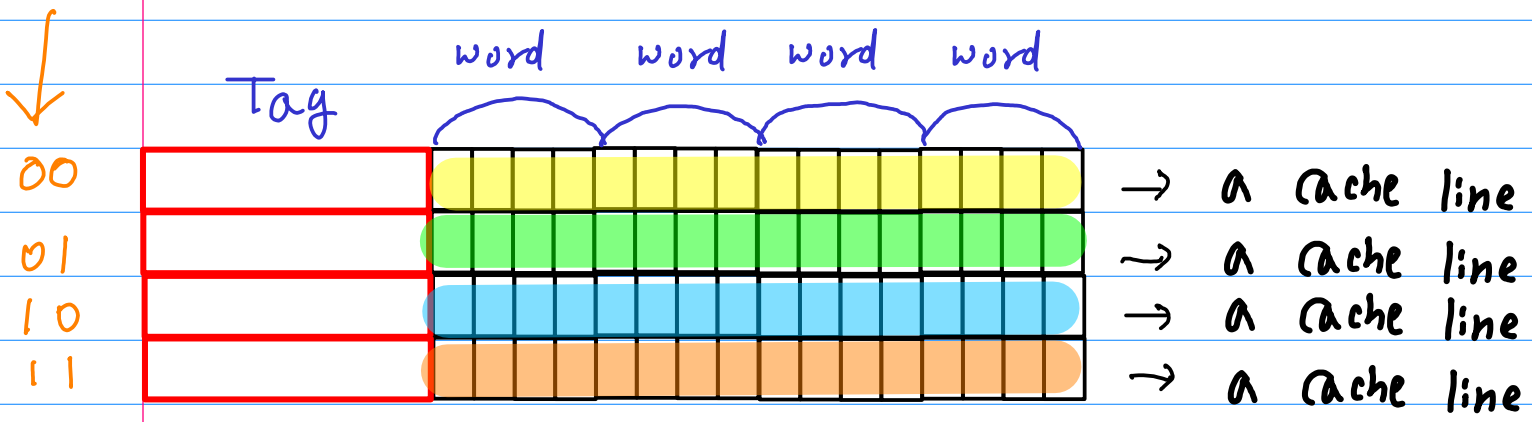
Word Address & Set Address



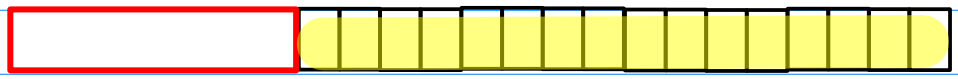
assume: 1 Line = 2 words (block)

2^3 sets

cache row (set address)



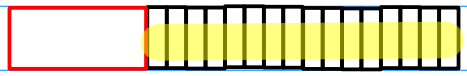
cache line (block)



$\left\{ \begin{array}{l} = \text{cache row} \quad \text{(only for the direct mapping)} \\ \quad \text{only one line per row} \\ \neq \text{cache row} \quad \text{(set-associative, fully-associative)} \\ \quad \text{more than one line per row} \end{array} \right.$

assume: 1 Line = 4 words (block)

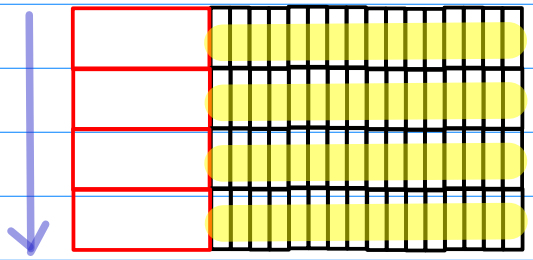
Cache line (block) →



- Tag
- a block of words

Cache row (set)

row 0 00
row 1 01
row 2 10

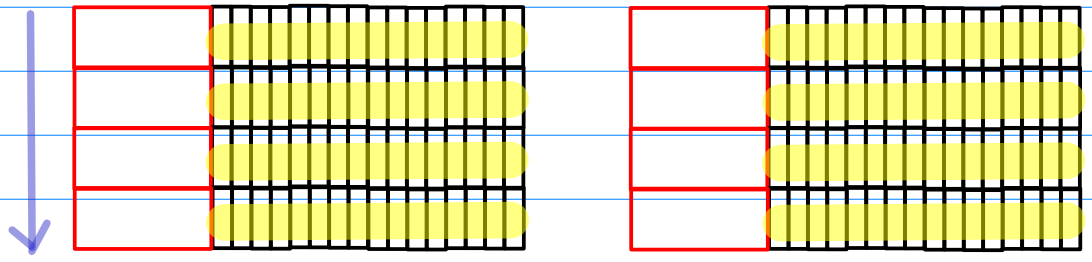


Way

Way 0

Way 1

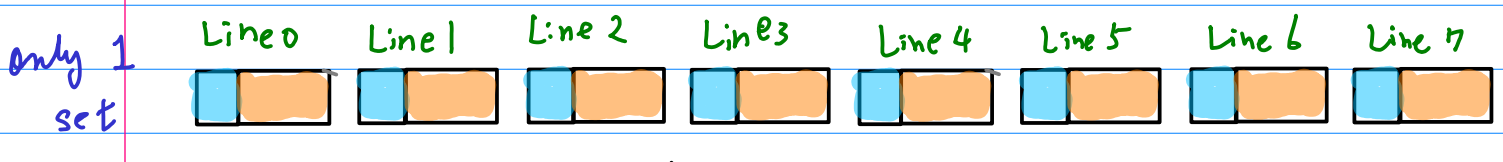
row 0 00
row 1 01
row 2 10



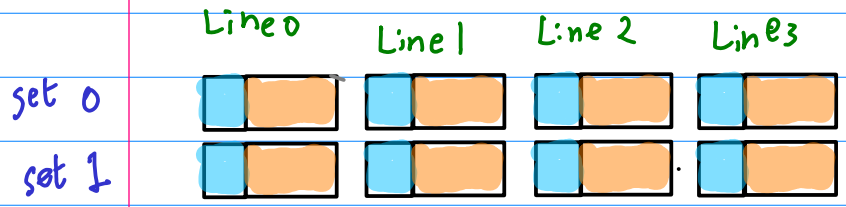
Line offset

which line in a set.

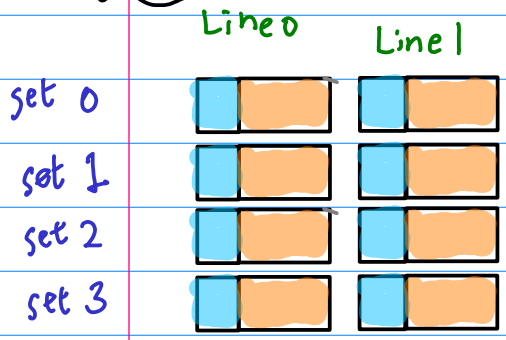
FA



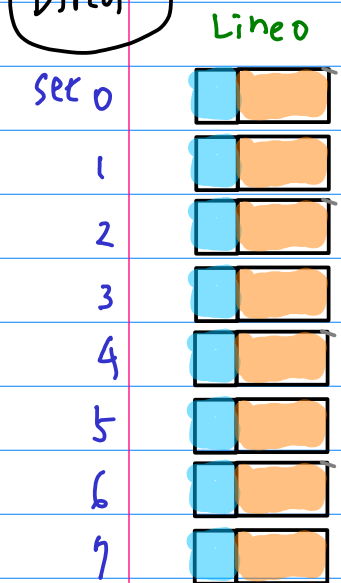
4-Way SA



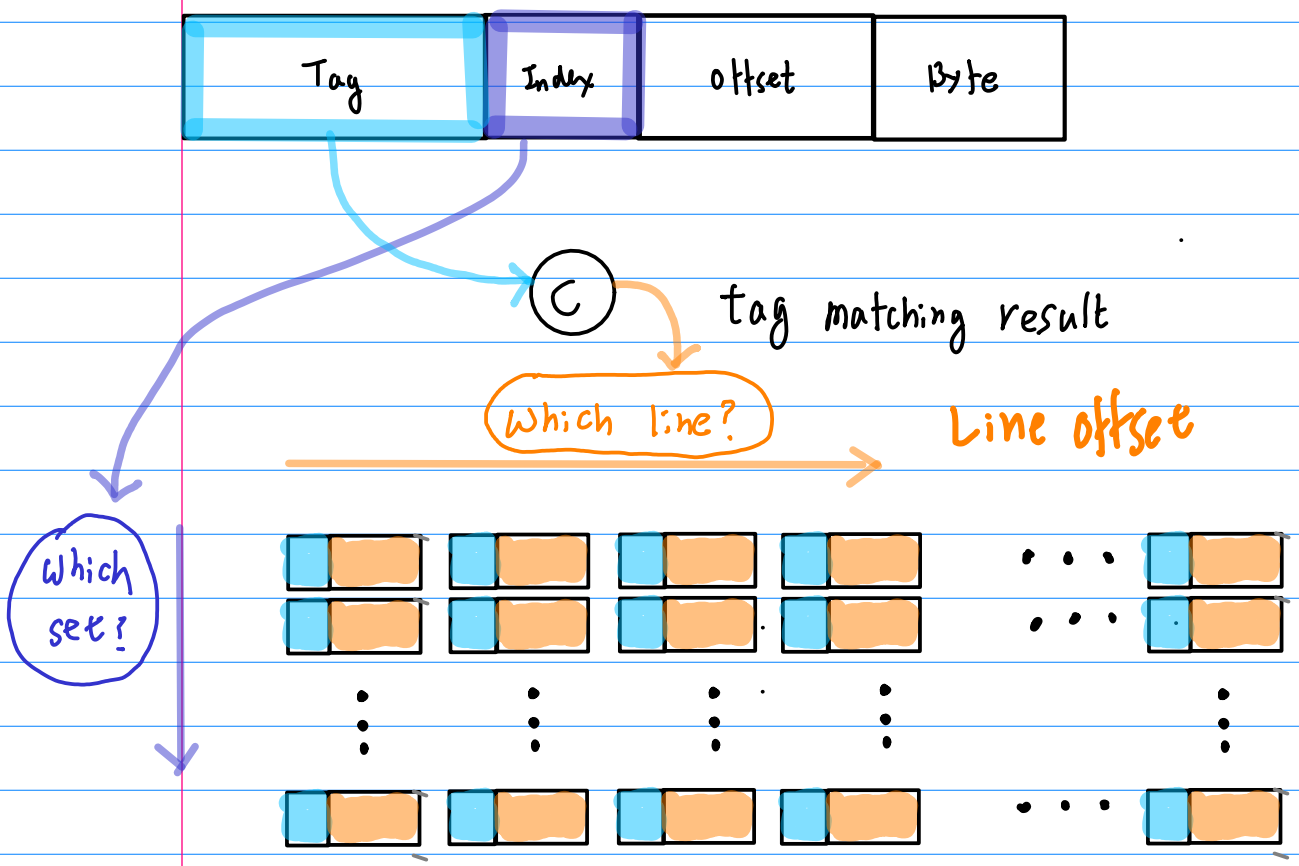
2-Way SA



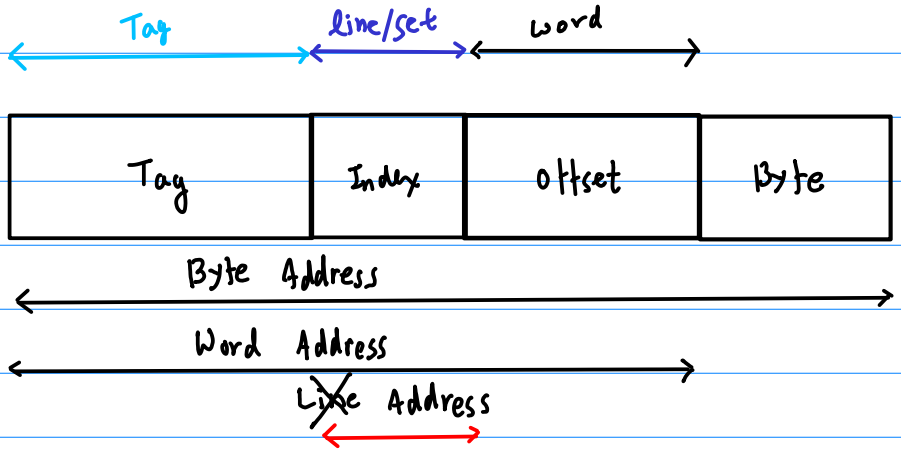
Direct



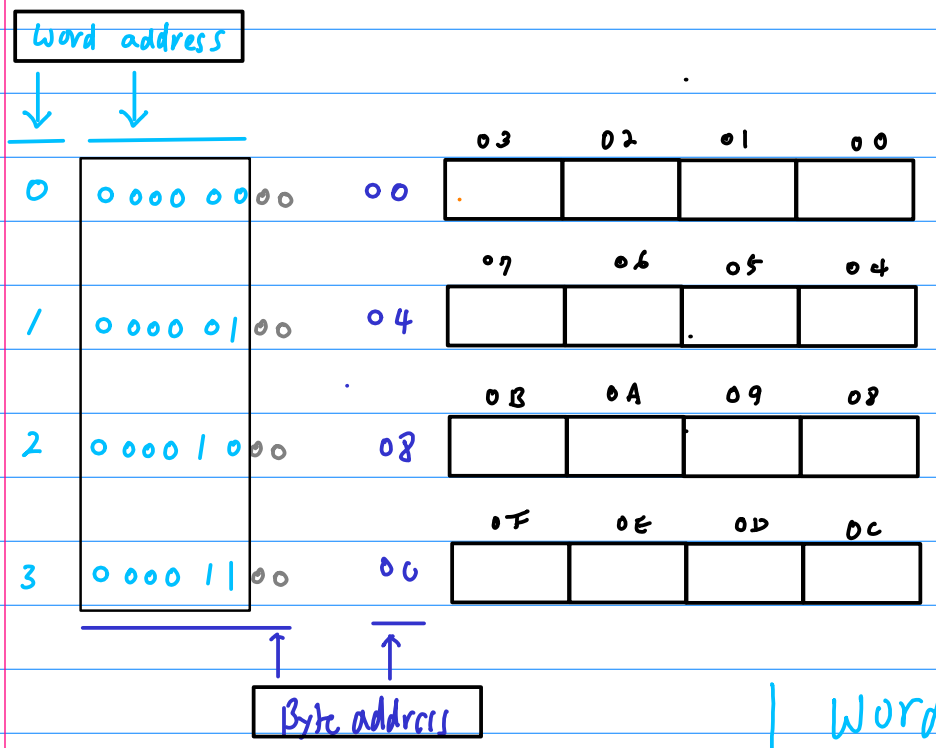
Line Offset which line in a set.



set address



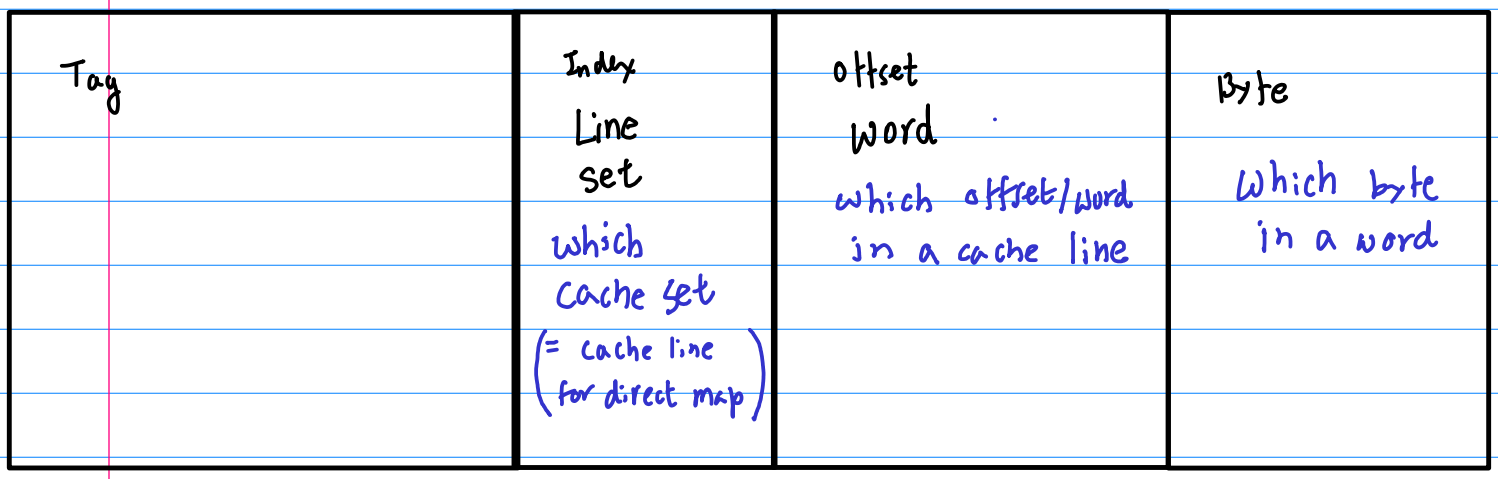
Set Address which set (row)

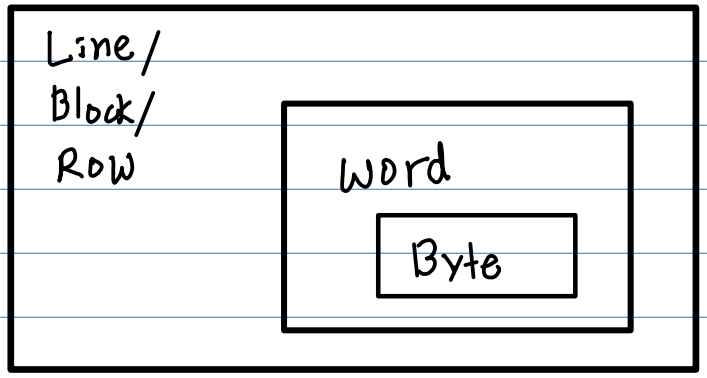


cf) Big Endian

Little Endian

| Word = 4 Bytes

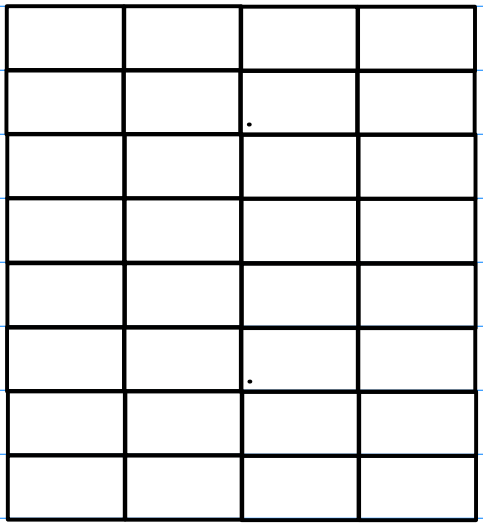

Tag
Index
Line
set
which
cache set
(= cache line
for direct map)
offset
word
which offset/word
in a cache line
Byte
which byte
in a word


Line/
Block/
Row
word
Byte

1 word = 4 Bytes

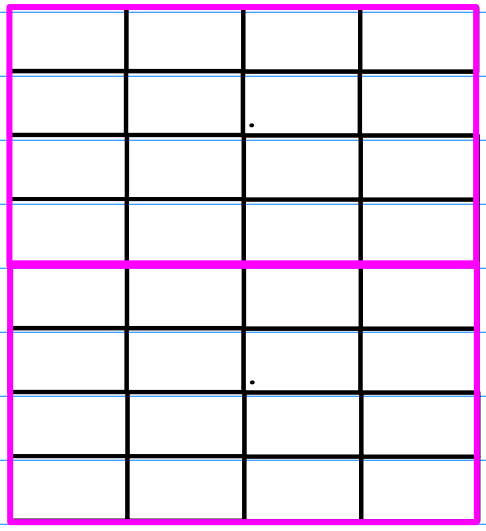
word address

0000 0000	00	
0000 0100	01	
0000 1000	02	
0000 1100	03	
0001 0000	04	
0001 0100	05	
0001 1000	06	
0001 1100	07	

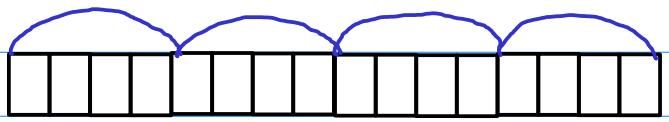


Set address

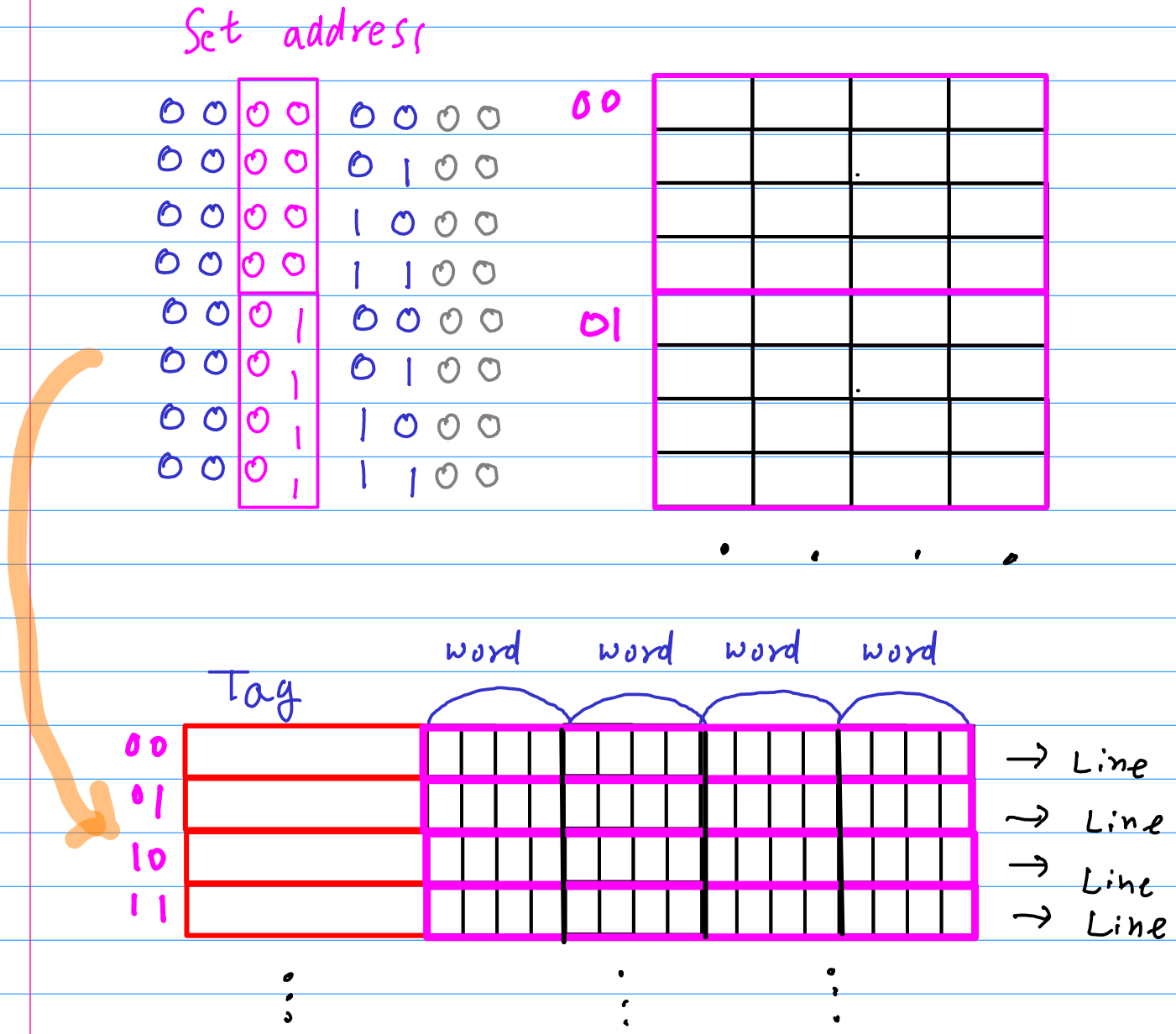
00 0000	00	
00 0100		
00 1000		
00 1100		
01 0000	01	
01 0100		
01 1000		
01 1100		



Line



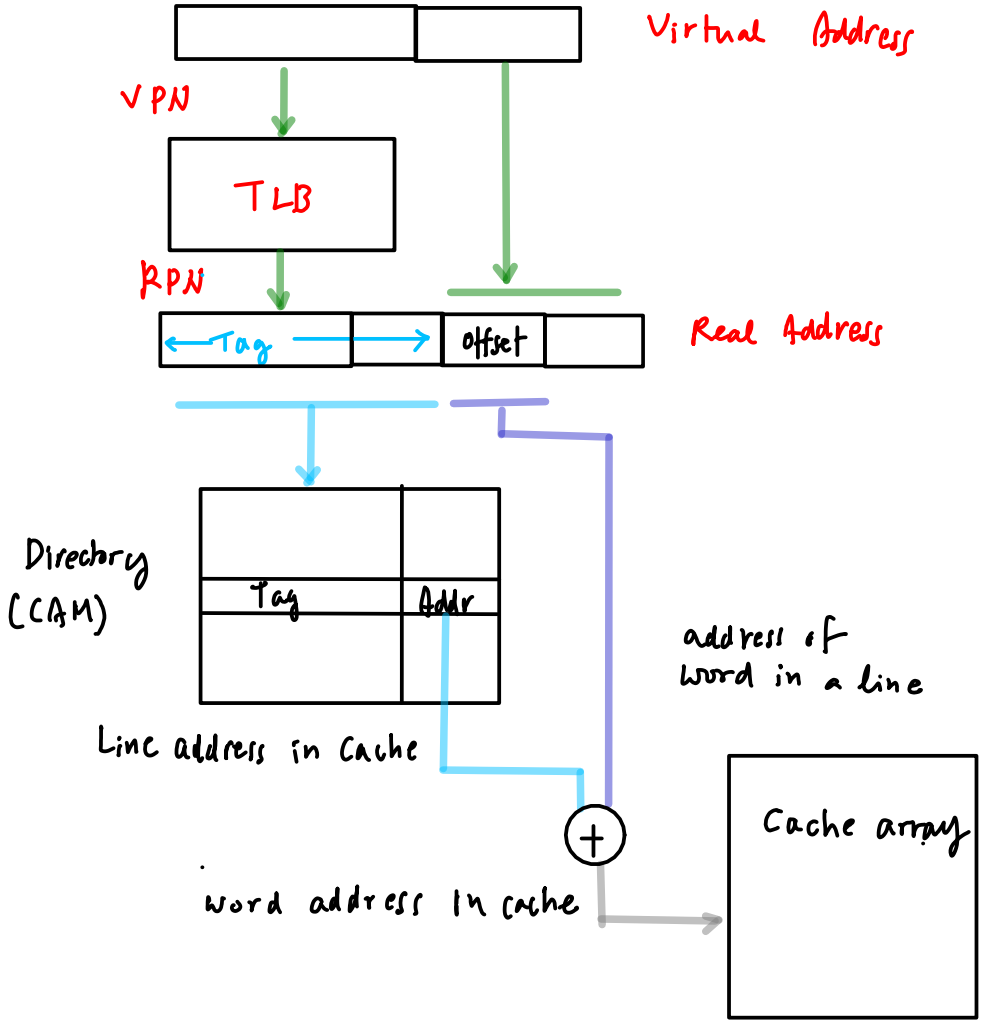
Assume 1 line = 4 words

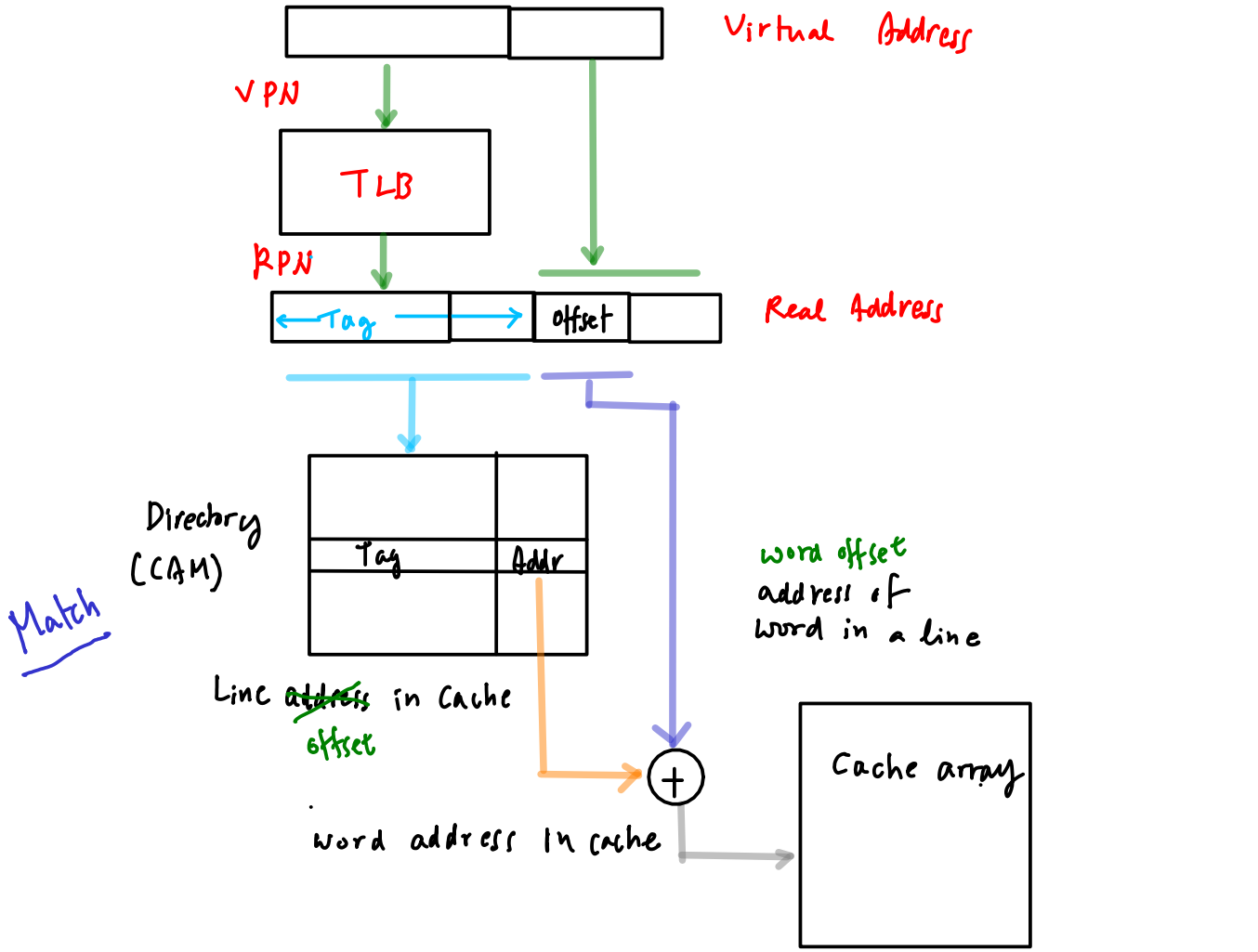


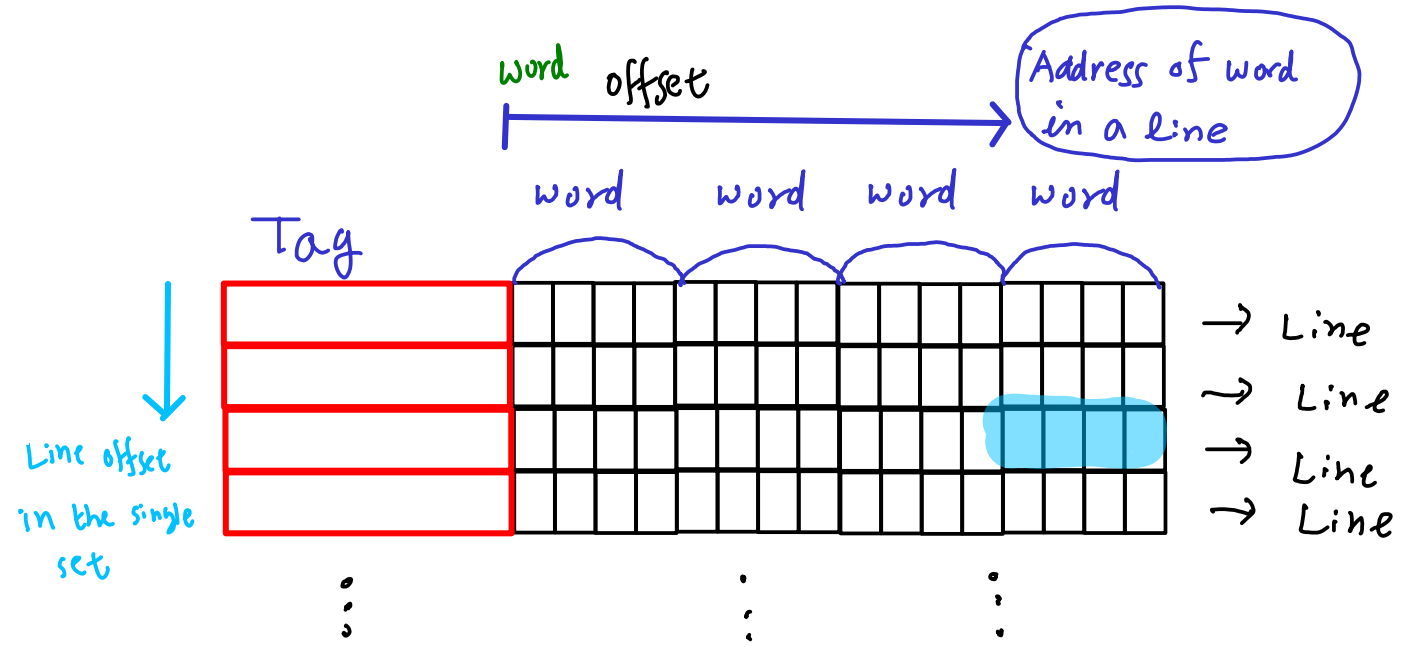
direct mapping assumed

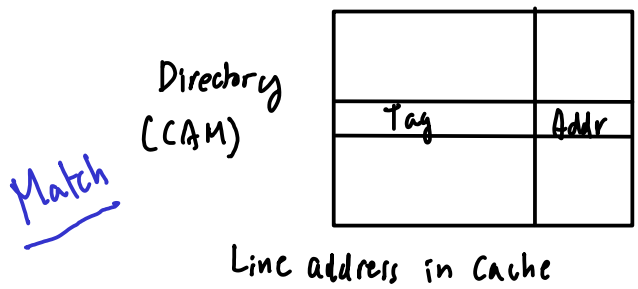
(line = set)

Fully Associative

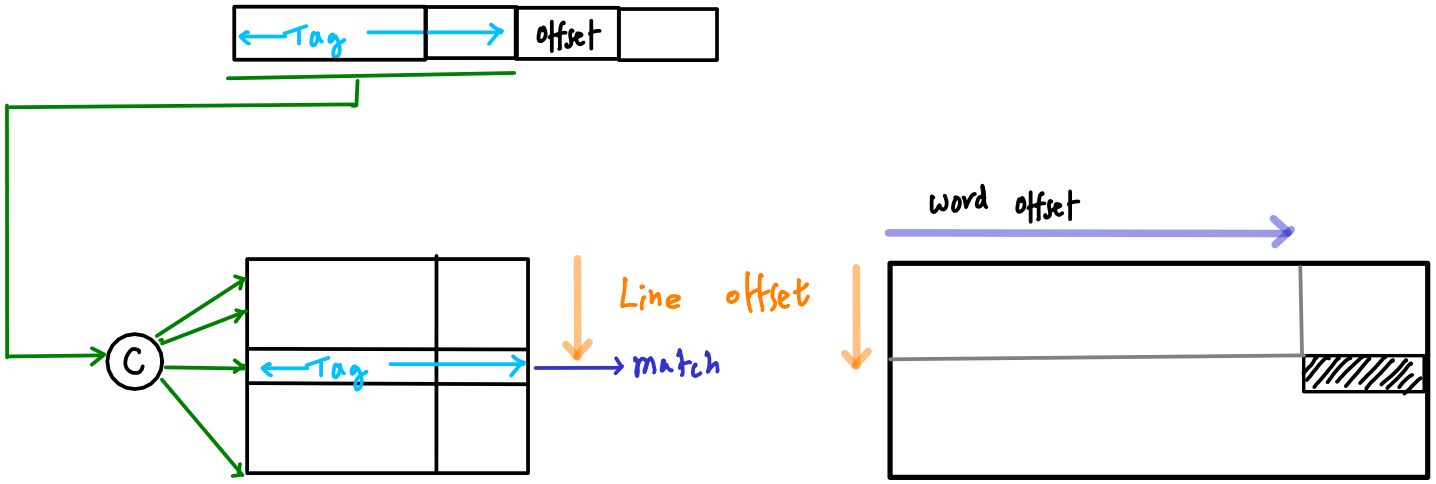



Virtual Address
VPN
TLB
RPN
Tag
offset
Real Address
Directory
(CAM)
Tag
Addr
Match
word offset
address of
word in a line
Line address in Cache
offset
word address in cache
Cache array


word offset
Address of word
in a line
word
word
word
word
Tag
Line offset
in the single
set
Line
Line
Line
Line

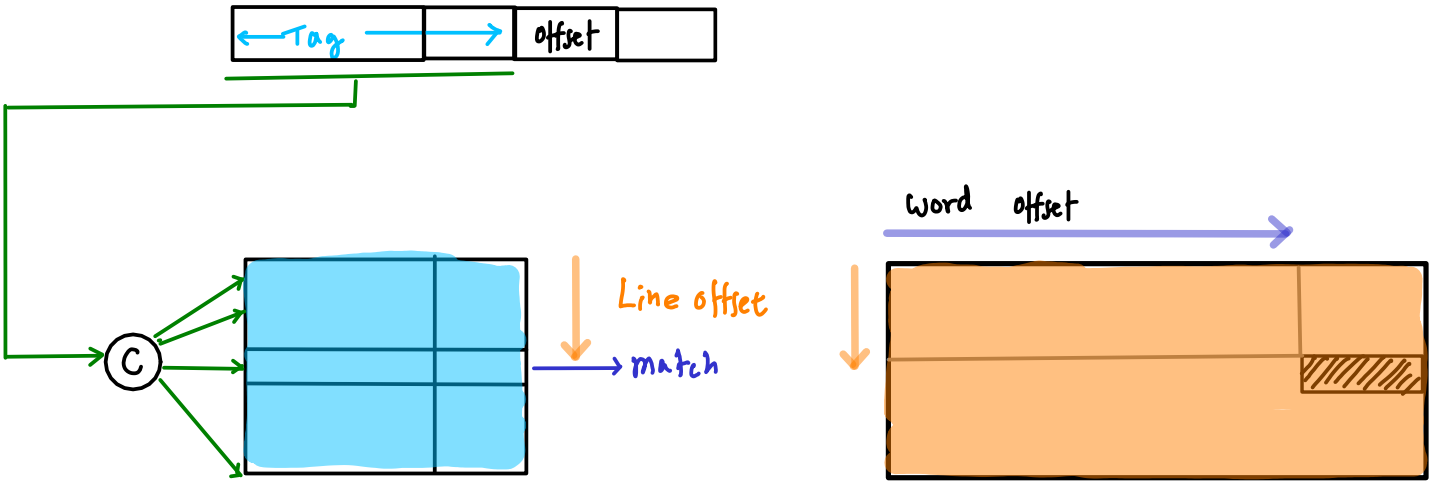


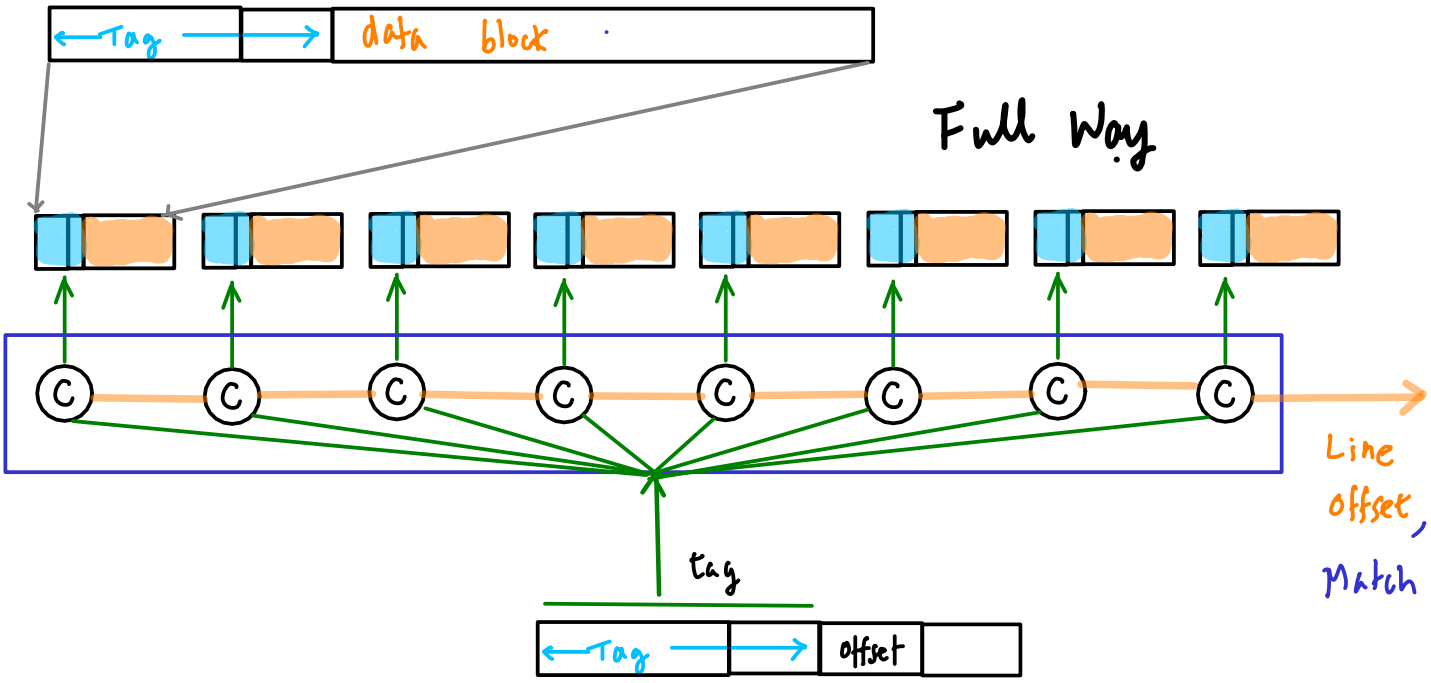
② No index field for fully associative mapping

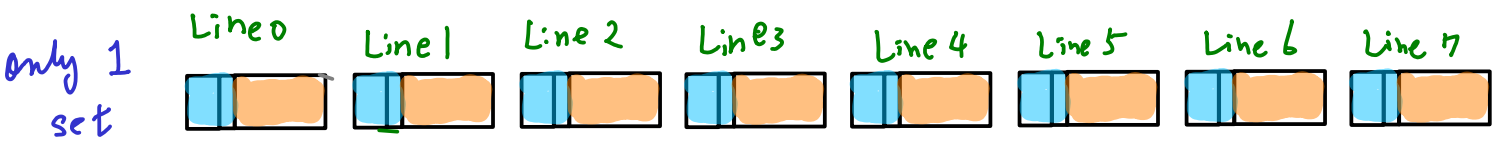


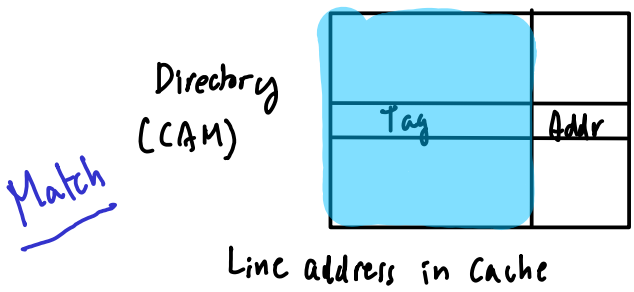
conventional CAM

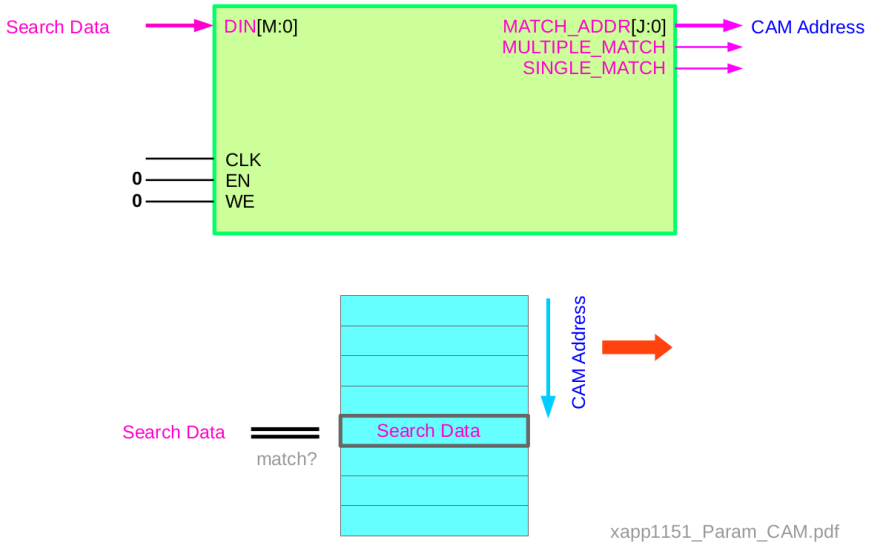
content addressable memory

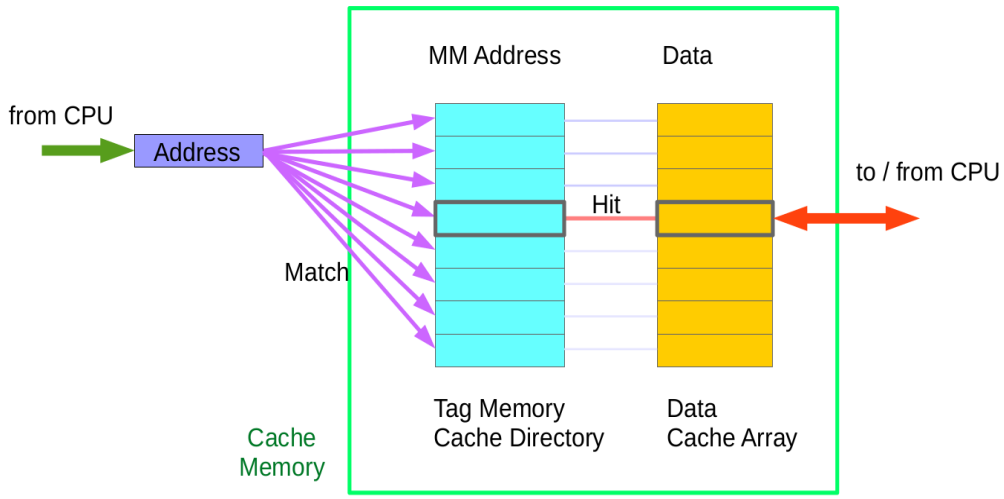

Tag
offset
C
Line offset
match
word offset


Tag
data block
Full Way
C
Line offset, Match
tag
Tag
offset

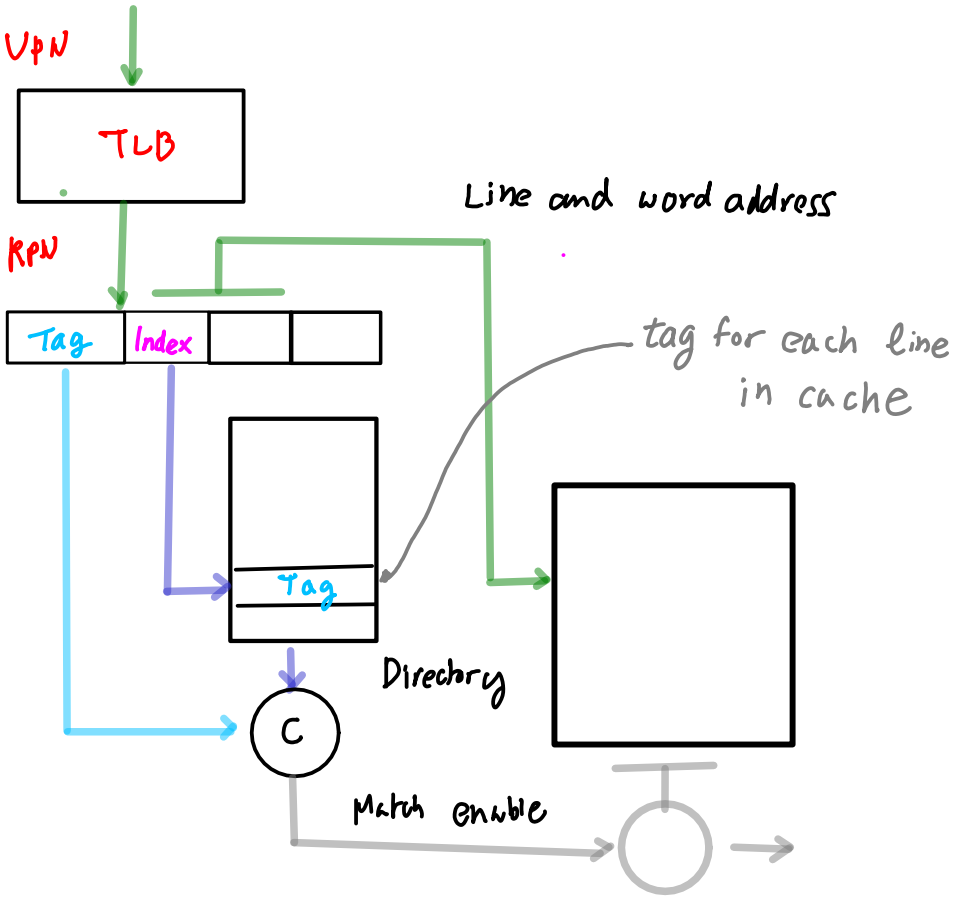

only 1 set
Line 0
Line 1
Line 2
Line 3
Line 4
Line 5
Line 6
Line 7

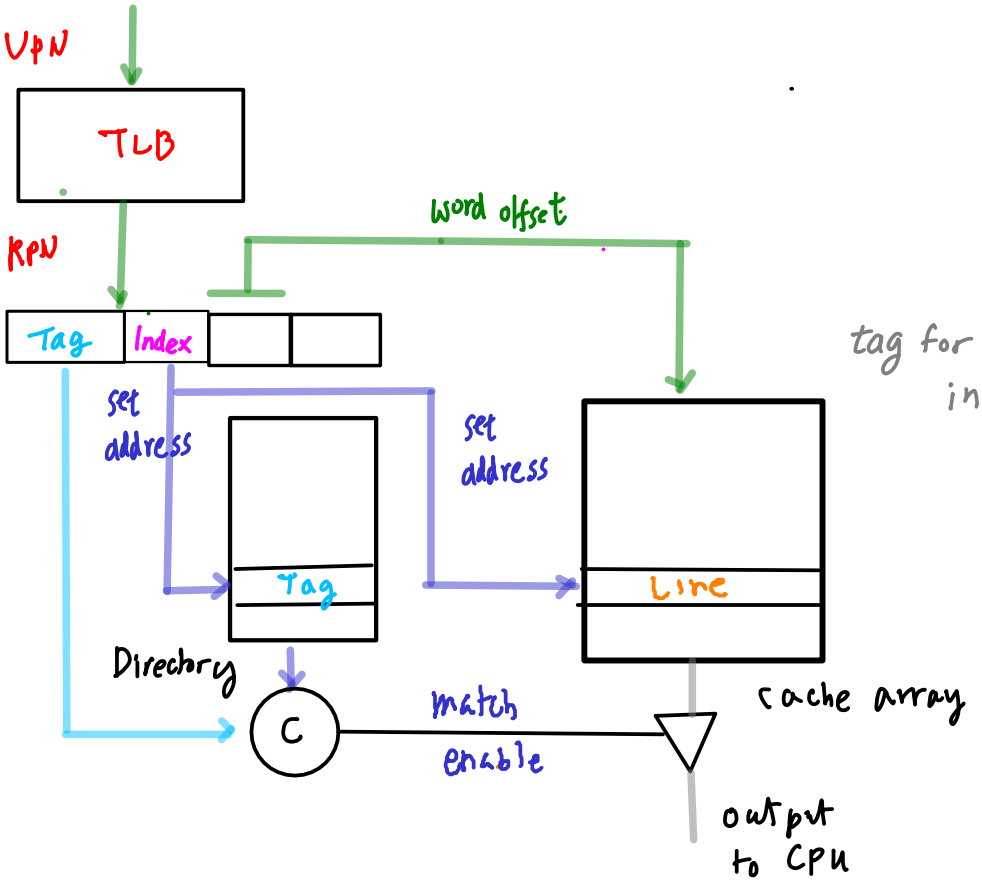

Directory
(CAM)
Tag
Addr
Match
Line address in Cache

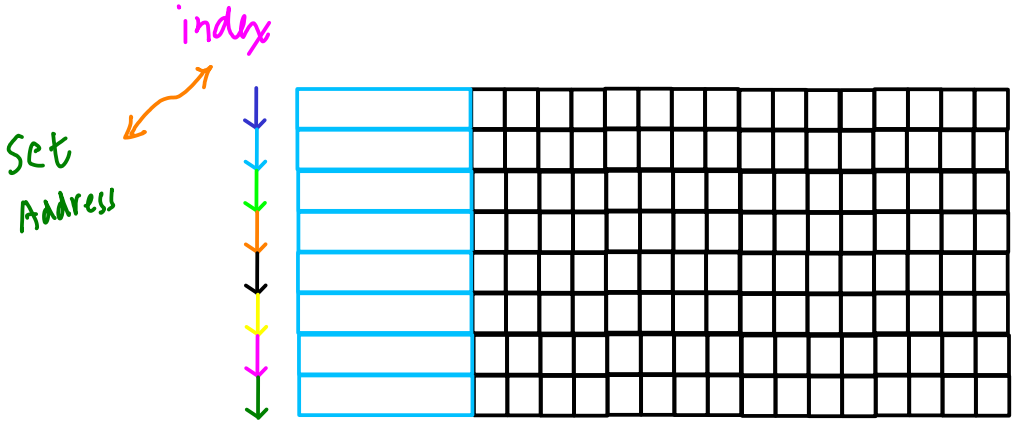

Search Data
DIN[M:0]
MATCH_ADDR[J:0]
MULTIPLE_MATCH
SINGLE_MATCH
CAM Address
CLK
0 EN
0 WE
CAM Address
Search Data
Search Data
match?
xapp1151_Param_CAM.pdf


MM Address
Data
from CPU
Address
to / from CPU
Hit
Match
Tag Memory
Cache Directory
Data
Cache Array
Cache
Memory

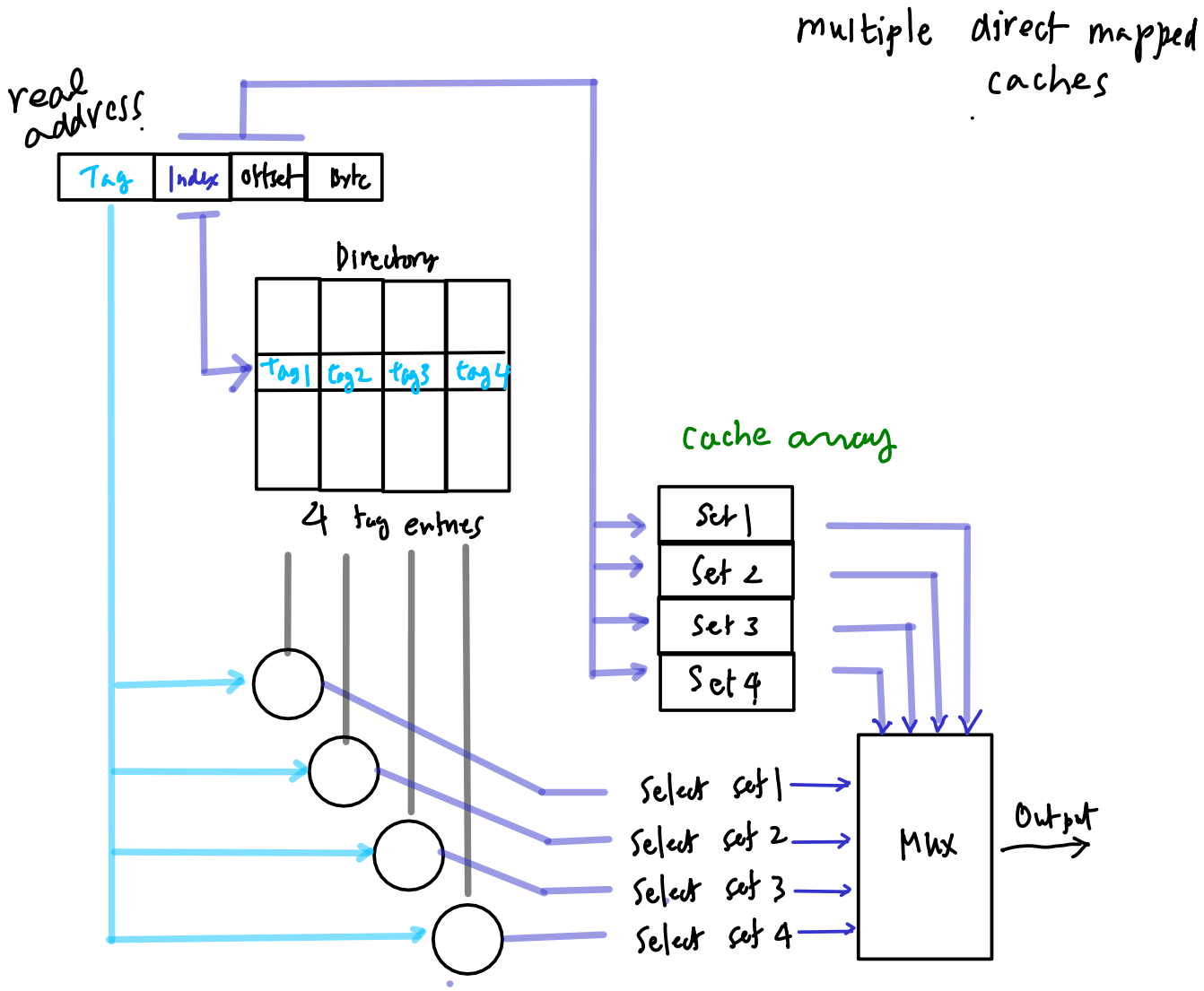
Direct Mapping

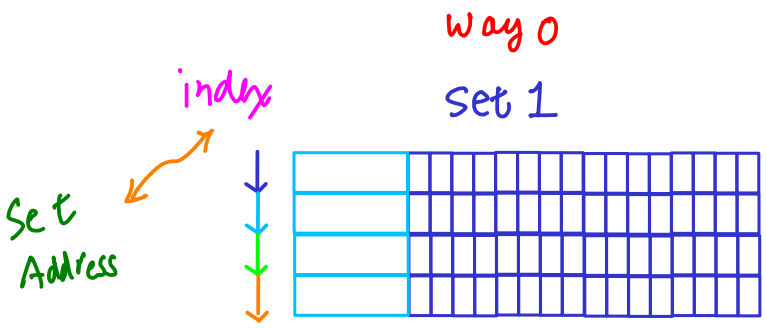


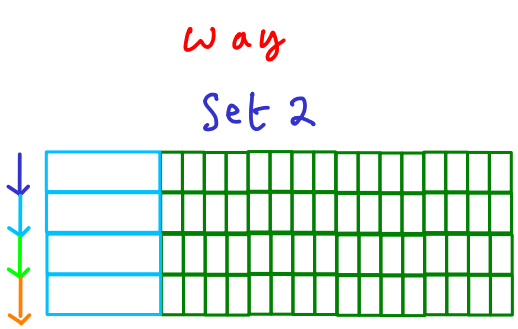

VPN
TLB
PPN
word offset
Tag
Index
set address
set address
tag for each line in cache
Tag
Line
Directory
C
match
enable
cache array
output to CPU

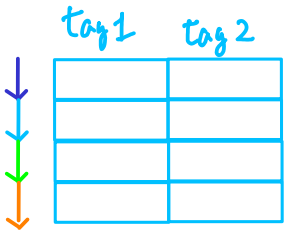

index
Set Address

Set Associative Mapping

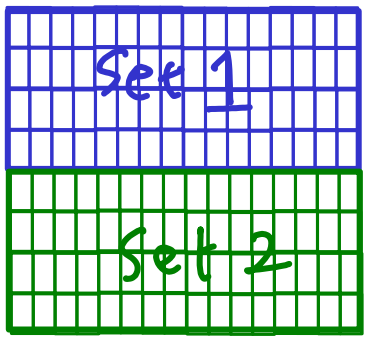






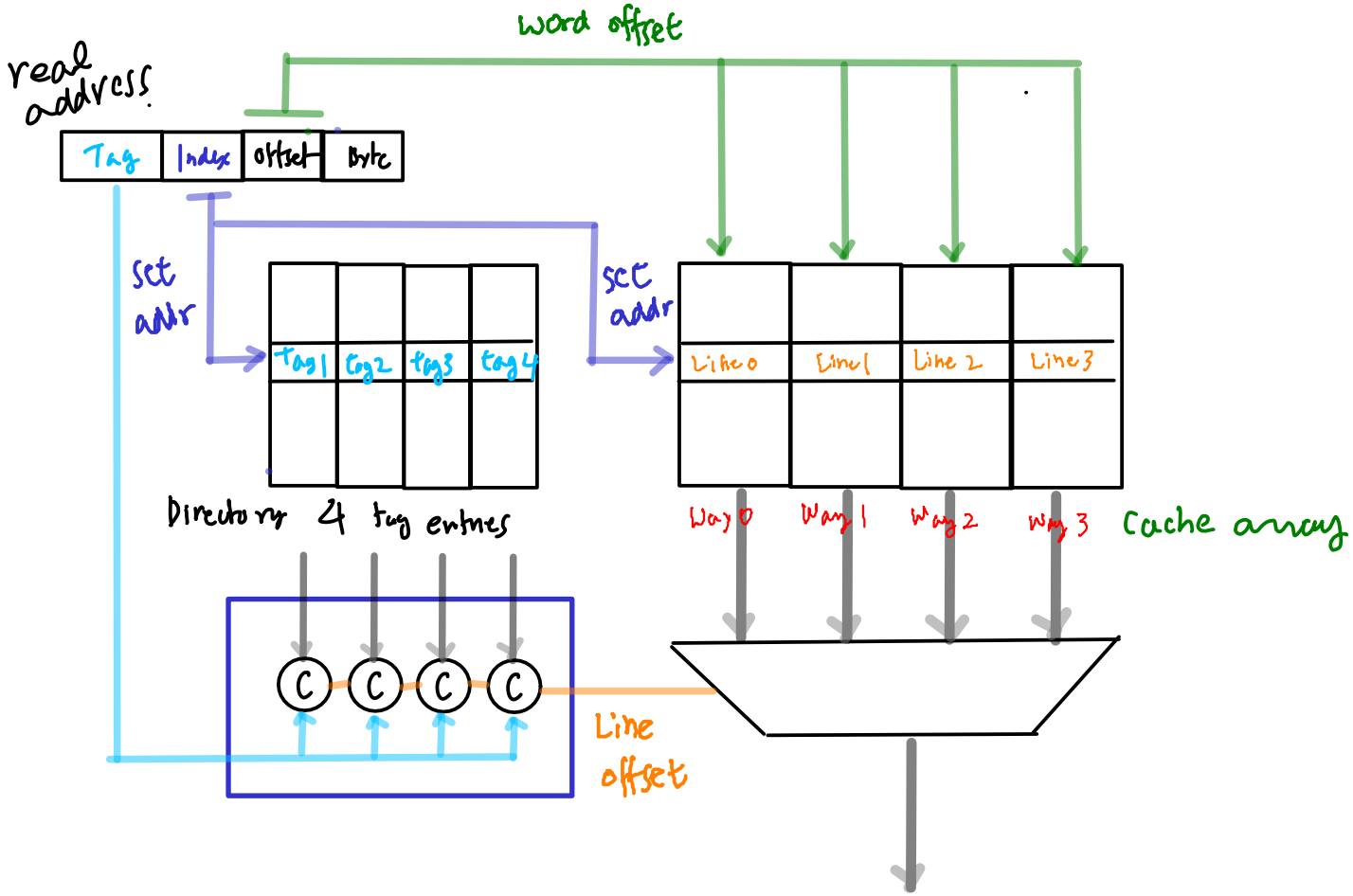


cache directory

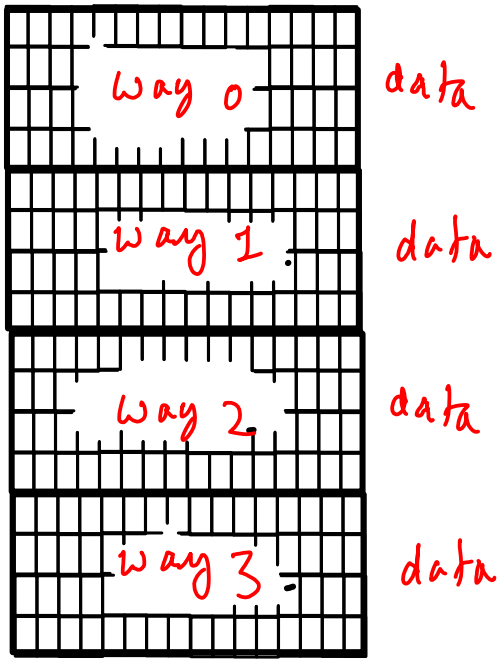


way 0 data

way 1 data


word offset
real address
Tag
Index
offset
Byte
set addr
set addr
tag1
tag2
tag3
tag4
Line 0
Line 1
Line 2
Line 3
Directory 4 tag entries
Way 0
Way 1
Way 2
Way 3
Cache array
C
C
C
C
Line offset

tag1
tag2
tag3
tag4


way 0
data
way 1
data
way 2
data
way 3
data