

Memory Arrays (3H)

Transistor Level Design

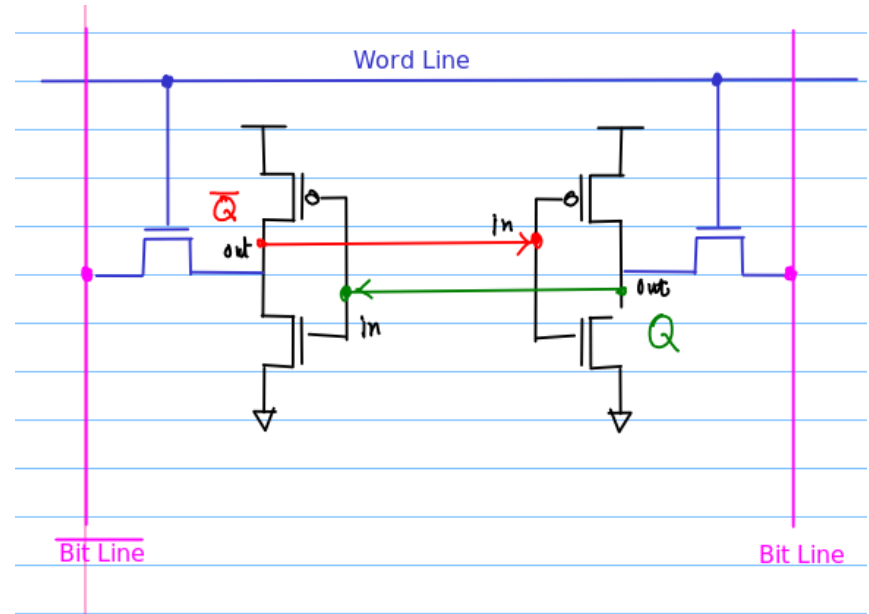
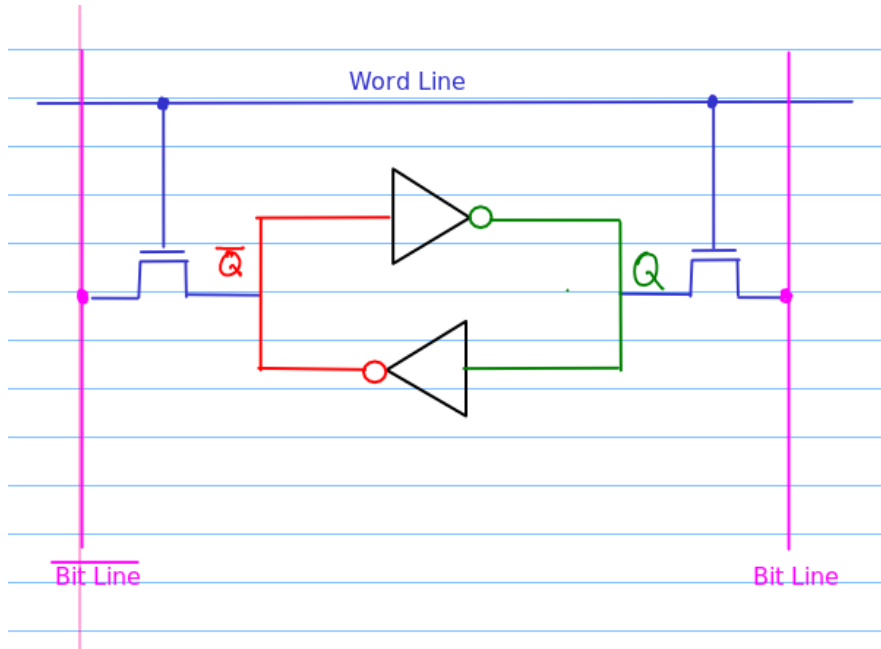
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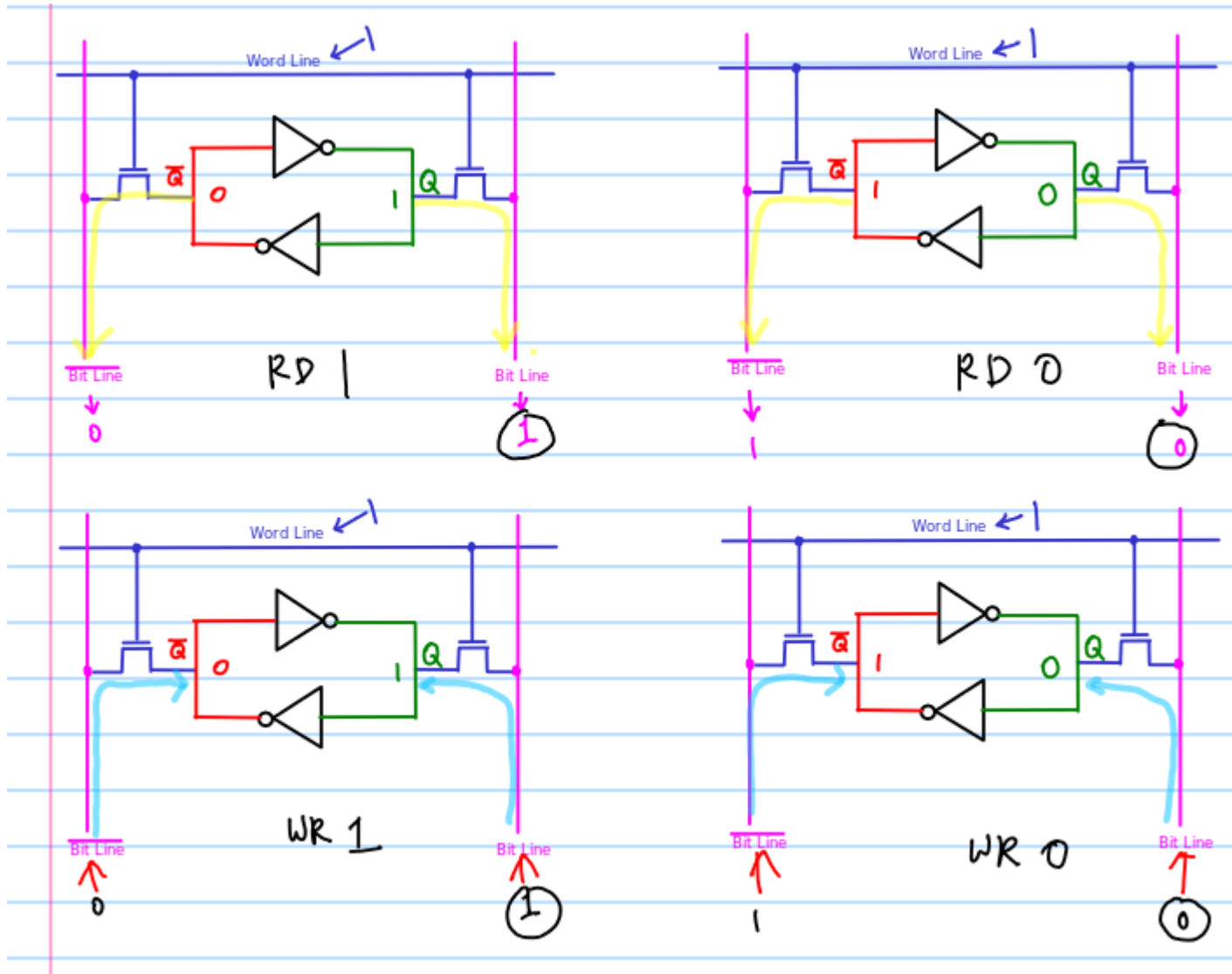
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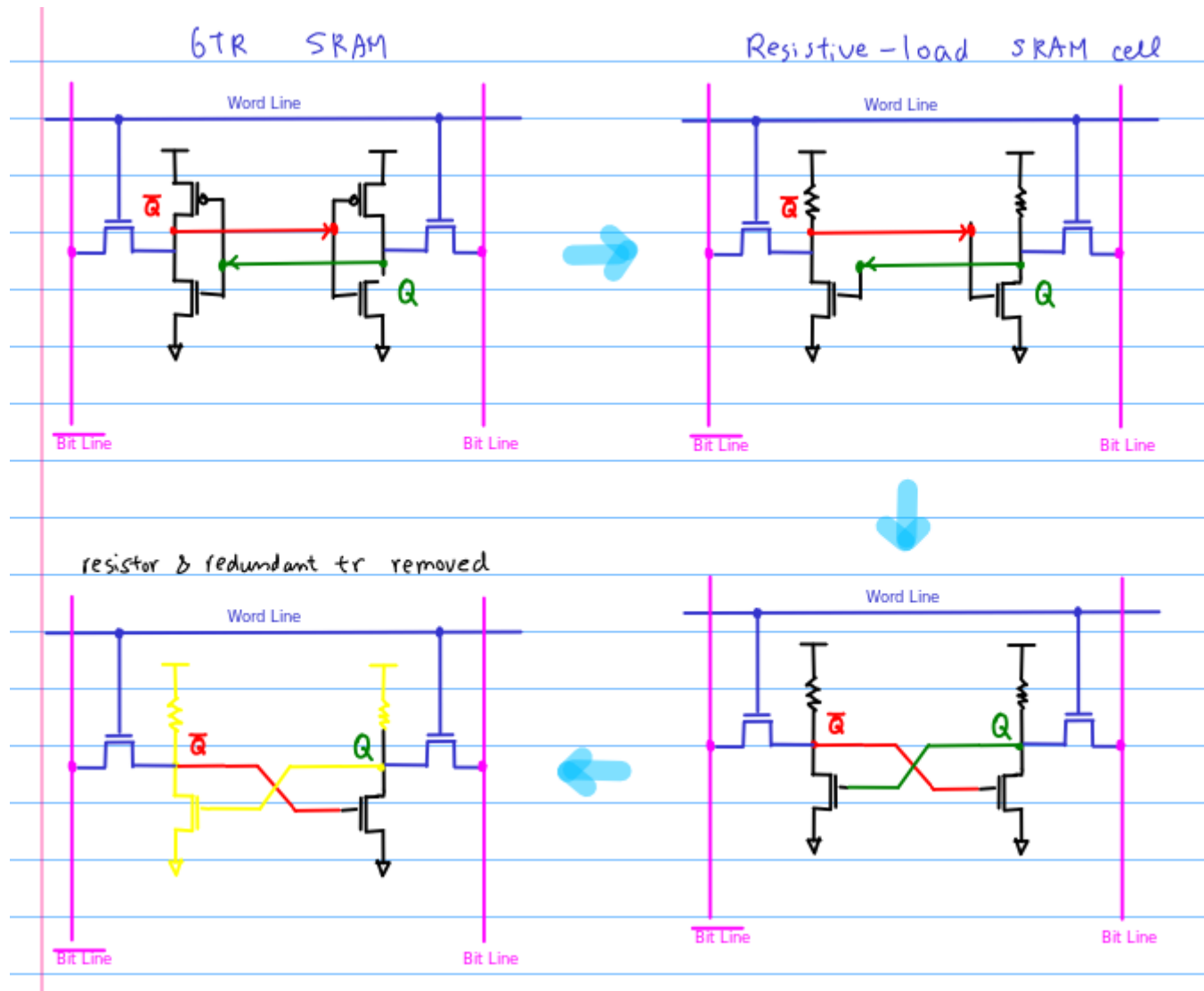
6-TR SRAM Cell



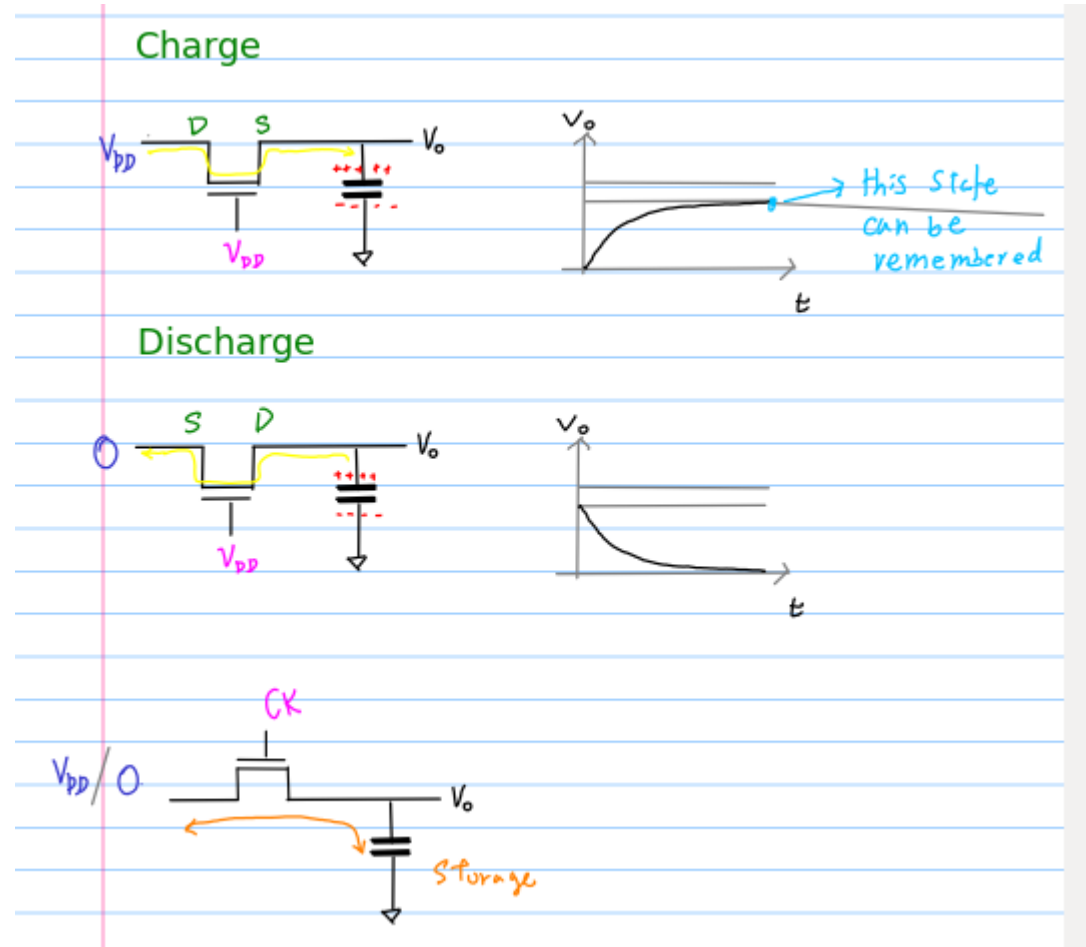
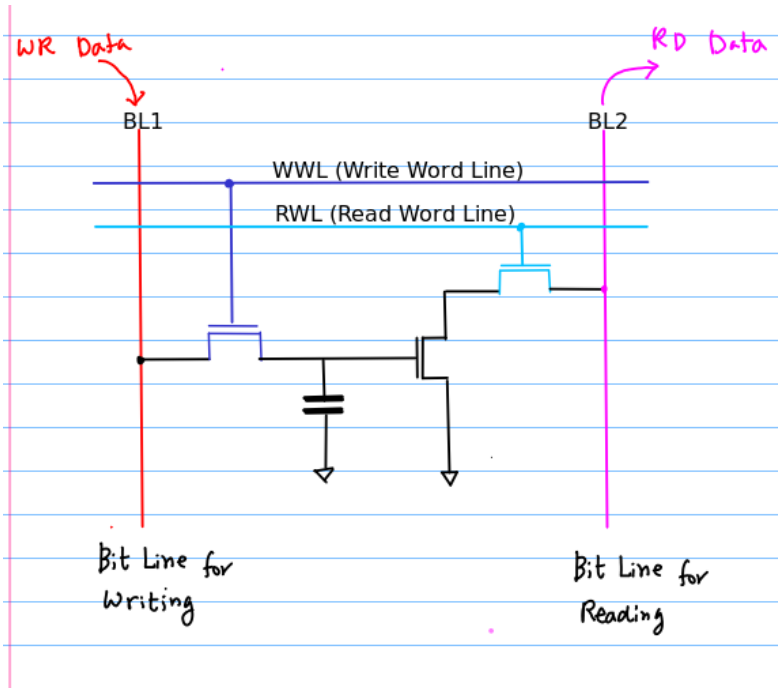
6-TR SRAM Cell Operation



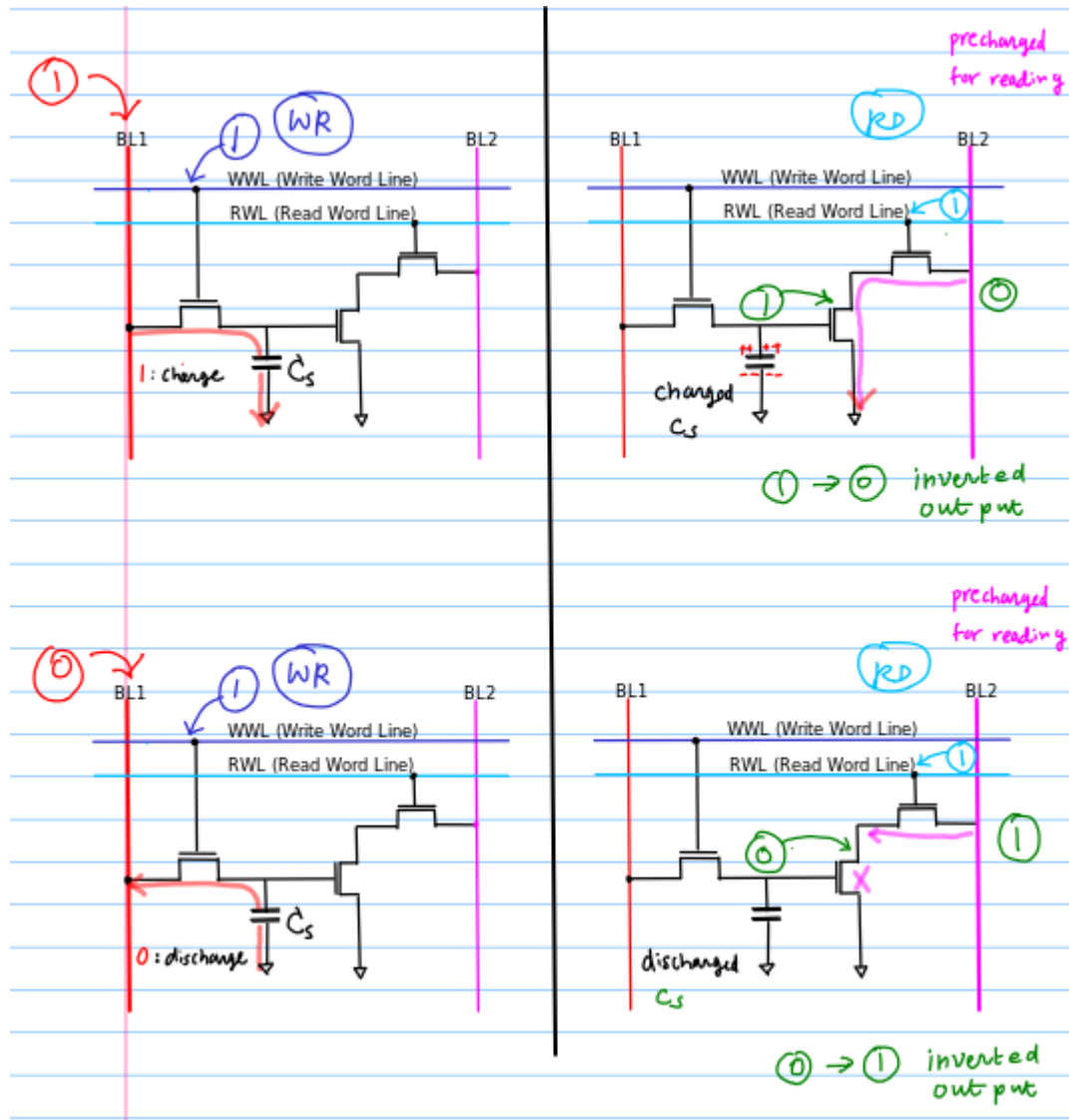
Reduce 6-TR SRAM Cell



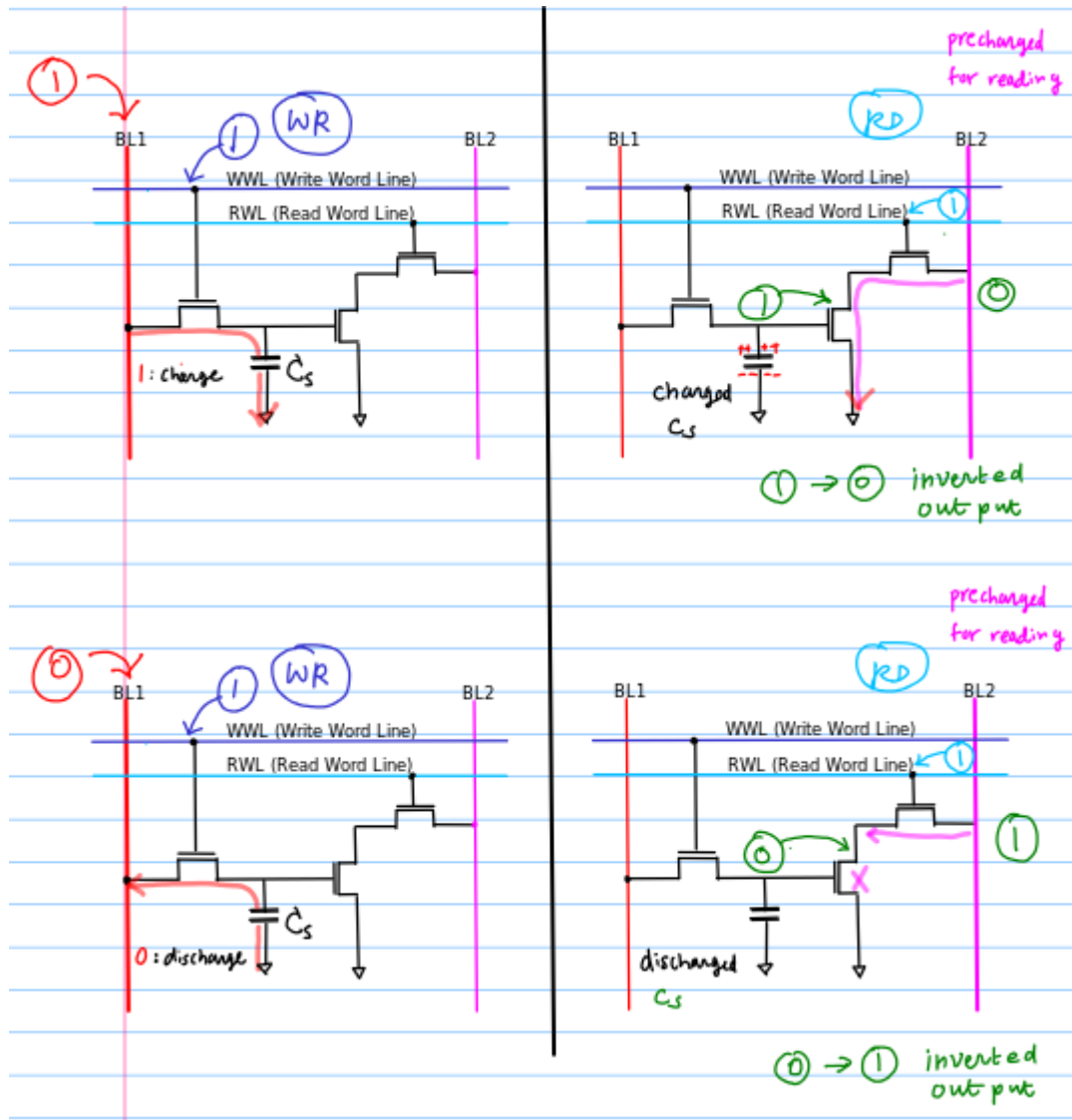
3-TR DRAM Cell



3-TR DRAM Cell Operation



3-TR DRAM Cell Operation



References

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