Memory Arrays (3H)

Transistor Level Design

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3/15/16

Please send corrections (or suggestions) to youngwlim@hotmail.com.

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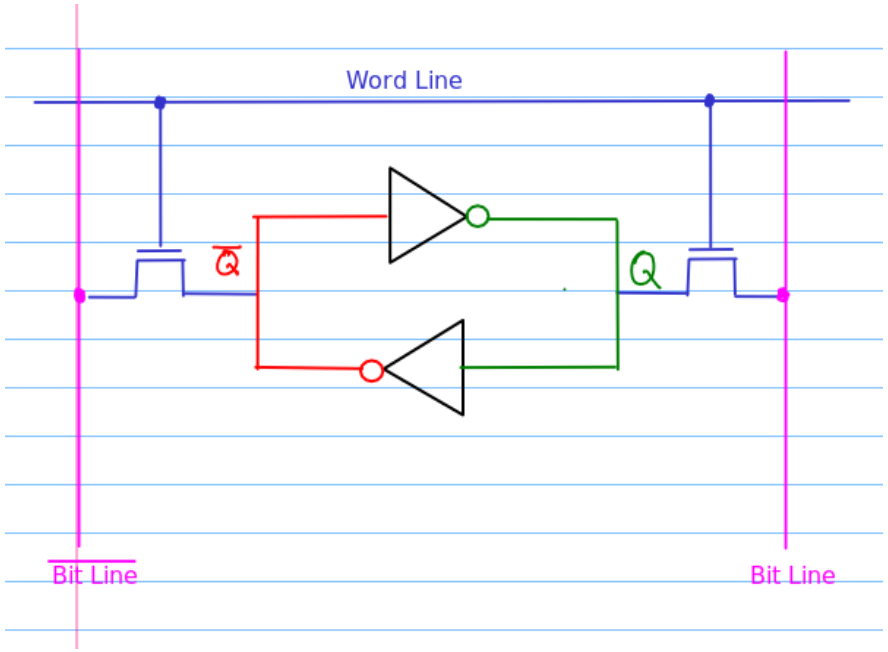
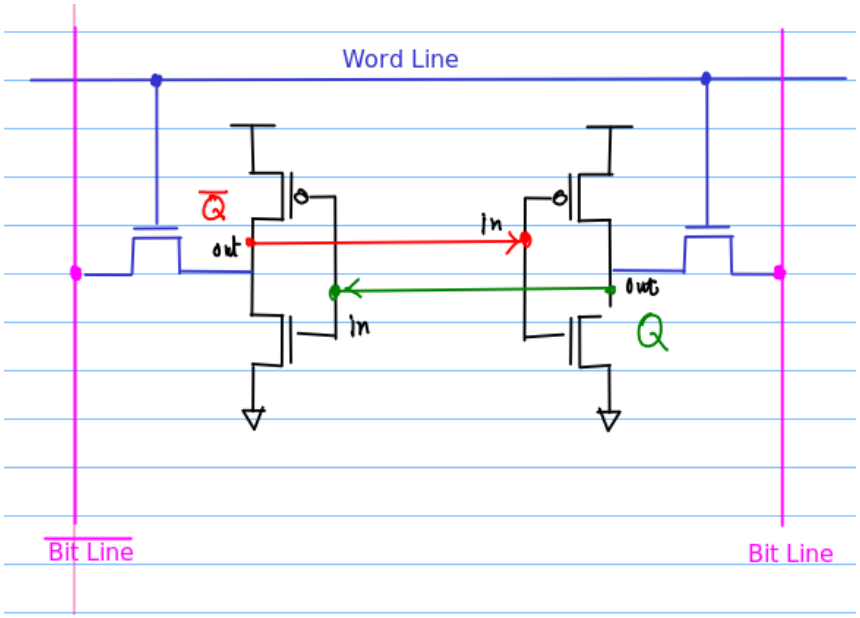
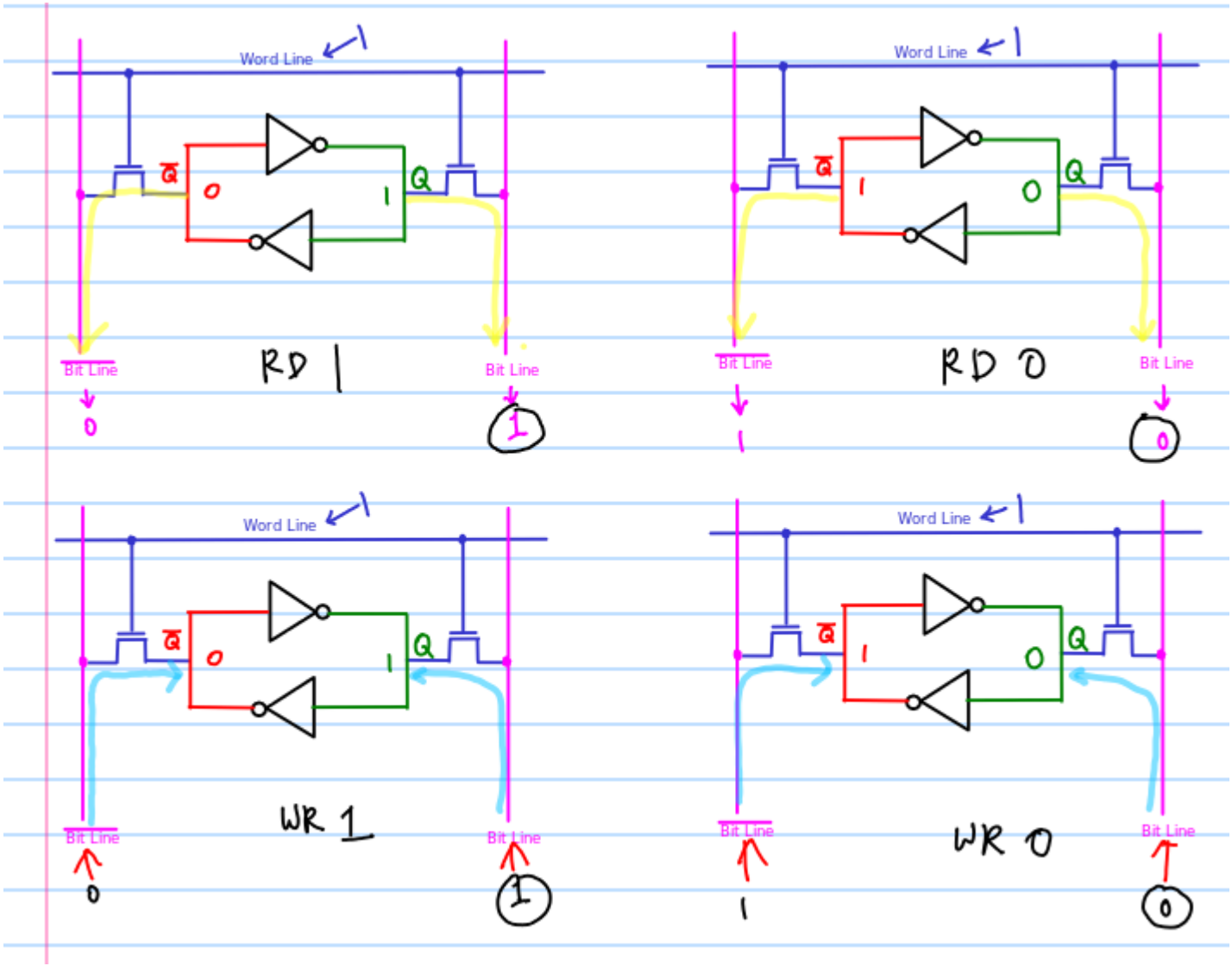
6-TR SRAM Cell

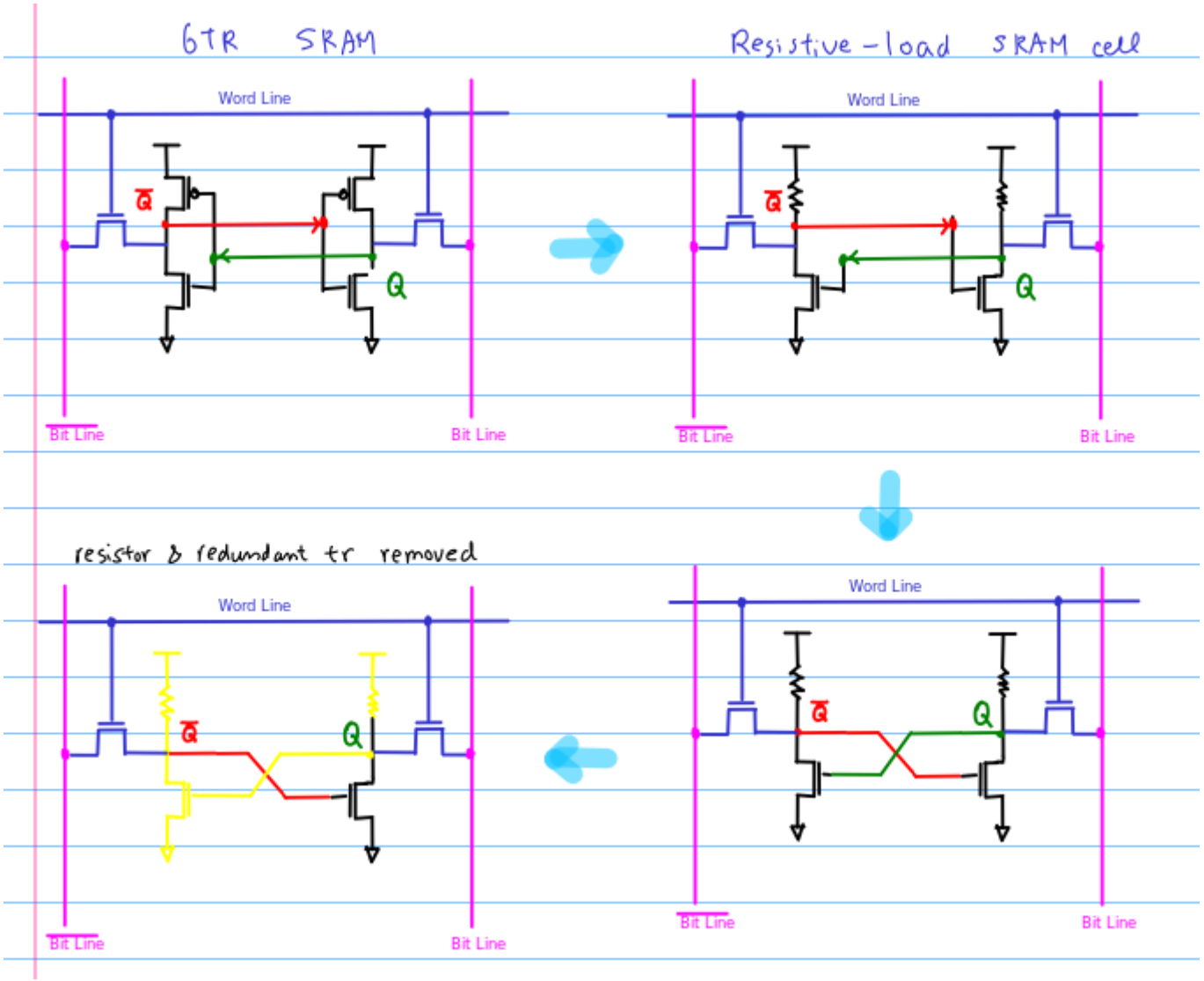




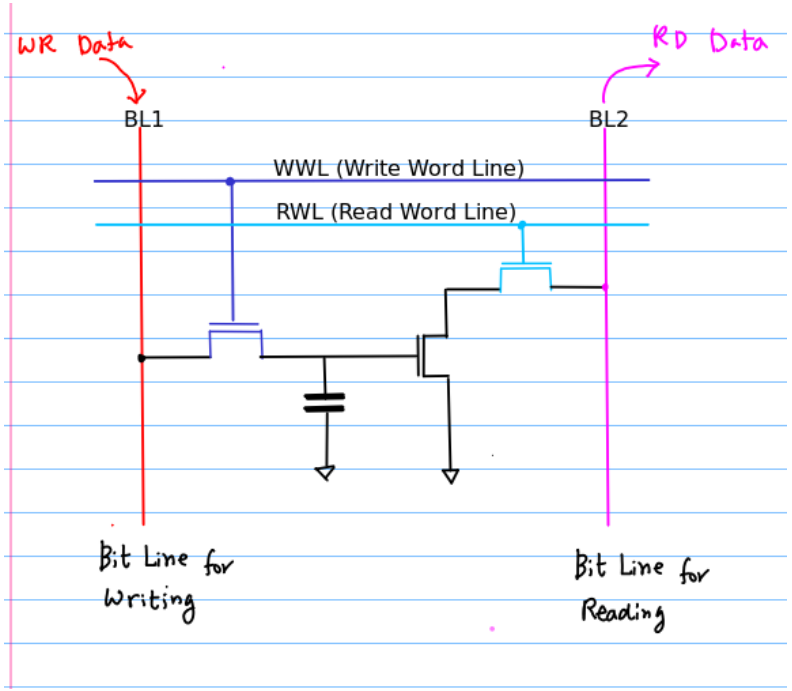
6-TR SRAM Cell Operation

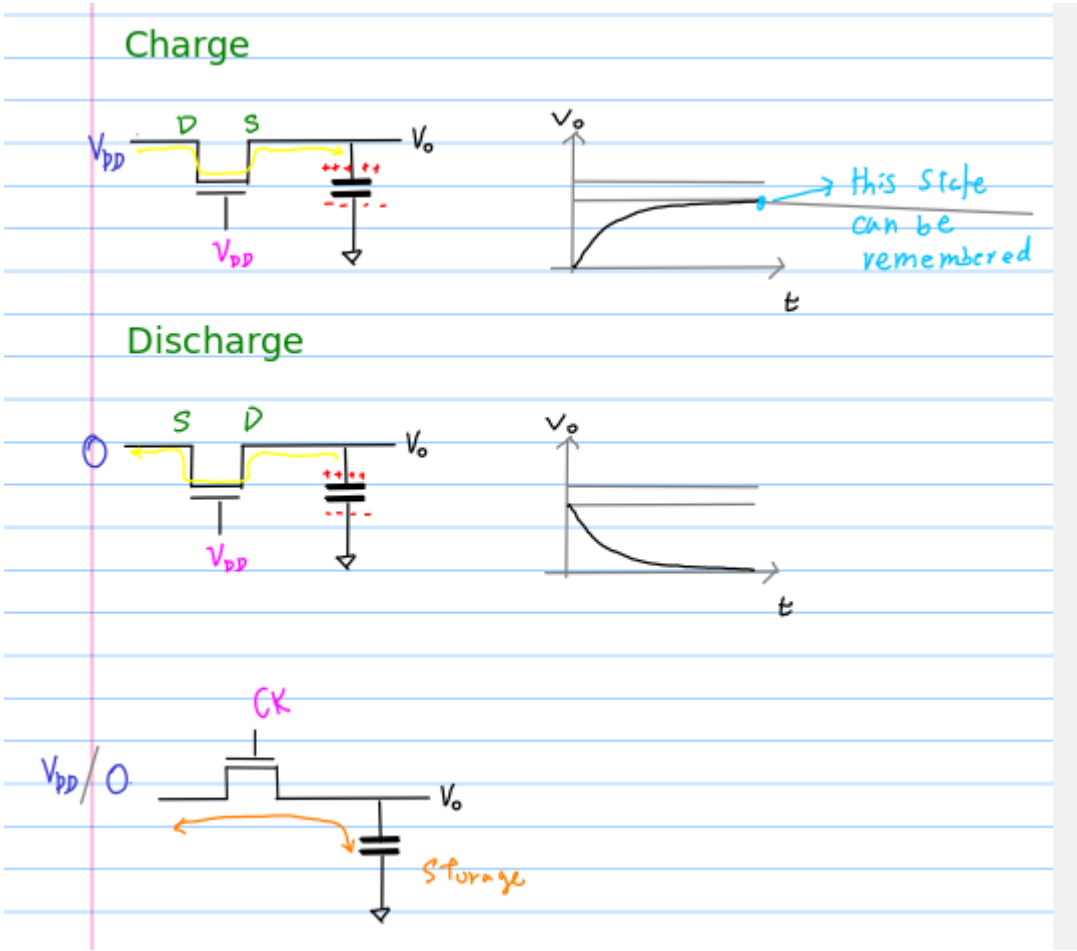


Reduce 6-TR SRAM Cell

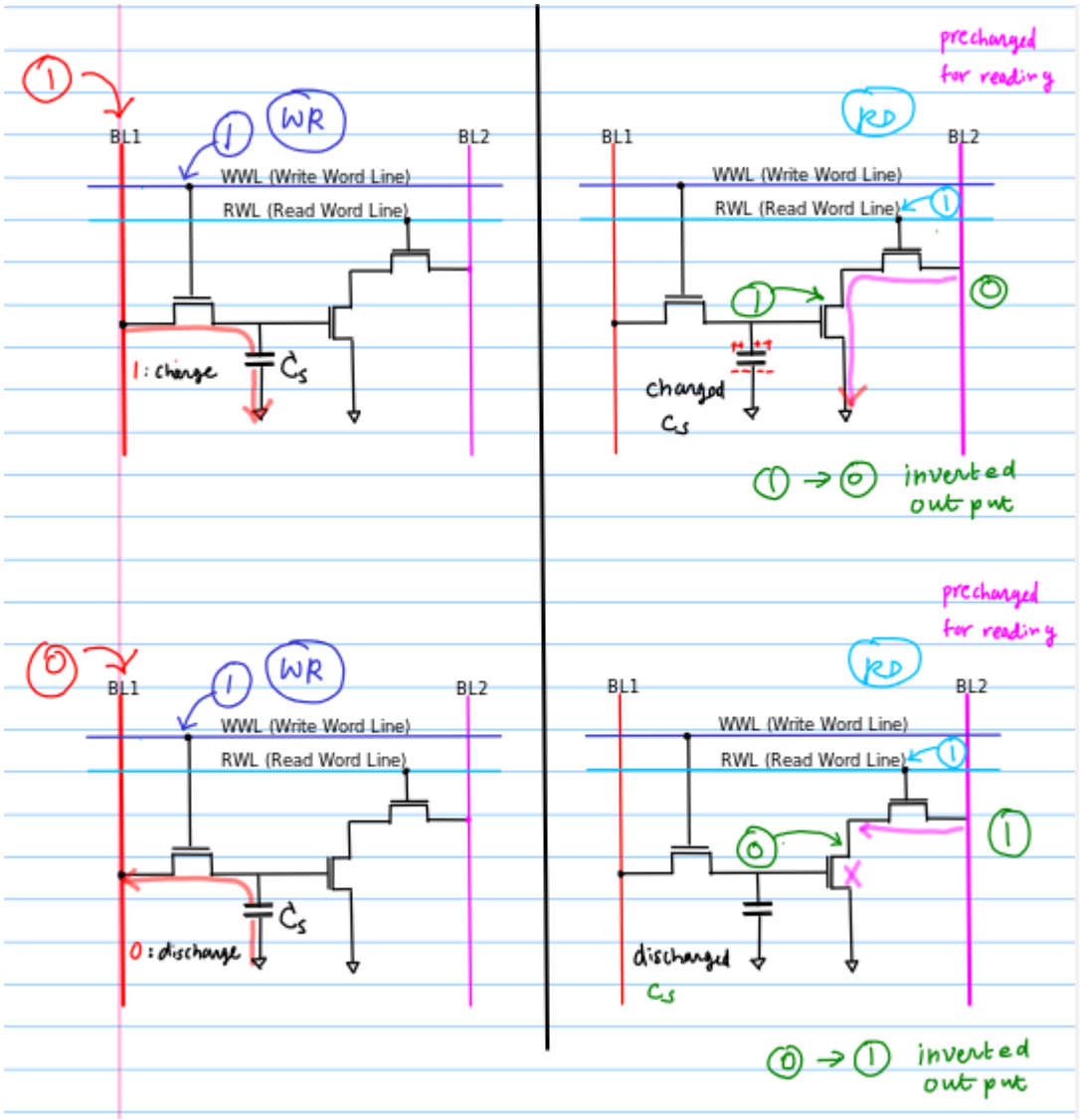


3-TR DRAM Cell

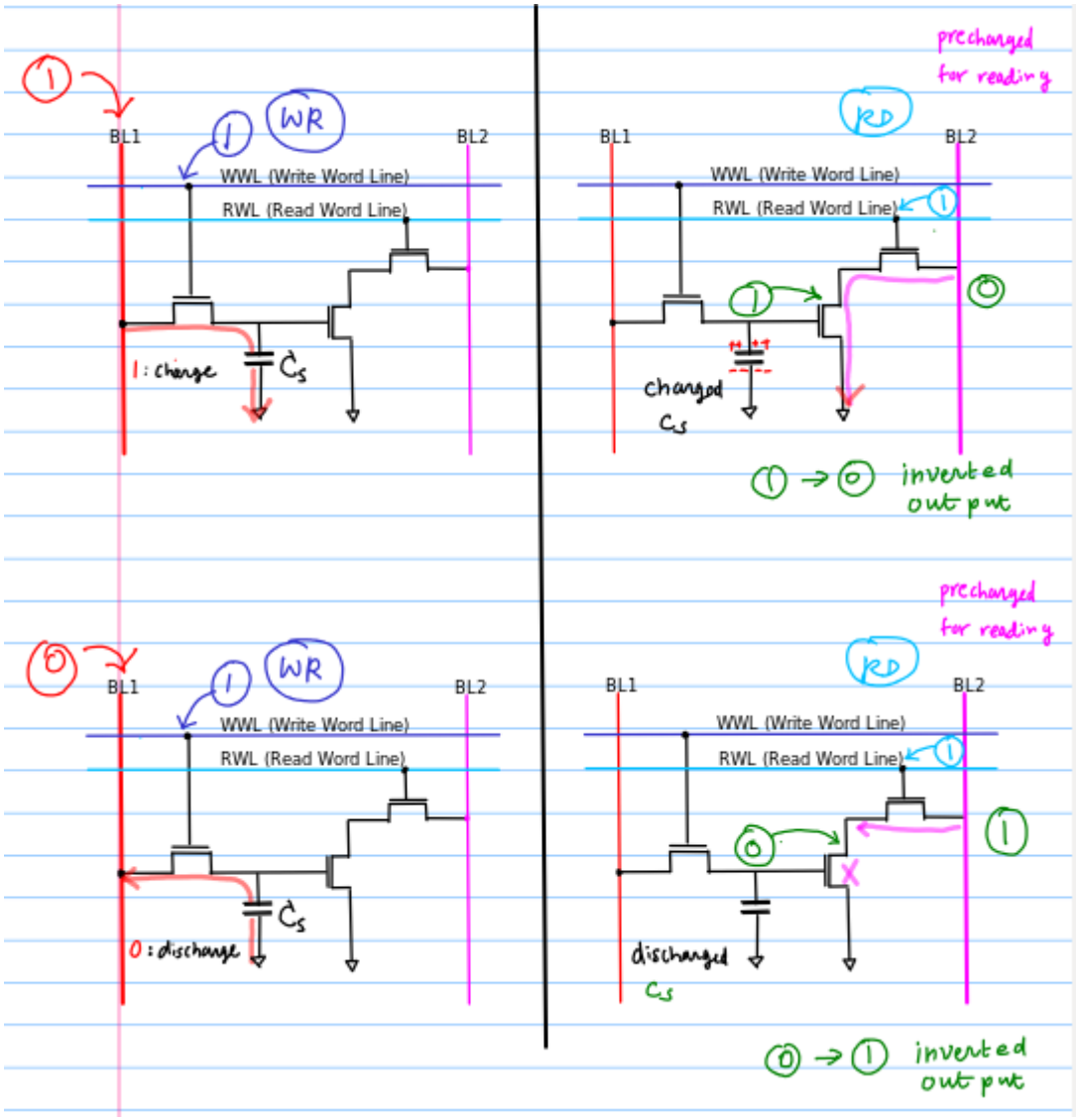




3-TR DRAM Cell Operation



3-TR DRAM Cell Operation



References

[1] http://en.wikipedia.org/
[2] http://www.allaboutcircuits.com/
[3] W. Wolf, “Modern VLSI Design : Systems on Silicon
[4] N. Weste, D. Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”
[5] J. P. Uyemura, “Introduction to VLSI Circuits and Systems”
[6] https://en.wikiversity.org/wiki/The_necessities_in_SOC_Design
[7] https://en.wikiversity.org/wiki/The_necessities_in_Digital_Design
[8] https://en.wikiversity.org/wiki/The_necessities_in_Computer_Design
[9] https://en.wikiversity.org/wiki/The_necessities_in_Computer_Architecture
[10] https://en.wikiversity.org/wiki/The_necessities_in_Computer_Organization