CMOS Delay-7 (H.8)
Delay Model

20170126

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References

Some Figures from the following sites

[1] http://pages.hmc.edu/harris/cmosvlsi/4e/index.html
Weste & Harris Book Site

[2] en.wikipedia.org

β : Device Transconductance Parameter

k : Process Transconductance Parameter

μ : Electron / Hole Mobility

pMOS $\quad \beta_p = k'_p \left(\frac{W}{L}\right)_p \qquad k'_p = \mu_p C_{ox} \qquad C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

nMOS $\quad \beta_n = k'_n \left(\frac{W}{L}\right)_n \qquad k'_n = \mu_n C_{ox} \qquad C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

pMOS $\quad \beta_p = \mu_p \frac{\varepsilon_{ox}}{t_{ox}} \left(\frac{W}{L}\right)_p$

nMOS $\quad \beta_n = \mu_n \frac{\varepsilon_{ox}}{t_{ox}} \left(\frac{W}{L}\right)_n$

Saturation Current

$$I_{dp} = \frac{\beta_p}{2}\left(V_{GSn} - |V_{Tp}|\right)^2 \qquad V_{Tp} < 0$$

$$I_{dn} = \frac{\beta_n}{2}\left(V_{GSn} - V_{Tn}\right)^2 \qquad V_{Tn} > 0$$

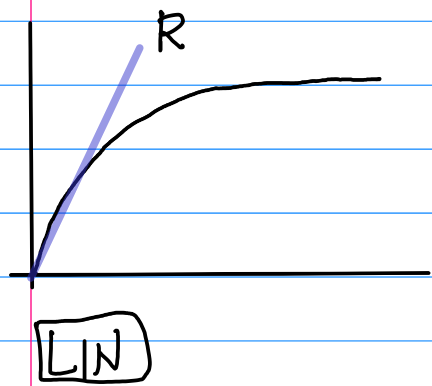
MODEL

$$\frac{\beta_n}{\beta_p} \simeq \frac{k'_n \left(\frac{W}{L}\right)_n}{k'_p \left(\frac{W}{L}\right)_p}$$

$$\frac{k'_n}{k'_p} = 2 \sim 3$$

$$\frac{k'_n}{k'_p} = \frac{\mu_n}{\mu_p} = r$$

$$\frac{\beta_n}{\beta_p} = \frac{k'_n \left(\frac{W}{L}\right)_n}{k'_p \left(\frac{W}{L}\right)_p}$$



$$R_n = \frac{1}{\beta_n (V_{DD} - V_{Tn})}$$

$$R_p = \frac{1}{\beta_n (V_{DD} - V_{Tn})}$$

fall time t_f $\quad$ $\tau_n = R_n C_{out}$

rise time t_r $\quad$ $\tau_p = R_p C_{out}$

$$C_{out} = C_{para} + C_L$$

MODEL

fall time	$t_f = 2.2\,\tau_n = \ln 9\,\tau_n$	$0.9\,V_{DD} \rightarrow 0.1\,V_{DD}$
rise time	$t_r = 2.2\,\tau_p = \ln 9\,\tau_p$	$0.1\,V_{DD} \rightarrow 0.9\,V_{DD}$
propagation delay time	$t_p = \frac{1}{2}(t_{pf} + t_{pr})$ $= 0.35(t_{pf} + t_{pr})$	$0.5\,V_{DD} \rightarrow 0.5\,V_{DD}$
propagation fall time	$t_{pf} = 0.7\,\tau_n = \ln 2\,\tau_n$	$V_{DD} \rightarrow 0.5\,V_{DD}$
propagation rise time	$t_{pr} = 0.7\,\tau_p = \ln 2\,\tau_p$	$0 \rightarrow 0.5\,V_{DD}$

$$\tau_n = R_n(C_{para} + C_L)$$

$$\tau_p = R_p(C_{para} + C_L)$$

$$C_{out} = C_{para} + C_L$$

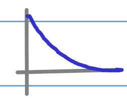
MODEL

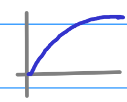
$$\left(\frac{W}{L}\right)_p = r\left(\frac{W}{L}\right)_n$$

$$r = \frac{\mu_n}{\mu_p} = \frac{k'_n}{k'_p} > 1$$

$$R_n = R_p = R = \frac{1}{\beta(V_{DD} - V_T)}$$

$$\begin{cases} V_{out}(t) = V_{DD}\left(1 - e^{-t/\tau}\right) \\ V_{out}(t) = V_{DD}\, e^{-t/\tau} \end{cases}$$





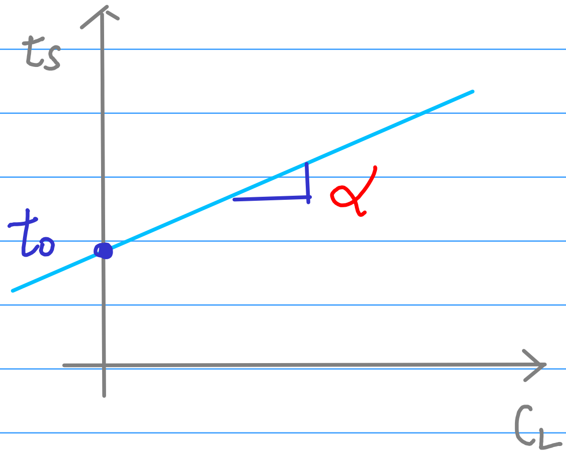
$$\tau = R\,C_{out} = R\left(C_{par} + C_L\right)$$

Generic Switching Delay

$$t_s = t_0 + \alpha C_L \quad \Rightarrow \quad t_s = t_r = t_f$$

Generic Switching Delay

$$t_s = t_0 + \alpha C_L$$



t_0 : zero delay

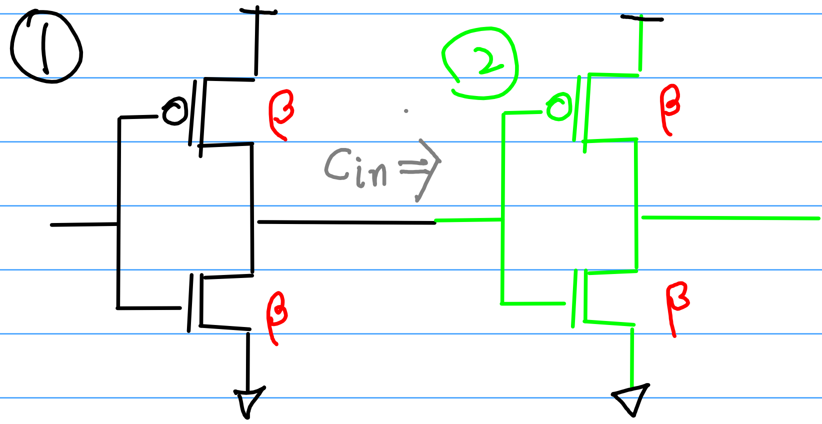
α : slope

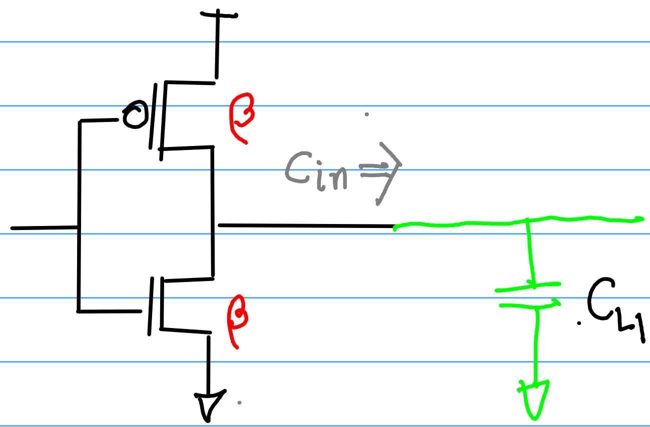
$$t \approx RC$$

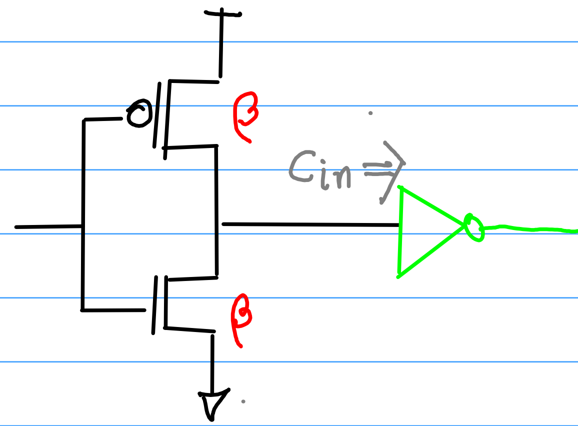
$$\alpha \propto \frac{1}{\beta (V_{DD} - V_T)}$$

C_L

MODEL







reference case $\boxed{C_{in} = C_{L1}}$

Generic Switching Delay of (1)

$$t_{s1} = t_0 + \alpha C_{L1}$$

$$= t_0 + \alpha C_{in}$$

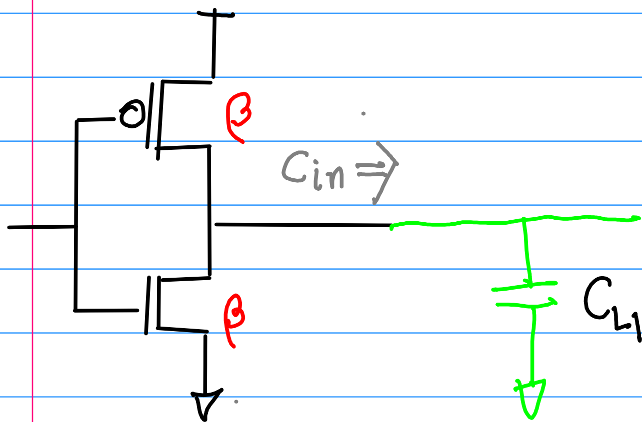
$$C_{in} = C_{Gn} + C_{Gp}$$
$$= C_{ox}(A_{Gn} + A_{Gp})$$

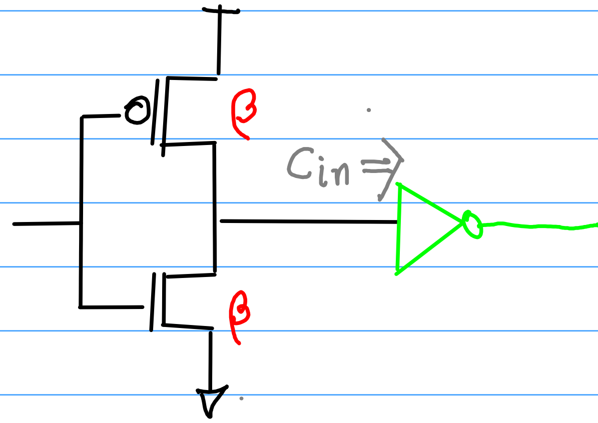
A: gate area

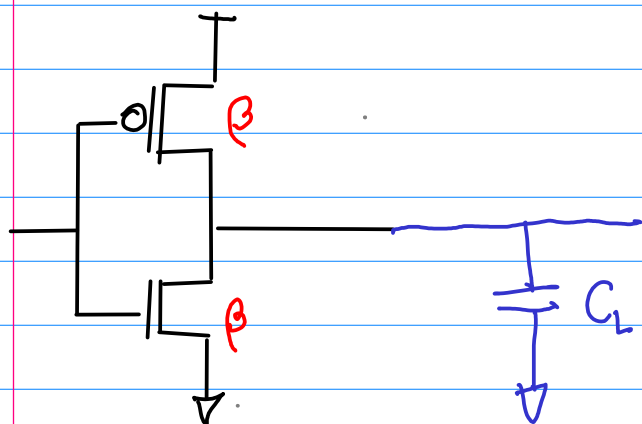
the channel length L assumed

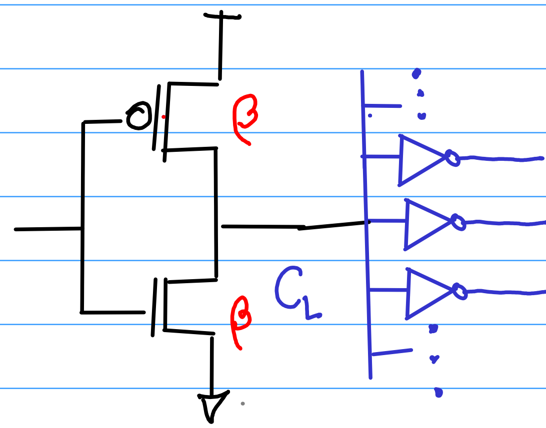
$$C_{in} = C_{ox} L (W_n + W_p)$$
$$= C_{ox} L (W_n + r W_p)$$
$$= C_{ox} L W_n \cdot (1 + r)$$
$$= C_{Gn} (1 + r)$$

When $C_L \gg C_{in}$









to minimize t_s

$\alpha \downarrow \Rightarrow R \downarrow \Rightarrow \beta \uparrow \Rightarrow$ bigger size

speed v.s. area tradeoff

$$t_s = t_0 + \alpha C_L \qquad t \approx RC$$

$$\alpha \propto \frac{1}{\beta (V_{DD} - V_T)} \qquad C_L$$

MODEL

to minimize t_s

$\alpha \downarrow \Rightarrow R \downarrow \Rightarrow \beta \uparrow \Rightarrow$ bigger size

speed v.s. area <u>tradeoff</u>

Scaling Factor S

$$\beta' = S\beta$$

$$R' = \frac{R}{S}$$

$$\alpha' = \frac{\alpha}{S}$$

$$t_s = t_0 + \underbrace{\frac{\alpha}{S}}_{R} \underbrace{C_L}_{C}$$

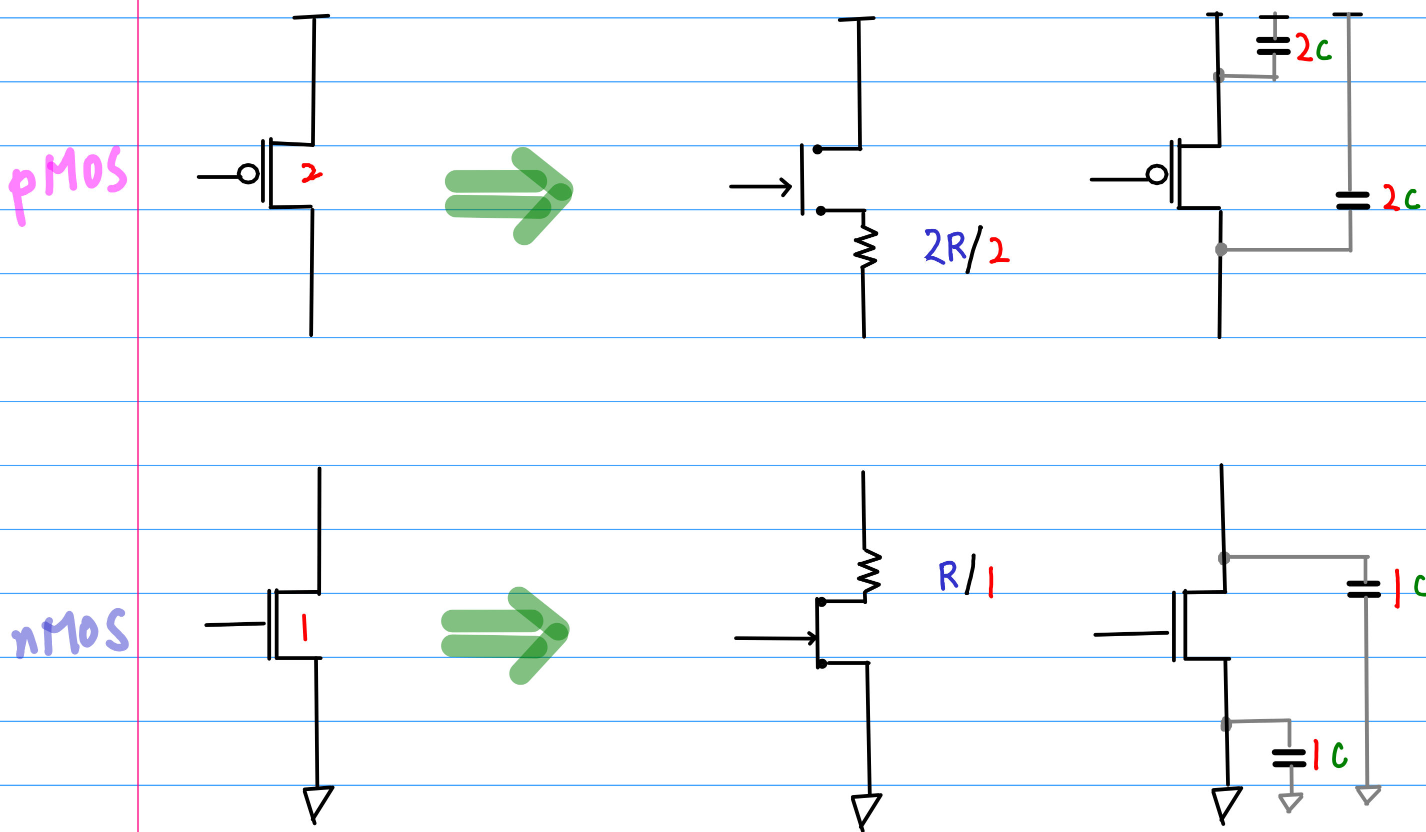
Compensation Factor $\frac{1}{S}$

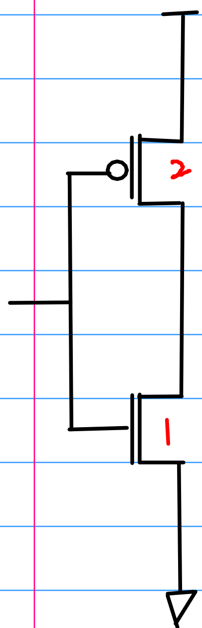
enables a NOT gate <u>drive</u> <u>larger values</u> of C_L

If $C_L = S\, C_{in}$ (increased by the scaling factor S)

then the switching time is the same

RC Delay Model

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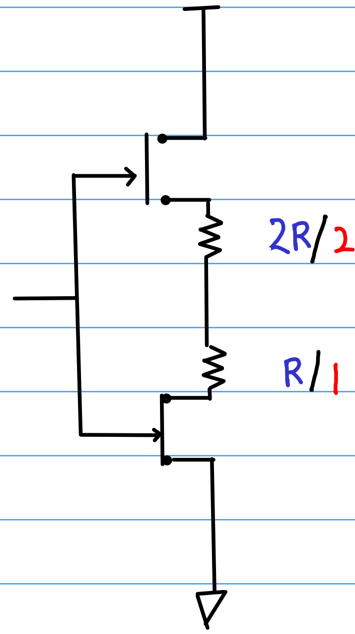
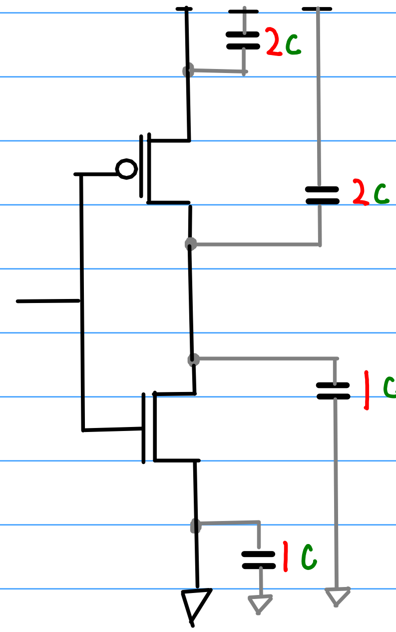
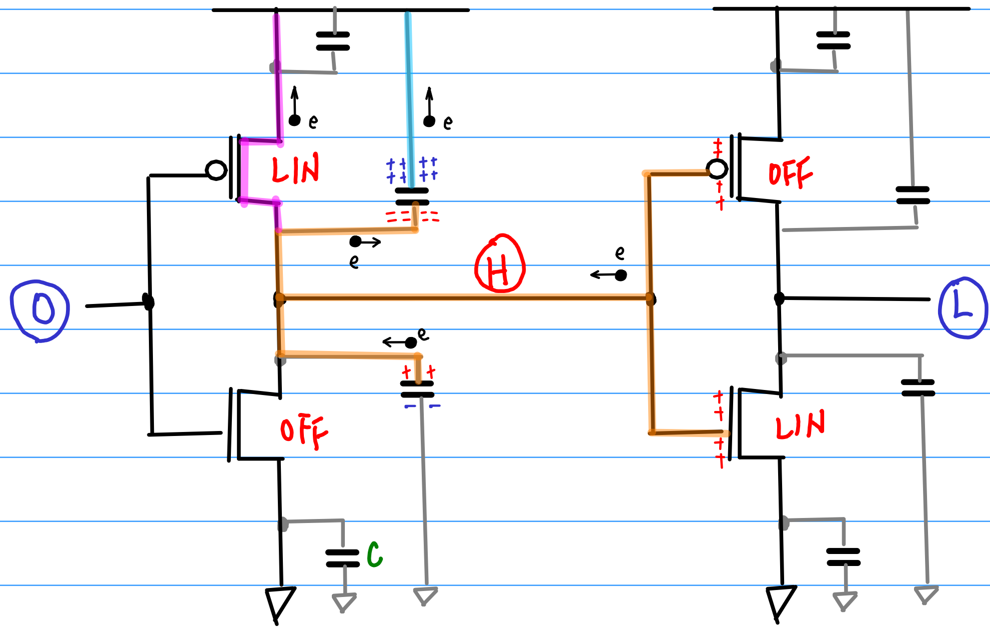
1


2R/2
R/1


2C
2C
1C
1C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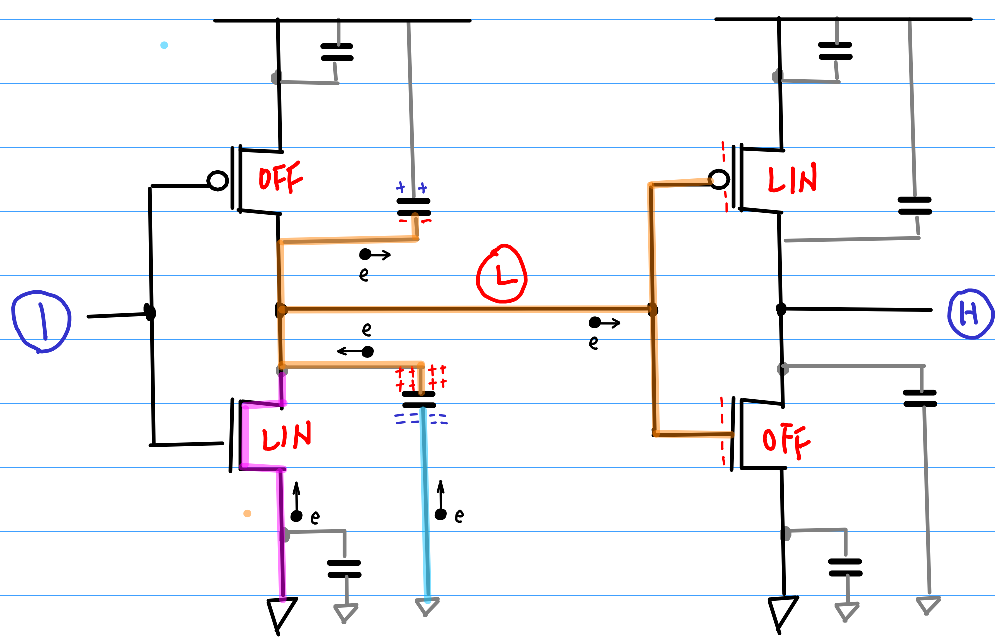
OFF
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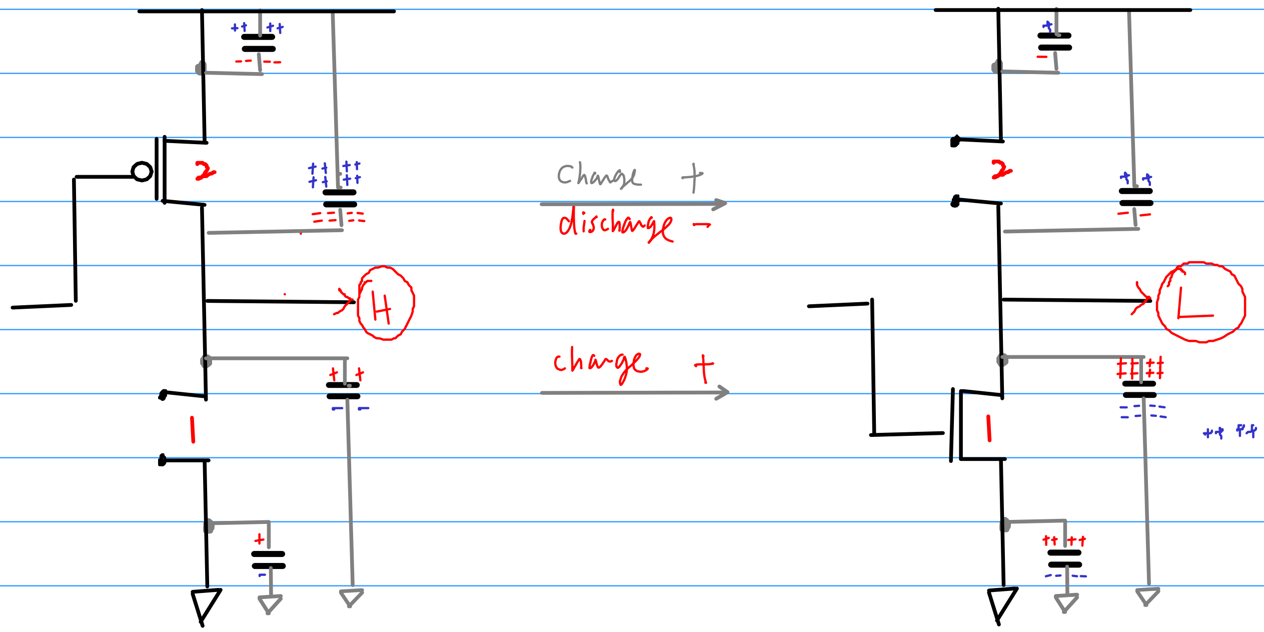
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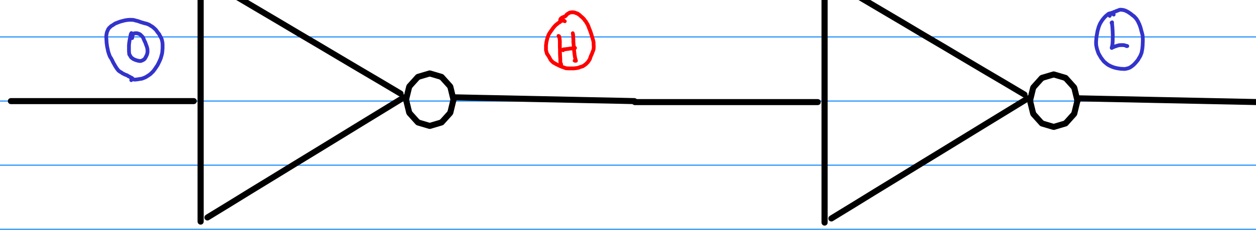
charge +
1
2
L
1


0
H
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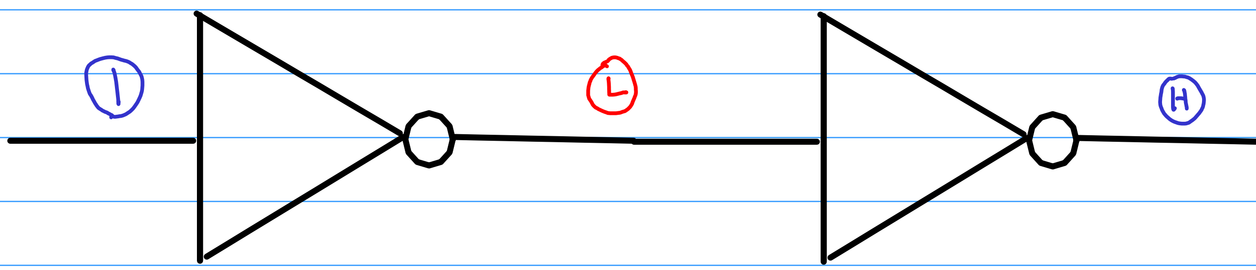
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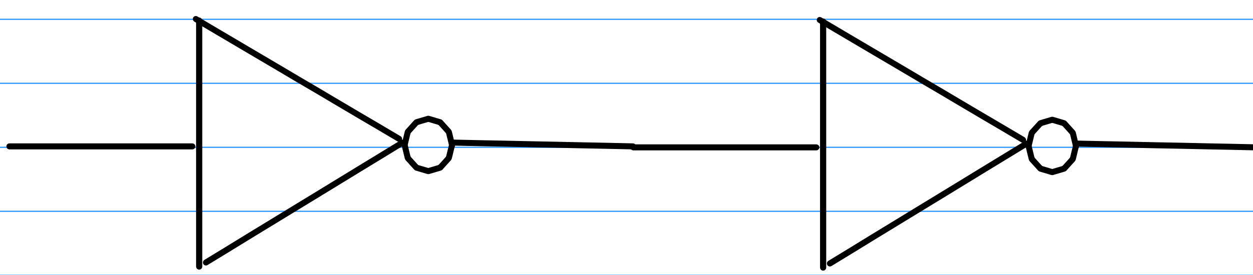

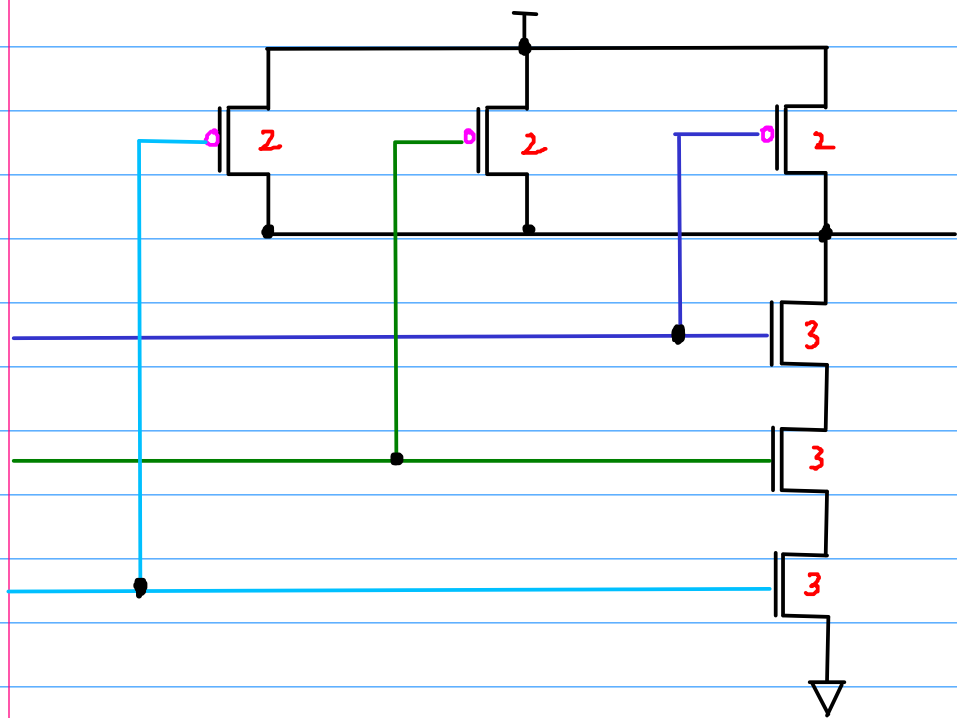
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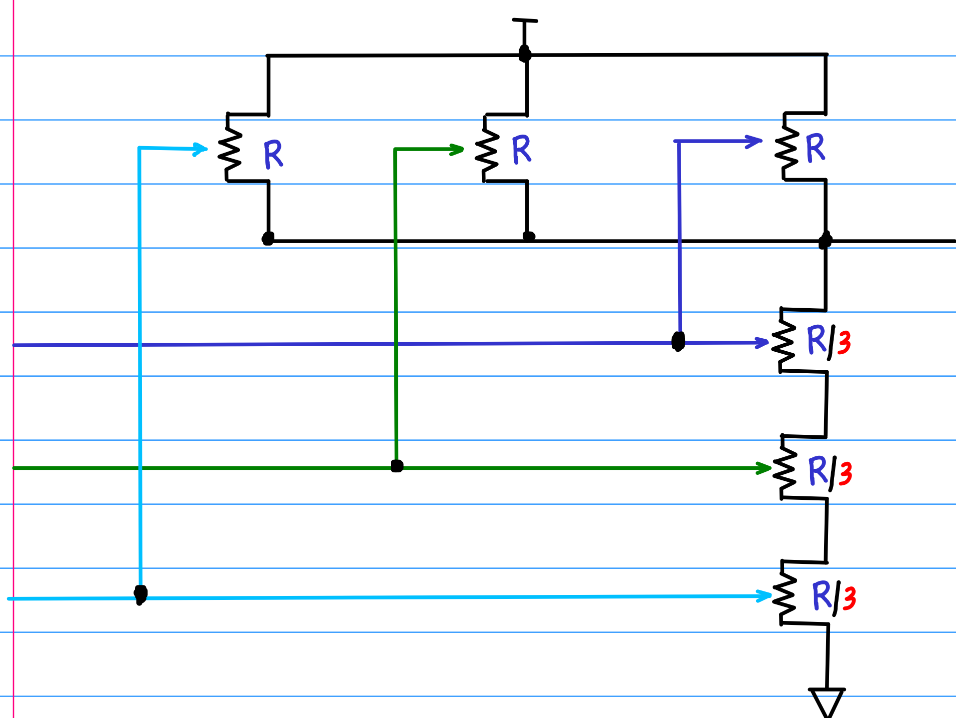
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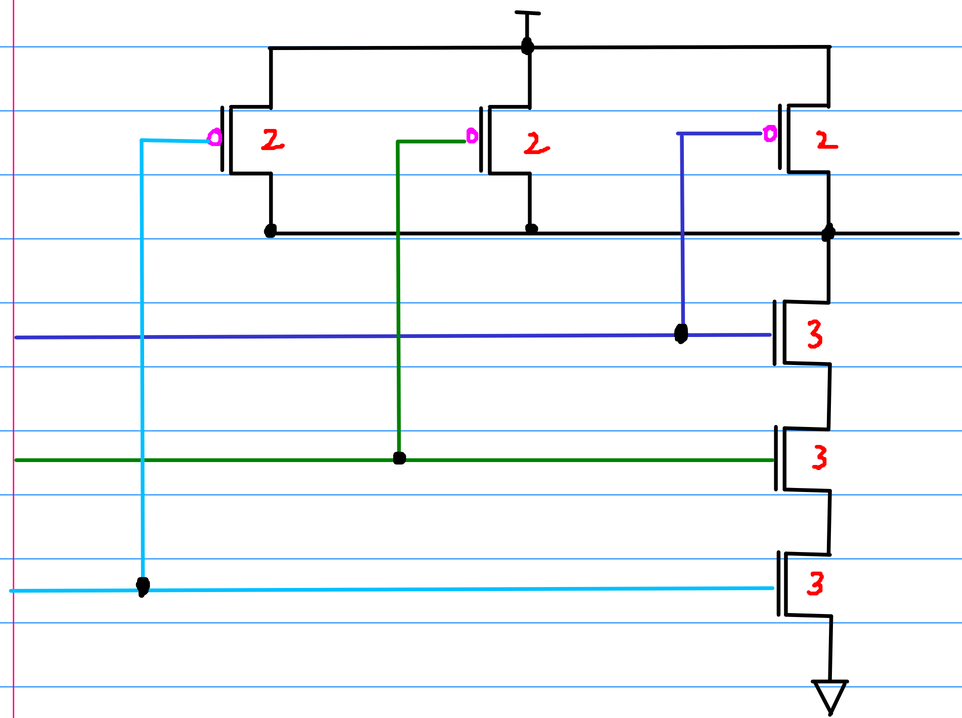
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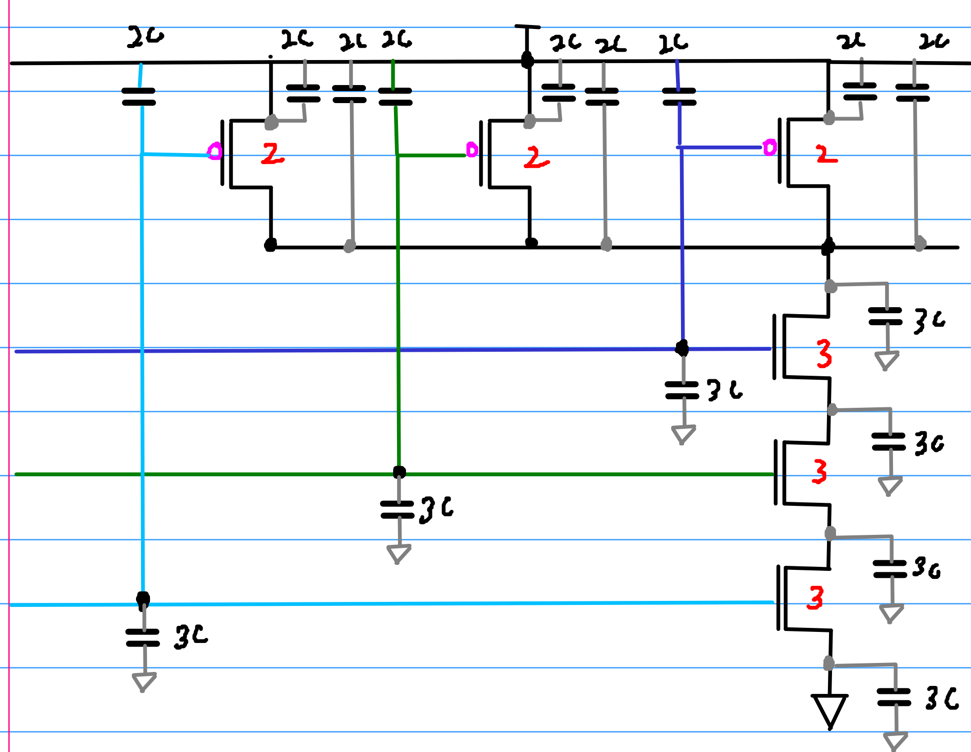
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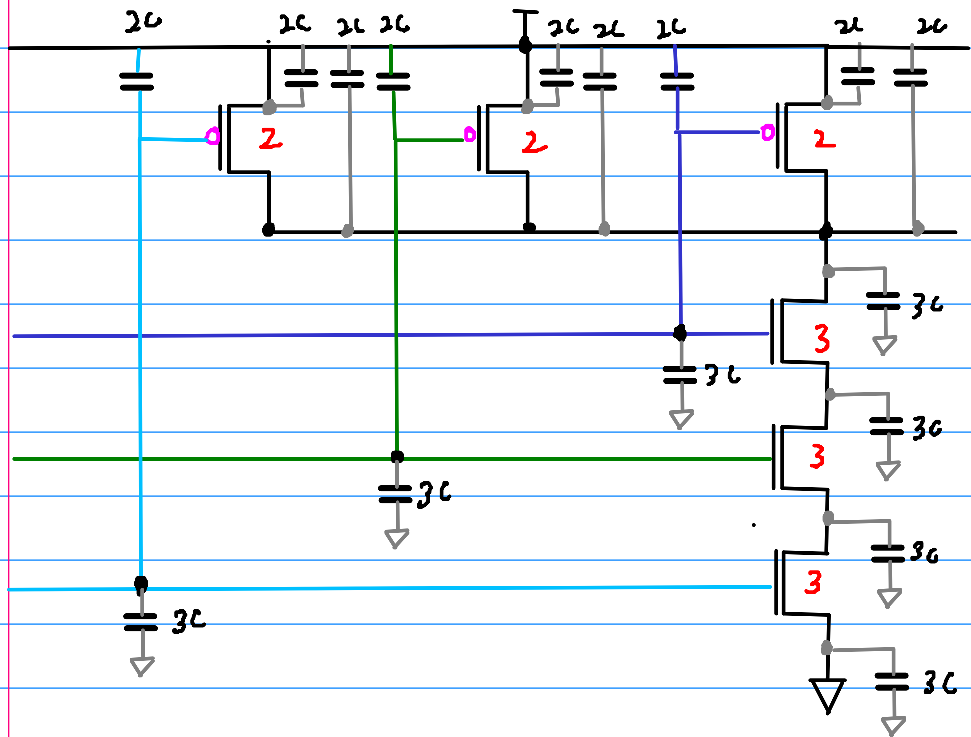

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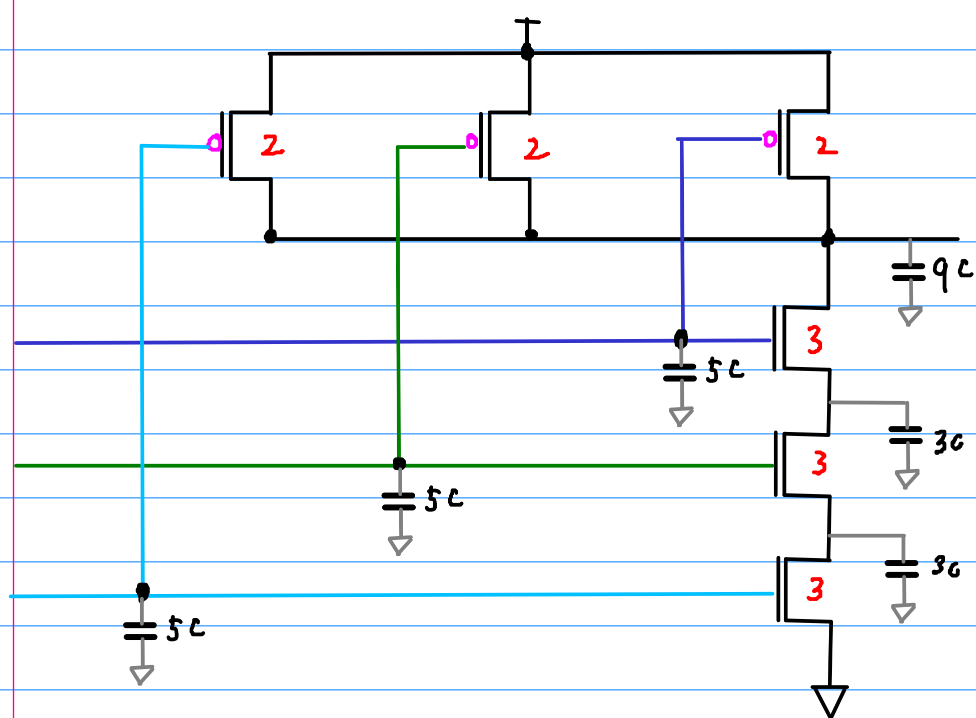

2
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3
5c
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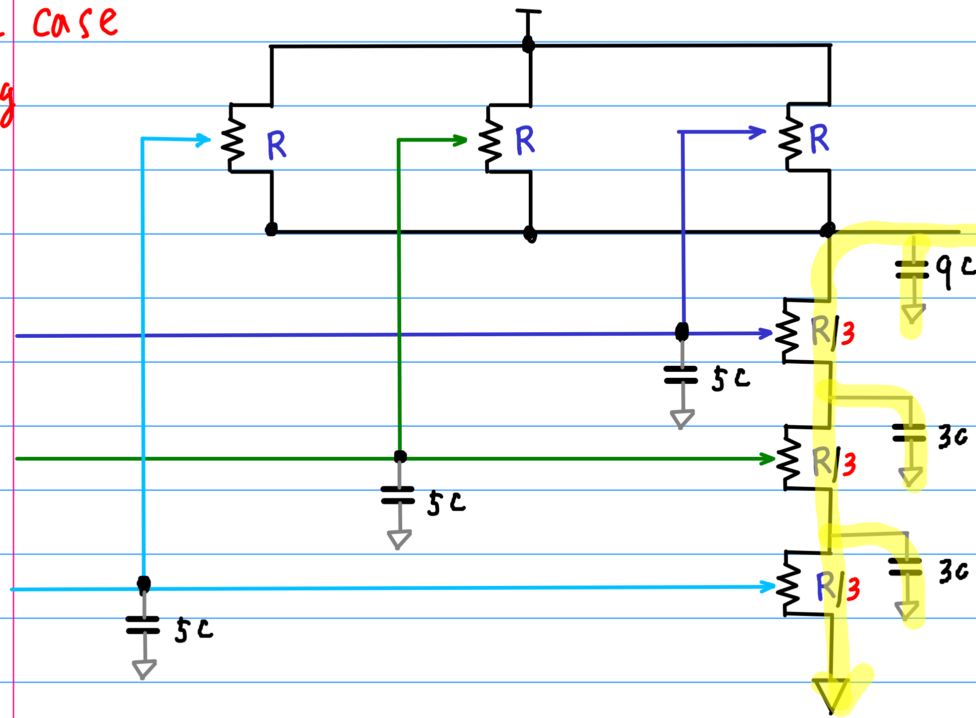
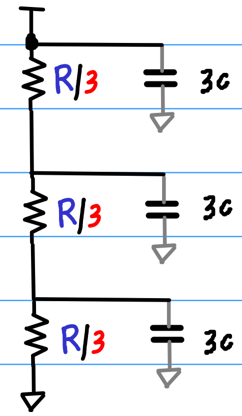
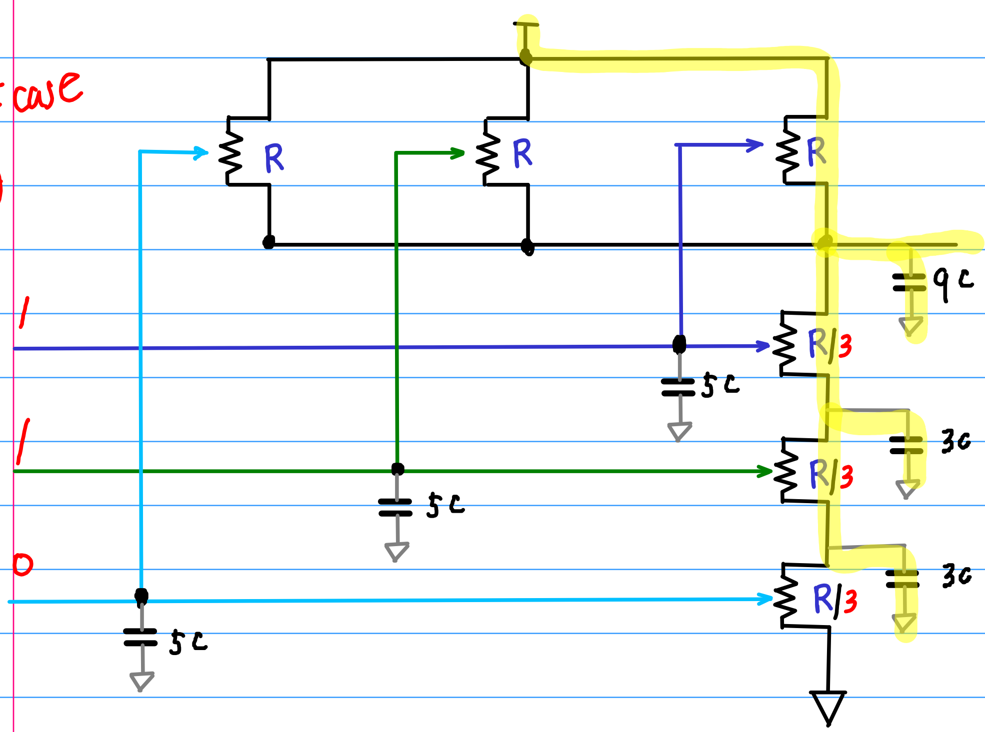
3
3c
5c

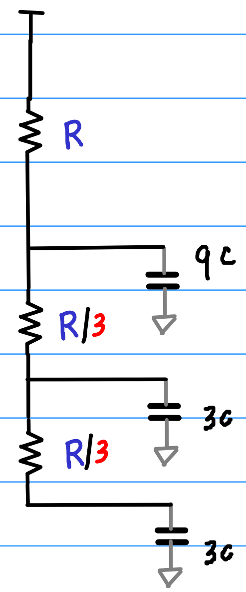
Worst case falling

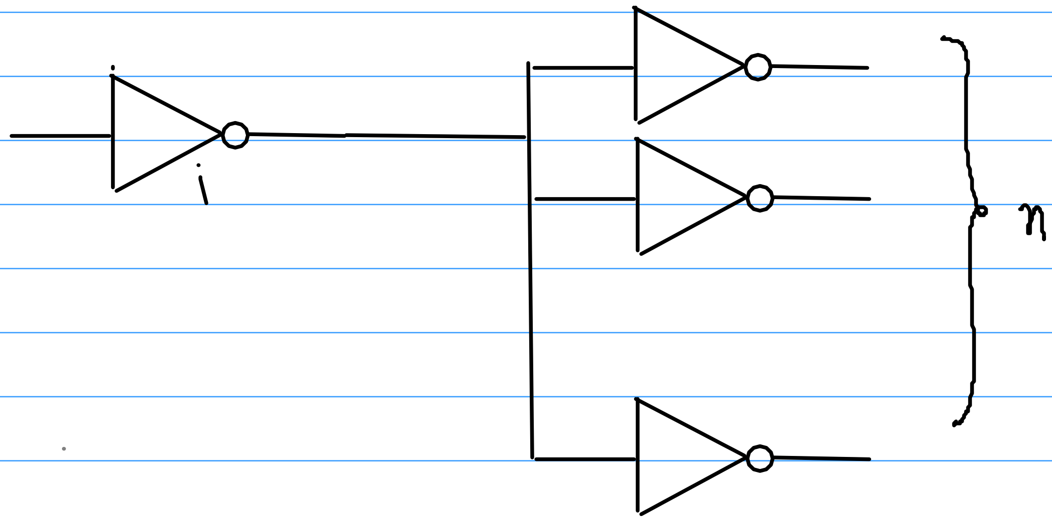




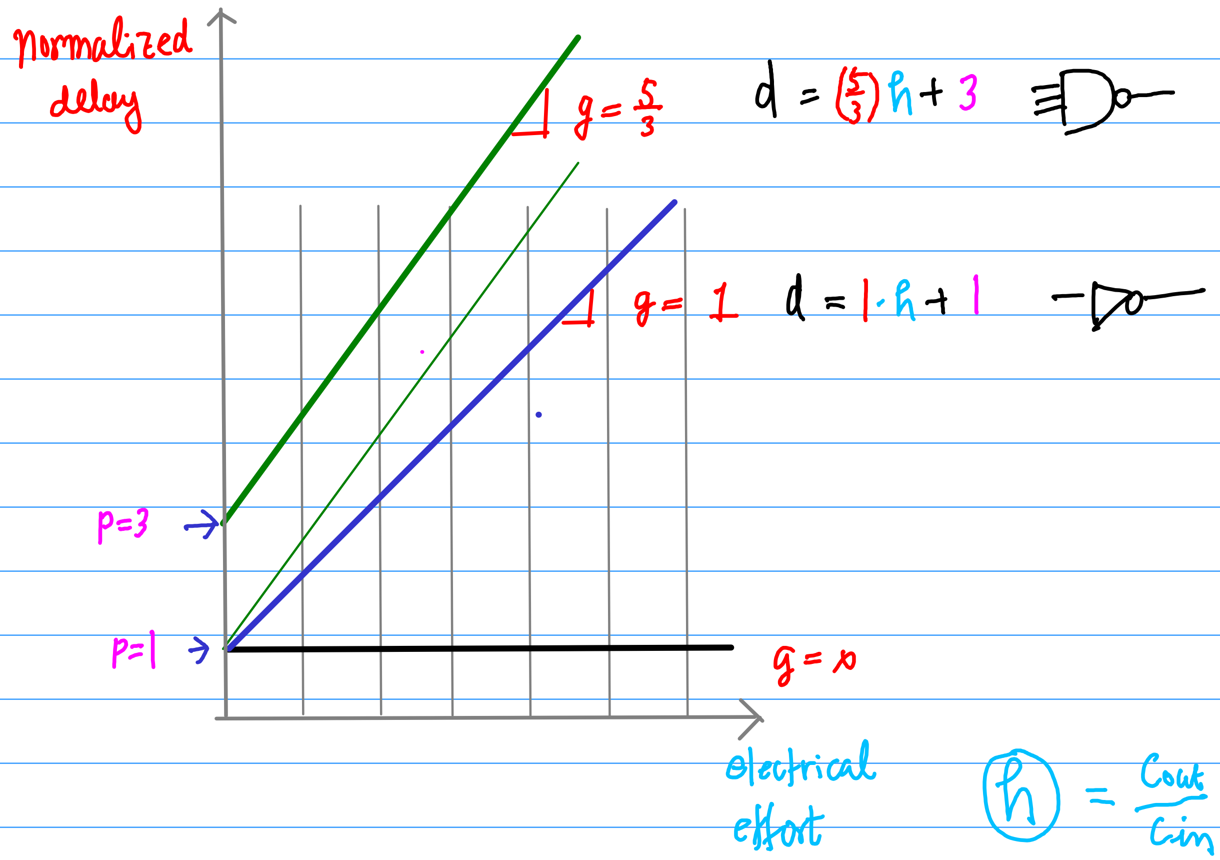
Worst case rising

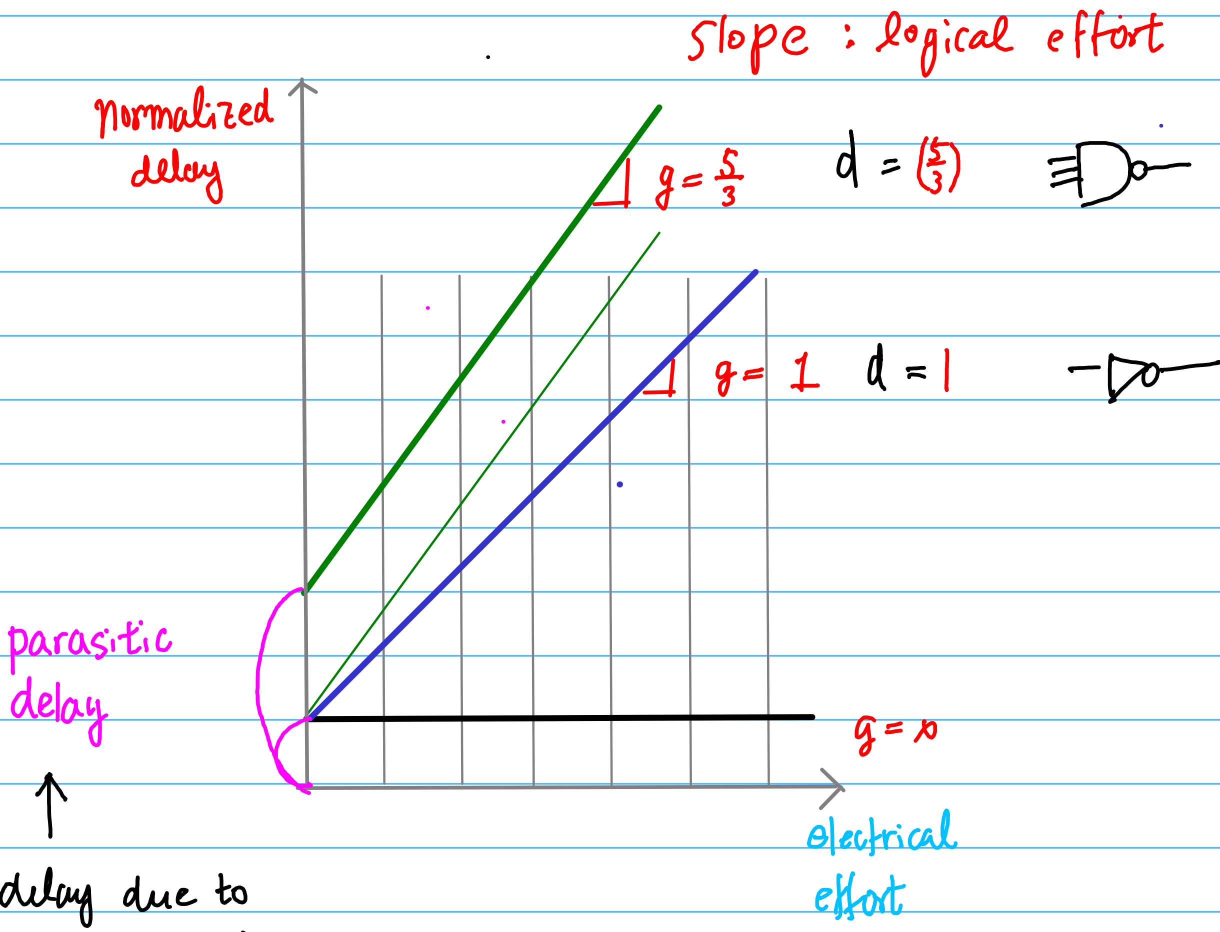





n

Linear Delay Model





↑

delay due to only internal cap without external load cap

$$d = g \cdot h + p$$

(k) (c) (c)