Device R & C

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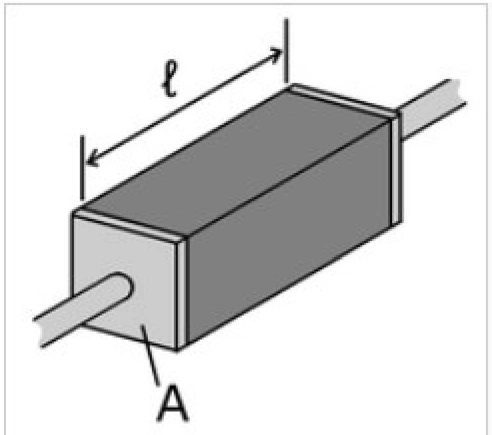
Resistance



A piece of resistive material with electrical contacts on both ends.

$$R = \rho \frac{\ell}{A},$$

$$G = \sigma \frac{A}{\ell}.$$

Ohm's law $V \propto I$

$$R = \frac{V}{I}, \qquad G = \frac{I}{V}$$

the derivative $\frac{dV}{dI}$ may be most useful; this is called the "differential resistance".

$$I_d = k' \frac{W}{L} \left[(v_{gs} - v_t) v_{ds} - \frac{1}{2} v_{ds}^2 \right]$$

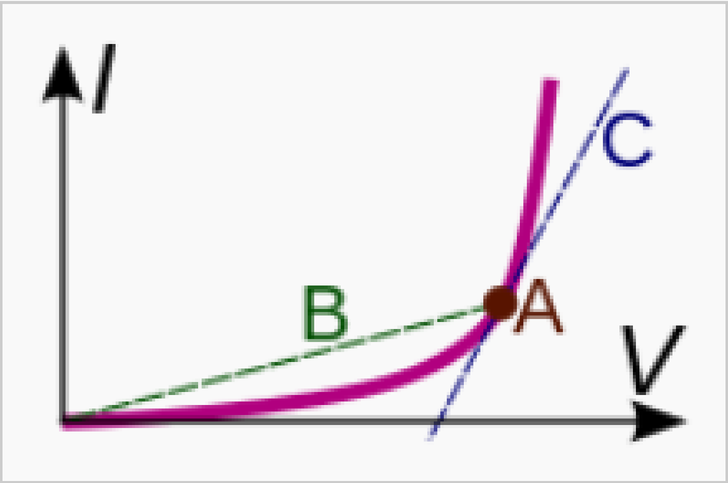
https://en.wikipedia.org/wiki/

The current-voltage characteristics of four devices: Two resistors, a diode, and a battery. The horizontal axis is voltage drop, the vertical axis is current. Ohm's law is satisfied when the graph is a straight line through the origin. Therefore, the two resistors are "ohmic", but the diode and battery are not.

Slope

the derivative $\frac{dV}{dI}$ may be most useful; this is called the "differential resistance".

Static & Derivative Resistance



The IV curve of a non-ohmic device (purple). Point A represents the current and voltage values right now. The **static resistance** is the inverse slope of line B through the origin. The **differential resistance** is the inverse slope of tangent line C.

- **Static resistance** (also called *chordal* or *DC resistance*) - This corresponds to the usual definition of resistance; the voltage divided by the current

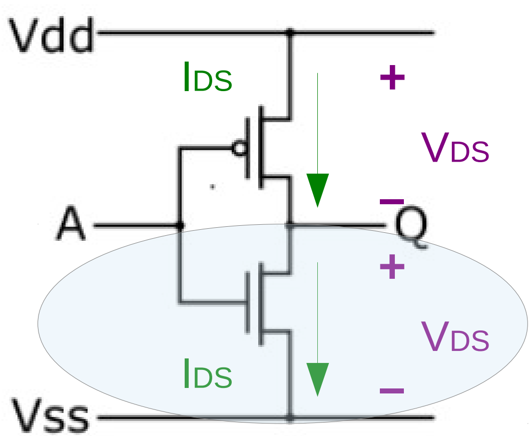
$$R_{\text{static}} = \frac{v}{i}.$$

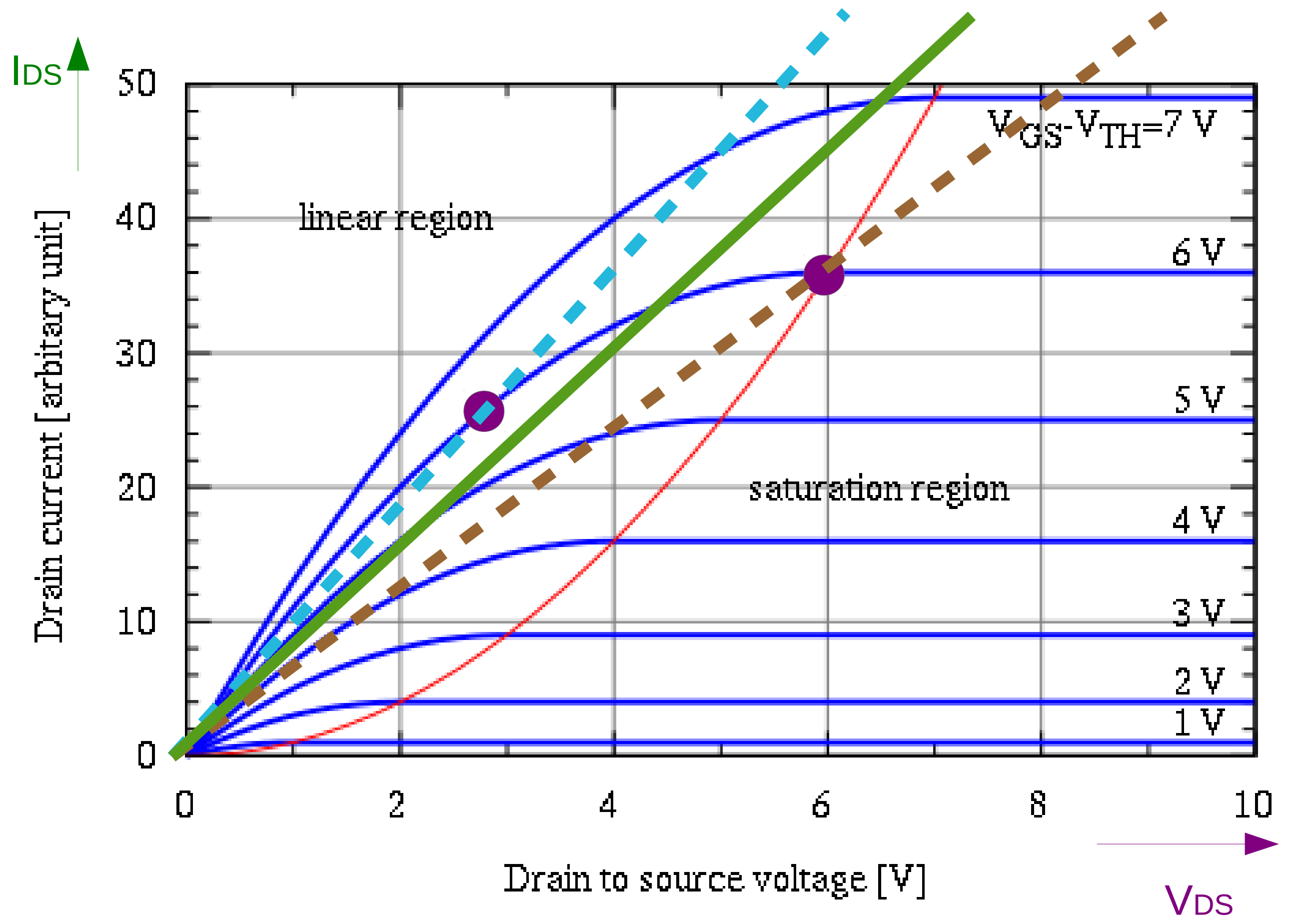
- **Differential resistance** (also called *dynamic*, *incremental* or *small signal resistance*) - Differential resistance is the derivative of the voltage with respect to the current; the slope of the *IV* curve at a point

$$R_{\text{diff}} = \frac{dv}{di}.$$

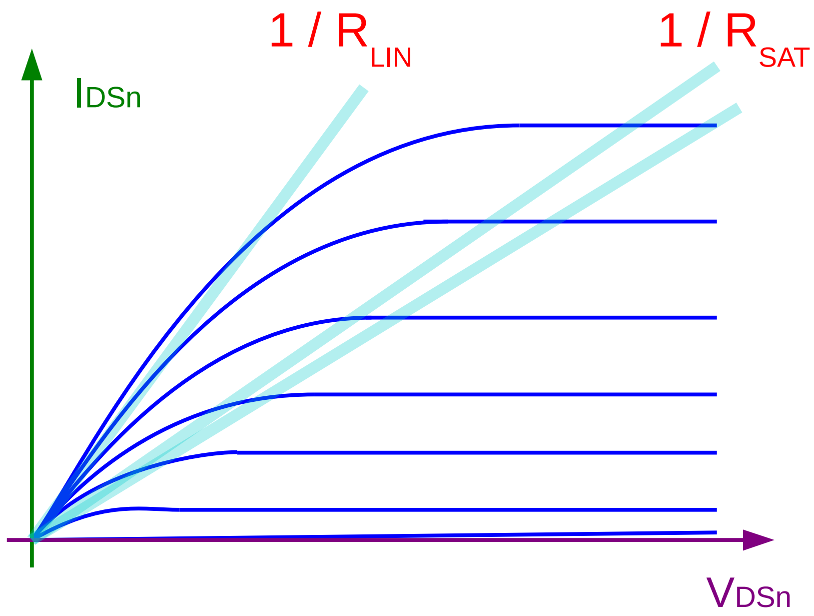
nMOS Resistance

https://en.wikipedia.org/wiki/





Transconductance Parameters



When $V_{GS} > V_t$ and $V_{DS} < (V_{GS} – V_t)$

$$I_d = k' \frac{W}{L} \left[(v_{gs} - v_t) v_{ds} - \frac{1}{2} v_{ds}^2 \right]$$

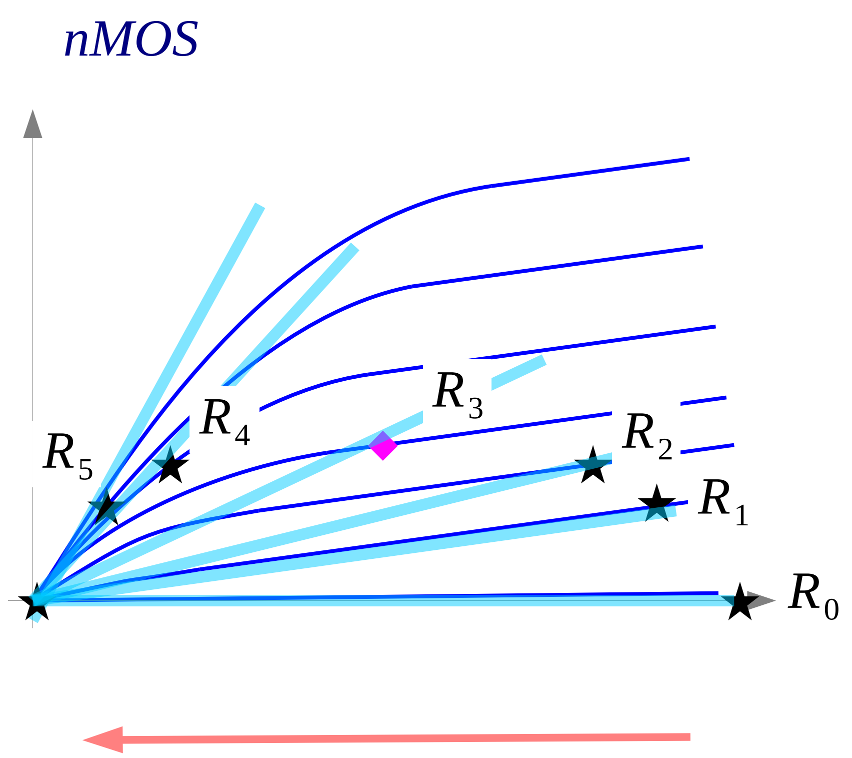
When $V_{GS} > V_t$ and $V_{DS} \geq (V_{GS} – V_t)$

$$I_d = \frac{1}{2} k' \frac{W}{L} (v_{gs} - v_t)^2$$

$$\beta_p = k'_p \left(\frac{W}{L} \right)_p \qquad \frac{1}{R_p}$$

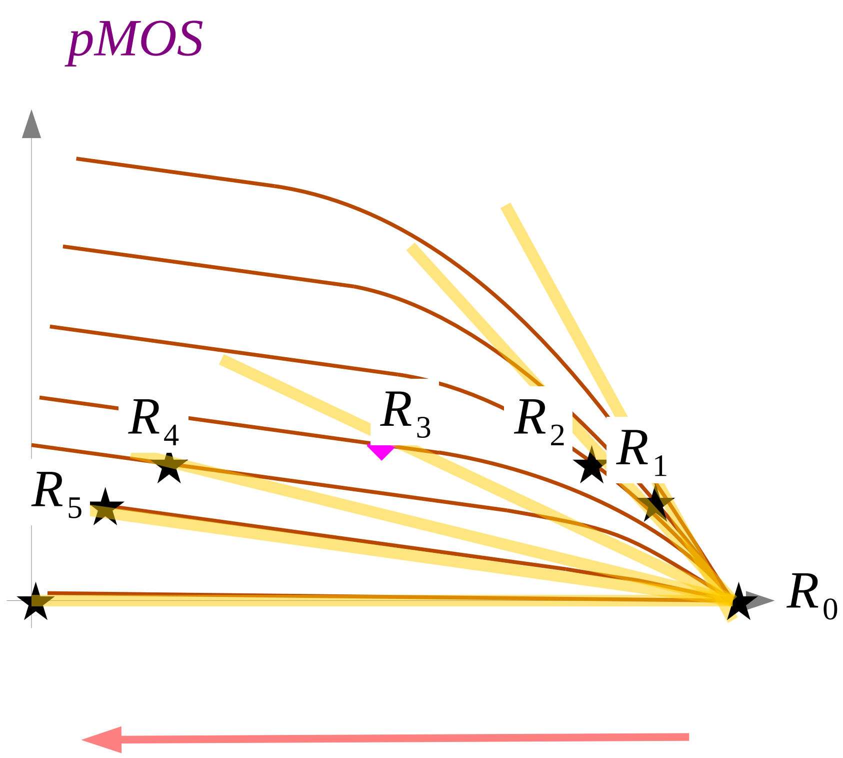
$$\beta_n = k'_n \left(\frac{W}{L} \right)_n \qquad \frac{1}{R_n}$$

Operating Points and Resistance



Decreasing Resistance

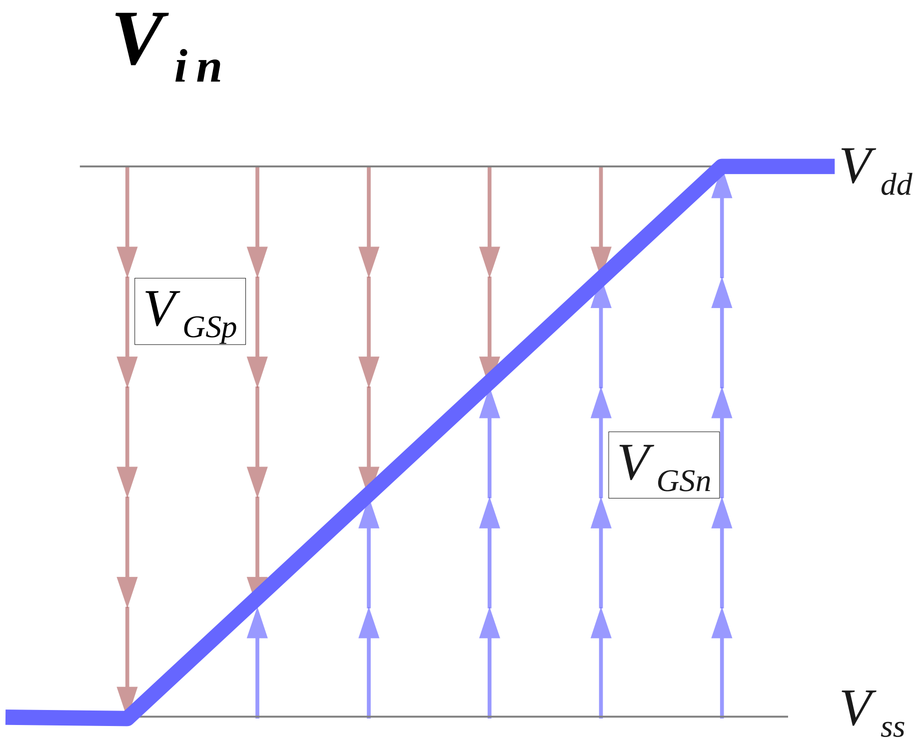
$$R_5 < R_4 < R_3 < R_2 < R_1 < R_0 = \infty$$

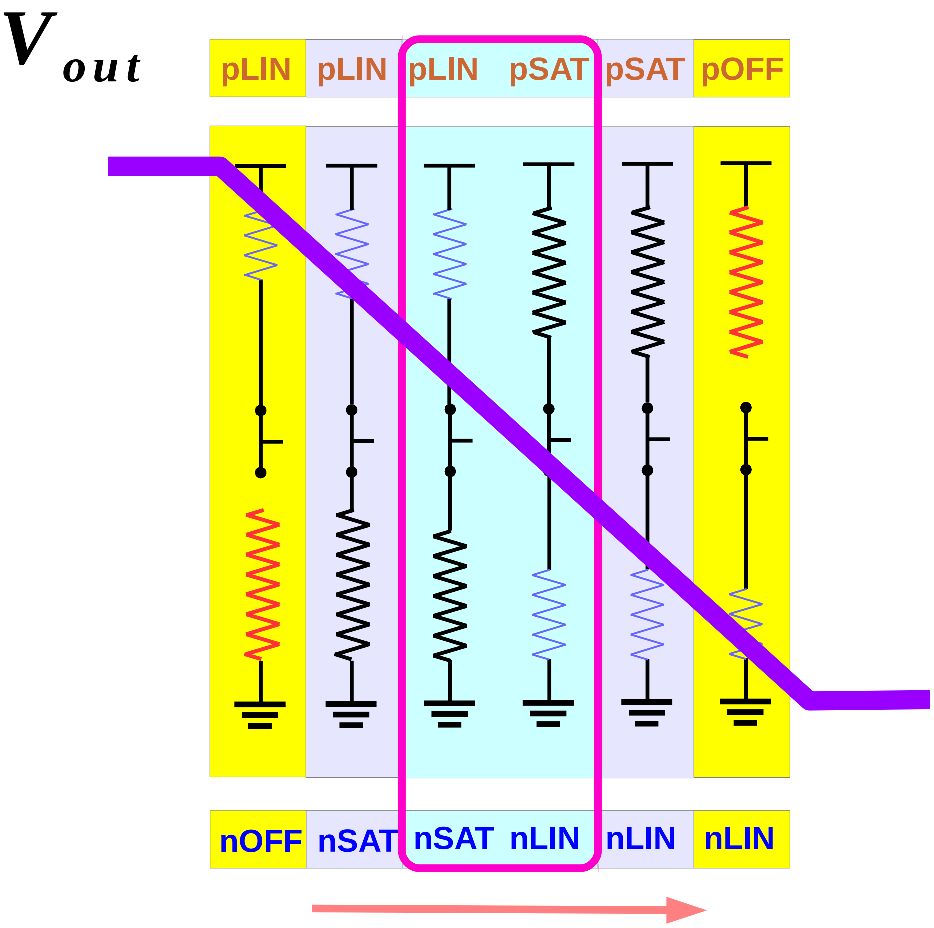


Increasing Resistance

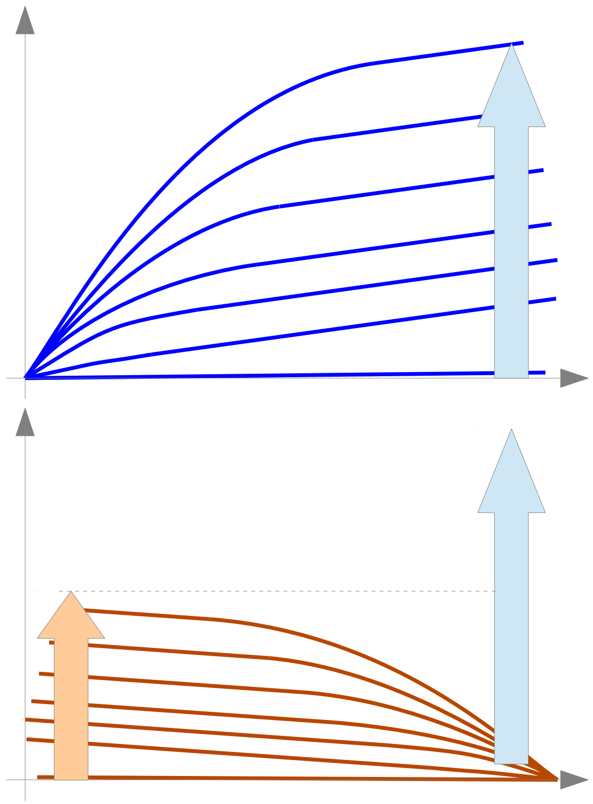
$$\infty = R_5 > R_4 > R_3 > R_2 > R_1 > R_0$$

Voltage Divider Output



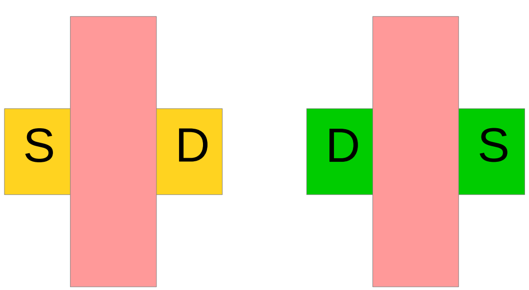


Transconductance and Transistor Size

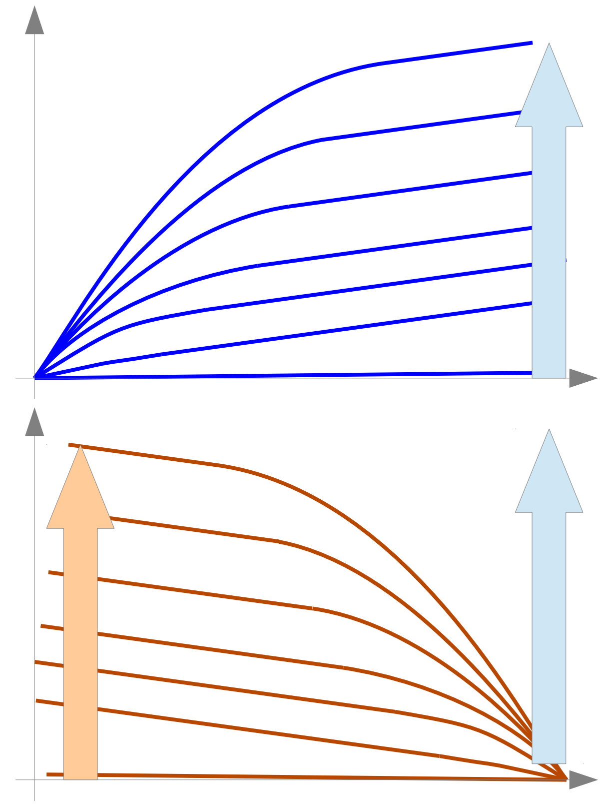


$$\frac{\beta_n}{\beta_p} = 2.0$$

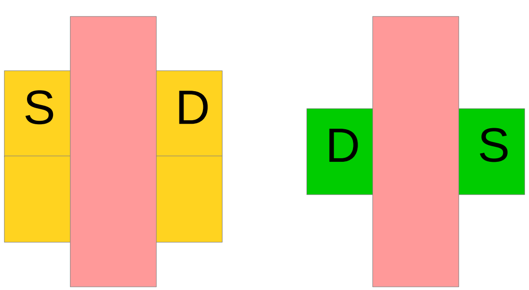
mobility



equal
size
pMOS
nMOS

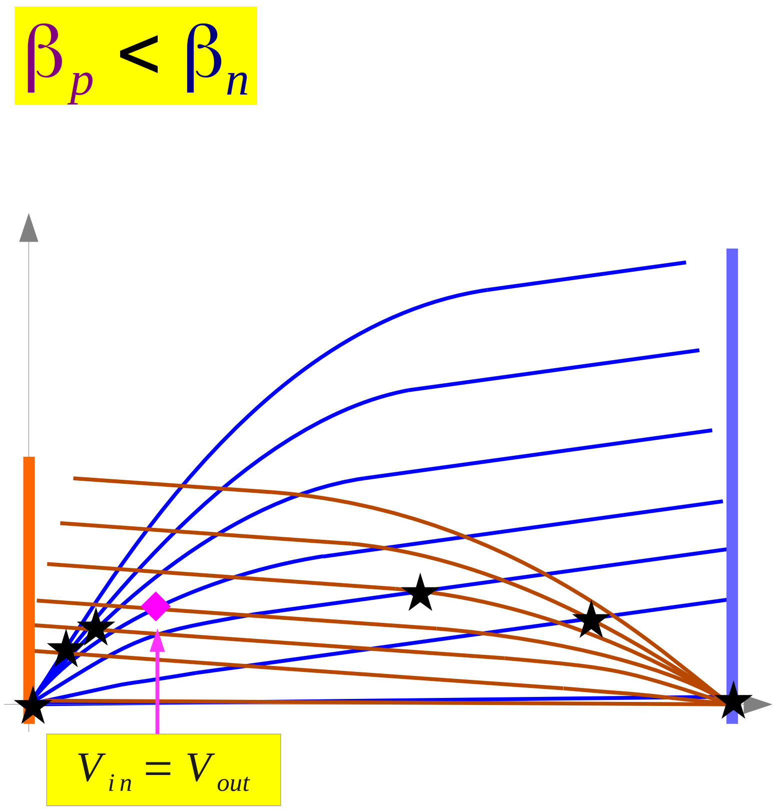


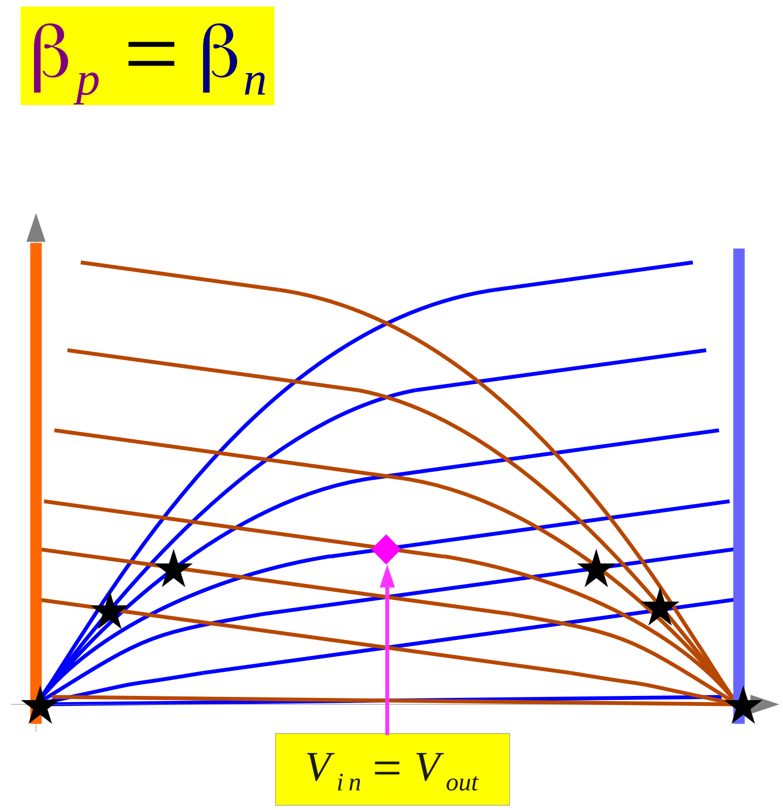
$$\frac{\beta_n}{\beta_p} = 1.0$$



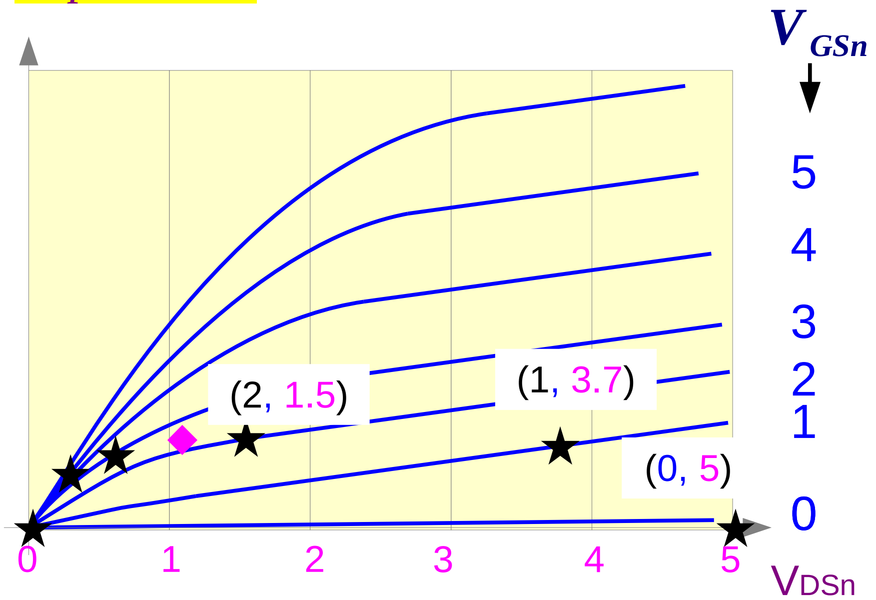
size(pMOS)
two times
larger than
size(nMOS)

Transconductance and Characteristic Curves

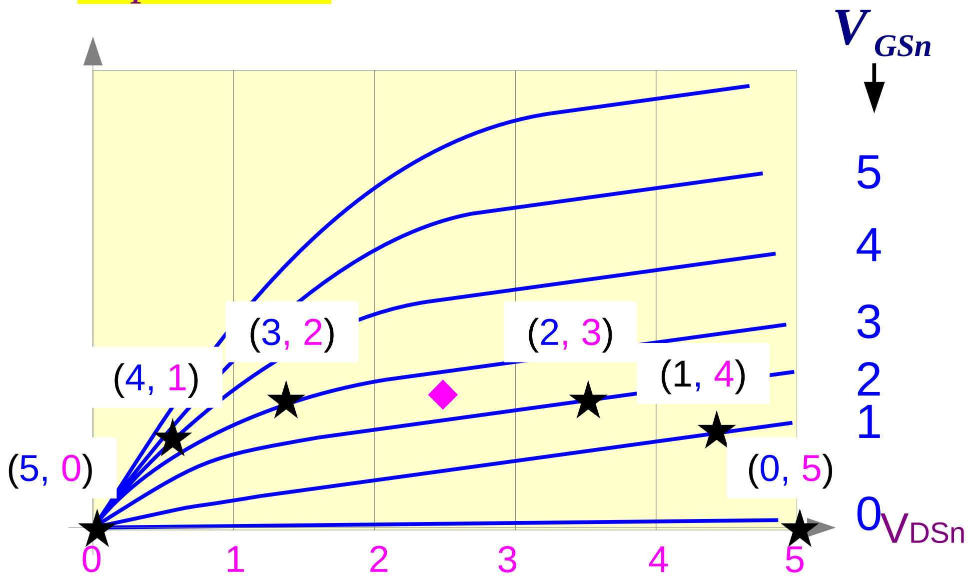




$\beta_p < \beta_n$



$\beta_p = \beta_n$

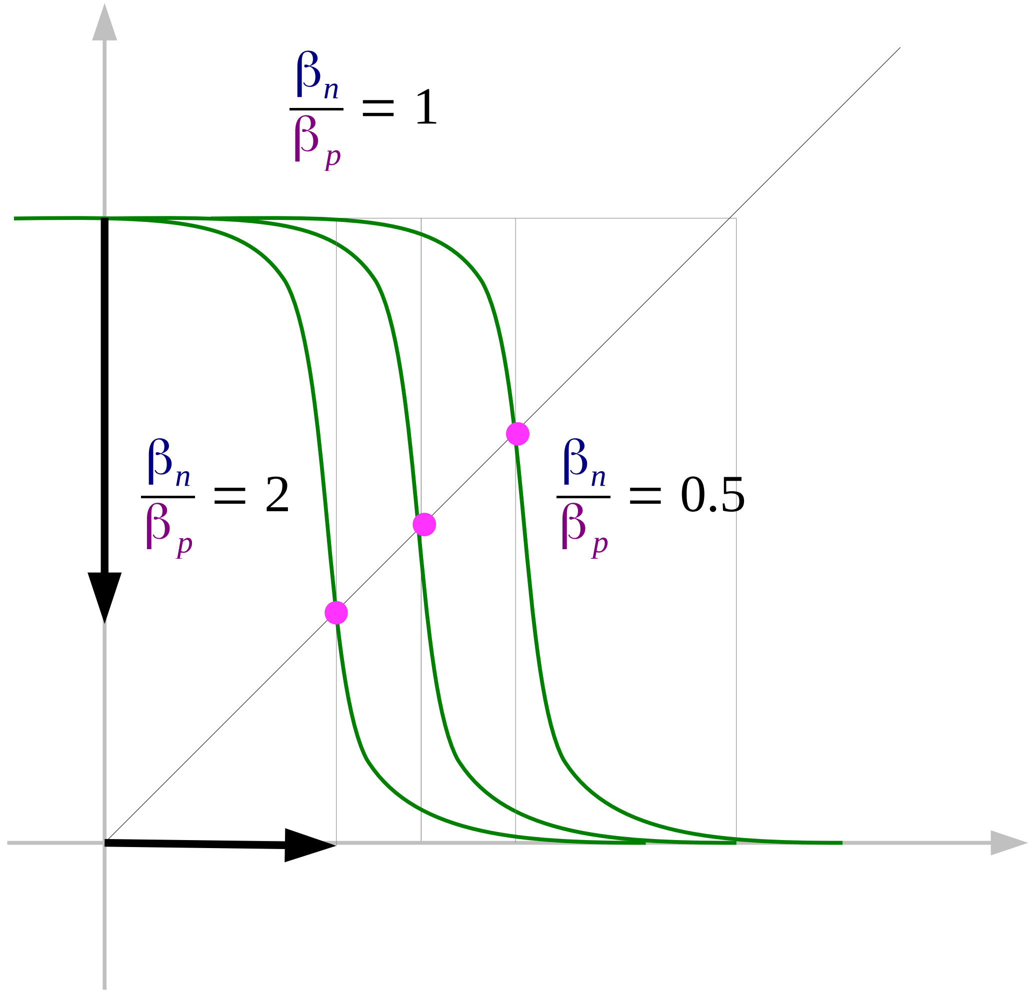


$\beta_p < \beta_n$ ➡ nMOS more easily turns on

V_{out} easily becomes **L**,
for smaller V_{in}

$$\left(V_{GSn}, V_{DSn}\right) = \left(V_{in}, V_{out}\right)$$

Transconductance Ratio and VTC

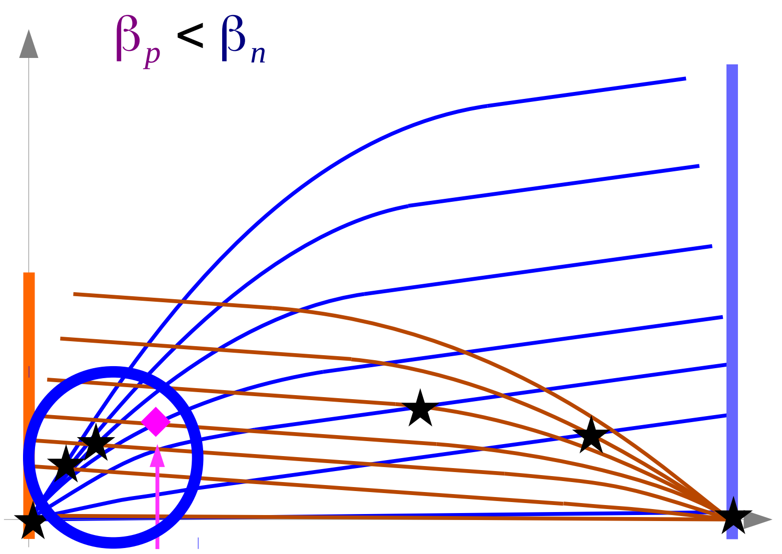


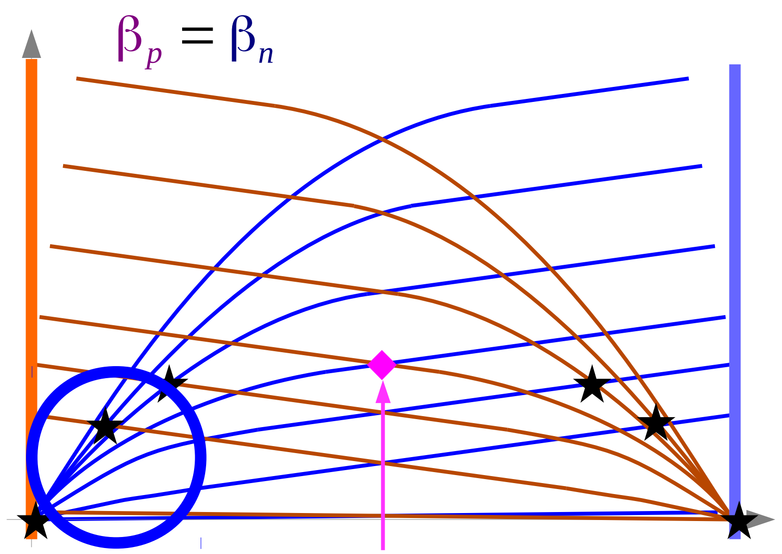
$\beta_n > \beta_p \qquad \left(\frac{\beta_n}{\beta_p} > 1\right)$

nMOS more easily turns on

V_{out} easily becomes L, for a smaller V_{in}

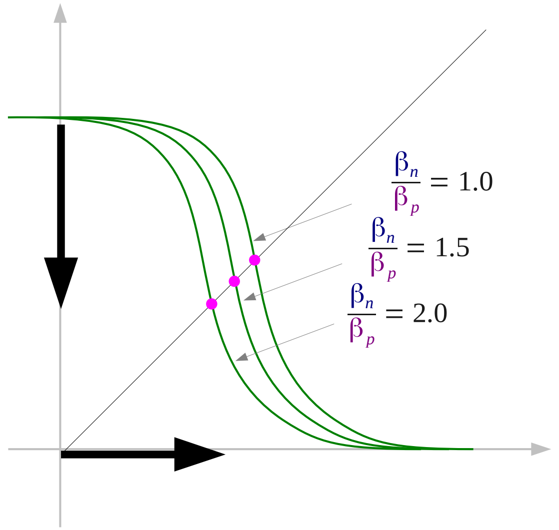
Characteristic Curves and VTC

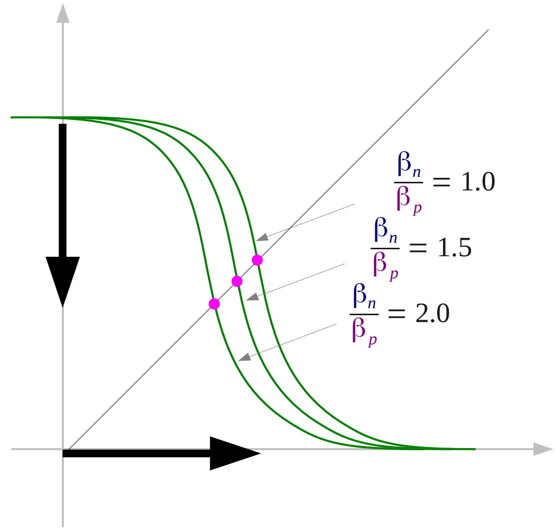




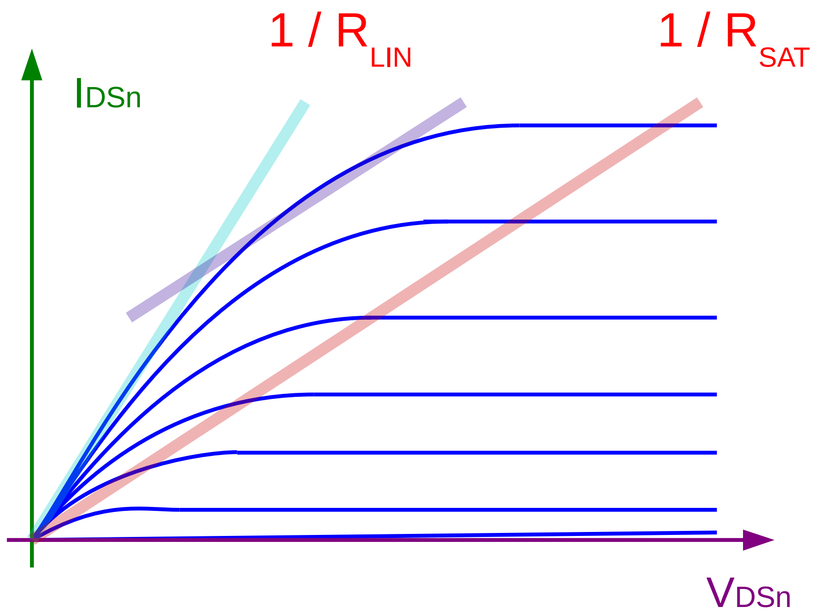
nMOS ON

nMOS ON





Rn



When $V_{GS} > V_t$ and $V_{DS} < (V_{GS} – V_t)$

$$I_d = k'\frac{W}{L}\left[(v_{gs} - v_t)v_{ds} - \frac{1}{2}v_{ds}^2\right]$$

When $V_{GS} > V_t$ and $V_{DS} \geq (V_{GS} – V_t)$

$$I_d = \frac{1}{2}k'\frac{W}{L}(v_{gs} - v_t)^2$$

$$I_d \approx k'\frac{W}{L}[(v_{gs} - v_t)v_{ds}] \qquad v_{ds} < 1$$

R_{LIN}

$$R_n \approx \frac{1}{\beta_n(v_{gs} - v_t)}$$

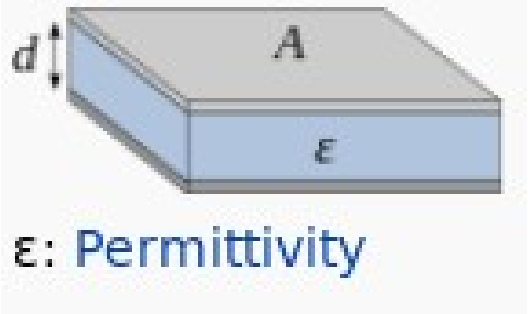
$$R_n \approx \frac{2}{\beta_n[2(v_{gs} - v_t) - v_{ds}]}$$

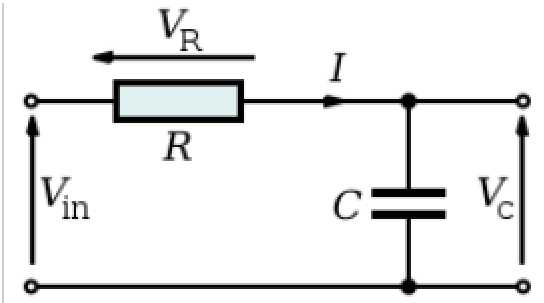
R_{SAT}

$$R_n \approx \frac{v_{ds}}{\beta_n[(v_{gs} - v_t)^2]}$$

Capacitance

$$\varepsilon A / d$$





Series RC circuit

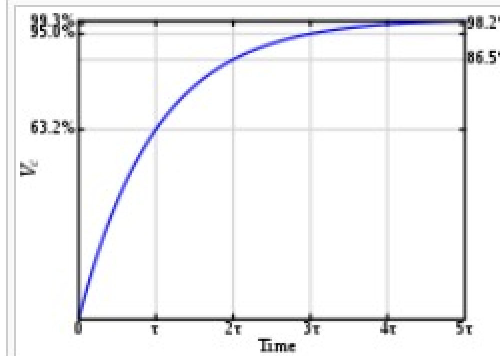
By viewing the circuit as a voltage divider, the voltage across the capacitor is:

$$V_C(s) = \frac{1/Cs}{R + 1/Cs} V_{in}(s) = \frac{1}{1 + RCs} V_{in}(s)$$

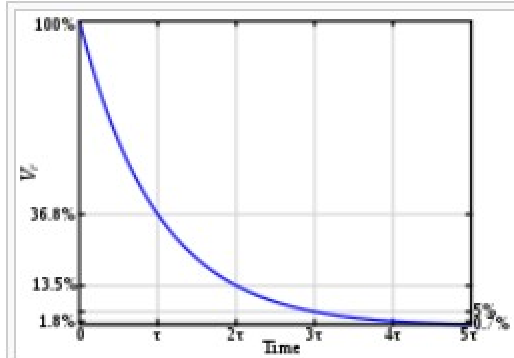
and the voltage across the resistor is:

$$V_R(s) = \frac{R}{R + 1/Cs} V_{in}(s) = \frac{RCs}{1 + RCs} V_{in}(s).$$

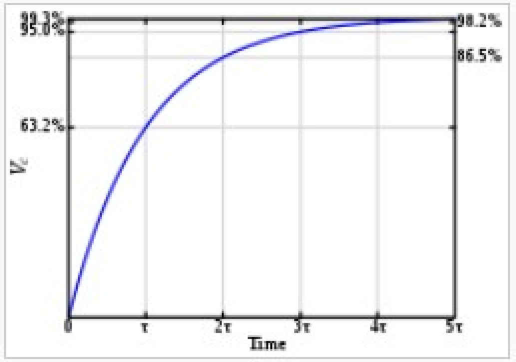
$$V_C(t) = V\left(1 - e^{-t/RC}\right)$$
$$V_R(t) = V e^{-t/RC}.$$



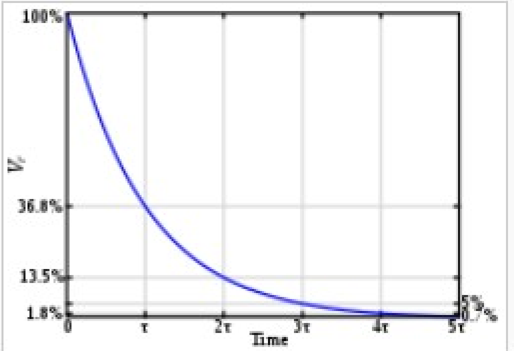
Capacitor voltage step-response.



Resistor voltage step-response.



Capacitor voltage step-response.



Resistor voltage step-response.

Thus, the voltage across the capacitor tends towards *V* as time passes, while the voltage across the resistor tends towards 0, as shown in the figures. This is in keeping with the intuitive point that the capacitor will be charging from the supply voltage as time passes, and will eventually be fully charged.

These equations show that a series RC circuit has a time constant, usually denoted $\tau = RC$ being the time it takes the voltage across the component to either rise (across C) or fall (across R) to within $1/e$ of its final value. That is, τ is the time it takes V_C to reach $V(1 - 1/e)$ and V_R to reach $V(1/e)$.

The rate of change is a *fractional* $\left(1 - \frac{1}{e}\right)$ per τ. Thus, in going from $t = N\tau$ to $t = (N+1)\tau$, the voltage will have moved about 63.2% of the way from its level at $t = N\tau$ toward its final value. So C will be charged to about 63.2% after τ, and essentially fully charged (99.3%) after about 5τ. When the voltage source is replaced with a short-circuit, with C fully charged, the voltage across C drops exponentially with *t* from V towards 0. C will be discharged to about 36.8% after τ, and essentially fully discharged (0.7%) after about 5τ. Note that the current, I, in the circuit behaves as the voltage across R does, via Ohm's Law.

Simple Model

v_{gs}

v_{ds}

I_d

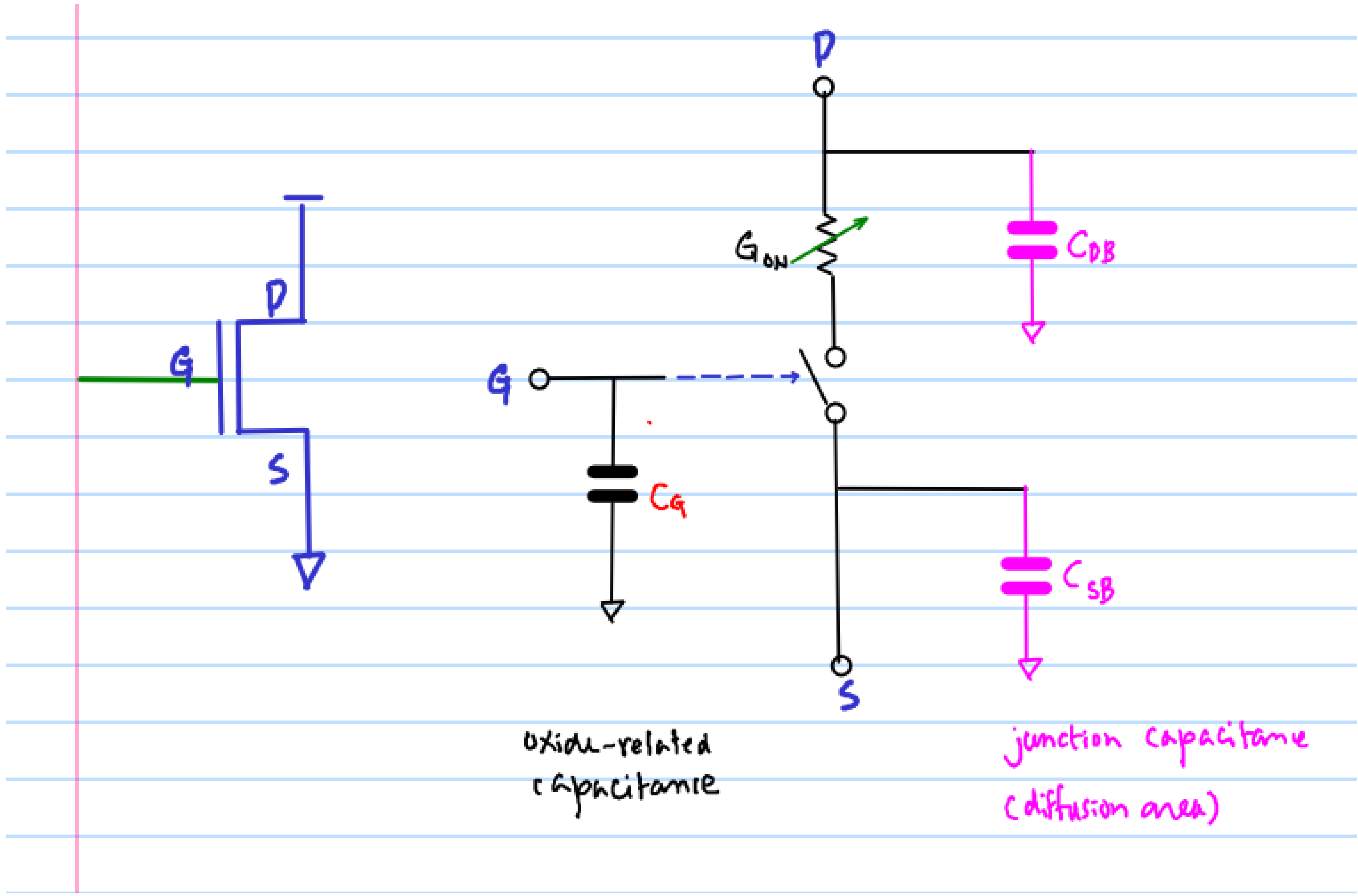
$$I_d = k'\frac{W}{L}\left[(v_{gs} - v_t)v_{ds} - \frac{1}{2}v_{ds}^2\right]$$

$$I_d = \frac{1}{2}k'\frac{W}{L}(v_{gs} - v_t)^2$$

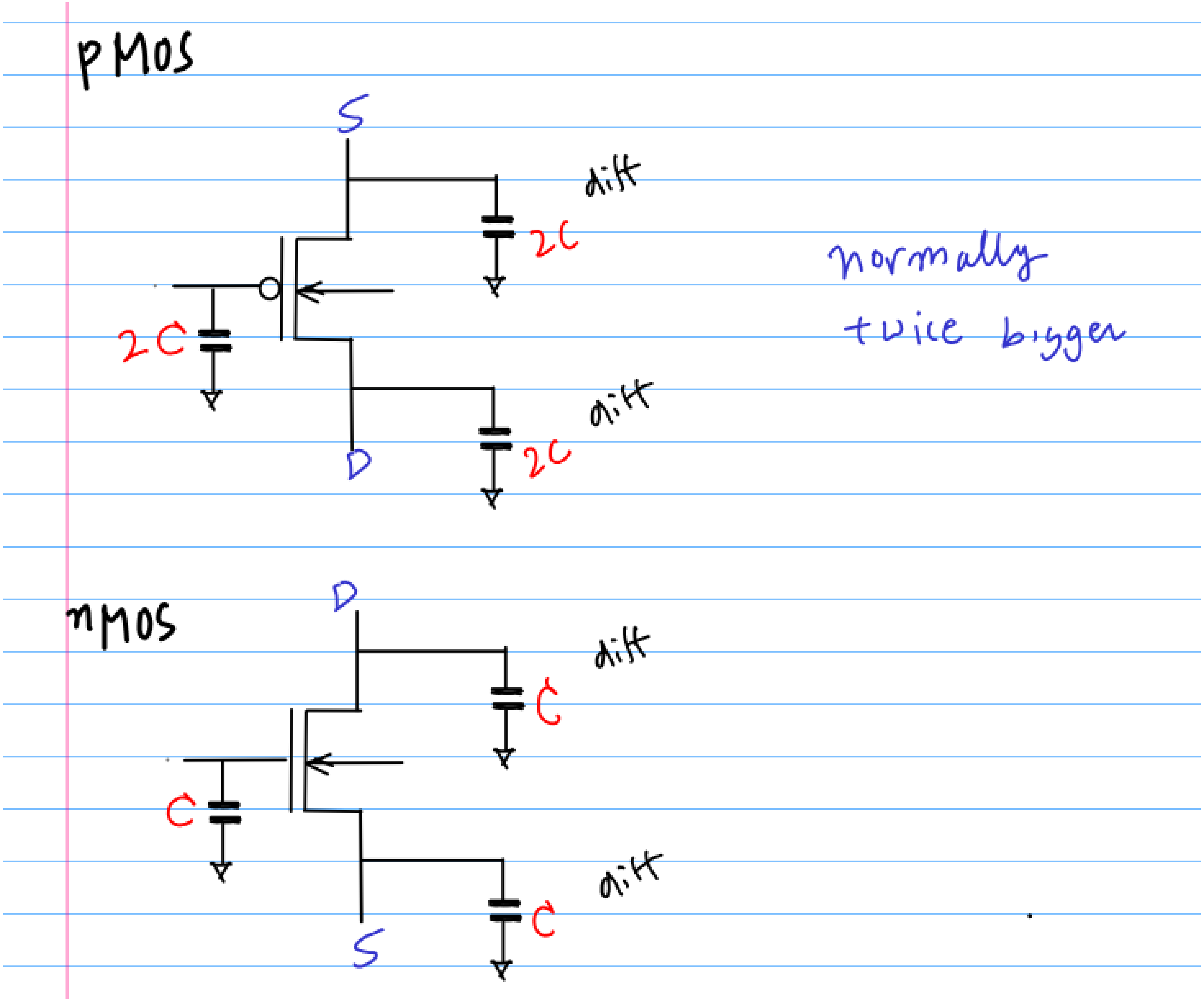
v_t, k' } measured

$\frac{W}{L}$ } determined by the layout tool used

Simple Model



Transistor Parasitics



Transistor Parasitics

C_g gate capacitance

C_{gs} C_{ds} source/drain overlap capacitance

Wire Parasitics

wires
vias
transistors

Spice Model

wires
vias
transistors

Design Rule

wires
vias
transistors

References

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[2] http://www.allaboutcircuits.com/
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[4] N. Weste, D. Harris, “CMOS VLSI Design: A Circuits and Systems Perspective”
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[10] https://en.wikiversity.org/wiki/The_necessities_in_Computer_Organization
[11] https://en.wikiversity.org/wiki/Verilog_programming_in_plain_view