

MetaStable State

Copyright (c) 2011-2013 Young W. Lim.

Permission is granted to copy, distribute and/or modify this document under the terms of the GNU Free Documentation License, Version 1.2 or any later version published by the Free Software Foundation; with no Invariant Sections, no Front-Cover Texts, and no Back-Cover Texts. A copy of the license is included in the section entitled "GNU Free Documentation License".

Please send corrections (or suggestions) to youngwlim@hotmail.com.

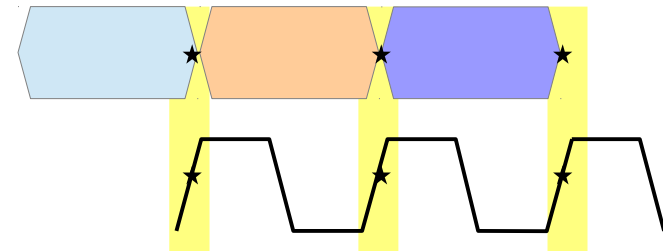
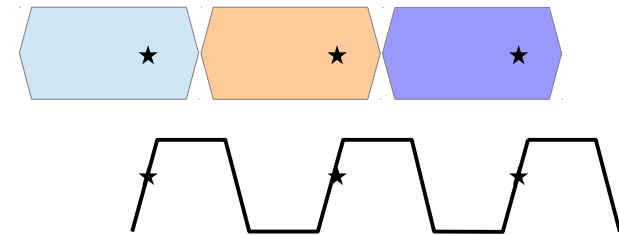
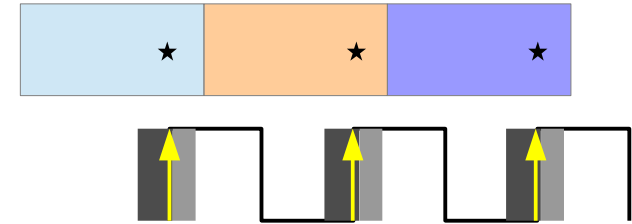
This document was produced by using OpenOffice and Octave.

Metastability

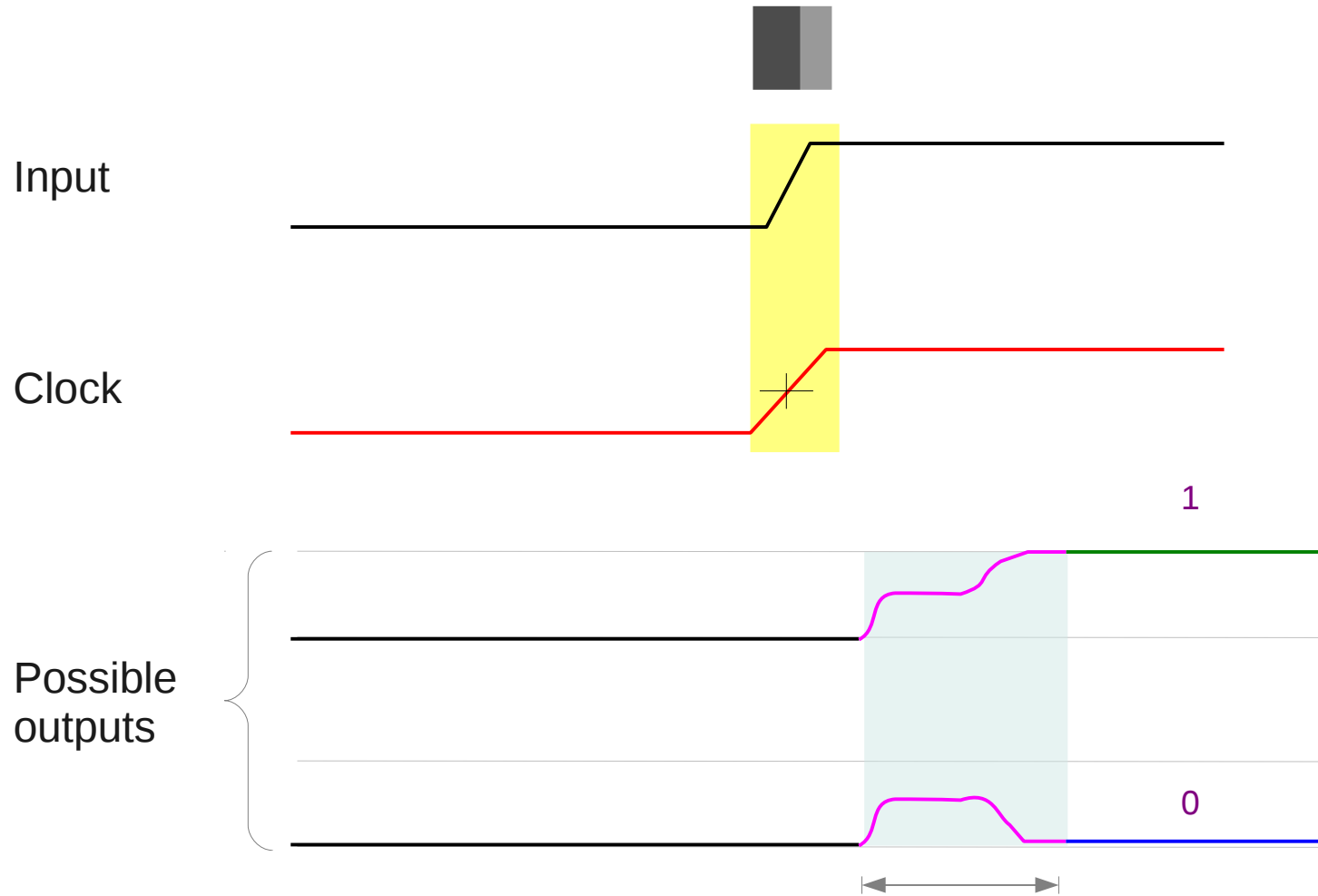
Metastability in electronics is the ability of a digital electronic system **to persist for an unbounded time** in an **unstable equilibrium** or **metastable state**.

In **metastable states**, the circuit may be **unable to settle** into a stable '0' or '1' logic level **within the time** required for proper circuit operation.

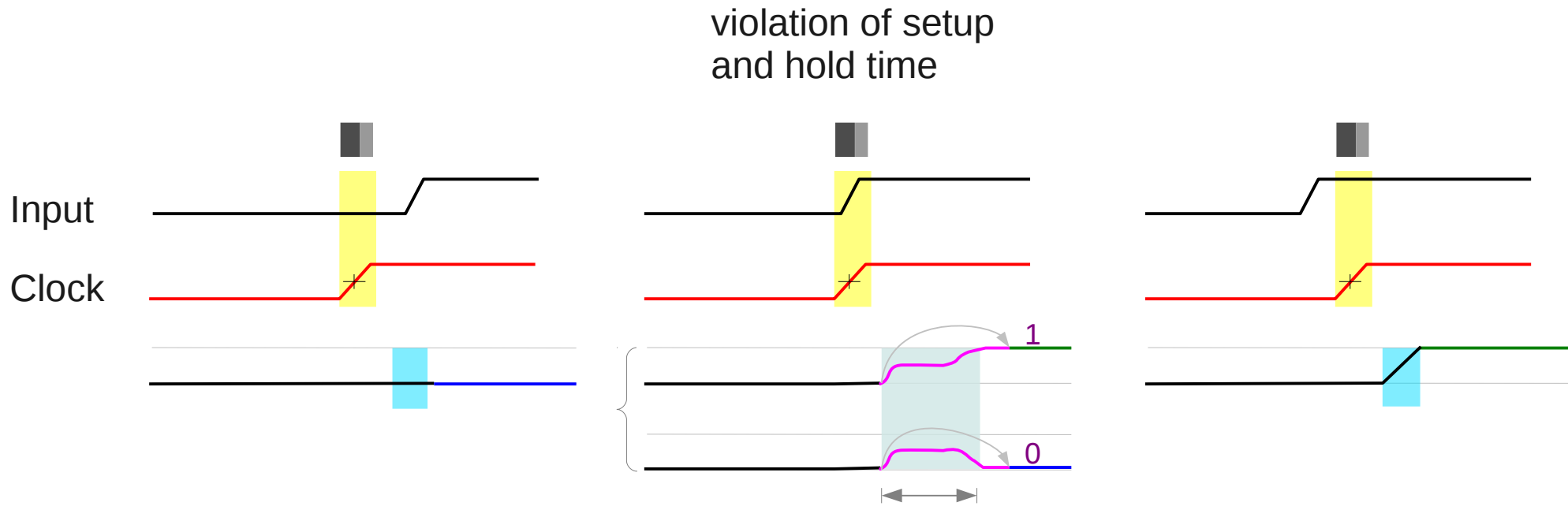
As a result, the circuit can act in **unpredictable ways**, and may lead to a system failure, sometimes referred to as a "glitch".



Possible Metastable Outputs

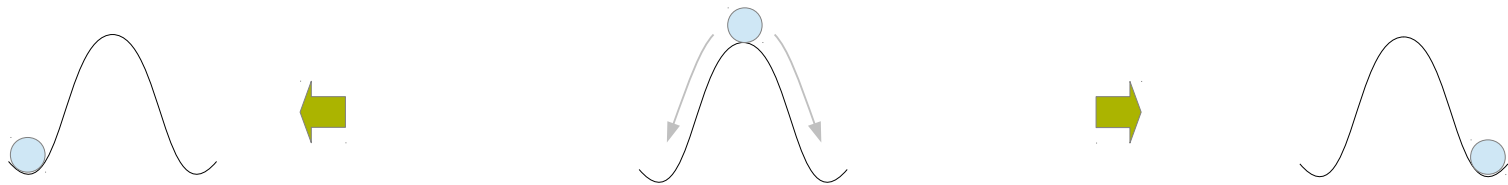


Metastability

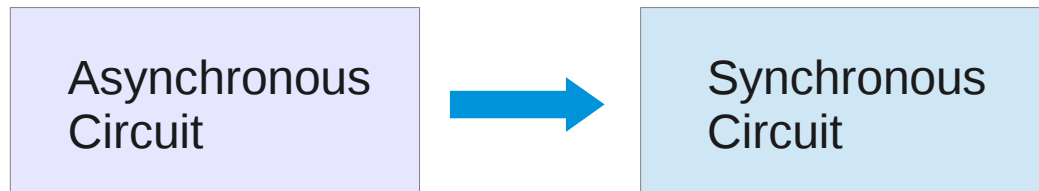


non-deterministic period
but longer than the normal
clock-to-output delay

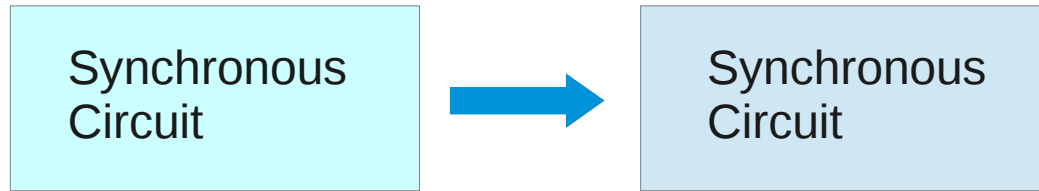
an electronic noise can
make either 0 or 1 state



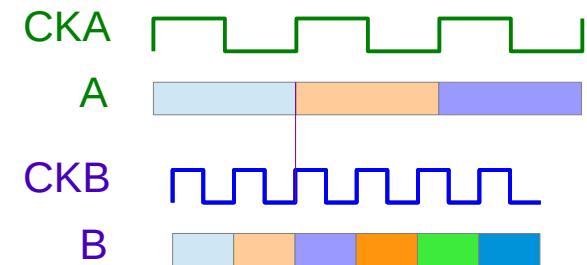
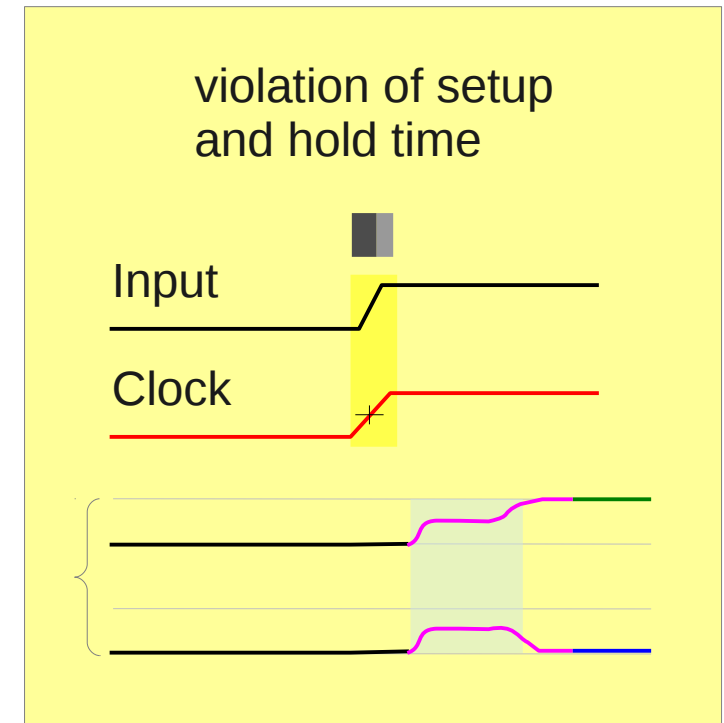
Causes of Metastability



Push button



unrelated clock domain



Resolution Time

References

- [1] <http://en.wikipedia.org/>
- [2] M. M. Mano, C. R. Kime, "Logic and Computer Design Fundamentals", 4th ed.
- [3] J. Stephenson, Understanding Metastability in FPGAs. Altera Corporation white paper. July 2009.