CMOS Delay-7 (H.8)
Delay Model

20170210

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References

Some Figures from the following sites

[1] http://pages.hmc.edu/harris/cmosvlsi/4e/index.html
Weste & Harris Book Site

[2] Introduction to VLSI Circuits and Systems, Uyemura

[2] en.wikipedia.org

MODEL

β : Device Transconductance Parameter
k : Process Transconductance Parameter
μ : Electron / Hole Mobility

pMOS $\beta_p = k'_p \left(\frac{W}{L}\right)_p$ $k'_p = \mu_p C_{ox}$ $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$

nMOS $\beta_n = k'_n \left(\frac{W}{L}\right)_n$ $k'_n = \mu_n C_{ox}$ $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$

pMOS $\beta_p = \mu_p \frac{\epsilon_{ox}}{t_{ox}} \left(\frac{W}{L}\right)_p$

nMOS $\beta_n = \mu_n \frac{\epsilon_{ox}}{t_{ox}} \left(\frac{W}{L}\right)_n$

Saturation Current

$I_{dp} = \frac{\beta_p}{2} (V_{GSn} - |V_{Tp}|)^2$ $V_{Tp} < 0$

$I_{dn} = \frac{\beta_n}{2} (V_{GSn} - V_{Tn})^2$ $V_{Tn} > 0$

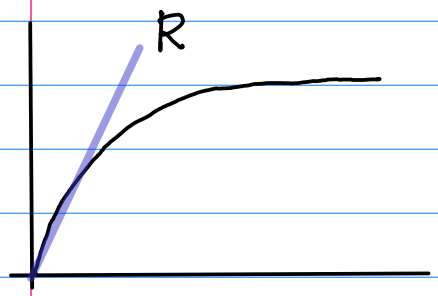
MODEL

$$\frac{\beta_n}{\beta_p} = \frac{k'_n \left(\frac{W}{L}\right)_n}{k'_p \left(\frac{W}{L}\right)_p}$$

$$\frac{k'_n}{k'_p} = 2 \sim 3$$

$$\frac{k'_n}{k'_p} = \frac{\mu_n}{\mu_p} = r$$

$$\frac{\beta_n}{\beta_p} = \frac{k'_n \left(\frac{W}{L}\right)_n}{k'_p \left(\frac{W}{L}\right)_p}$$



LIN

$$R_n = \frac{1}{\beta_n (V_{DD} - V_{Tn})}$$

$$R_p = \frac{1}{\beta_n (V_{DD} - V_{Tn})}$$

fall time t_f $\quad \tau_n = R_n C_{out}$

rise time t_r $\quad \tau_p = R_p C_{out}$

$$C_{out} = C_{para} + C_L$$

MODEL

fall time	$t_f = 2.2\,\tau_n = \ln 9\,\tau_n$	$0.9\,V_{DD} \rightarrow 0.1\,V_{DD}$
rise time	$t_r = 2.2\,\tau_p = \ln 9\,\tau_p$	$0.1\,V_{DD} \rightarrow 0.9\,V_{DD}$
propagation delay time	$t_p = \frac{1}{2}(t_{pf} + t_{pr})$ $= 0.35(t_{pf} + t_{pr})$	$0.5\,V_{DD} \rightarrow 0.5\,V_{DD}$
propagation fall time	$t_{pf} = 0.7\,\tau_n = \ln 2\,\tau_n$	$V_{DD} \rightarrow 0.5\,V_{DD}$
propagation rise time	$t_{pr} = 0.7\,\tau_p = \ln 2\,\tau_p$	$0 \rightarrow 0.5\,V_{DD}$

$$\tau_n = R_n (C_{para} + C_L)$$

$$\tau_p = R_p (C_{para} + C_L)$$

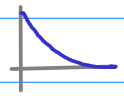
$$C_{out} = C_{para} + C_L$$

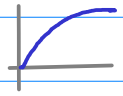
$$\left(\frac{W}{L}\right)_p = r\left(\frac{W}{L}\right)_n$$

$$r = \frac{\mu_n}{\mu_p} = \frac{k'_n}{k'_p} > 1$$

$$R_n = R_p = R = \frac{1}{\beta(V_{DD} - V_T)}$$

$$\begin{cases} V_{out}(t) = V_{DD}\left(1 - e^{-t/\tau}\right) \\ V_{out}(t) = V_{DD}\, e^{-t/\tau} \end{cases}$$





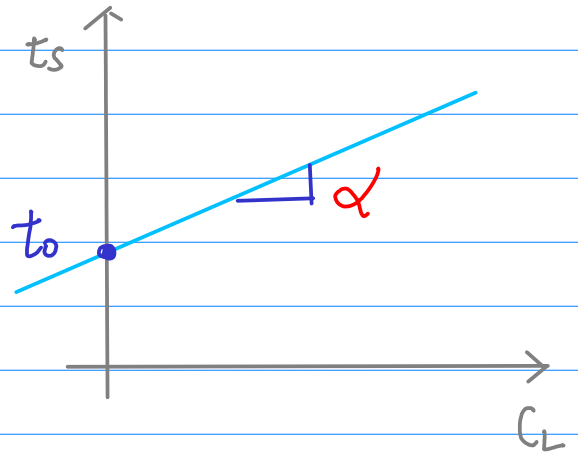
$$\tau = R C_{out} = R\left(C_{par} + C_L\right)$$

Generic Switching Delay

$$t_s = t_0 + \alpha C_L \quad \Rightarrow \quad t_s = t_r = t_f$$

Generic Switching Delay

$$t_s = t_0 + \alpha C_L$$



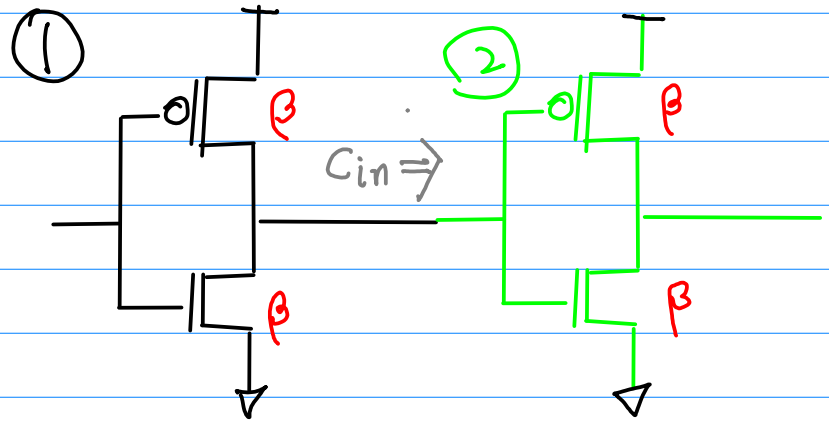
t_0 : zero delay

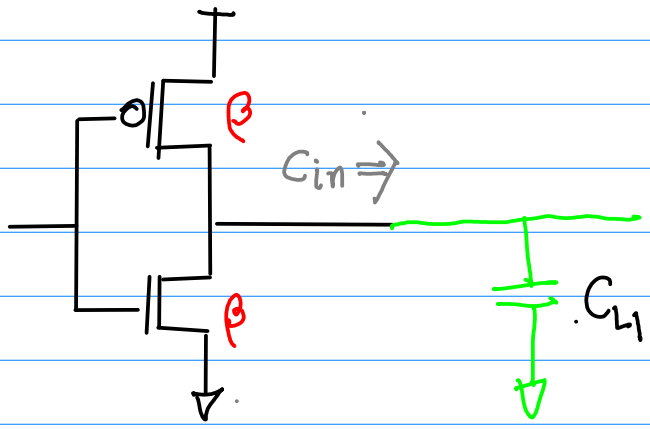
α : slope

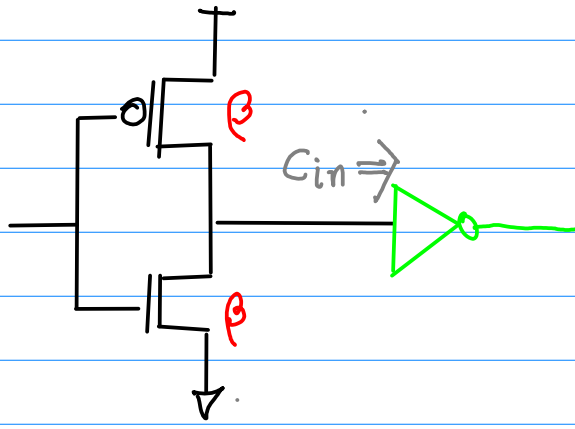
$$t \approx RC$$

$$\alpha \propto \frac{1}{\beta(V_{DD} - V_T)}$$

C_L







reference case $C_{in} = C_{L1}$

Generic Switching Delay of (1)

$$t_{s1} = t_0 + \alpha C_{L1}$$

$$= t_0 + \alpha C_{in}$$

$$C_{in} = C_{Gn} + C_{Gp}$$

$$= C_{ox}(A_{Gn} + A_{Gp}) \qquad A: \text{gate area}$$

the channel length L assumed

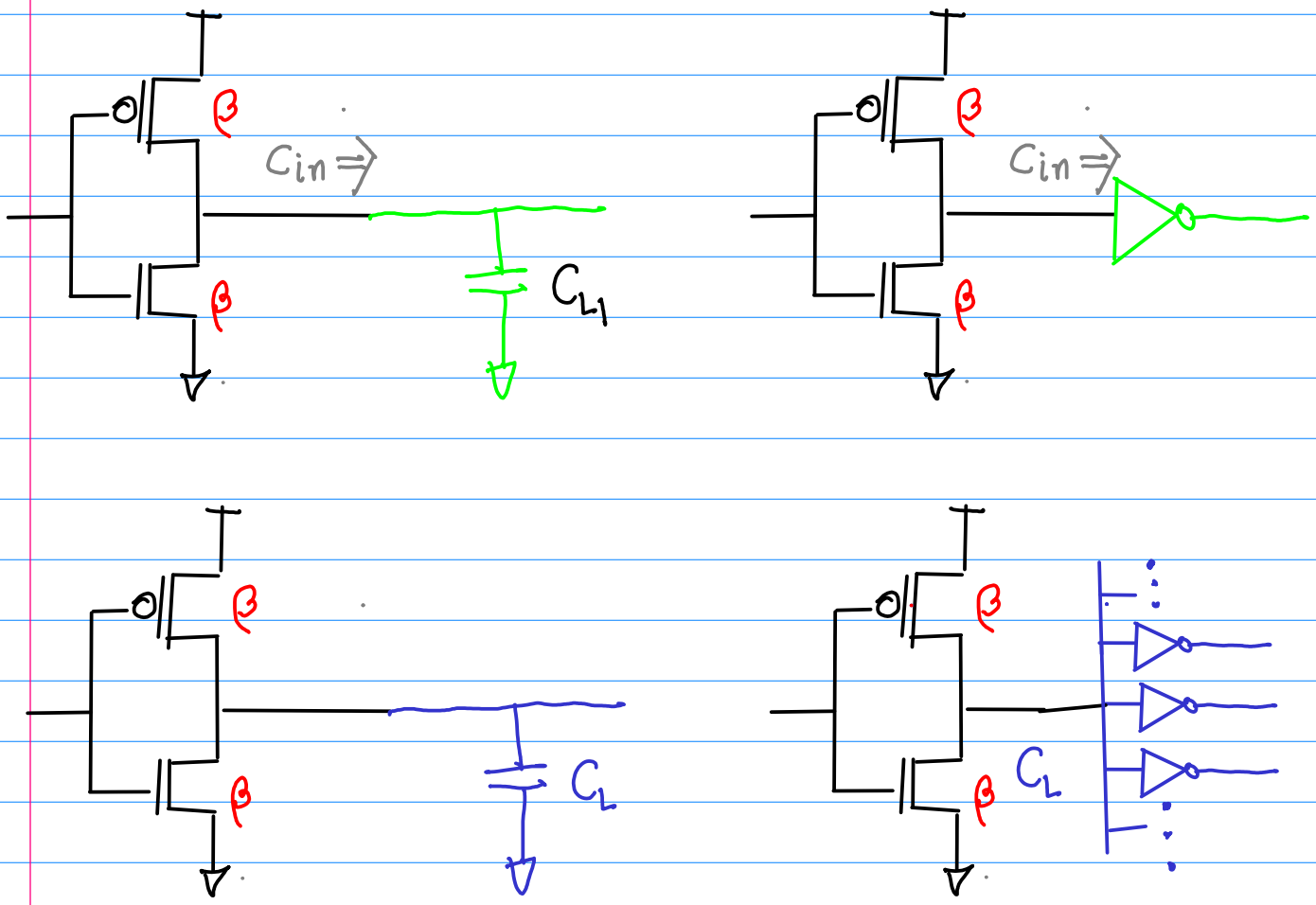
$$C_{in} = C_{ox} L (W_n + W_p)$$

$$= C_{ox} L (W_n + r W_p)$$

$$= C_{ox} L W_n \cdot (1 + r)$$

$$= C_{Gn} (1 + r)$$

When $C_L \gg C_{in}$



to minimize t_s

$\alpha \downarrow \Rightarrow R \downarrow \Rightarrow \beta \uparrow \Rightarrow$ bigger size

speed v.s. area tradeoff

$t_s = t_0 + \alpha C_L \quad t \approx RC$

$\alpha \propto \frac{1}{\beta(V_{DD} - V_T)}$

C_L

to minimize t_s

$\alpha \downarrow \Rightarrow R \downarrow \Rightarrow \beta \uparrow \Rightarrow$ bigger size

speed v.s. area tradeoff

Scaling Factor S

$$\beta' = S\beta$$

$$R' = \frac{R}{S}$$

$$\alpha' = \frac{\alpha}{S}$$

$$t_s = t_0 + \frac{\alpha}{S} C_L$$

($\frac{\alpha}{S}$: R, C_L: C)

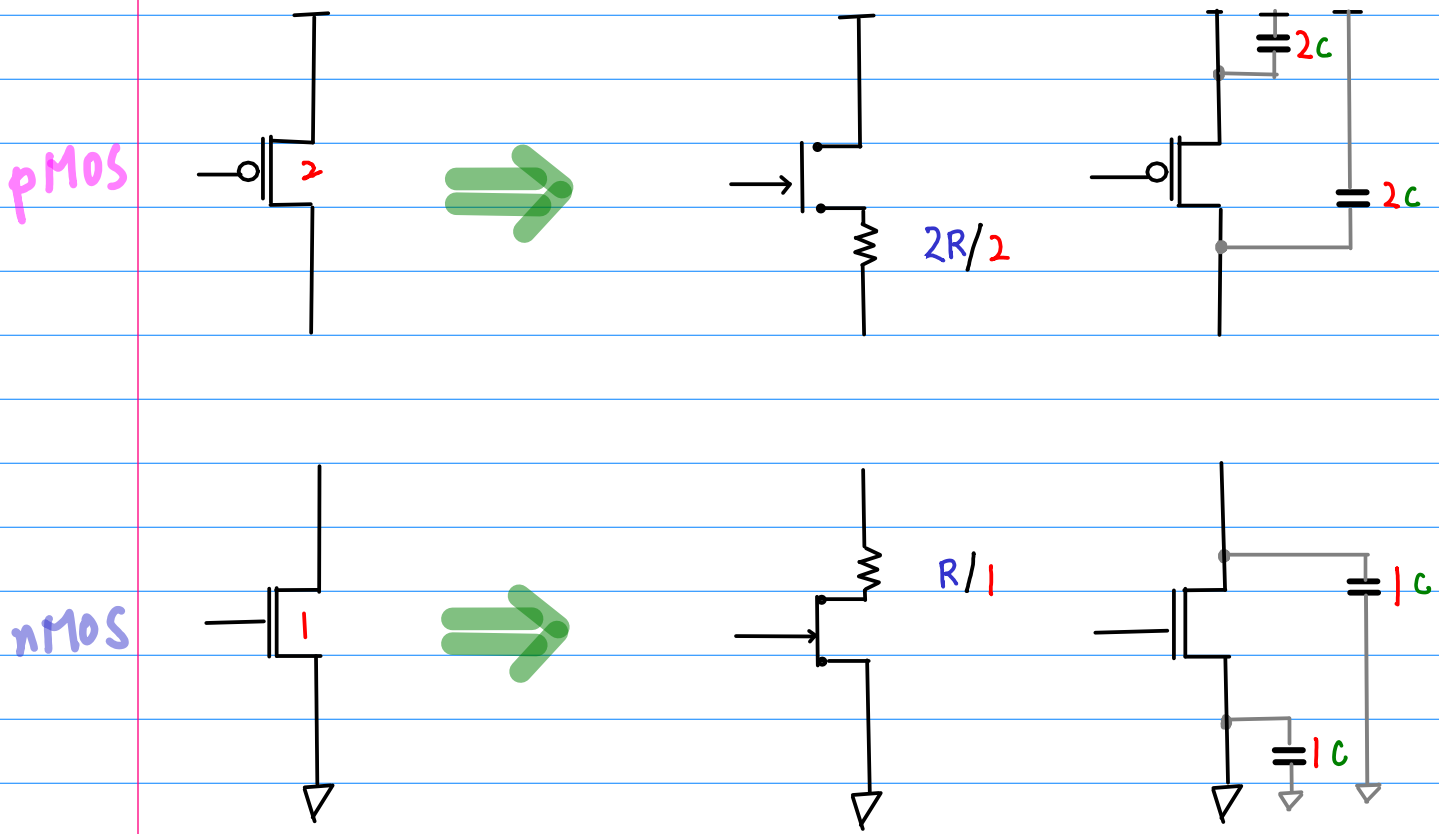
Compensation Factor $\frac{1}{S}$

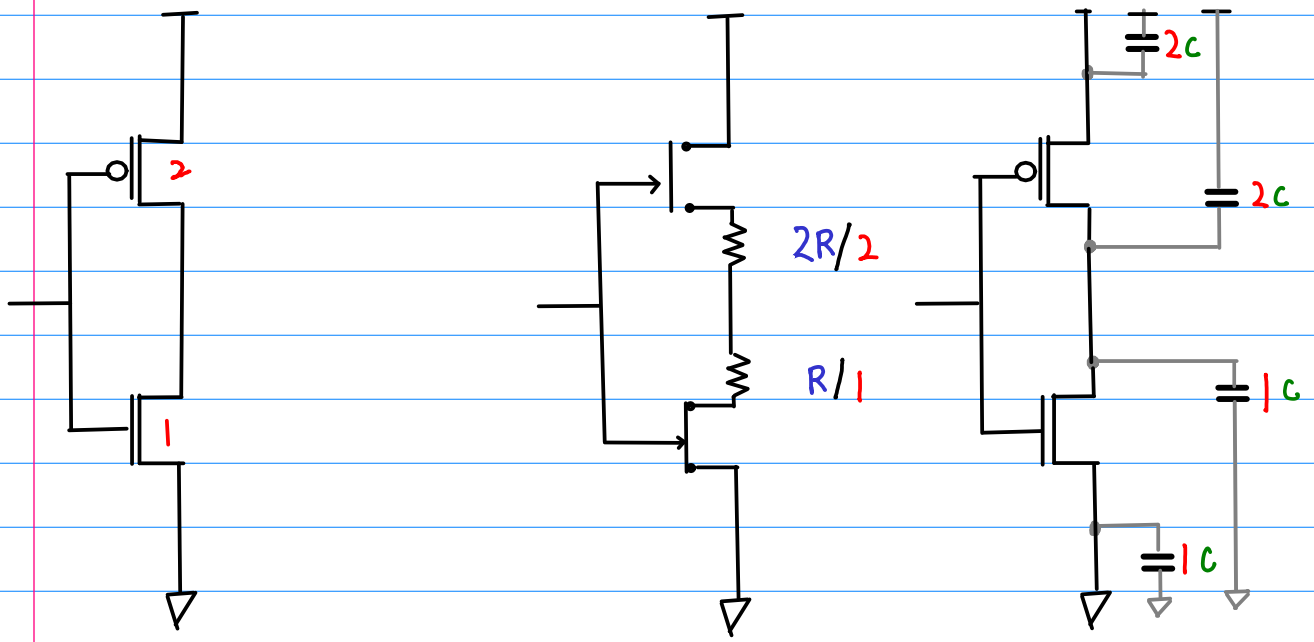
enables a NOT gate drive larger values of C_L

If $C_L = S\, C_{in}$ (increased by the scaling factor S)

then the switching time is the same

RC Delay Model

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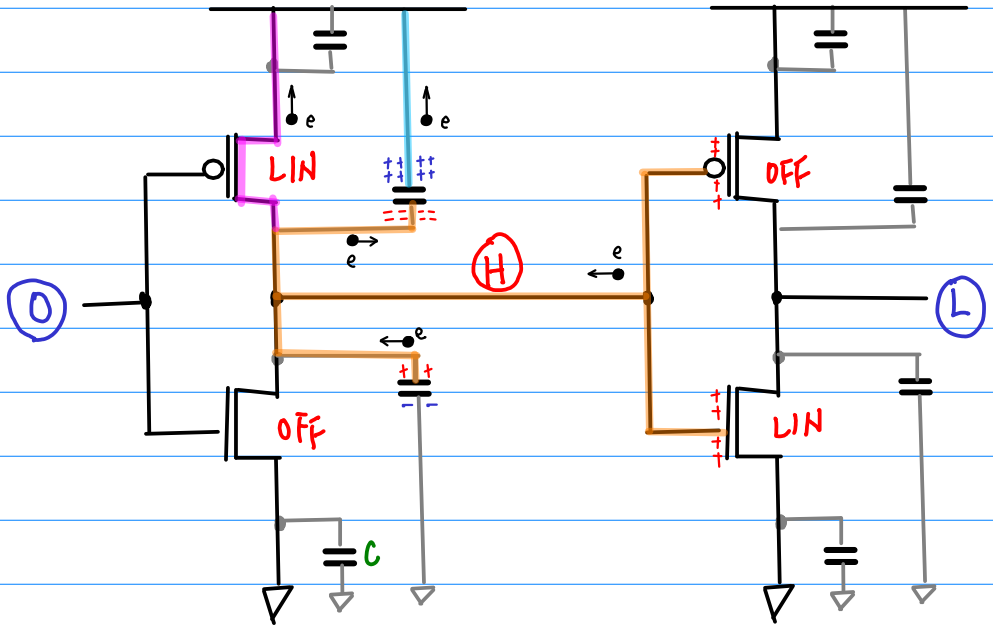
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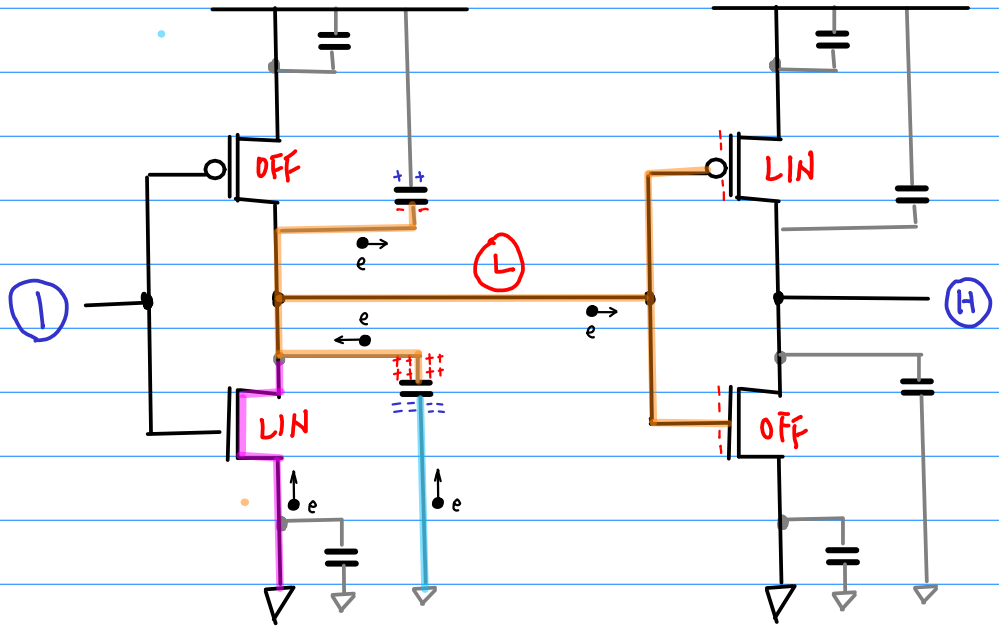
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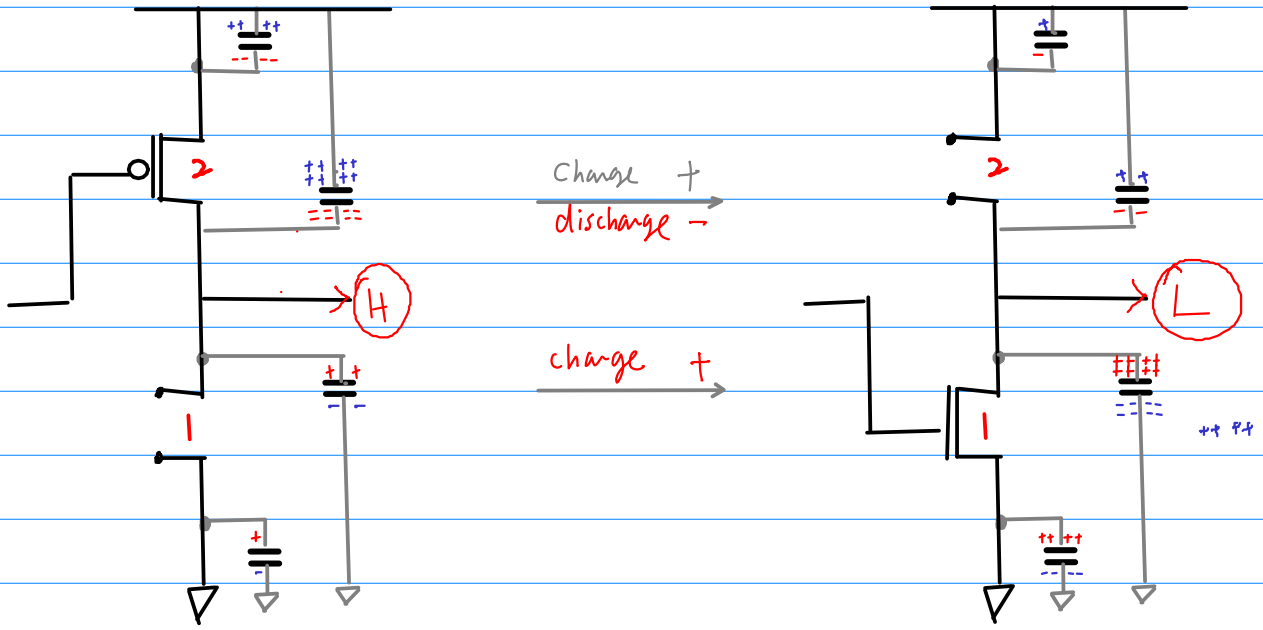
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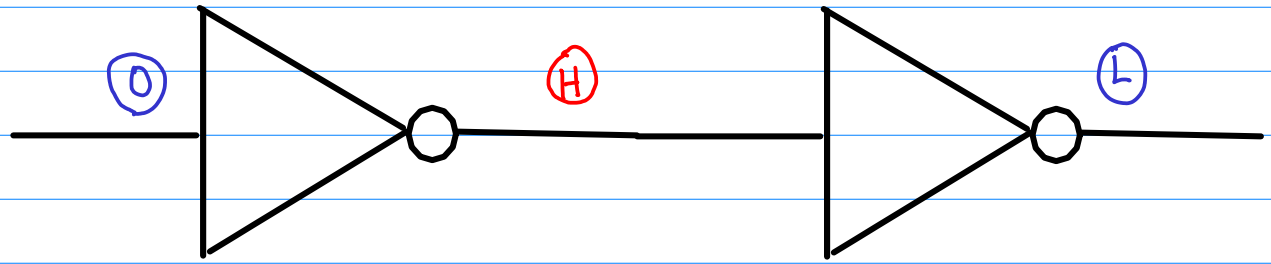
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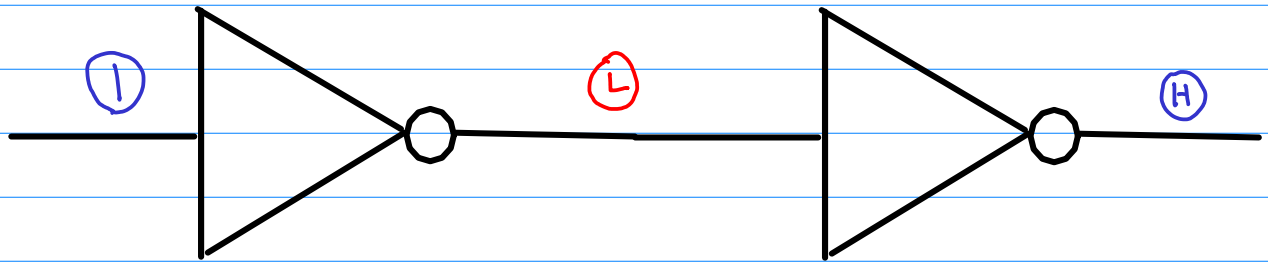
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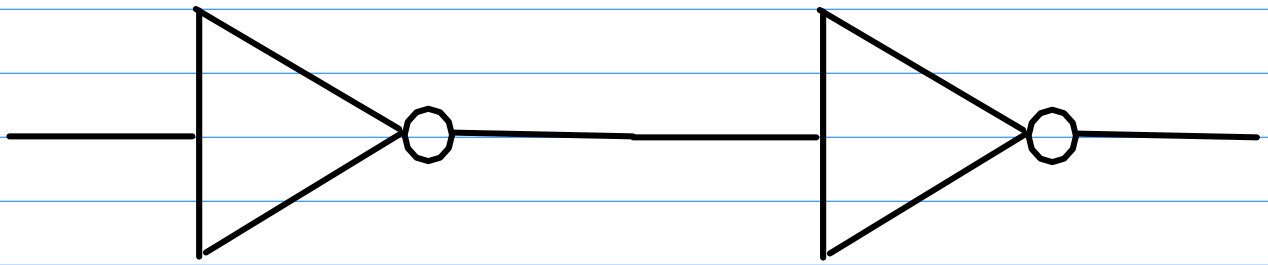

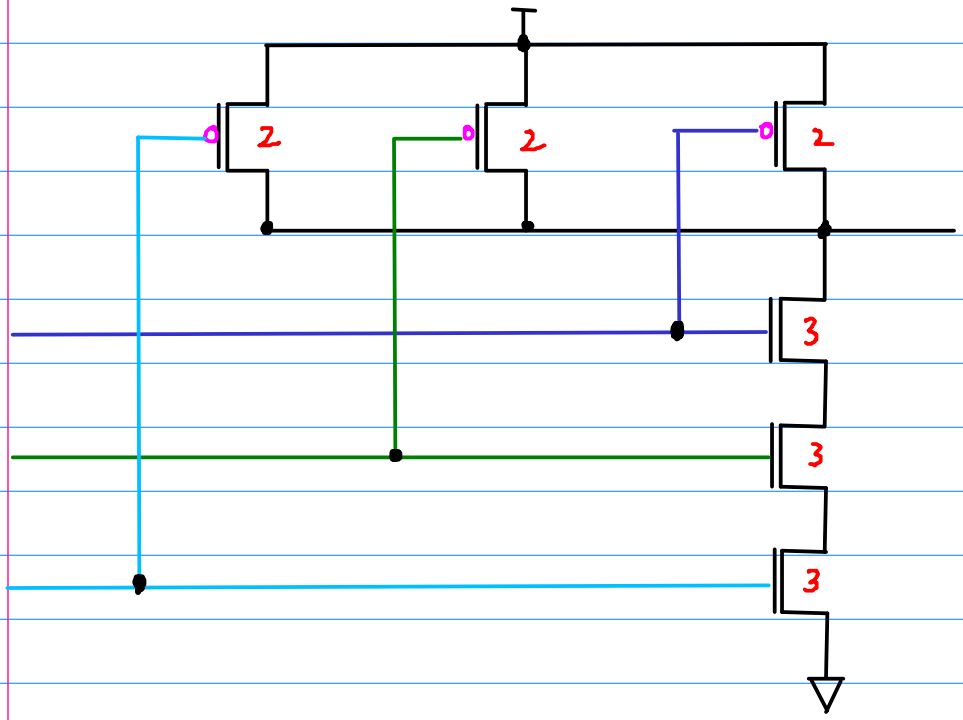
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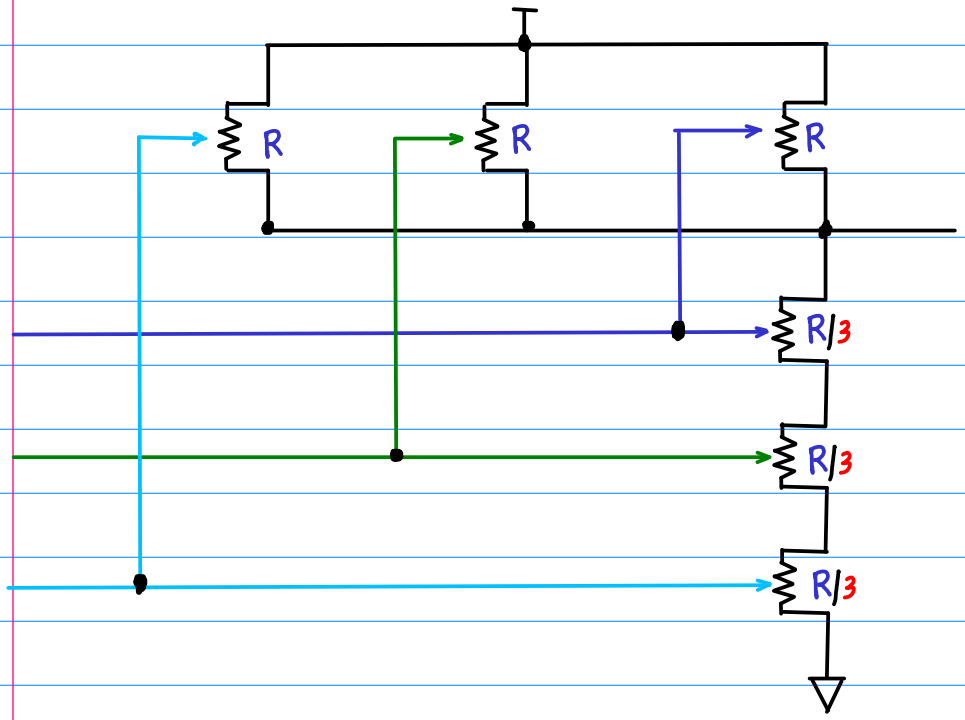
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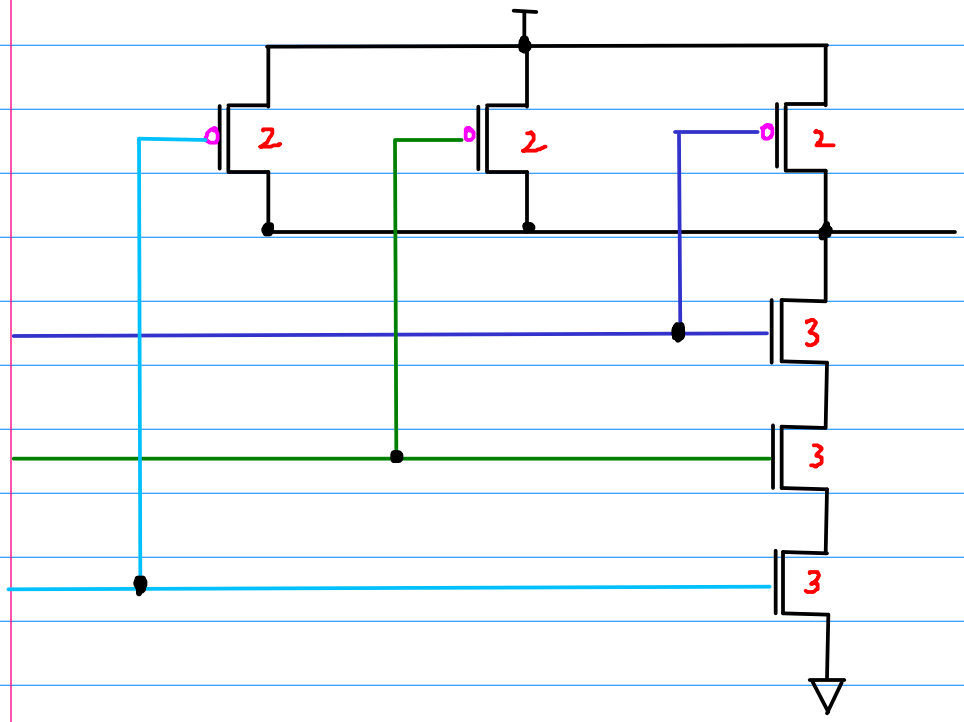
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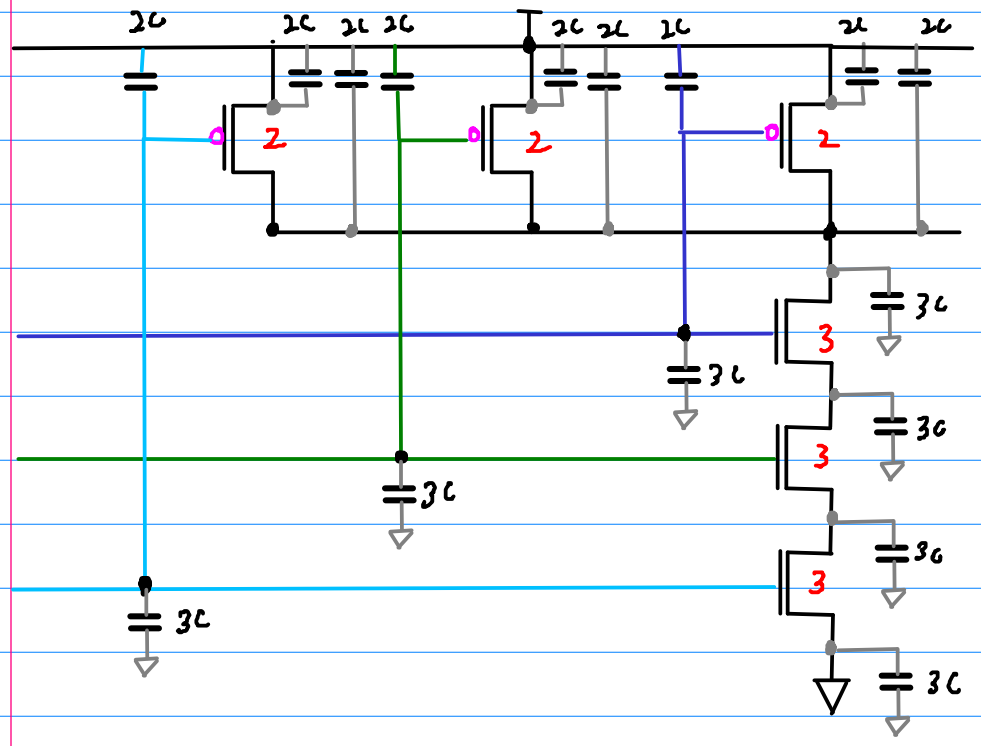
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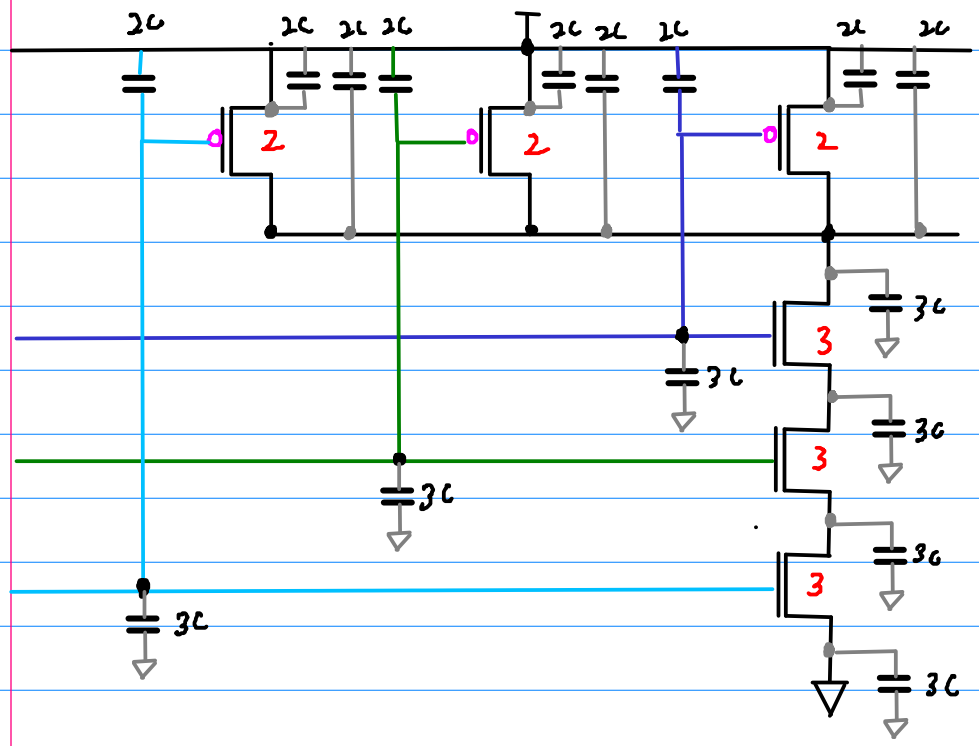
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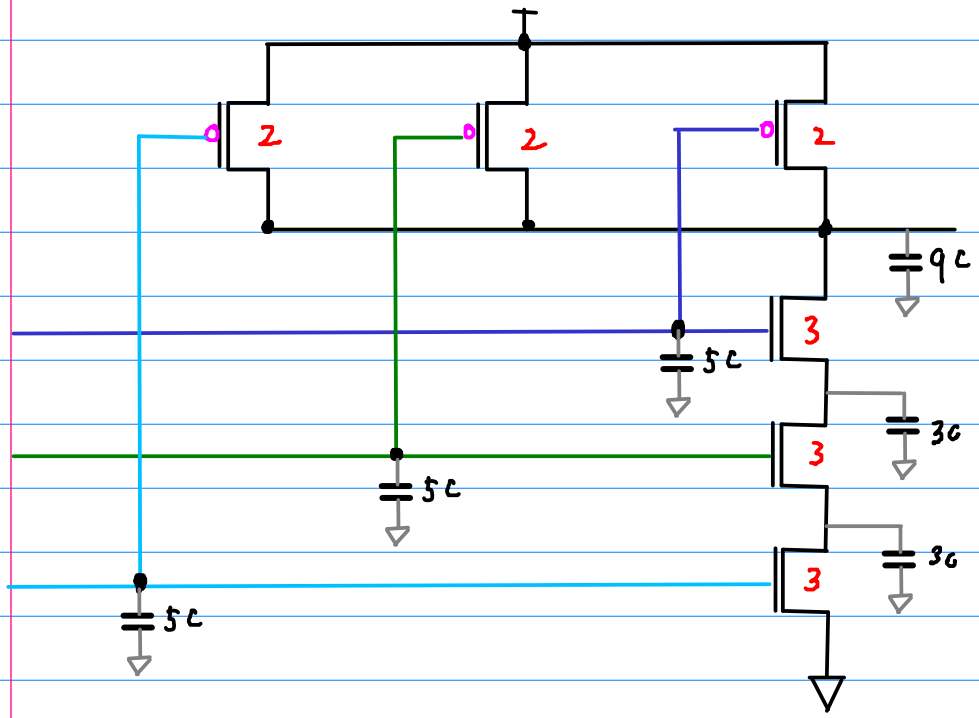
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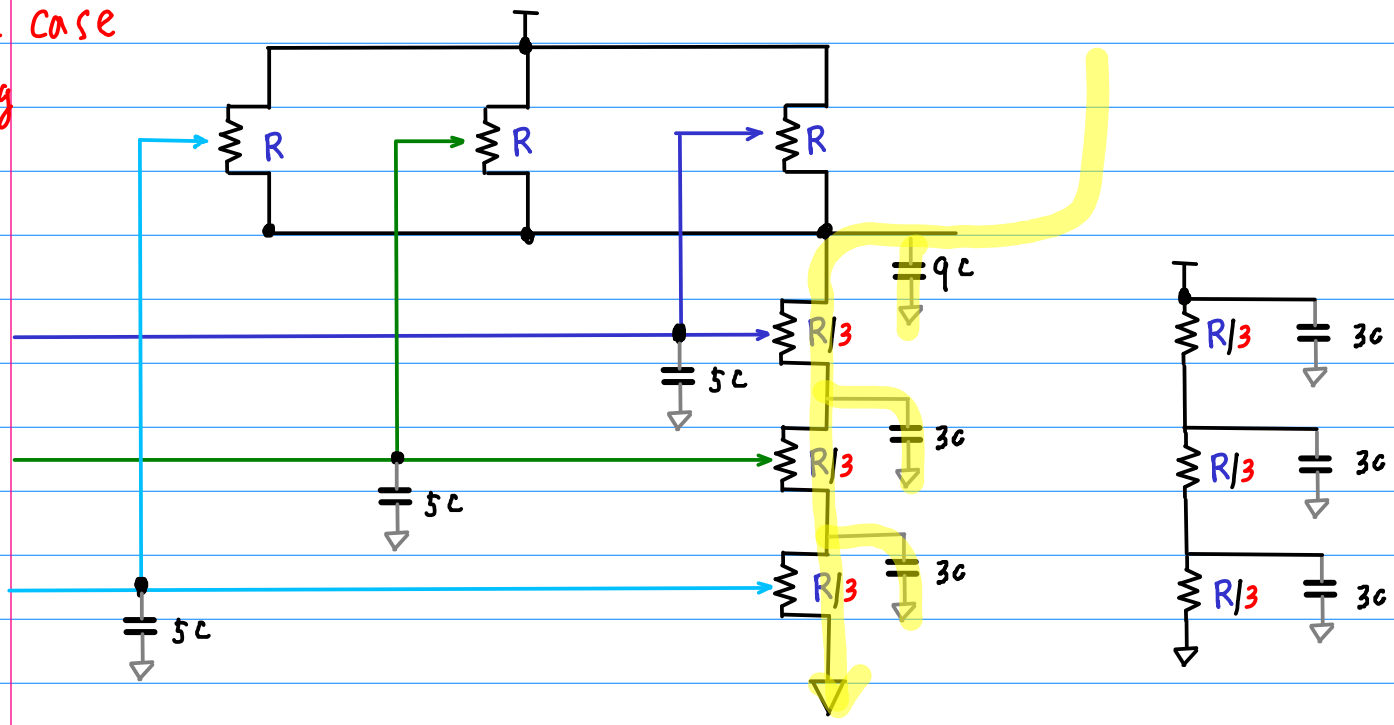
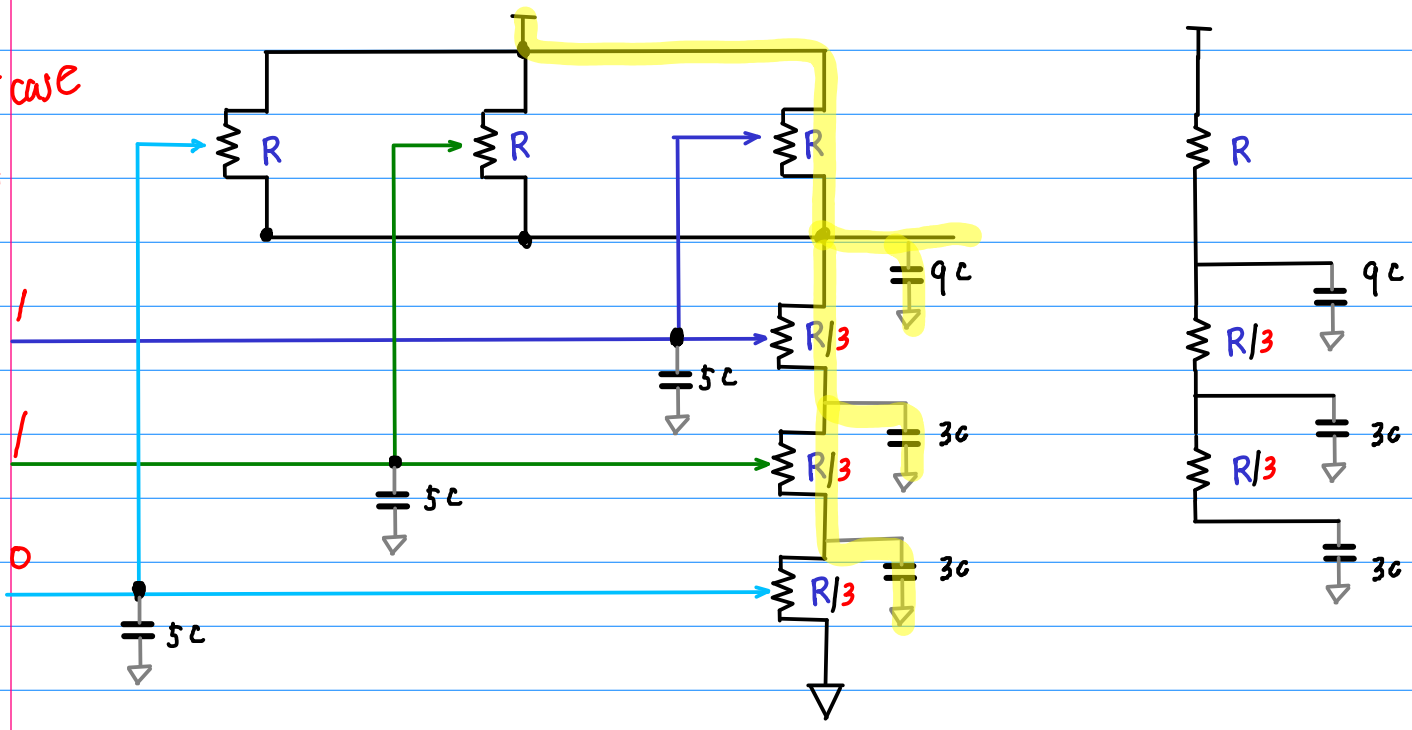
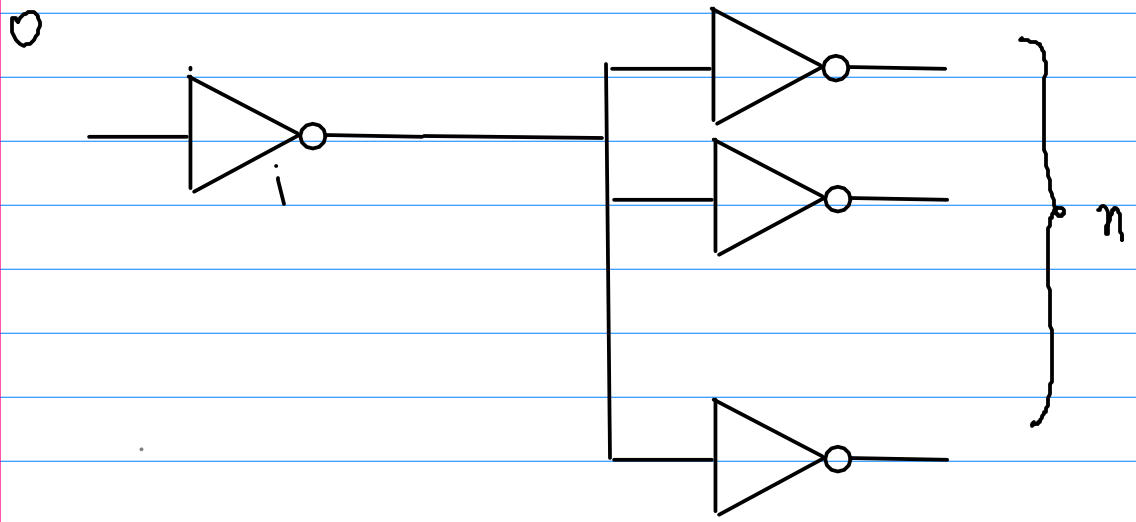
Worst case falling



Worst case rising

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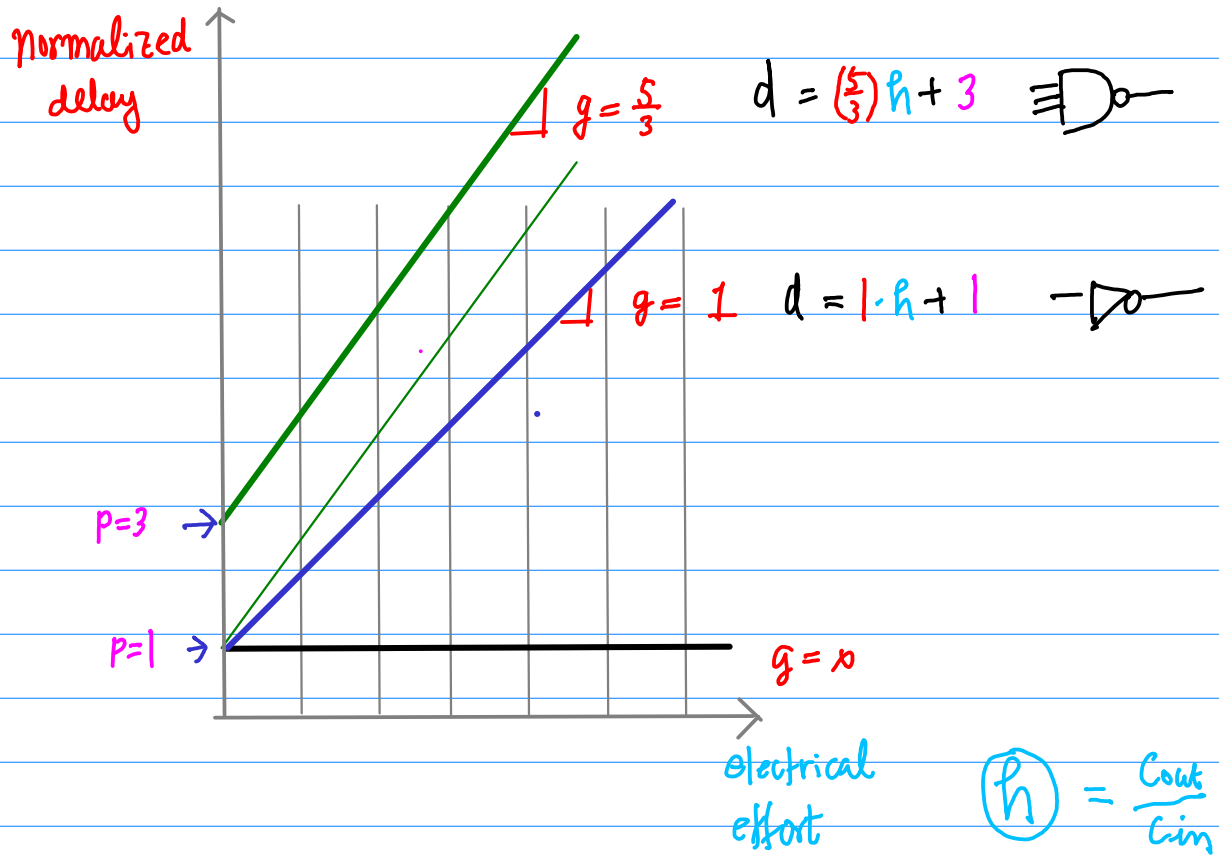
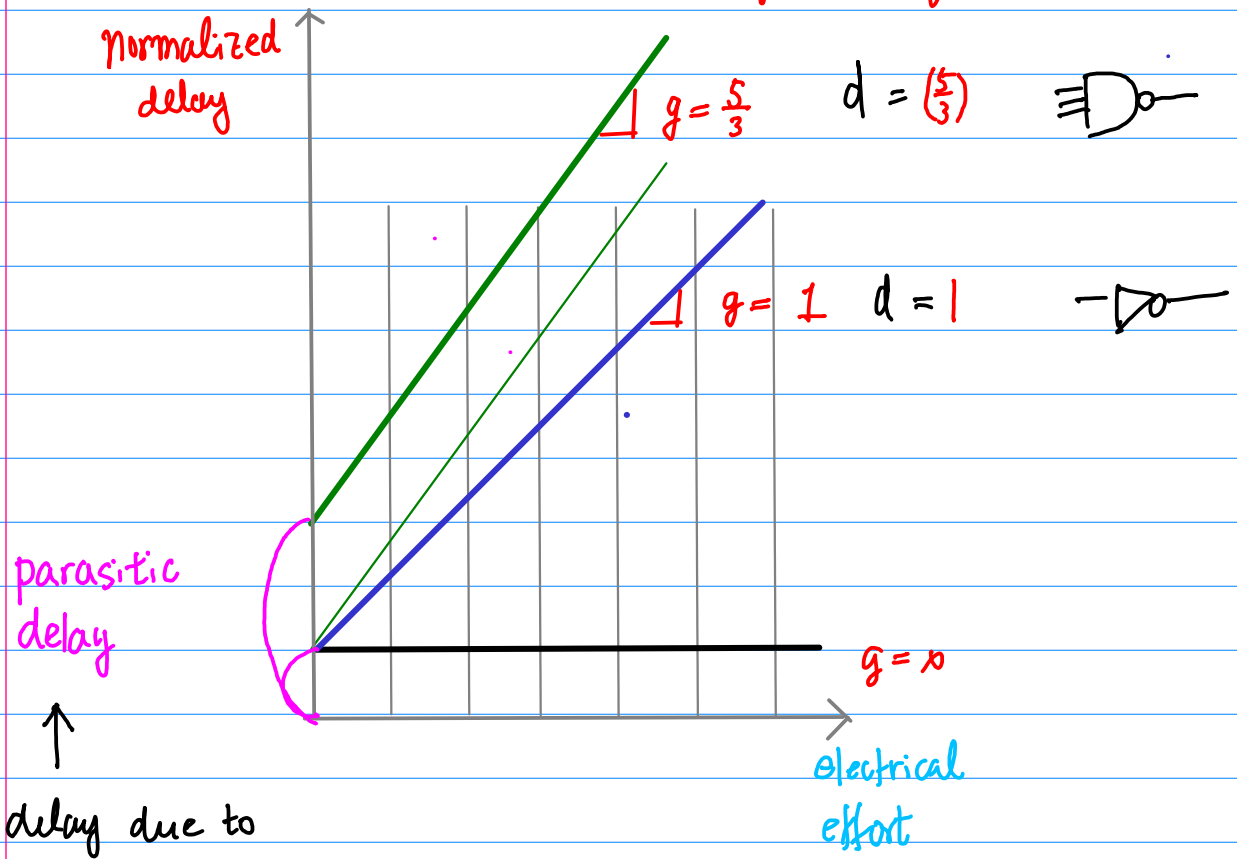
Linear Delay Model



Slope : logical effort



delay due to only internal cap without external load cap

$$d = g \cdot h + p$$

(k) (c) (c)

FET RC Model

$$R_n = \frac{V_{DSn}}{I_{Dn}}$$

$$I_{dn} \cong \beta_n (V_{GSn} - V_{Tn}) V_{DSn}$$

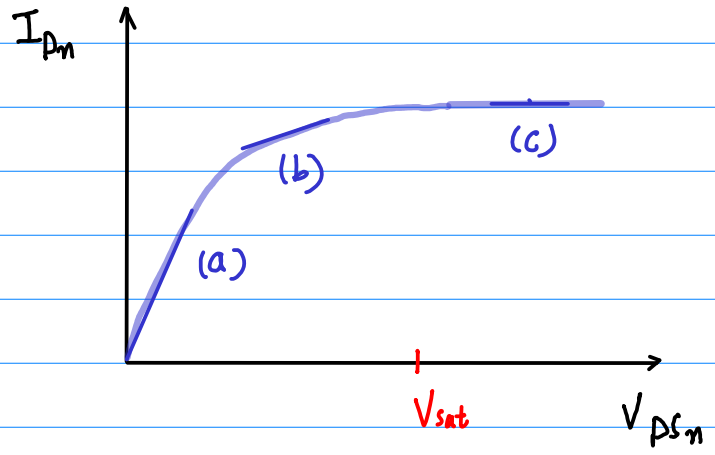
non-saturated

$$R_n \cong \frac{1}{\beta_n (V_{GSn} - V_{Tn})} \quad \text{(a) small } V_{DSn} \quad V_{DSn}^2 \approx 0$$

$$R_n = \frac{2}{\beta_n [2(V_{GSn} - V_{Tn}) - V_{DSn}]} \quad \text{(b)} \quad V_{DS} \neq 0$$

saturated

$$R_n = \frac{2V_{DSn}}{\beta_n (V_{GSn} - V_{Tn})^2} \quad \text{(c)}$$



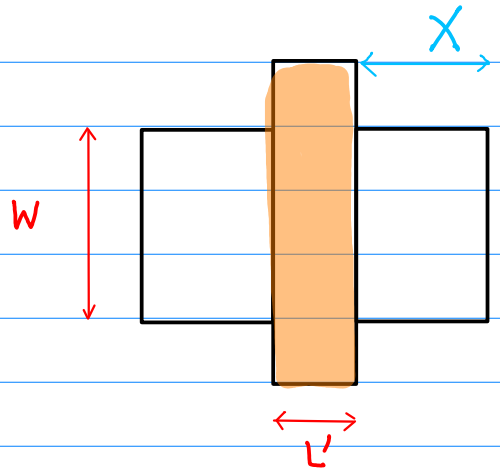
$$R_n \propto \frac{1}{\beta_n} \qquad \beta_n = k'_n \left(\frac{W}{L}\right)_n$$

$$R_n = \frac{\eta}{\beta_n (V_{DD} - V_{Tn})} \qquad \eta = 1 \sim 6$$

↑ largest possible V_{GSn}

$$\boxed{R_n = \frac{1}{\beta_n (V_{DD} - V_{Tn})}}\ \Omega \qquad \eta = 1$$

MOS Capacitance



$$C_G = C_{ox} A_G \qquad A_G = W L'$$

$$= C_{ox} W L'$$

$$C_{GS} = \frac{1}{2} C_G$$

$$C_{GD} = \frac{1}{2} C_G$$

Junction Capacitance

A_{pn}: area of p-n junction

V_R: the reverse bias voltage

$$C_0 = C_j A_{pn}$$

C_0: zero-bias capacitance ($V_R = 0$)

$$C = \frac{C_0}{\left(1 + \frac{V_R}{\phi_0}\right)^{m_j}}$$

m_j: grading coefficient

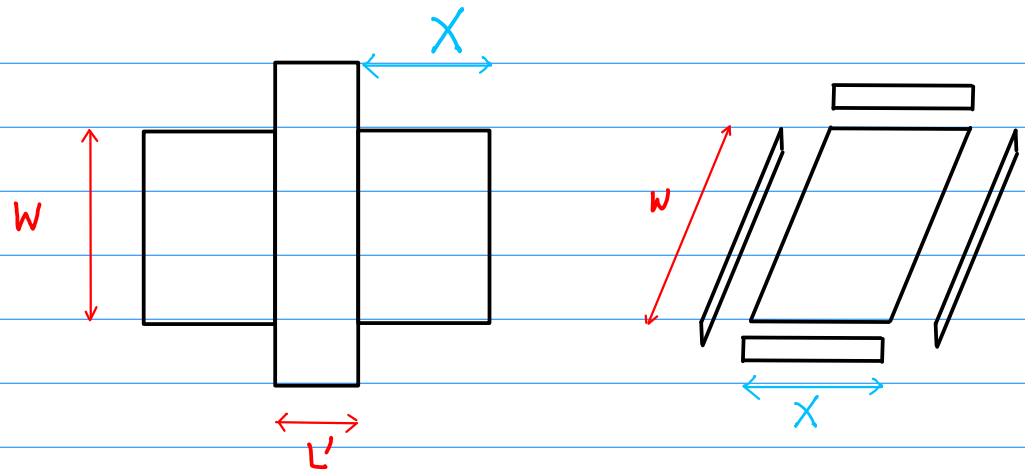
ϕ_0: built-in potential

m_j, ϕ_0 ← doping characterisstics

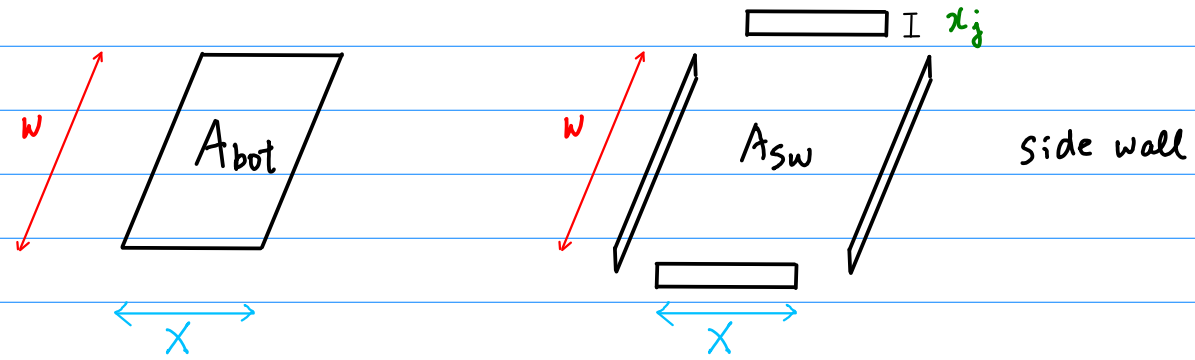
$$\phi_0 = \left(\frac{kT}{q}\right) \ln\left[\frac{N_d N_a}{n_i^2}\right]$$

for an abrupt (step) junction

for a linearly graded function



bottom **sidewall**



$A_{bot} = X\,W$

$A_{sw} = 2(W \cdot x_j) + 2(X \cdot x_j)$

$= x_j P_{sw} = x_j (2W + 2X)$

$C_{bot} = C_j A_{bot}$

$C_{sw} = C_j A_{sw}$

$= C_j x_j P_{sw}$

$= C_{jsw} P_{sw}$

$A_{bot} = XW$

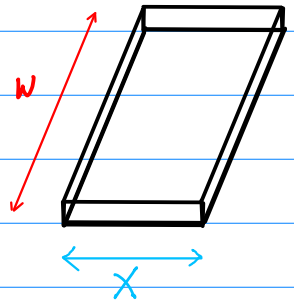
$A_{sw} = 2(W \cdot x_j) + 2(X \cdot x_j)$

$P_{sw} = (2W + 2X)$

$C_{jsw} = C_j x_j$

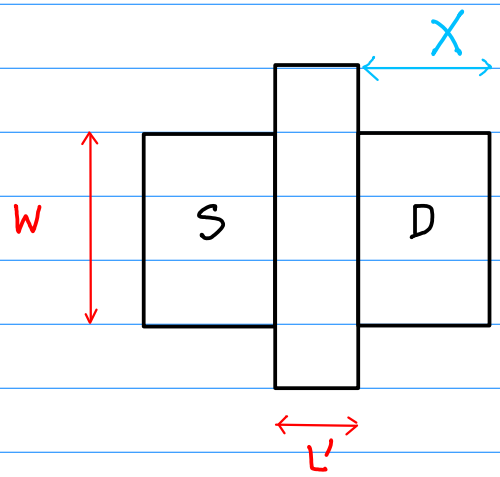
for overlap $X \leftarrow X + L_o$

the total zero-bias capacitance of n+ region



$$C_n = C_{bot} + C_{sw}$$
$$= C_j A_{bot} + C_{jsw} P_{sw}$$

$C_n \Rightarrow C_{SB}$ & C_{DB}



$$C_S = C_{GS} + C_{SB}$$
$$C_D = C_{GD} + C_{DB}$$

non-linear version

$$C_n = \frac{C_j A_{bot}}{\left(1 + \frac{V}{\phi_0}\right)^{m_j}} + \frac{C_{jsw} P_{sw}}{\left(1 + \frac{V}{\phi_{osw}}\right)^{m_{jsw}}}$$

V : reverse voltage

m_j : grading coefficients
ϕ_0 : built-in potential
) bottom

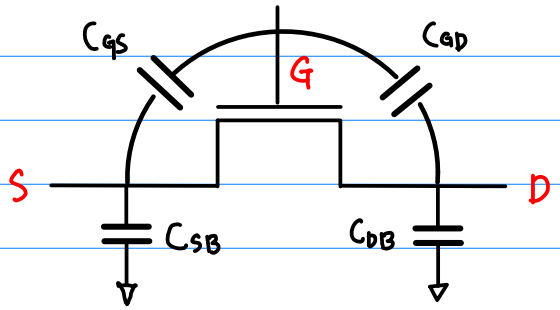
m_{jsw} : grading coefficients
ϕ_{osw} : built-in potential
) sidewalls

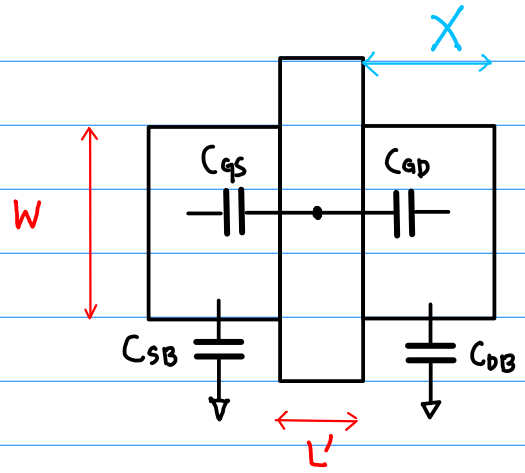
$$C_S = C_{GS} + C_{SB}$$
$$C_D = C_{GD} + C_{DB}$$

$$C_{GS} = \frac{1}{2} C_G \qquad C_{SB} = C_n$$
$$C_{GD} = \frac{1}{2} C_G \qquad C_{DB} = C_n$$

$$C_G = C_{ox} W L' \qquad C_n = C_j \{ X W + 2 x_j (W + X) \}$$

gate cap junction cap





pFET Characteristics

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$I_{Dp} = \frac{\beta_p}{2}\left(V_{SGp} - |V_{Tp}|\right)^2$$

$$\beta_p = k'_p \left(\frac{W}{L}\right)_p$$

$$k'_p = \mu_p C_{ox}$$

$$r = \frac{\mu_n}{\mu_p} = 2 \sim 3$$

$$\beta_n = k'_n \left(\frac{W}{L}\right)_n$$
$$\beta_p = k'_p \left(\frac{W}{L}\right)_p$$

$$V_{sat} = V_{SGp} - |V_{Tp}|$$

$$I_{Dp} = \frac{\beta_p}{2}\left[2\left(V_{SGp} - |V_{Tp}|\right)V_{SDp} - V_{SDp}^2\right]$$

$$I_{Dp} = \frac{\beta_p}{2}\left[V_{SGp} - |V_{Tp}|\right]^2$$

$$R_p = \frac{1}{\beta_p\left(V_{DD} - |V_{Tp}|\right)}$$

$$R_p \propto \frac{1}{\beta_p} = \frac{1}{k'_p \left(\frac{W}{L}\right)_p}$$

$$C_{Gp} = C_{ox}\left(W\,L\right)_p$$

$$C_{GS} = \frac{1}{2} C_{GP} \simeq C_{GP}$$

$$C_p = C_j A_{bot} + C_{jsw} P$$

Inverter Switching Characteristics

$$R_n = \frac{1}{\beta_n (V_{DD} - V_{Tn})}$$

$$R_p = \frac{1}{\beta_p (V_{DD} - |V_{Tp}|)}$$

$$C_{Dn} = C_{GDn} + C_{DBn} = \frac{1}{2} C_{ox} L' W_n + C_{jn} A_n + C_{jswn} P_n$$

$$C_{Dp} = C_{GDp} + C_{DBp} = \frac{1}{2} C_{ox} L' W_p + C_{jp} A_p + C_{jswp} P_p$$

$$C_{in} = C_{Gp} + C_{Gn}$$

$$C_L = 3 C_{in}$$

$$C_{out} = C_{FET} + C_L$$

$$C_{FET} = C_{Dn} + C_{Dp}$$

Fall Time Calculation

$$i = -C_{out}\frac{dV_{out}}{dt} = \frac{V_{out}}{R_n}$$

$$V_{out}(t) = V_{DD}\, e^{-t/\tau_n}$$

$$\tau_n = R_n C_{out}$$

$$t = \tau_n \ln\left(\frac{V_{DD}}{V_{out}}\right)$$

$$t_f = t_y - t_x = \tau_n \ln\left(\frac{V_{DD}}{0.1\,V_{DD}}\right) - \tau_n \ln\left(\frac{V_{DD}}{0.9\,V_{DD}}\right)$$
$$= \tau_n \ln(9)$$

$$t_{HL} = t_f \cong 2.2\tau_n$$

Rise Time Calculation

$$i = -C_{out}\frac{dV_{out}}{dt} = \frac{V_{DD} - V_{out}}{R_p}$$

$$V_{out}(t) = V_{DD}\left[1 - e^{-t/\tau_p}\right]$$

$$\tau_p = R_p C_{out}$$

$$t = \tau_p \ln\left(\frac{V_{DD}}{V_{out}}\right)$$

$$t_f = t_v - t_u = \tau_p \ln\left(\frac{V_{DD}}{0.1 V_{DD}}\right) - \tau_n \ln\left(\frac{V_{DD}}{0.9 V_{DD}}\right)$$
$$= \tau_p \ln(9)$$

$$t_{LH} = t_r \cong 2.2\tau_p$$

Propagation Delay

$$t_p = \frac{(t_{pf} + t_{pr})}{2}$$

$$t_{pf} = \ln(2) \cdot \tau_n$$
$$t_{pr} = \ln(2) \cdot \tau_p$$

$$t_p \cong 0.35 (\tau_n + \tau_p)$$

General Analysis

$$C_{out} = C_{FET} + C_L$$

$$t_r = 2.2 R_p (C_{FET} + C_L) = 2.2 R_p C_{out}$$
$$t_f = 2.2 R_n (C_{FET} + C_L) = 2.2 R_n C_{out}$$

$$t_r = t_{r0} + \alpha_p C_L$$
$$t_f = t_{r0} + \alpha_n C_L$$

$C_L = 0 \rightarrow$ $t_r = t_{r0} \cong 2.2 R_p C_{FET}$

$C_L = 0$ $t_f = t_{r0} \cong 2.2 R_n C_{FET}$

$$\alpha_p = 2.2 R_p = \frac{2.2}{\beta_p (V_{DD} - |V_{Tp}|)}$$

$$\alpha_n = 2.2 R_n = \frac{2.2}{\beta_n (V_{DD} - |V_{Tn}|)}$$

$$\beta_p = k'_p \left(\frac{W}{L}\right)_p$$

$$\beta_n = k'_n \left(\frac{W}{L}\right)_n$$