Cache Memory HW

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6/10/16

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Briefly describe the following terms.

- Tag
- Line
- Block
- Word

Describe the following in detail with figures and examples.

- Direct Mapping
- K-way Set Associative Mapping
- Fully Associative Mapping

Direct Mapping

- Tag : t-bits
- Line : l-bits
- Word : w-bits

- Main memory address bits? (t+l+w)-bit
- How many blocks exist in main memory? Upto 2^(t+l) blocks
- How many words in a block? 2^w words
- How many lines in the cache? 2^l lines
- Cache memory size? 2^l * (t+2^w) words

* valid bits are excluded

K-way Set Associative Mapping

- Tag : t-bits
- Set : s-bits
- Word : w-bits

- Main memory address bits? (t+s+w)-bit
- How many blocks exist in main memory? Upto 2^(t+s) blocks
- How many words in a block? 2^w words
- How many lines in the cache? 2^s lines
- Cache memory size? 2^s * (t+2^w) * K words

* valid bits are excluded

Fully Associative Mapping

- Tag : t-bits
- Word : w-bits

- Main memory address bits? (t+w)-bit
- How many blocks exist in main memory? Upto 2^t blocks
- How many words in a block? 2^w words
- How many lines in the cache? N lines assumed
- Cache memory size? 1 * (t+2^w) * N words

* valid bits are excluded

References

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