Structure (1A)

- Component

Please send corrections (or suggestions) to youngwlim@hotmail.com.

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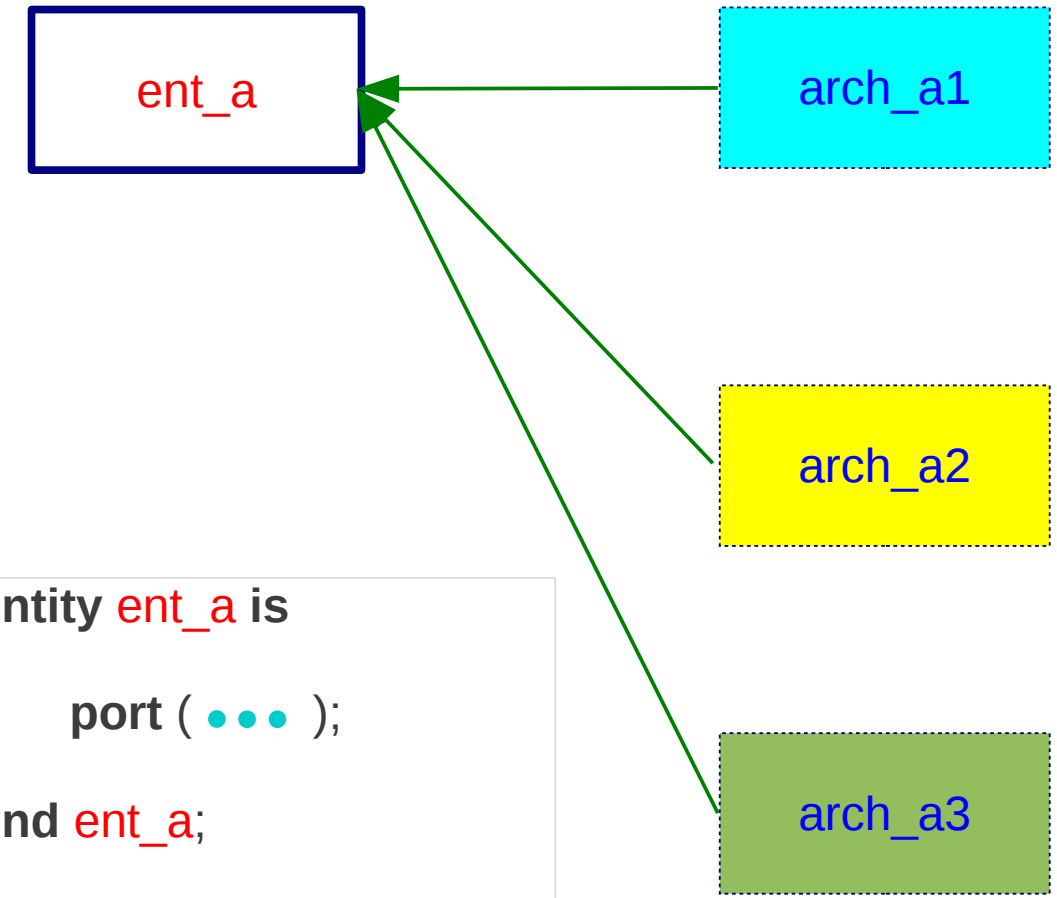
08/04/2012

Entity and Architecture


```
entity ent_a is

    port (  •••);

end ent_a;
```

```
architecture arch_a of ent_a is

        •••

end ent_a;
```

Many Architectures



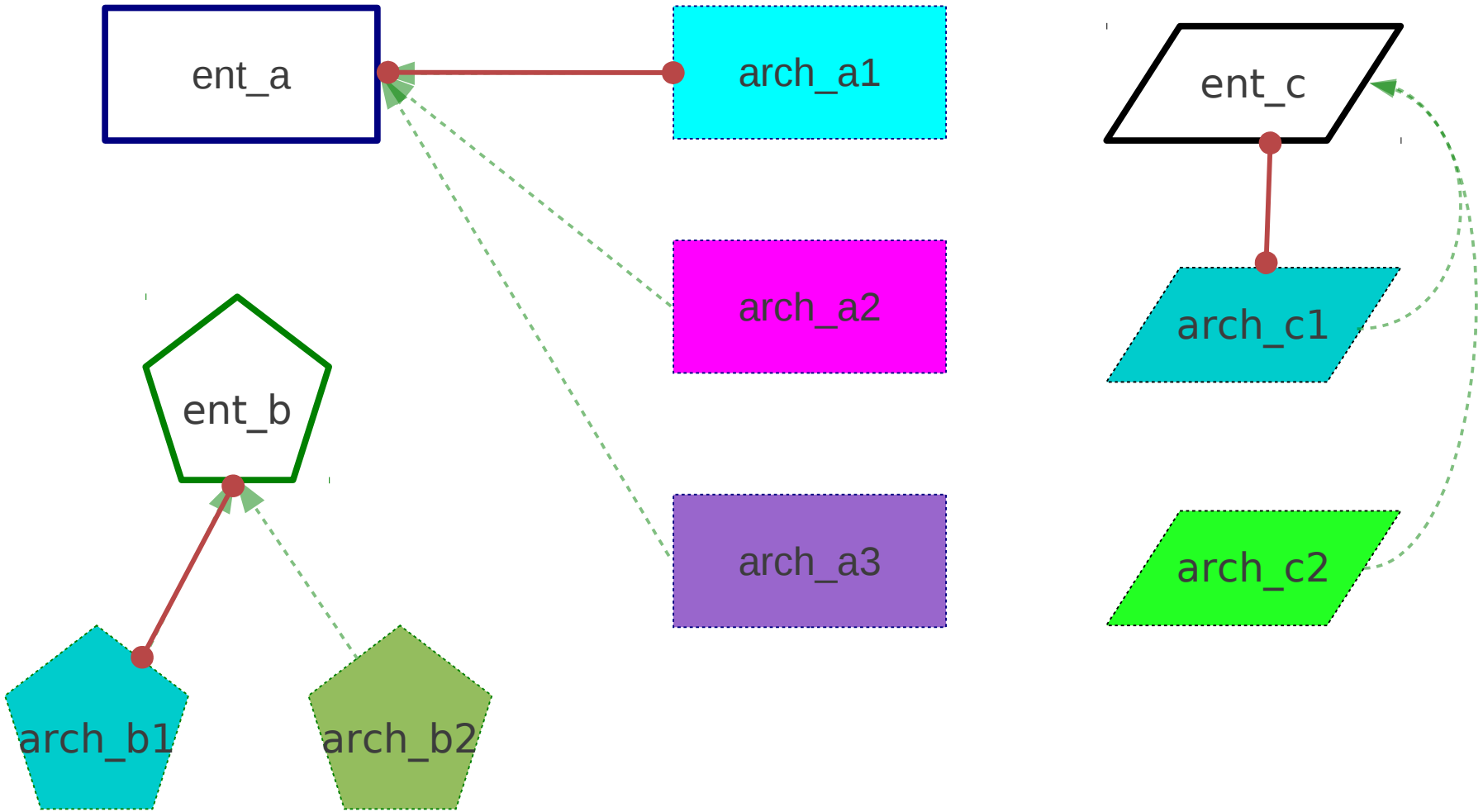

```
entity ent_a is
    port ( ••• );
end ent_a;
```

```
architecture arch_a1 of ent_a is
    •••
end ent_a;
```

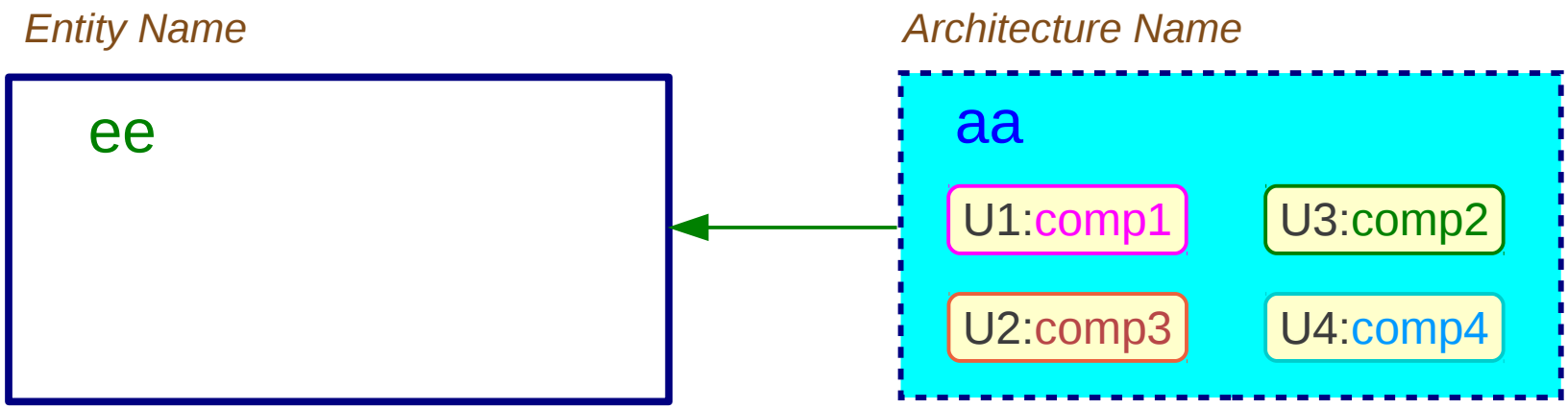
```
architecture arch_a2 of ent_a is
    •••
end ent_a;
```

```
architecture arch_a3 of ent_a is
    •••
end ent_a;
```

Entity – Architecture Binding



Hierarchical Component



Component Declaration

```
component comp1 is
        port (        );
end comp1;

component comp2 is
        port (        );
end comp2;

component comp3 is
        port (        );
end comp3;

component comp4 is
        port (        );
end comp4;
```

Only external view of a component

Component Name

comp1 comp2 comp3 comp4

Types and directions of a component ports

```
port (        );
```

Componet Declaration

Entity Name

ee

Architecture Name

aa

U1:comp1 U3:comp2

U2:comp3 U4:comp4

Component Declaration

```
component comp1 is
        port (        );
end comp1;

component comp2 is
        port (        );
end comp2;

component comp3 is
        port (        );
end comp3;

component comp4 is
        port (        );
end comp4;
```

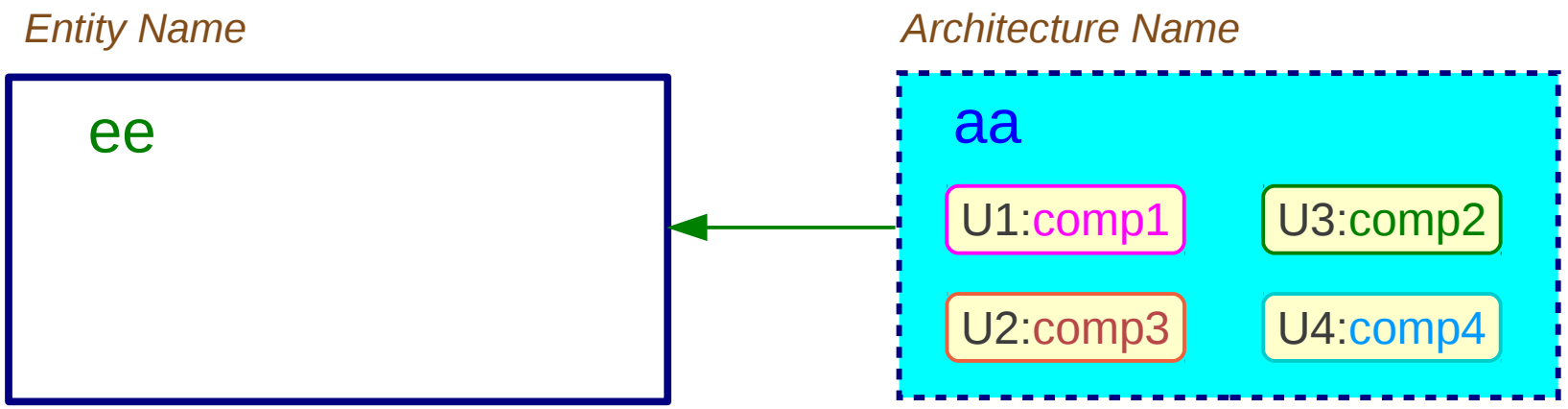
```
architecture aa of ee is

begin
```

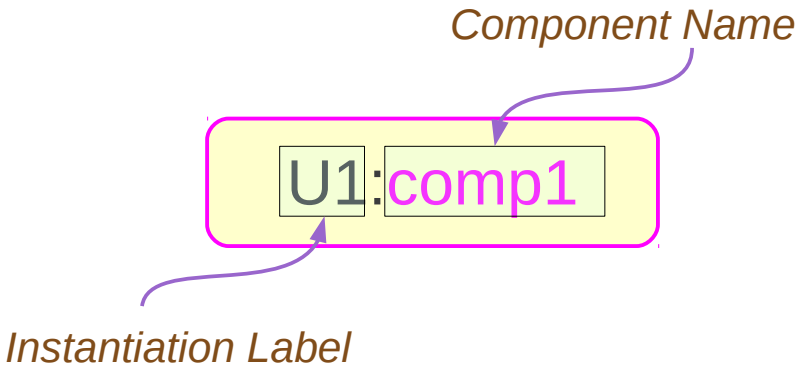
Component Instantiation

```
U1: comp1 port map (      );
U2: comp2 port map (      );
U3: comp3 port map (      );
U4: comp4 port map (      );
```

```
end aa;
```

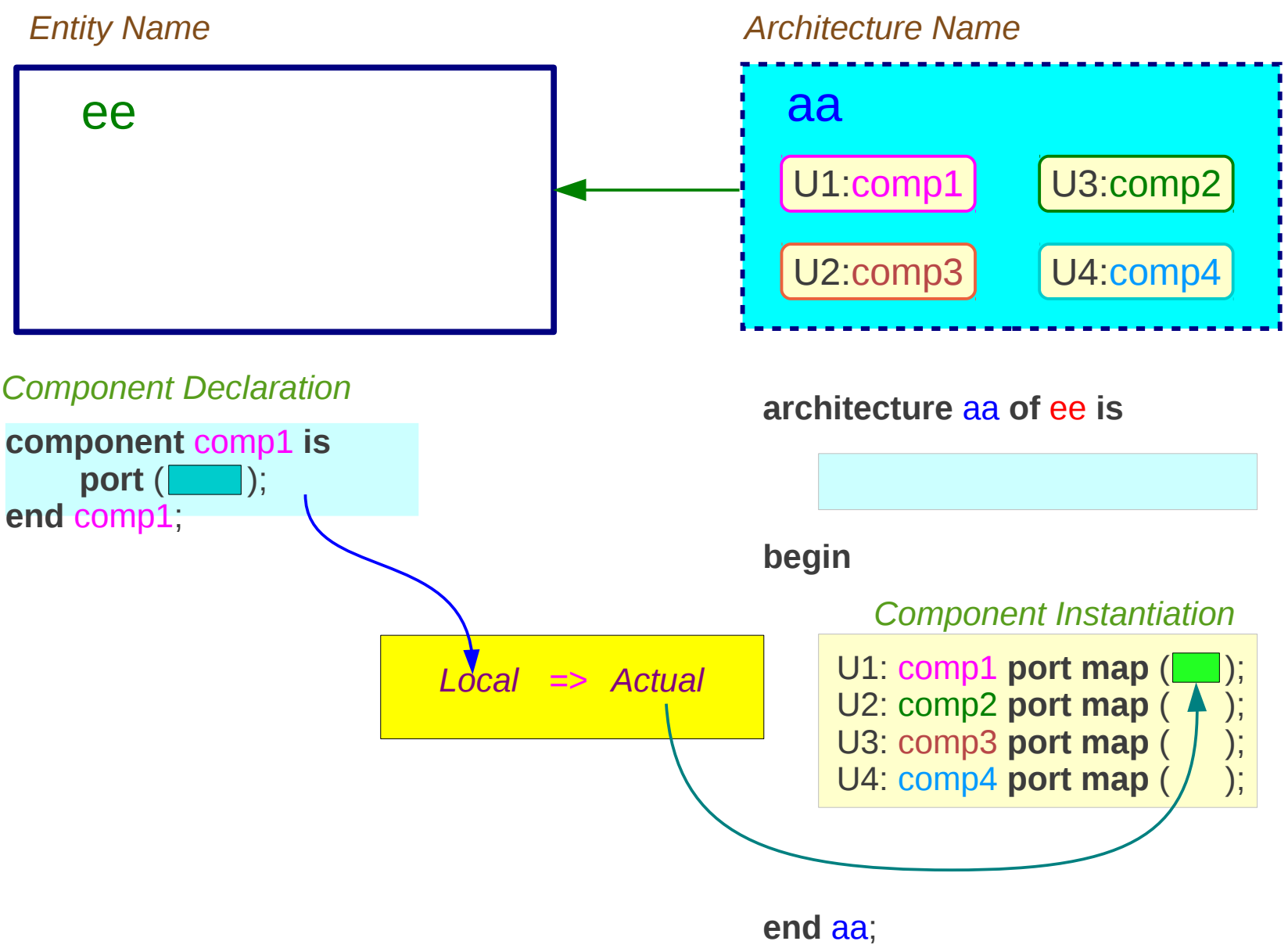
Component Instantiation



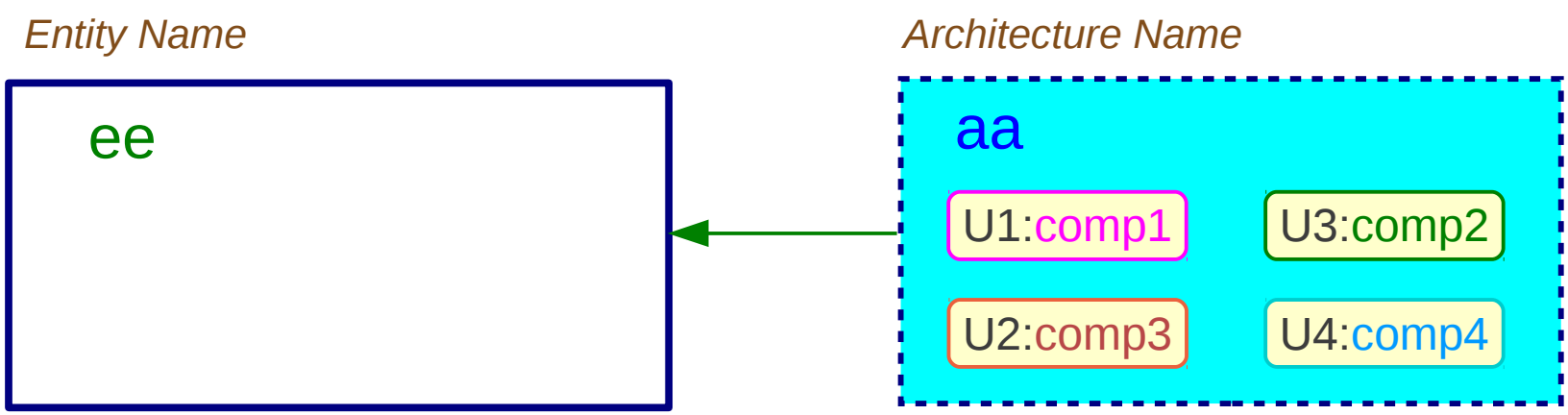



```
architecture aa of ee is

begin

    Component Instantiation
    U1: comp1 port map (      );
    U2: comp2 port map (      );
    U3: comp3 port map (      );
    U4: comp4 port map (      );

end aa;
```

Port Map


Entity Name
ee
Architecture Name
aa
U1:comp1
U3:comp2
U2:comp3
U4:comp4
Component Declaration
component comp1 is
port ( );
end comp1;
architecture aa of ee is
begin
Component Instantiation
U1: comp1 port map ( );
U2: comp2 port map ( );
U3: comp3 port map ( );
U4: comp4 port map ( );
Local => Actual
end aa;

Positional & Named Associations




```
port (I0, I1; in std_logic; O; out std_logic);
```

Local Port	=>	*Actual Signal*

Positional Association

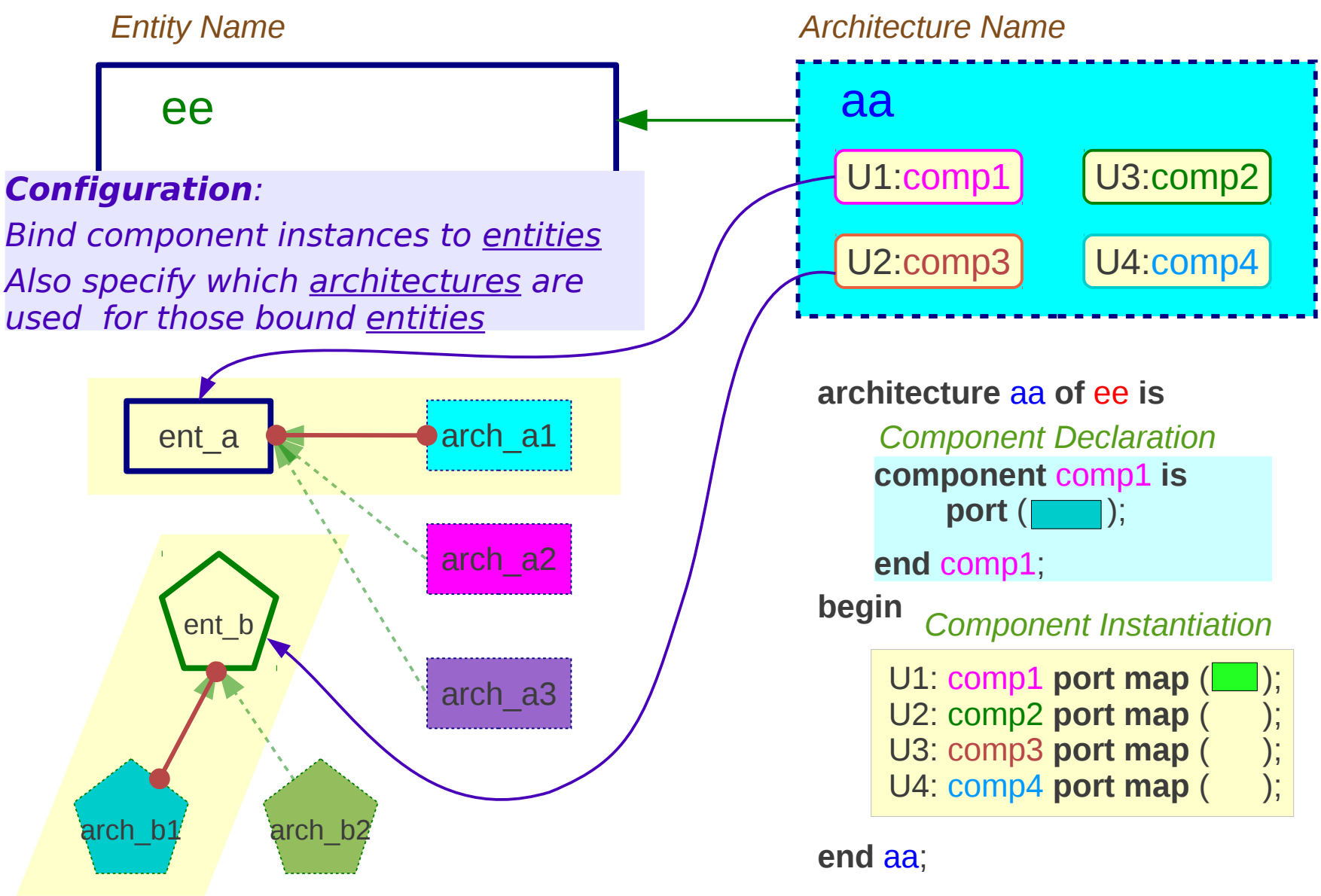
```
port map (A, B, TMP1);
```

Named Association

```
port map (I0=>A, I1=>B, O=>TMP1);
```

```
architecture aa of ee is
    Component Declaration
    component comp1 is
        port ( );
    end comp1;
begin
    Component Instantiation
    U1: comp1 port map ( );
    U2: comp2 port map ( );
    U3: comp3 port map ( );
    U4: comp4 port map ( );

end aa;
```

Configuration



References

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http://www.seas.upenn.edu/~ese171/vhdl/vhdl_primer.html
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