

# CMOS Delay-7 (H.8) Delay Model

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# References

Some Figures from the following sites

[1] <http://pages.hmc.edu/harris/cmosvlsi/4e/index.html>  
Weste & Harris Book Site

[2] [en.wikipedia.org](http://en.wikipedia.org)

$\beta$  : Device Transconductance Parameter

$k$  : Process Transconductance Parameter

$\mu$  : Electron/Hole Mobility

$$\text{PMOS} \quad \beta_p = k'_p \left(\frac{W}{L}\right)_p \quad k'_p = \mu_p C_{ox} \quad C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

$$\text{nMOS} \quad \beta_n = k'_n \left(\frac{W}{L}\right)_n \quad k'_n = \mu_n C_{ox} \quad C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$$

Saturation Current

$$I_{d_p} = \frac{\beta_p}{2} (V_{GSn} - |V_{Tp}|)^2 \quad V_{Tp} < 0$$

$$I_{d_n} = \frac{\beta_n}{2} (V_{GSn} - V_{Tn})^2 \quad V_{Tn} > 0$$

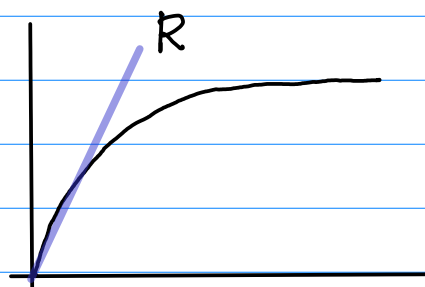
$$\frac{\beta_n}{\beta_p} = \frac{k'_n \left(\frac{W}{L}\right)_n}{k'_p \left(\frac{W}{L}\right)_p}$$

$$\frac{k'_n}{k'_p} = 2 \sim 3$$

$$\frac{k'_n}{k'_p} = \frac{\mu_n}{\mu_p} = \gamma$$

fall time  $t_f$

rise time  $t_r$



$$R_n = \frac{1}{\beta_n (V_{DD} - V_{Tn})}$$

$$R_p = \frac{1}{\beta_p (V_{DD} - V_{Tp})}$$

$$\tau_n = R_n C_{out}$$

$$\tau_p = R_p C_{out}$$

$$C_{out} = C_{para} + C_L$$

fall time	$t_f = 2.2 \tau_n = \ln 9 \tau_n$	$0.9 V_{DD} \rightarrow 0.1 V_{DD}$
rise time	$t_r = 2.2 \tau_p = \ln 9 \tau_p$	$0.1 V_{DD} \rightarrow 0.9 V_{DD}$
propagation delay time	$t_p = \frac{1}{2} (t_{pf} + t_{pr})$ $= 0.35 (t_{pf} + t_{pr})$	$0.5 V_{DD} \rightarrow 0.5 V_{DD}$
propagation fall time	$t_{pf} = 0.7 \tau_n = \ln 2 \tau_n$	$V_{DD} \rightarrow 0.5 V_{DD}$
propagation rise time	$t_{pr} = 0.7 \tau_p = \ln 2 \tau_p$	$0 \rightarrow 0.5 V_{DD}$

$$\tau_n = R_n (C_{para} + C_L)$$

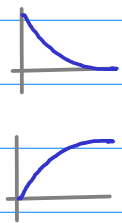
$$\tau_p = R_p (C_{para} + C_L)$$

$$C_{out} = C_{para} + C_L$$

$$\left(\frac{W}{L}\right)_p = r \left(\frac{W}{L}\right)_n$$

$$r = \frac{\mu_n}{\mu_p} = \frac{k'_n}{k'_p} > 1$$

$$R_n = R_p = R = \frac{1}{\beta(V_{DD} - V_T)}$$

$$\begin{cases} V_{out}(t) = V_{DD} (1 - e^{-t/\tau}) \\ V_{out}(t) = V_{DD} e^{-t/\tau} \end{cases}$$


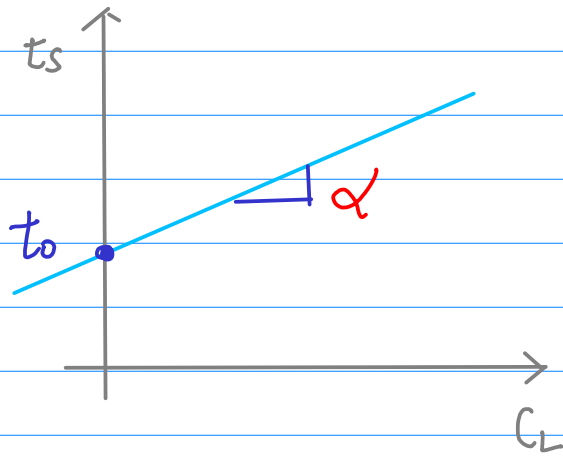
$$\tau = RC_{out} = R(C_{par} + C_L)$$

### Generic Switching Delay

$$t_s = t_0 + \alpha C_L \Rightarrow t_s = t_r = t_f$$

## Generic Switching Delay

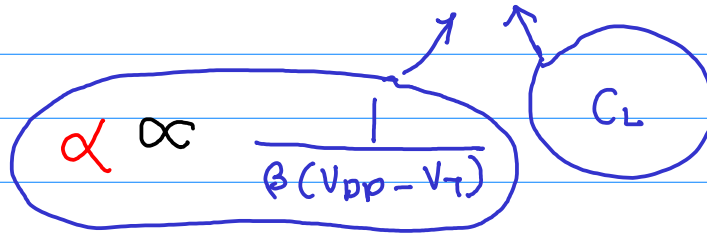
$$t_s = t_0 + \alpha C_L$$

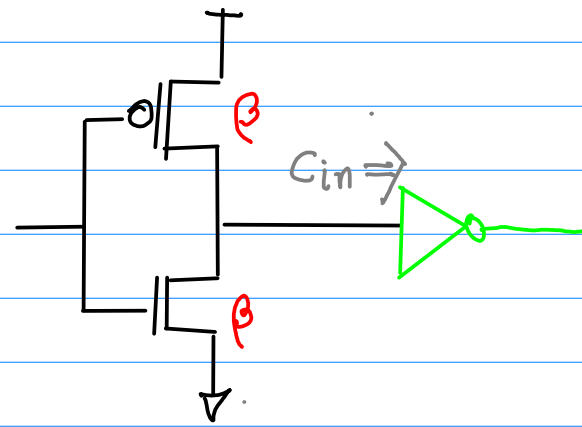
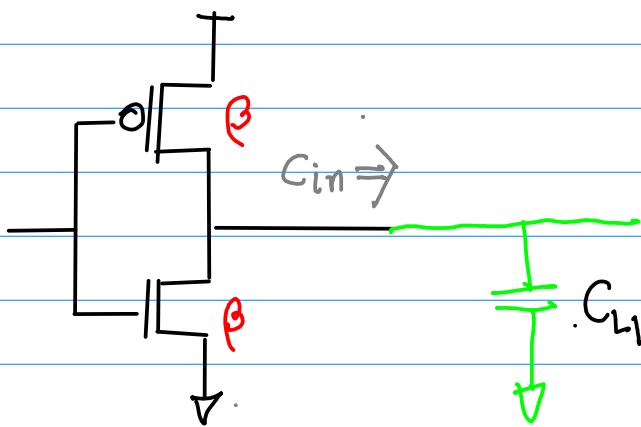
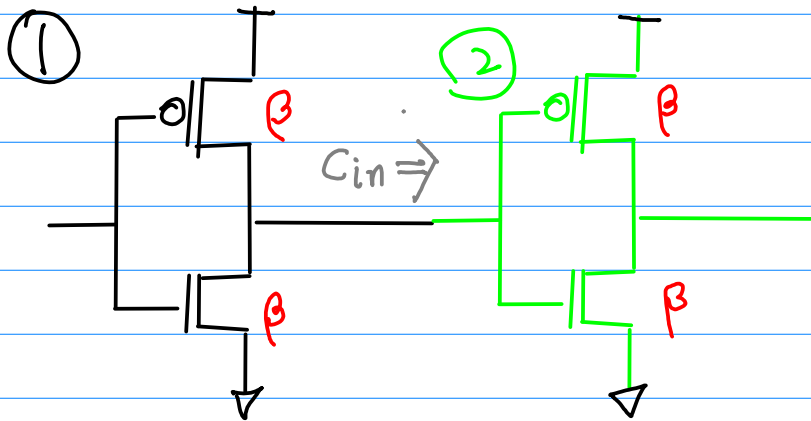


$t_0$  : zero delay

$\alpha$  : slope

$$\tau \approx RC$$





reference case

$$C_{in} = C_{L1}$$

Generic Switching Delay of ①

$$t_{s1} = t_0 + \alpha C_{L1}$$

$$= t_0 + \alpha C_{in}$$



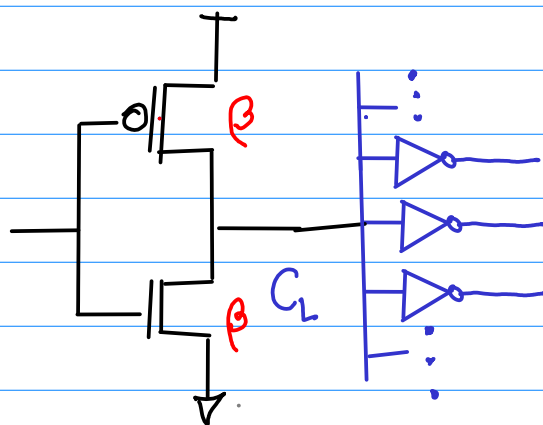
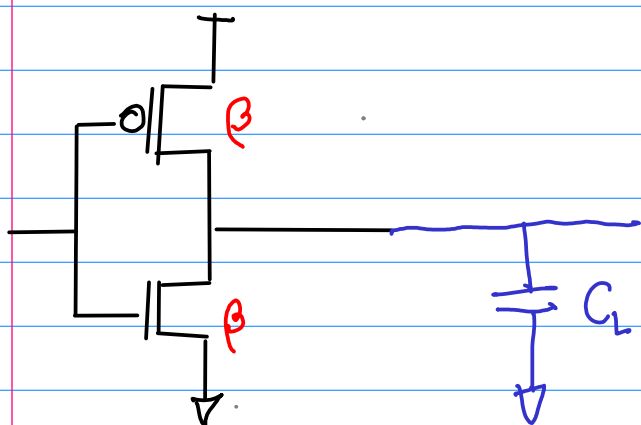
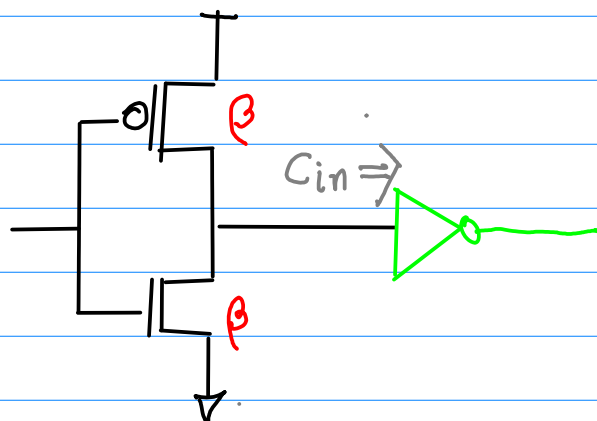
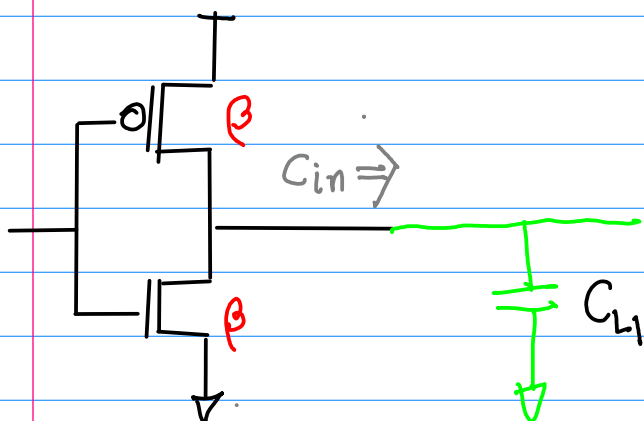
$$\begin{aligned}C_{in} &= C_{Gn} + C_{Gp} \\ &= C_{ox} (A_{Gn} + A_{Gp})\end{aligned}$$

$A_i$ : gate area

the channel length  $L$  assumed

$$\begin{aligned}C_{in} &= C_{ox} L (W_n + W_p) \\ &= C_{ox} L (W_n + r W_p) \\ &= C_{ox} L W_n \cdot (1 + r) \\ &= C_{Gn} (1 + r)\end{aligned}$$

When  $C_L \gg C_{in}$



to minimize  $t_s$

$\alpha \downarrow \Rightarrow R \downarrow \Rightarrow \beta \uparrow \Rightarrow$  bigger size

speed v.s. area tradeoff

$$t_s = t_0 + \alpha C_L \quad t \approx RC$$

$$\alpha \propto \frac{1}{\beta(V_{DD} - V_T)}$$

Diagram showing the relationship between  $\alpha$  and  $C_L$ . The expression  $\alpha \propto \frac{1}{\beta(V_{DD} - V_T)}$  is circled in blue. An arrow points from this expression to the  $\alpha$  term in the equation above. Another arrow points from a circled  $C_L$  to the  $C_L$  term in the equation above.

to minimize  $t_s$

$$\alpha \downarrow \Rightarrow R \downarrow \Rightarrow \beta \uparrow \Rightarrow \text{bigger size}$$

Speed v.s. area tradeoff

Scaling Factor  $S$

$$\beta' = S \beta$$

$$R' = \frac{R}{S}$$

$$\alpha' = \frac{\alpha}{S^2}$$

$$t_s = t_0 + \left( \frac{\alpha}{S} \right) C_L$$

Compensation Factor  $\left( \frac{1}{S} \right)$

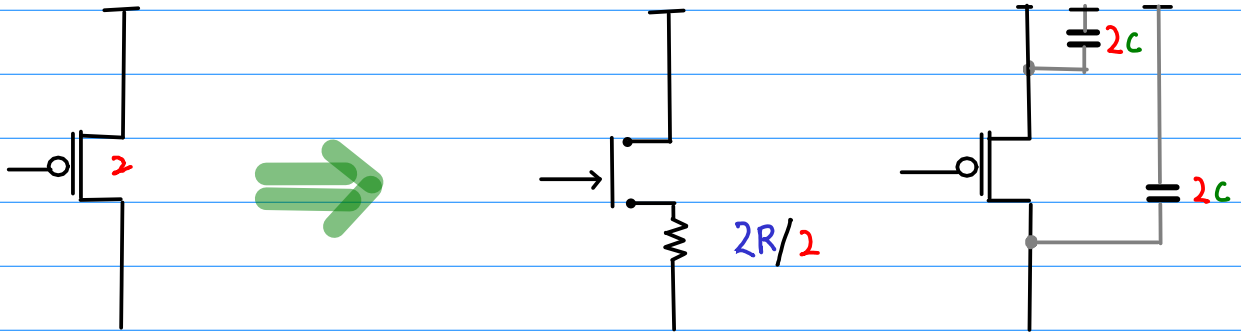
enables a NOT gate drive larger values of  $C_L$

If  $C_L = S C_{in}$  (increased by the scaling factor  $S$ )

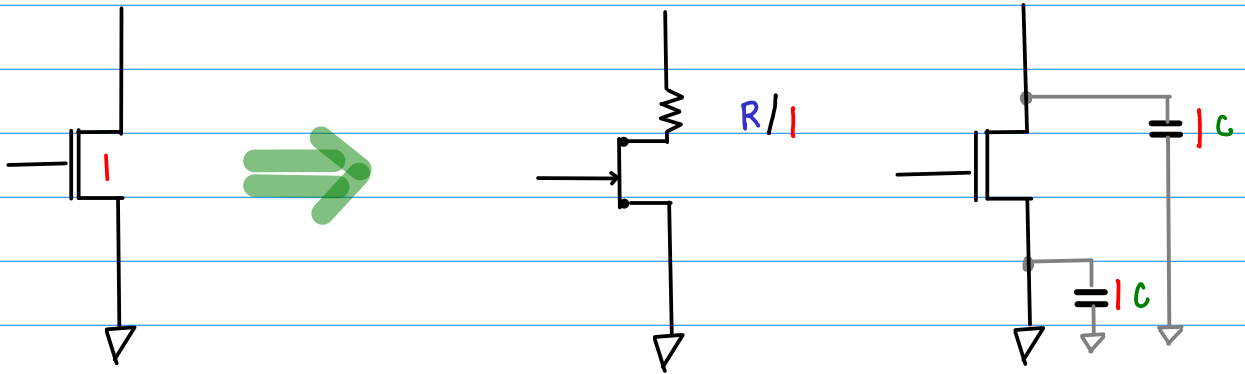
then the switching time is the same

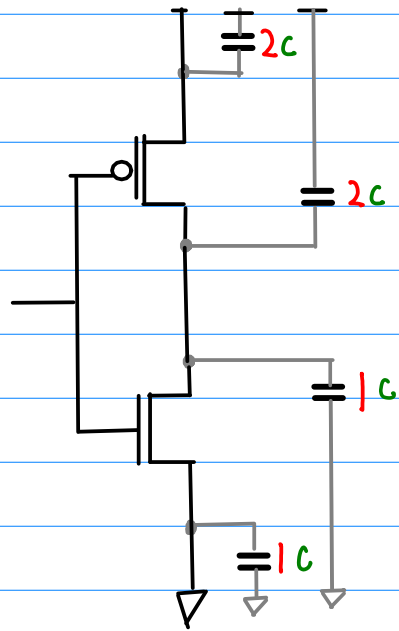
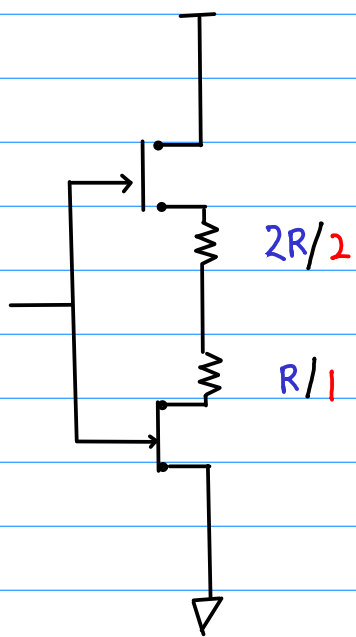
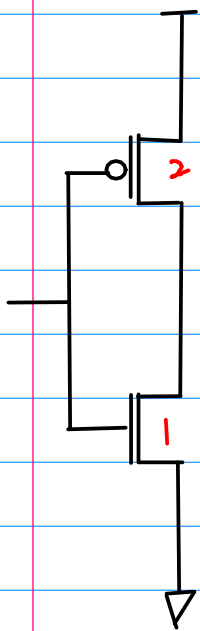
# RC Delay Model

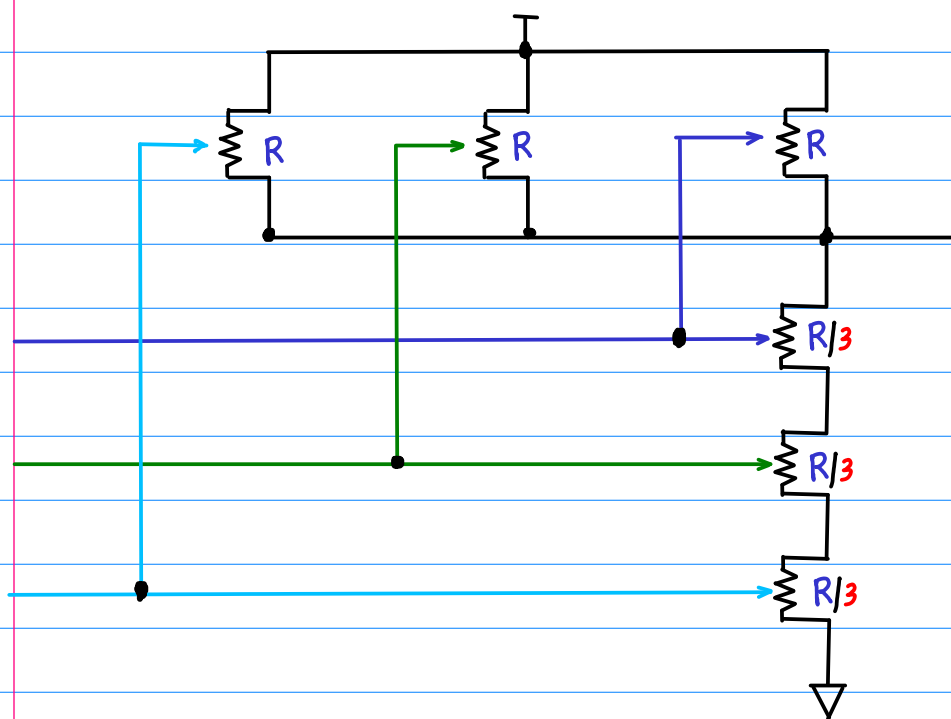
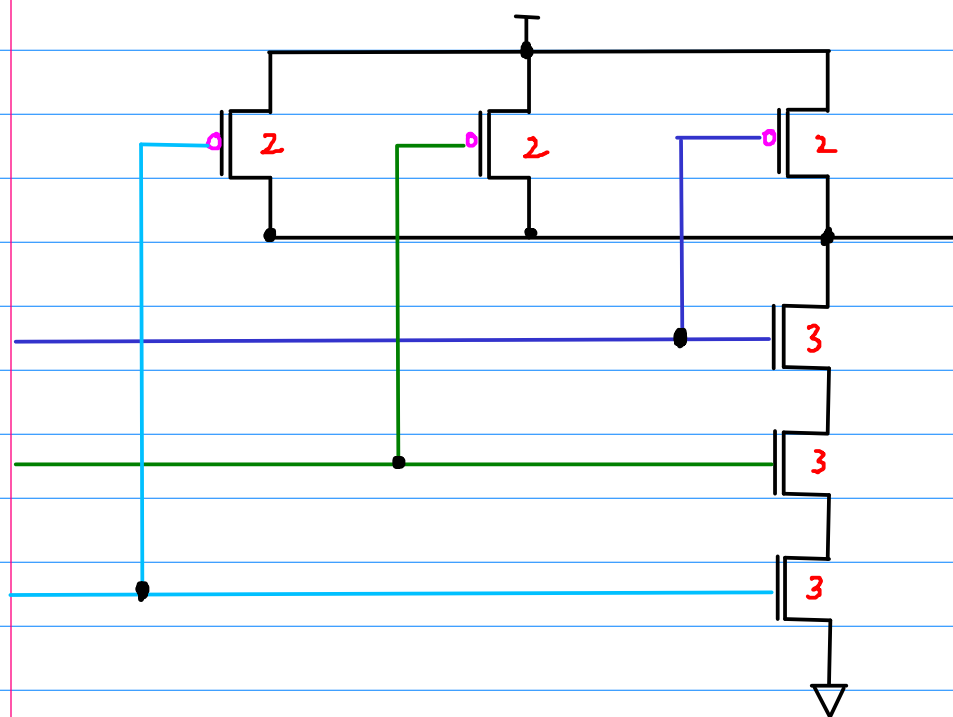
pMOS

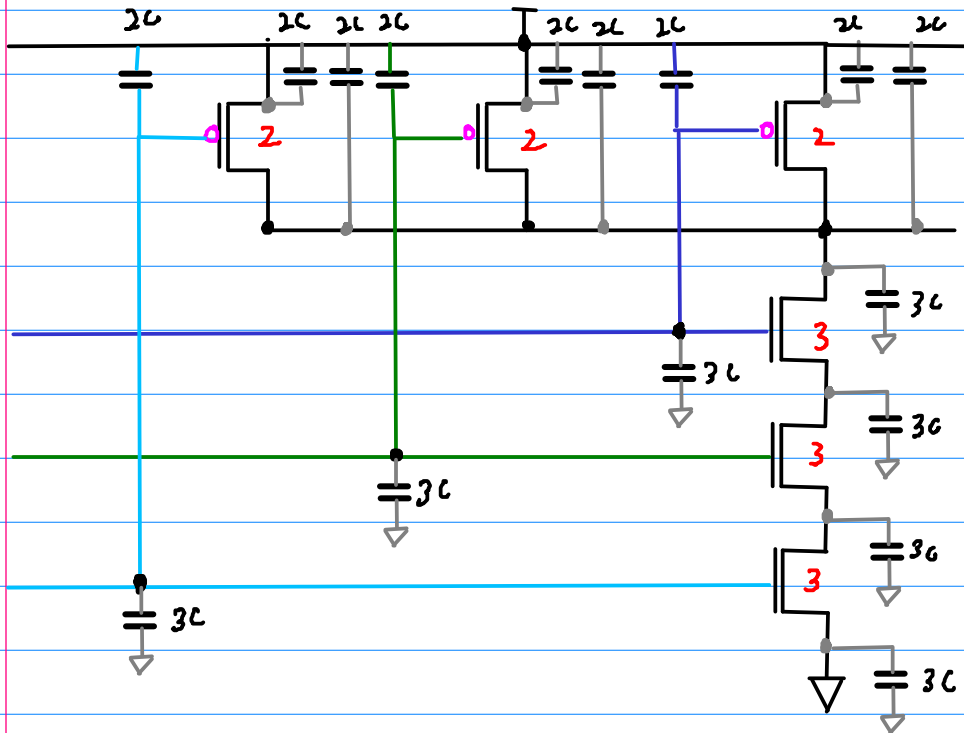
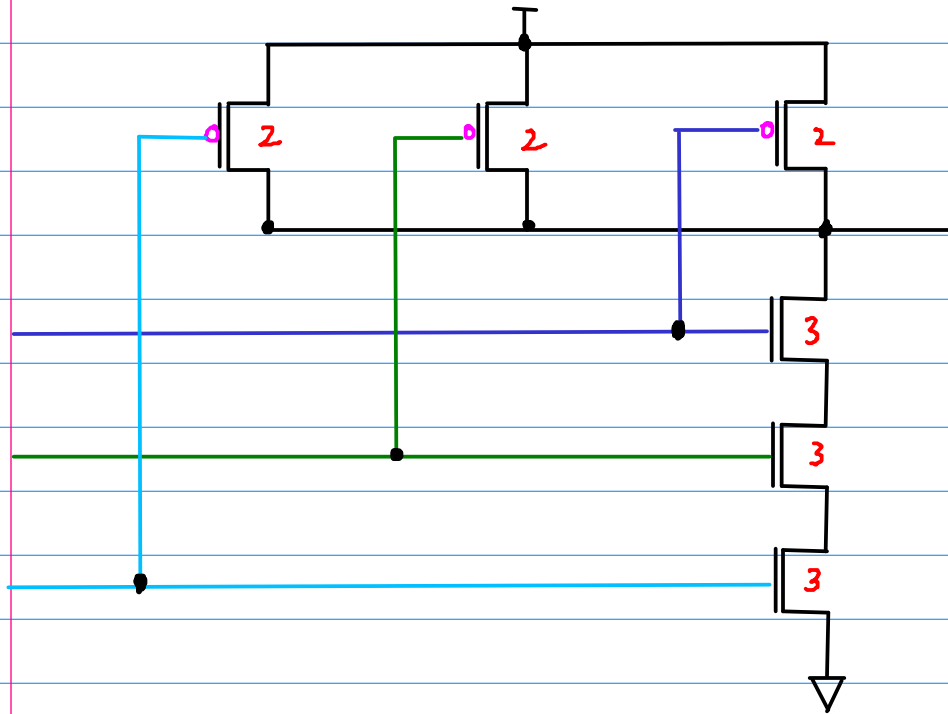


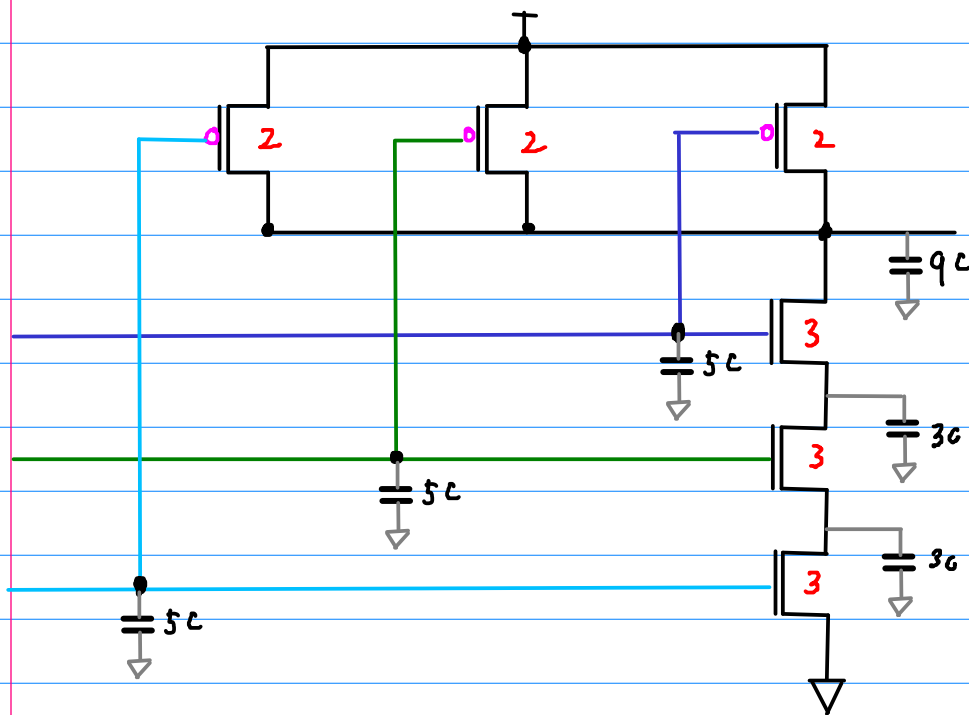
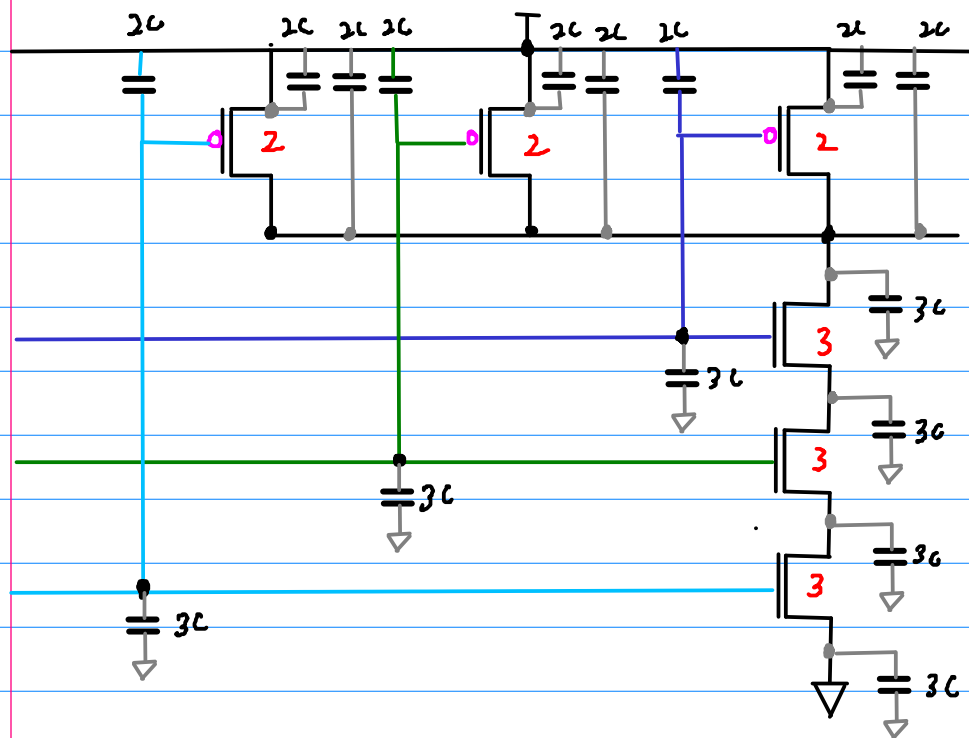
nMOS





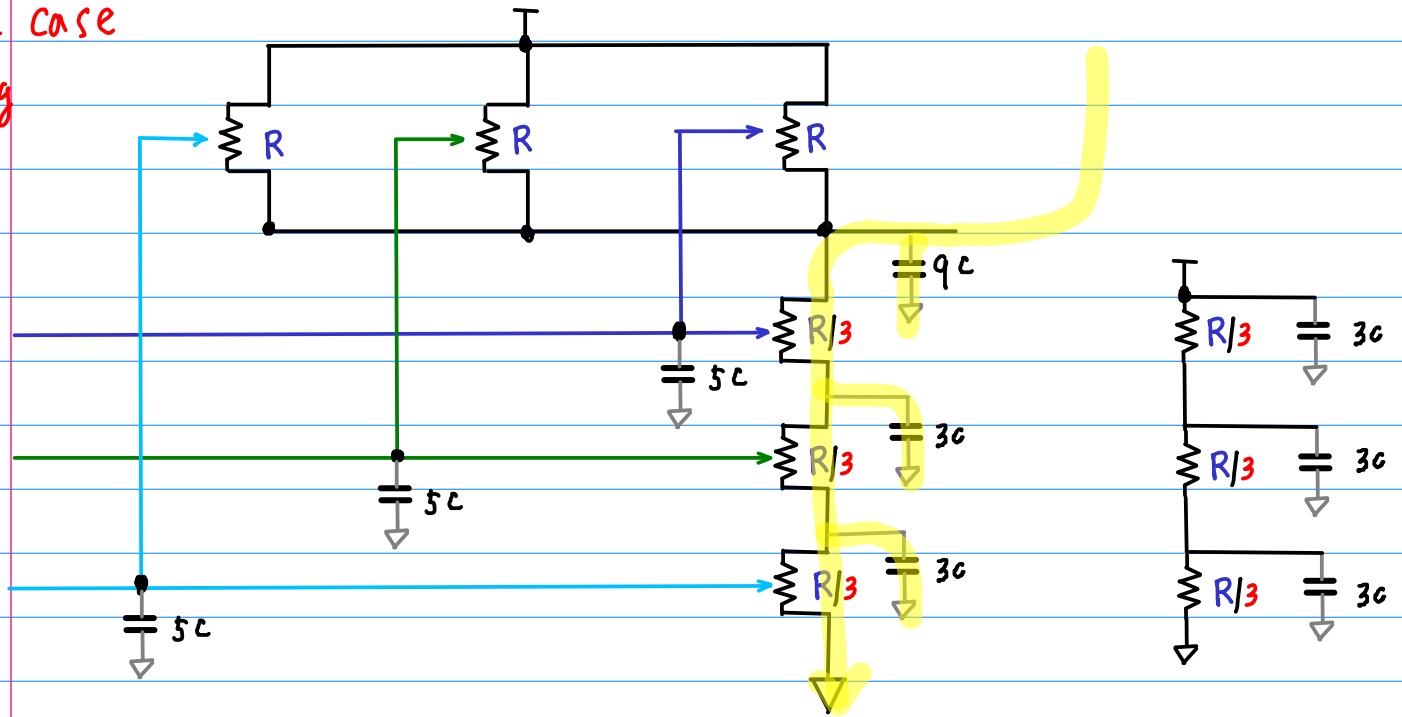




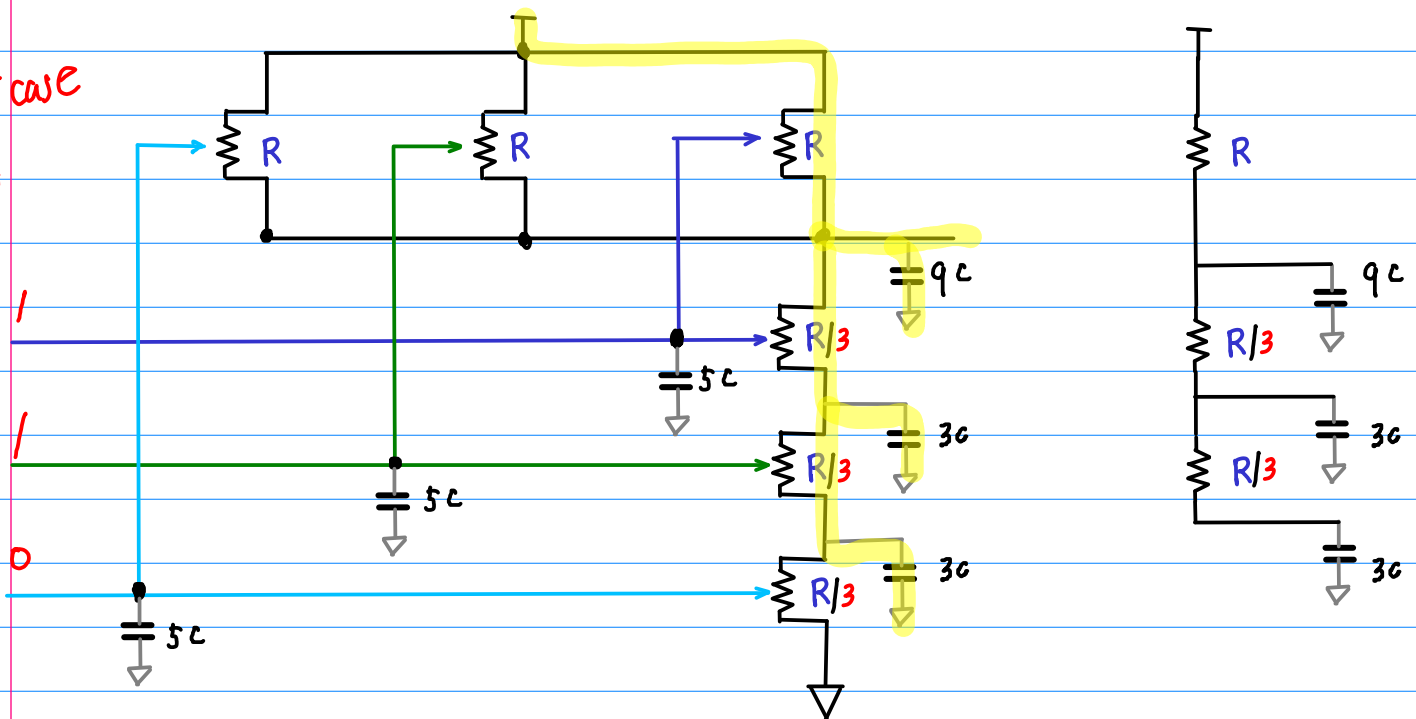




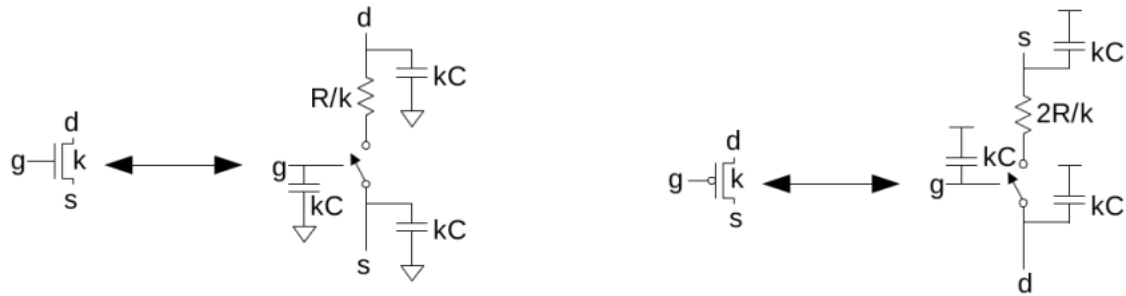
Worst case falling



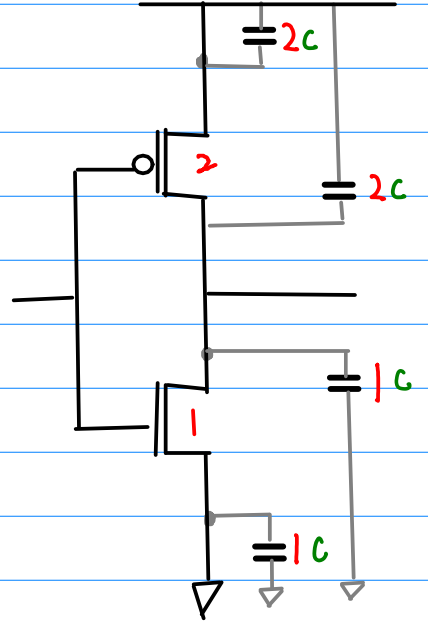
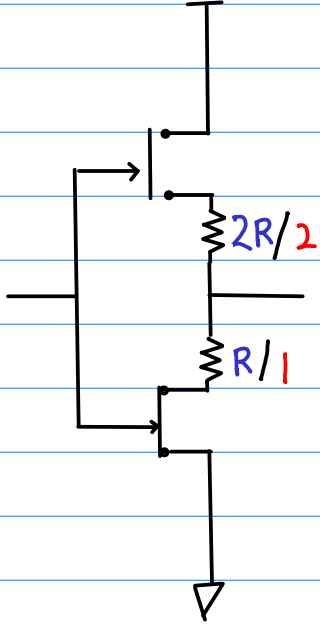
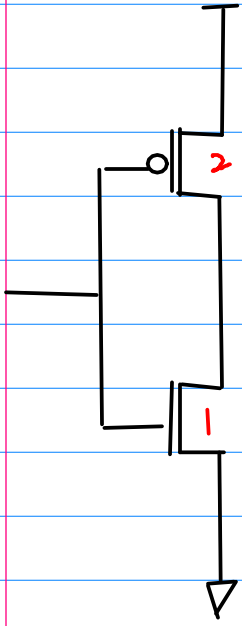
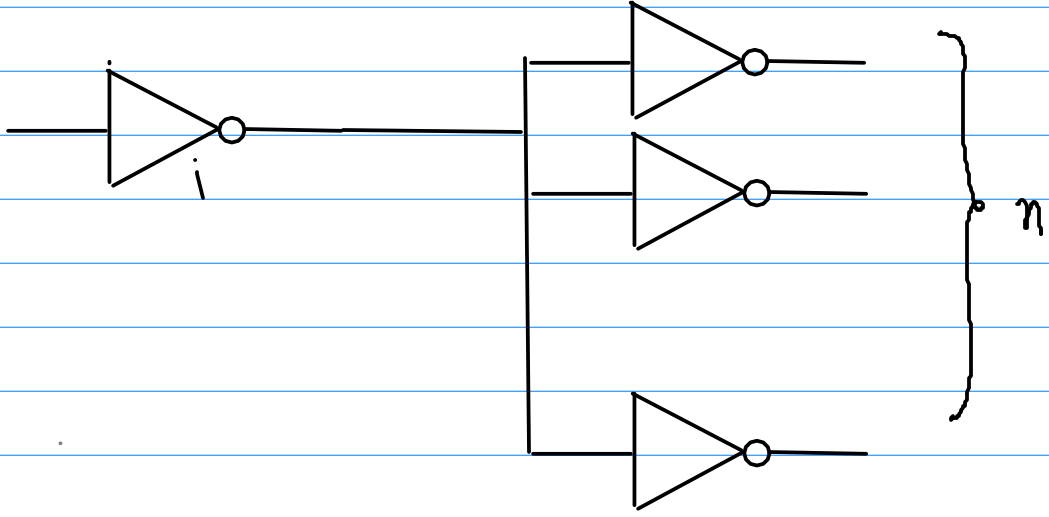
Worst case rising

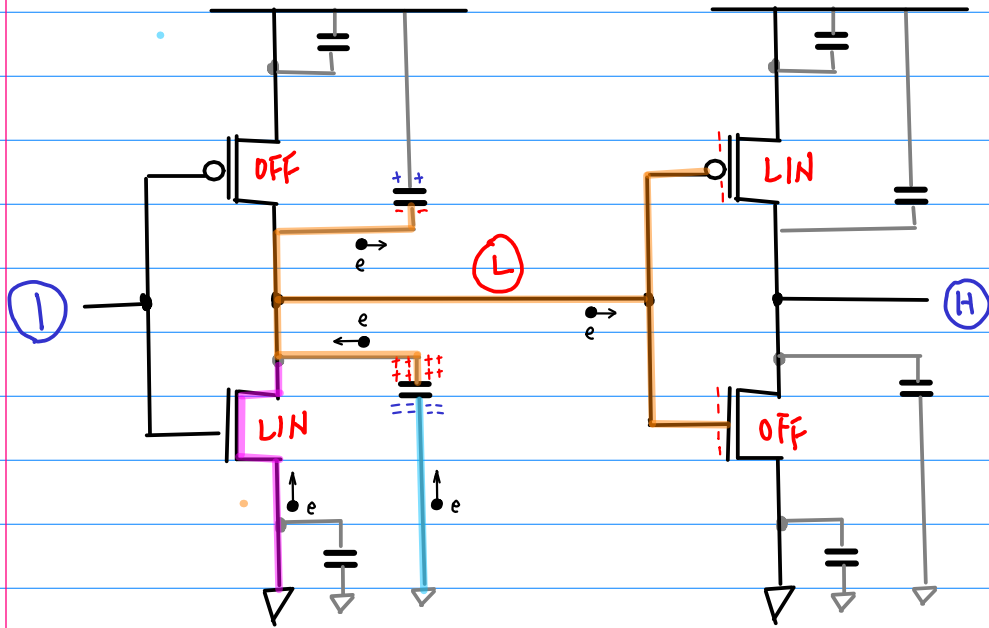
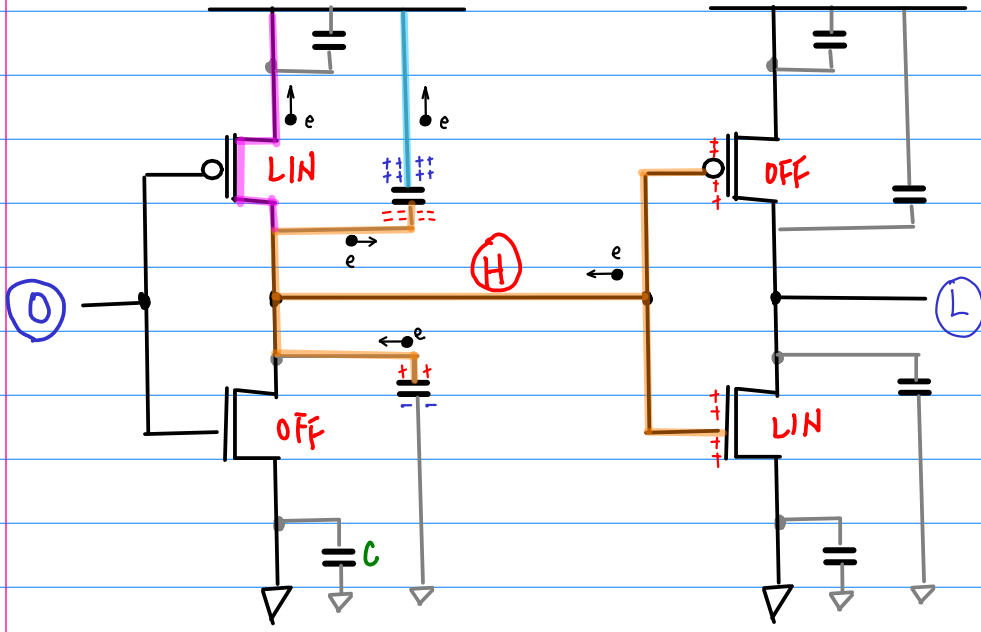


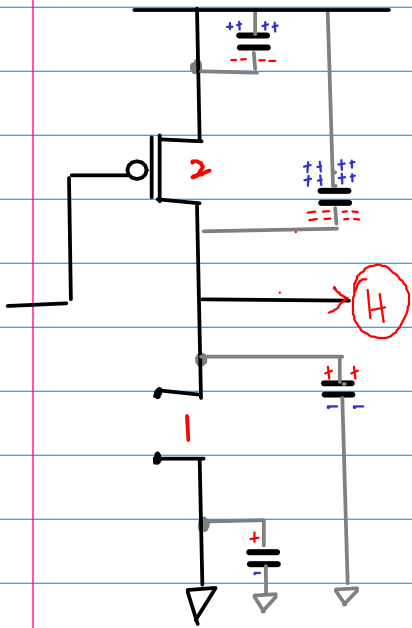
□ Resistance inversely proportional to width



0

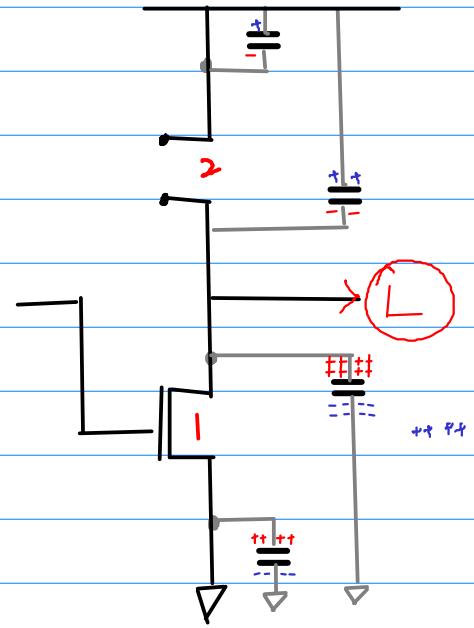




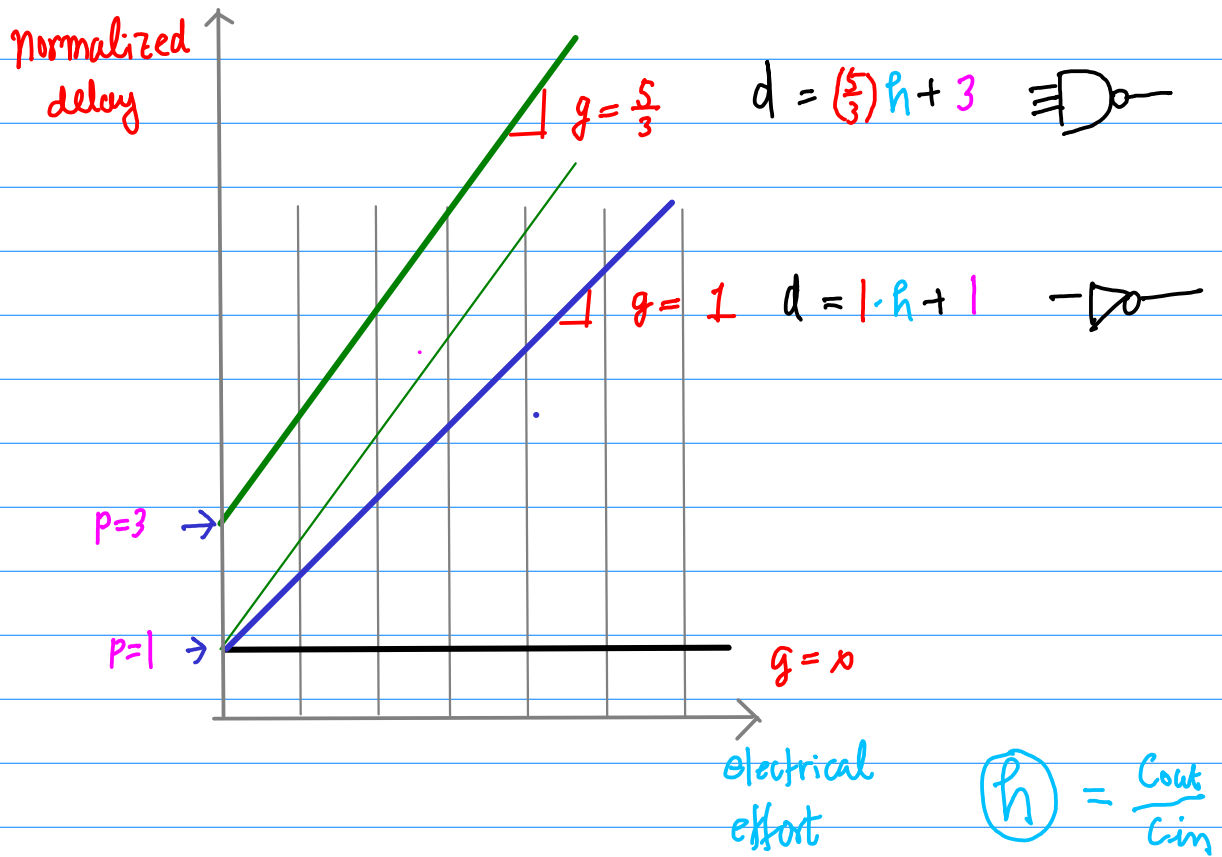


charge +  
discharge -

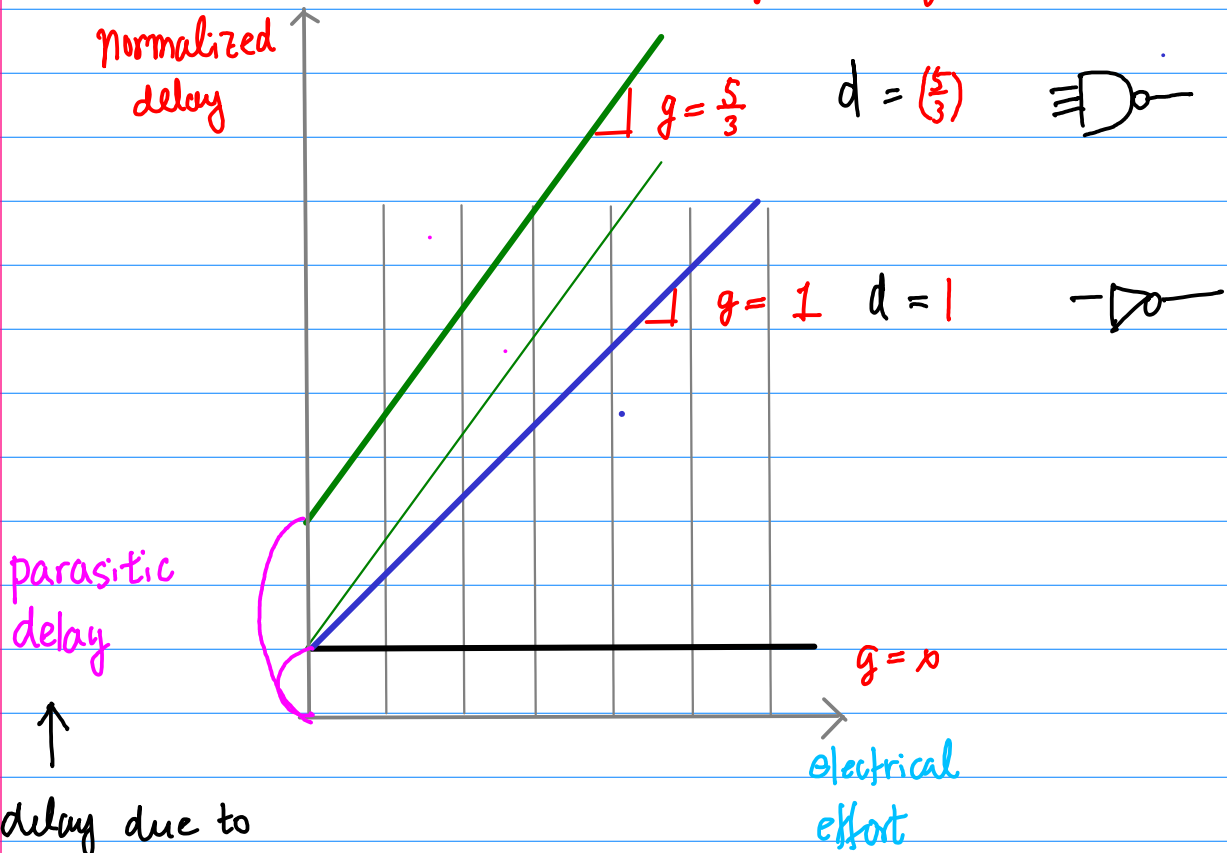
charge +



# Linear Delay Model



Slope : logical effort



delay due to  
only internal cap  
without external load cap

$$d = g \cdot h + p$$

↑     ↑     ↑  
k    c    c





