# Instruction Set Architecture Overview (1A)

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#### Based on

ARM System-on-Chip Architecture, 2<sup>nd</sup> ed, Steve Furber

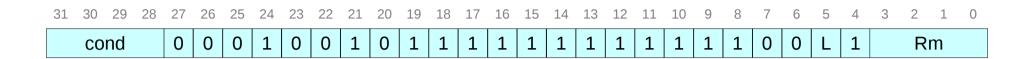
#### **Condition Code**

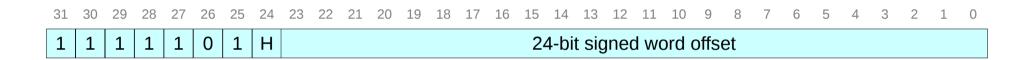
31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

cond

#### Branch and Branch with Link (B, BL)

#### Branch, Branch with Link and eXchange (BX, BLX)





# SWI (Software Interrupt)

## **Data Processing Instructions**

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
cond				0	0 0 #			opcode			S		R	Rn			Rd			Operand 2											

## **ARM Exception Handling**

C R R RRRRRR RR R R R R RR R R R R Ν Ζ V R R R|R|R|R R R

#### References

- [1] ftp://ftp.geoinfo.tuwien.ac.at/navratil/HaskellTutorial.pdf
- [2] https://www.umiacs.umd.edu/~hal/docs/daume02yaht.pdf