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[Look Inside](#)
[Documentation](#)
[Tools](#)
[Links](#)
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Table of Contents

Front Material

1	Introduction
2	MOS Transistor Theory
3	CMOS Processing Technology
4	Delay
5	Power
6	Interconnect
7	Robustness
8	Circuit Simulation
9	Combinational Circuit Design
10	Sequential Circuit Design
11	Datapath Subsystems
12	Array Subsystems
13	Special-Purpose Subsystems
14	Design Methodology and Tools
15	Testing, Debugging, and Verification
A	Hardware Description Languages
	Bibliography (with live links)

Note that some chapters are available here to let you peek inside. The bibliography contains links to the original papers. You need to be at an institution or company with access to IEEE Explore to read the IEEE papers.

제1장 VLSI 세계로의 초대

제2장 디바이스

제3장 동작속도

제4장 전력

제5장 배선

제6장 스케일링, 신뢰도 및 가변성

제7장 SPICE

제8장 게이트

제9장 순차화

제10장 데이터 경로

제11장 메모리

제12장 패키지, 전원, 클럭, I/O

제13장 방법론

제14장 테스트

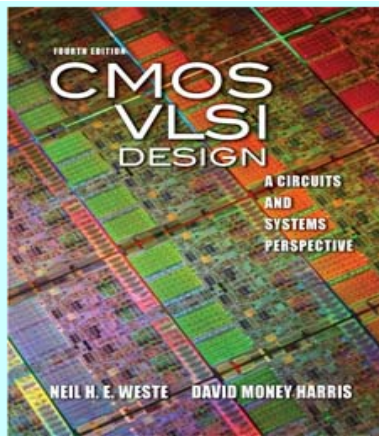
제15장 제조공명

⑬ Special Purpose Subsystems

⑭ Design Methodology and Tools

⑮ Testing, Debugging, and Verification

③ CMOS processing Technology



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Lectures

Lecture	Topic	PowerPoint	PDF
0	Introduction	ppt	pdf
1	Circuits & Layout	ppt	pdf
2	Design Flow	ppt	pdf
3	Transistor Theory	ppt	pdf
4	Nonideal Transistors	ppt	pdf
5	DC & Transient Response	ppt	pdf
6	Logical Effort	ppt	pdf
7	Power	ppt	pdf
8	Simulation	ppt	pdf
9	Combinational Circuit Design	ppt	pdf
10	Circuit Families	ppt	pdf
11	Sequential Circuit Design	ppt	pdf
12	Design for Testability	ppt	pdf
14	Wires	ppt	pdf
15	Scaling	ppt	pdf
16	Pitfalls & Reliability	ppt	pdf
17	Adders	ppt	pdf
18	Datapaths	ppt	pdf
19	SRAM	ppt	pdf
20	ROMs, CAMs, & PLAs	ppt	pdf
21	Packaging, Power, & Clock	ppt	pdf
22	PLLs & DLLs	ppt	pdf
23	I/O	ppt	pdf
24	Microprocessor Hall of Fame	ppt	pdf

The necessities in SOC Design

From Wikiversity

Contents

- 1 **Overview**
- 2 **Fabrication of VLSI Circuits**
- 3 **Device Level Design**
 - 3.1 Performance Metrics
 - 3.2 Device Level Design Tools
- 4 **Transistor Level Design**
 - 4.1 Performance Metric
 - 4.2 Design Issues
 - 4.3 Transistor Level Design Tools
- 5 **Gate Level Design**
 - 5.1 Performance Metric
 - 5.2 Design Issues
 - 5.3 Gate Level Design Tools
- 6 **RTL Level Design**
 - 6.1 Performance Metric
 - 6.2 Design Issues
 - 6.3 RTL Design Tools
- 7 **Architecture Level Design**
 - 7.1 Design Issues
 - 7.2 Design Tools
- 8 **System Level Design**
 - 8.1 Typical SOC's
 - 8.2 Design Issues
 - 8.3 Design Tools
- 9 **Design Flow**
 - 9.1 Design Examples
 - 9.2 RTL / Logic Level Design
 - 9.3 Physical Design
- 10 **Printed Circuit Board**
- 11 **Test**
- 12 **Logical Verification**
- 13 **References**

Overview

- SoC in the wikipedia pages (pdf)
- Some useful links in VLSI design (pdf)

- HW#1 (pdf)
- HW#2 (pdf)

Fabrication of VLSI Circuits

- Fabrication in the wikipedia pages (pdf)
- Wafer (pdf)
- Mask (pdf)
- Package (pdf)
- Test (pdf)

- CMOS Fabrication (pdf)

Device Level Design

- MOSFET Transistor (pdf)
- CMOS Inverter (pdf)

- Digital Implementation (pdf) - ASIC, FPGA
- Analog Implementation (pdf) - Linear IC, Power IC, RF IC, Mixed Signal IC

Performance Metrics

- Device R, C (pdf)
- Device Size (pdf)
- Device Delay (pdf)

- [Device Power \(pdf\)](#)

Device Level Design Tools

- Spice Simulator
- VLSI CAD tools - Layout, Floorplanning, Placement and Routing, Physical Verification (LVS/DRC/ERC)

Transistor Level Design

- [Combinational Designs \(pdf\)](#)
- [Sequential Designs \(pdf\)](#)
- [Subsystem](#)
 - [Arithmetic Subsystem \(pdf\)](#)
 - [Memory Array Subsystem \(pdf\)](#)
 - Logic Array Subsystem

Performance Metric

- Gate Area (pdf)
- Gate Delay (pdf)
- Gate Power (pdf)

Design Issues

- Clock
- PLL & DLL
- I/O

Transistor Level Design Tools

- Spice

Gate Level Design

- [Combinational Designs \(pdf\)](#)
- [Sequential Designs \(pdf\)](#)
- [Subsystem](#)
 - [Arithmetic Subsystem \(pdf\)](#)
 - [Memory Array Subsystem \(pdf\)](#)
 - Logic Array Subsystem

Performance Metric

- Gate Count
- Path Delay (pdf)
- Switch Activity (pdf)

Design Issues

- Static Timing Analysis
- Scan and Boundary Scan Cells
- Formal Verification

Gate Level Design Tools

- Verilog
- VHDL
- Static Timing Analysis
- Formal Verification

RTL Level Design

- [Register \(pdf\)](#)
- [FSM \(pdf\)](#)
- One Hot Controller
- [Pipeline \(pdf\)](#)

Performance Metric

- Estimation of

4/12/2016

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- Gate Count
- Critical Path
- Power
- Latency
- Throughput

Design Issues

- Partitioning and Coding Style
- Constraining Designs
- Optimizing Designs
- Design for Test (DFT)
- Pre-layout & Post-layout Simulation

RTL Design Tools

- Verilog
- VHDL
- Logic Synthesis

Architecture Level Design

- Tiny CPU Examples (pdf)

- CISC, RISC, VLIW, Dataflow

- CPU, DSP, GPU, NPU

- MCU, ASIP, TTA

Design Issues

- Memory Hierarchy
- Storage and I/O
- Instruction Level Parallelism
- Data Level Parallelism
- Thread Level Parallelism

Design Tools

- ADL (Architecture Design Language)
 - LISA
 - EXPRESSION
 - nML

System Level Design

- IP
- OCP-IP, OpenCore
- Transaction Level Modeling

Typical SOC's

- Embedded System
- MPSOC
- NoC

Design Issues

- Hardware Software Partition
- Hardware Software Co-simulation
- Integration of Hardware IP Blocks
- Integration of Software IP Modules
- FPGA Based Emulation Platform

Design Tools

- High-Level Synthesis
- HVL (High-Level Verification Language)
 - SystemC (See "SystemC programming in plain view")
 - SystemVerilog
- Mixed Signal
 - VHDL-AMS
 - Verilog-AMS

Design Flow

Design Examples

- RTL Design Examples (pdf)
- Gate Level Design Examples (pdf)
- Transistor Level Design Examples (pdf)

RTL / Logic Level Design

- Logic Synthesis
- Logic Simulation
- Logic Timing Verification
- Logic Power Verification
- Test Synthesis
- Test Verification
- Testbench
- Code Coverage
- Equivalence Check
- Timing Verification
- Design Constraint
- STA (Static Timing Analysis)
- Scan Chain
- Back Annotation
- ATPG (Automatic Test Pattern Generation)

Physical Design

- Floorplanning
- Placement
- Routing
- Power Network
- Clock Distribution
- Physical Verification
- DRC (Design Rule Check)
- DV (Design Verification)
- GV (Geometry Verification)
- LVS (Layout Versus Schematic)
- SV (Schematic Verification)

Printed Circuit Board

Test

- Design For Test
- ATPG (Automatic Test Pattern Generation)
- Analog and Mixed Signal Test
- JTAG (Joint Test Action Group) IEEE 1149.1
- Embedded Core Test IEEE 5000

test access mechanisms (TAMs)
Core test language (CTL)

Logical Verification

- Assertion Based Verification
- Transaction Level Models
- Formal Property Verification

References

- The necessities in Digital Design
- The necessities in Computer Design
- The necessities in Computer Architecture
- The necessities in Computer Organization
- Understanding VLSI Design
- VHDL programming in plain view"
- SystemC programming in plain view"

asic-world.com (<http://asic-world.com/systemc/index.html>)

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ASIC design flow (lth.edu) (http://www.eit.lth.se/fileadmin/eit/courses/etin01/manual_etc/dasic.pdf)

For Tiny CPU, See

Tiny CPU (http://www.ele.uri.edu/Courses/ele405/f07/Tiny_Doc.pdf)

For general buses, See

PCI bus

(<http://www.uio.no/studier/emner/matnat/fys/FYS3240/v11/undervisningsmateriale/forelesninger/Lecture5%20%20Computer%20buses%20and%20interfaces.pdf>)

general buses (<http://www.ece.cmu.edu/~ece548/handouts/18bus.pdf>)

old buses (<http://www.taoli.ece.ufl.edu/teaching/4744/private/lectures/lecture6-part1-4pg.pdf>)

For AMBA, See

Embedded Processor & AMBA (<http://www.eit.lth.se/fileadmin/eit/courses/eti135/slides/EmbeddedProcessors.pdf>)

AMBA overview (<http://web.mit.edu/clarkds/www/Files/ahblite.pdf>)

For DDR, See

DDR overview (<http://www.micron.com/~media/Documents/Products/Technical%20Note/DRAM/TN4605.pdf>)

DDR (<http://www.ece.umd.edu/~blj/talks/DRAM-Tutorial-isca2002.pdf>)

For UART, See

UART Overview (<http://www.cs.ucsb.edu/~chris/teaching/cs170/doc/cs170-11.pdf>)

ARM UART Notes (<http://csserver.evansville.edu/~blandfor/EE311/ARMLecture/UARTNotes.pdf>)

For DMA, See

DMA Overview (<http://www.pmar.it/ce2/common/local/dma.pdf>)

DMA & IO (<http://www.cs.utah.edu/~rajeev/cs3810/slides/3810-22.pdf>)

DMA & OS (<http://www.cs.ucsb.edu/~chris/teaching/cs170/doc/cs170-11.pdf>)

For Embedded Programming, See

Embedded Programming (http://www.cis.upenn.edu/~lee/06cse480/lec-into_to_prog_embedded_systems.pdf)

Discovering STM32 microcontroller (<http://www.cs.indiana.edu/~geobrown/book.pdf>)

For TLM, See

TLM Overview (http://www.ict.kth.se/courses/IL2452/Aug2012/Lectures/TLM_4in1_2012.pdf)

TLM (<http://www.cs.rice.edu/~vardi/comp607/TLMwithSystemC.pptx>)

TLM & AMBA (<http://www.scarpaz.com/2100-papers/SystemC/01186667.pdf>)

For the final, Computer Arch

VHDL Primer (upenn.edu) (http://www.seas.upenn.edu/~ese171/vhdl/vhdl_primer.html)

ASIC design flow (lth.edu) (http://www.eit.lth.se/fileadmin/eit/courses/etin01/manual_etc/dasic.pdf)

Tiny CPU (http://www.ele.uri.edu/Courses/ele405/f07/Tiny_Doc.pdf)

Memory

DRAM (<http://upload.wikimedia.org/wikiversity/en/1/10/CDesign.2.A.DRAM.20130527.pdf>)

GPIO, UART, DMA, Int/Poll

UART Overview (<http://www.cs.ucsb.edu/~chris/teaching/cs170/doc/cs170-11.pdf>)

GPIO Programming (http://elinux.org/images/3/33/GPIO_Programming_on_the_Beaglebone.pdf)

AMBA Bus

ARM (<http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.ih0011a/index.html>)

TLM

TLM (<http://www.cs.rice.edu/~vardi/comp607/TLMwithSystemC.pptx>)

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