

# Tiny CPU

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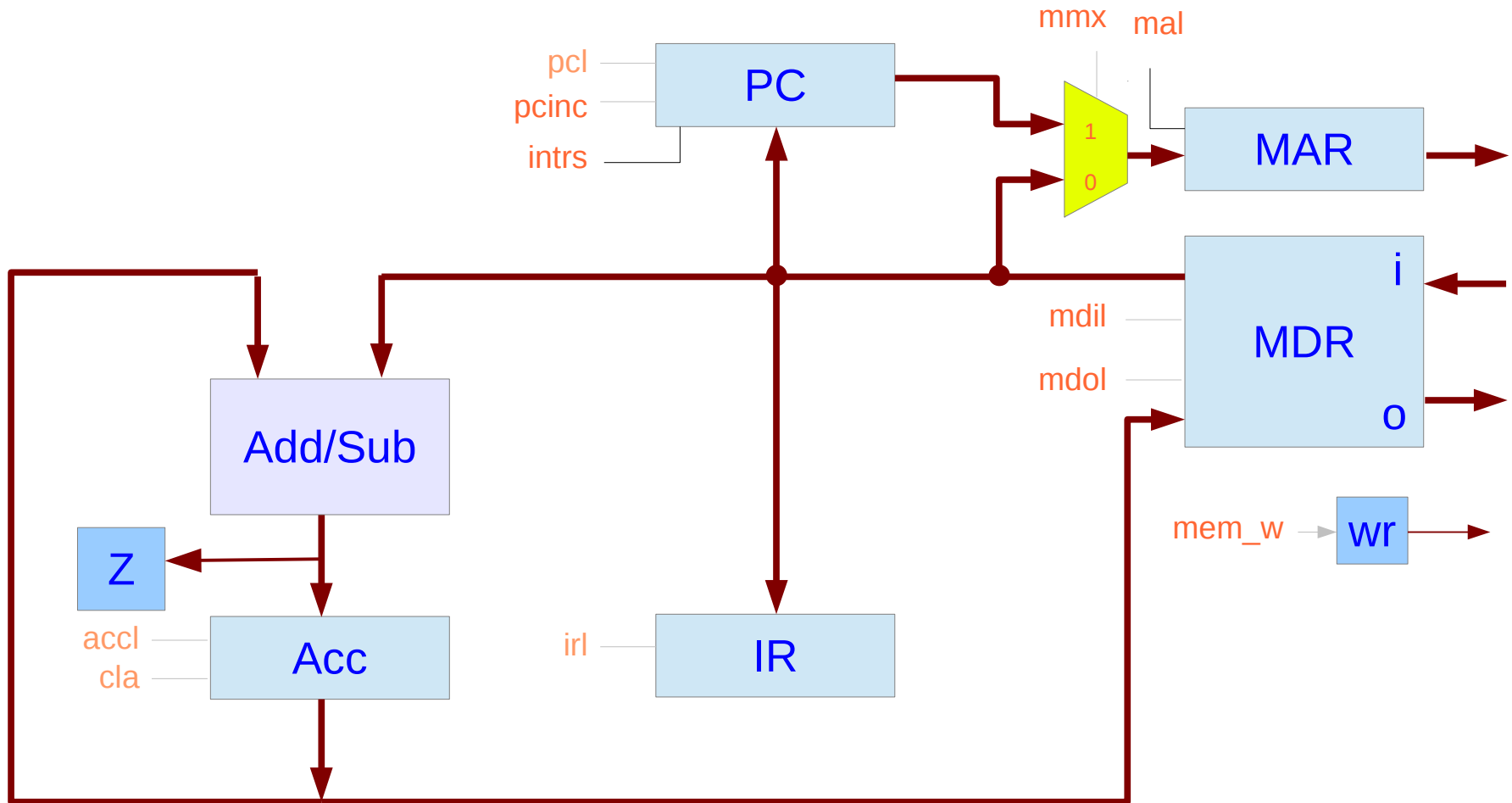
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Please send corrections (or suggestions) to [youngwlim@hotmail.com](mailto:youngwlim@hotmail.com).

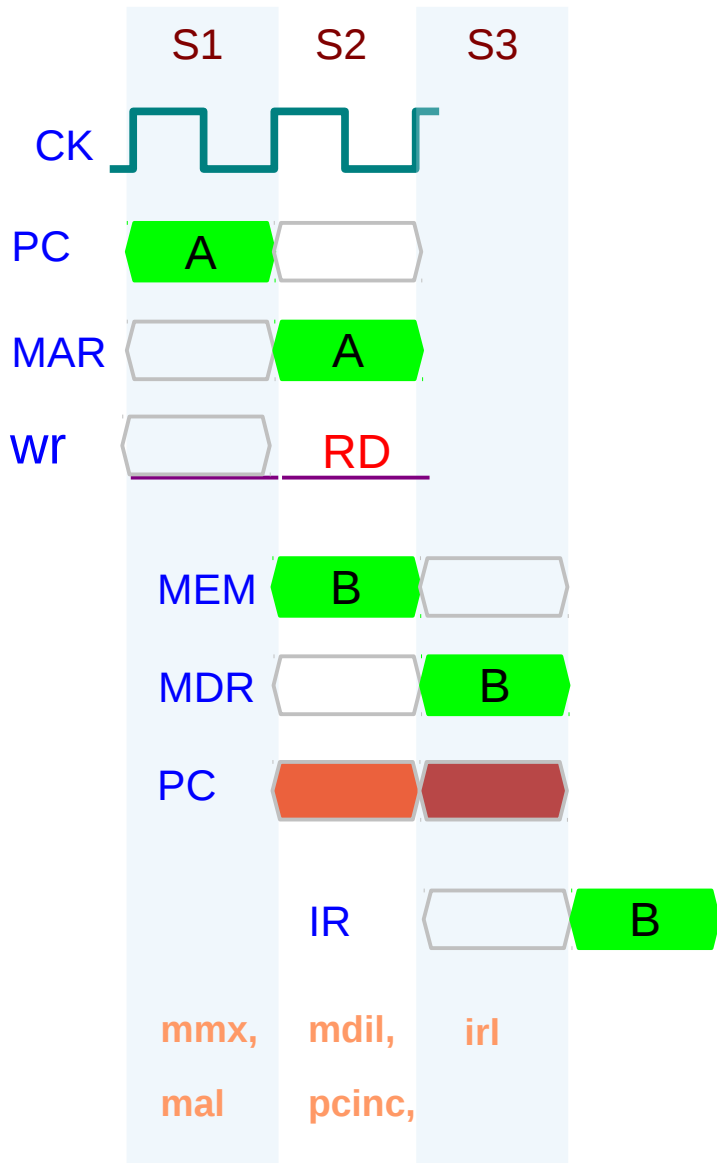
This document was produced by using OpenOffice and Octave.

# Data Path



Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>

# IF (S1,S2,S3)

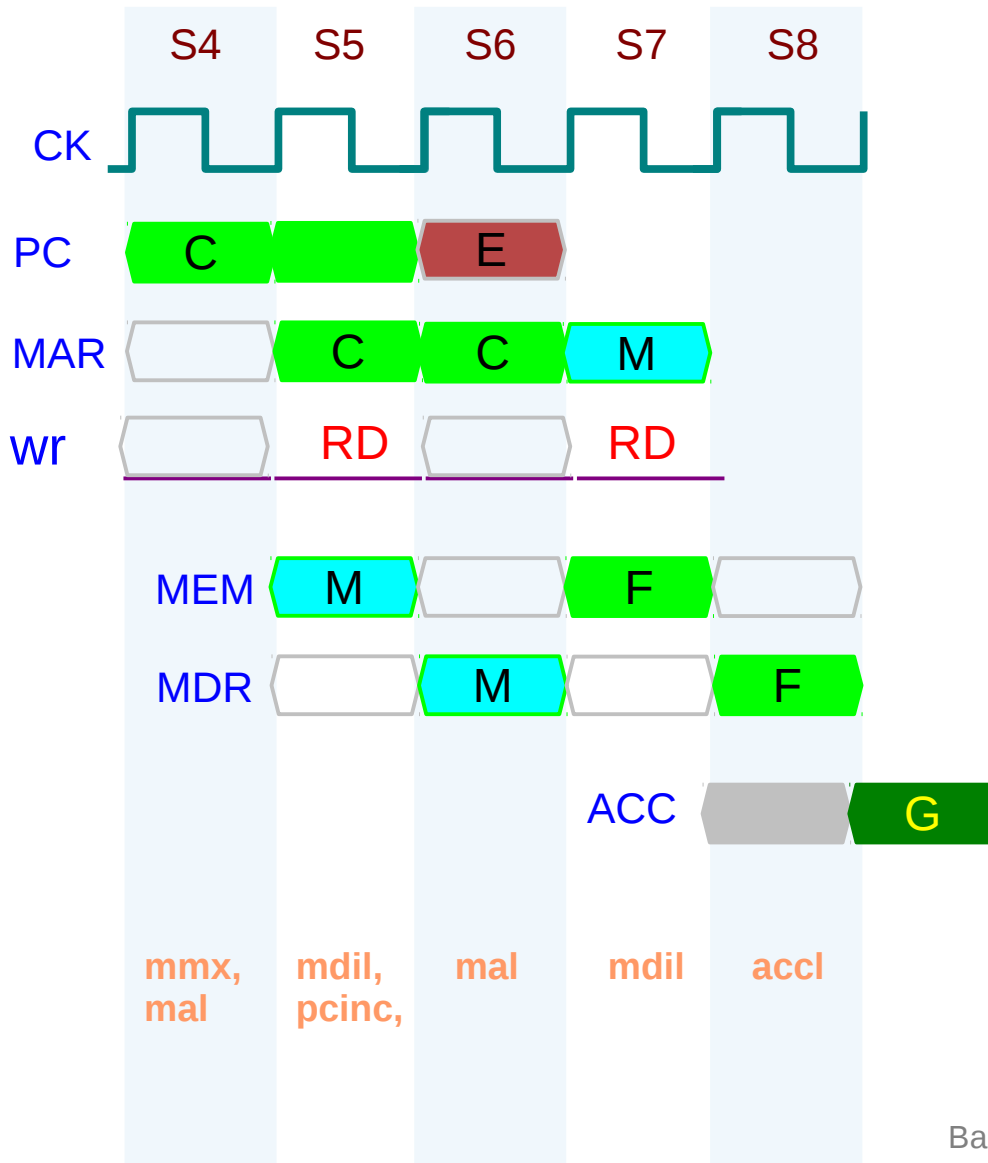


S1 MAR  $\leftarrow$  PC; MEM\_RD;  
 S2 MDR  $\leftarrow$  MEM; PC  $\leftarrow$  PC+1;  
 S3 IR  $\leftarrow$  MDR

	IR[7:5]
ADD	001
STR	010
CLA	011
JNZ	101
RST	111

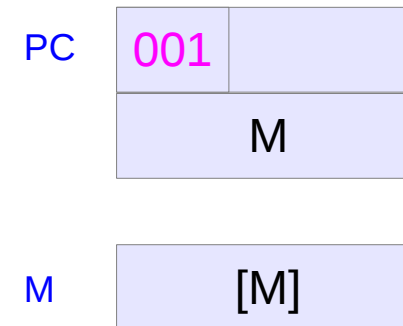
Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>

# ADD (S4,S5,S6,S7,S8)



S4 MAR ← PC; MEM\_RD  
 S5 MDR ← MEM; PC ← PC+1  
 S6 MAR ← MDR; MEM\_RD  
 S7 MDR ← MEM;  
 S8 ACC ← ACC + MDR;

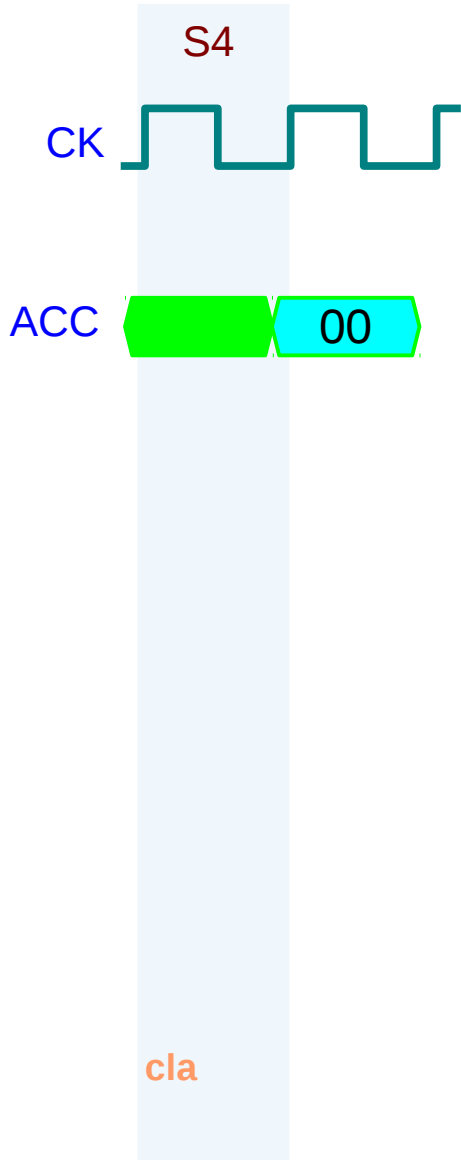
**ADD** \$M ; ACC ← ACC + [M]



Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>



# CLA (S4)



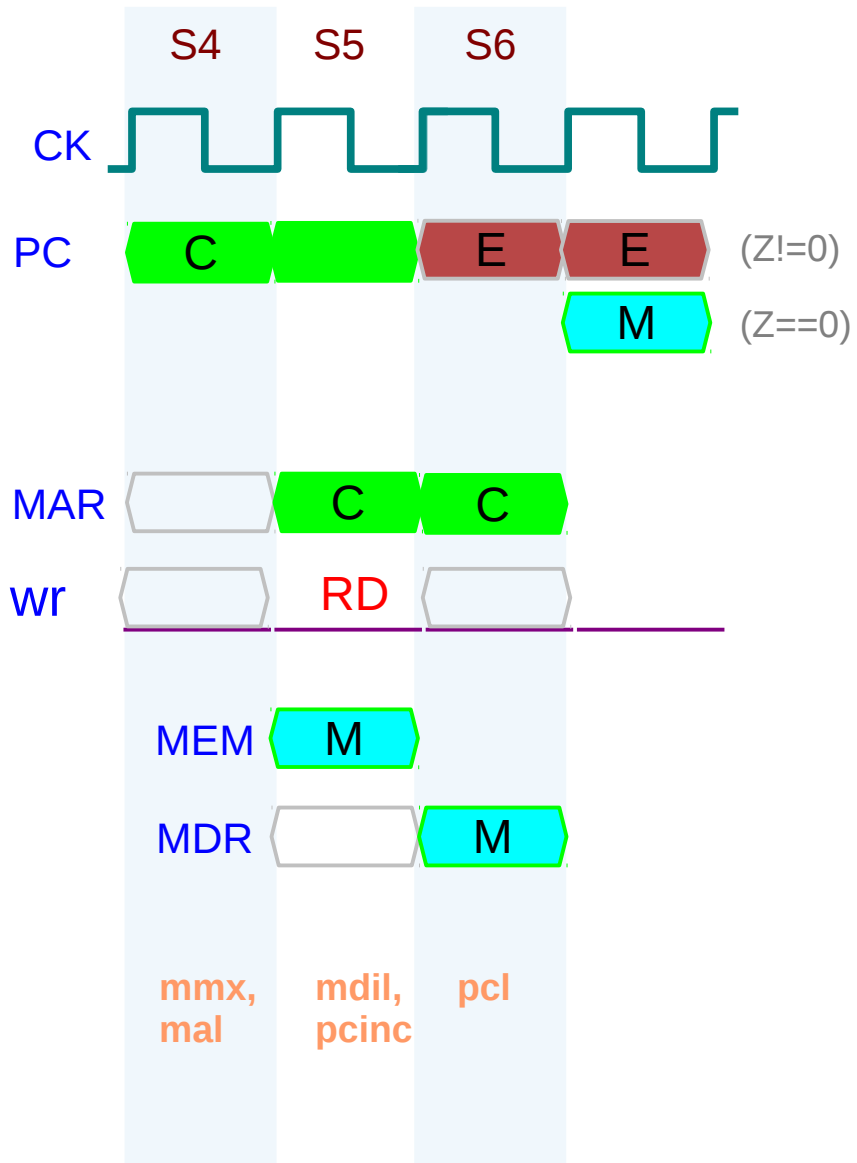
S4 ACC ← "00"

CLA ; ACC ← 0

PC 011

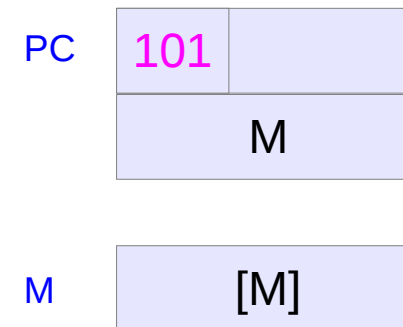
Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>

# JNZ (S4,S5,S6)



S4 MAR  $\leftarrow$  PC; MEM\_RD;  
 S5 MDR  $\leftarrow$  MEM; PC  $\leftarrow$  PC + 1  
 S6 If (Z=='0') PC  $\leftarrow$  MDR;

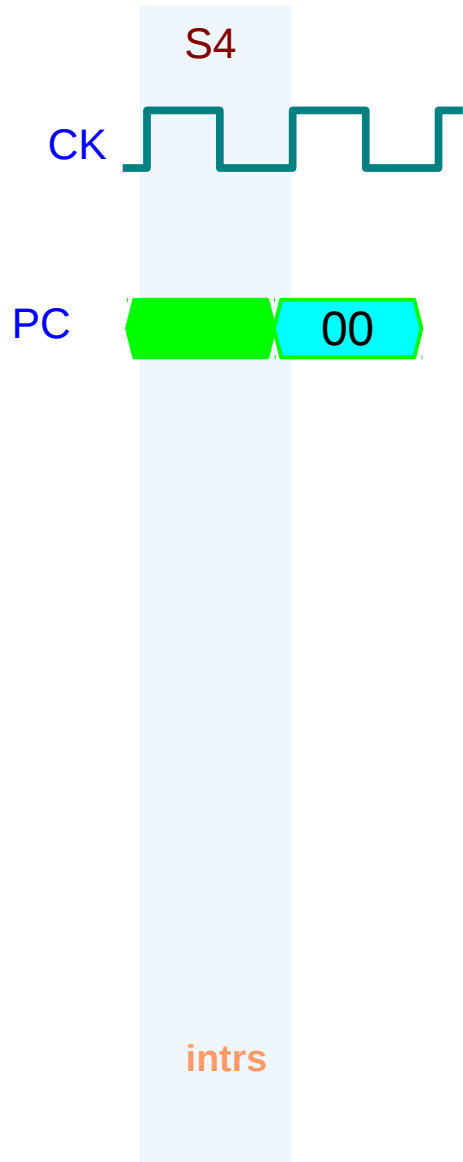
JNZ \$M ; PC  $\leftarrow$  [M] if Z=0



Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>



# RST (S4)



S4 PC ← "00";

RST ; PC ← 0

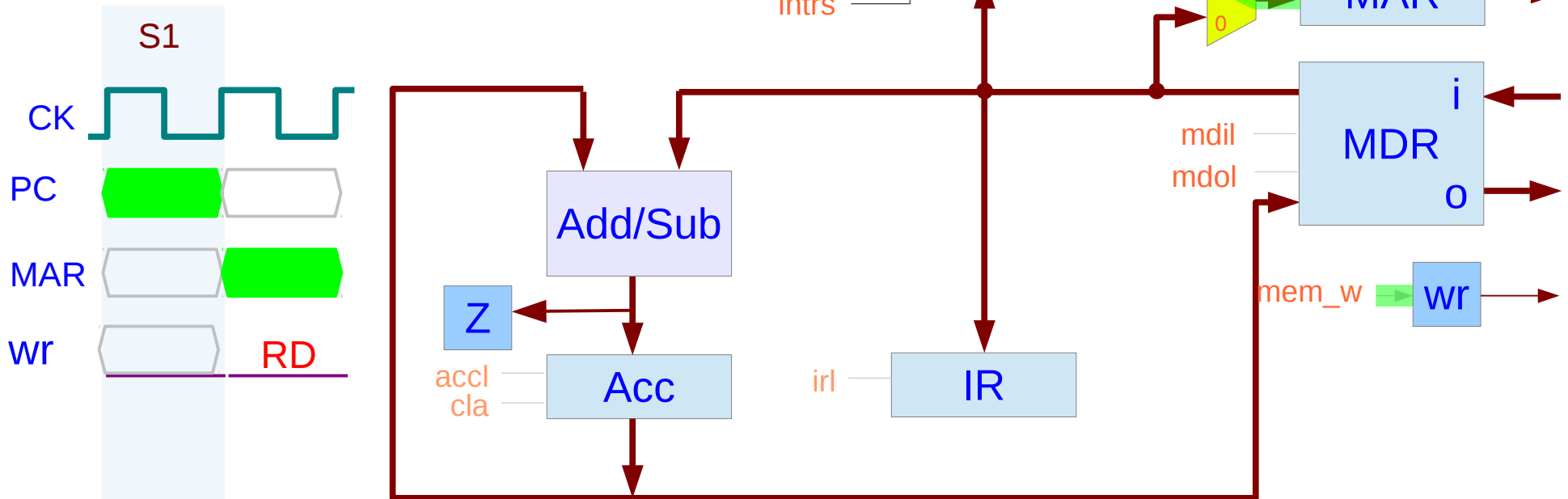


Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>



# Data Path (IF, S1)

MAR ← PC; MEM\_RD;



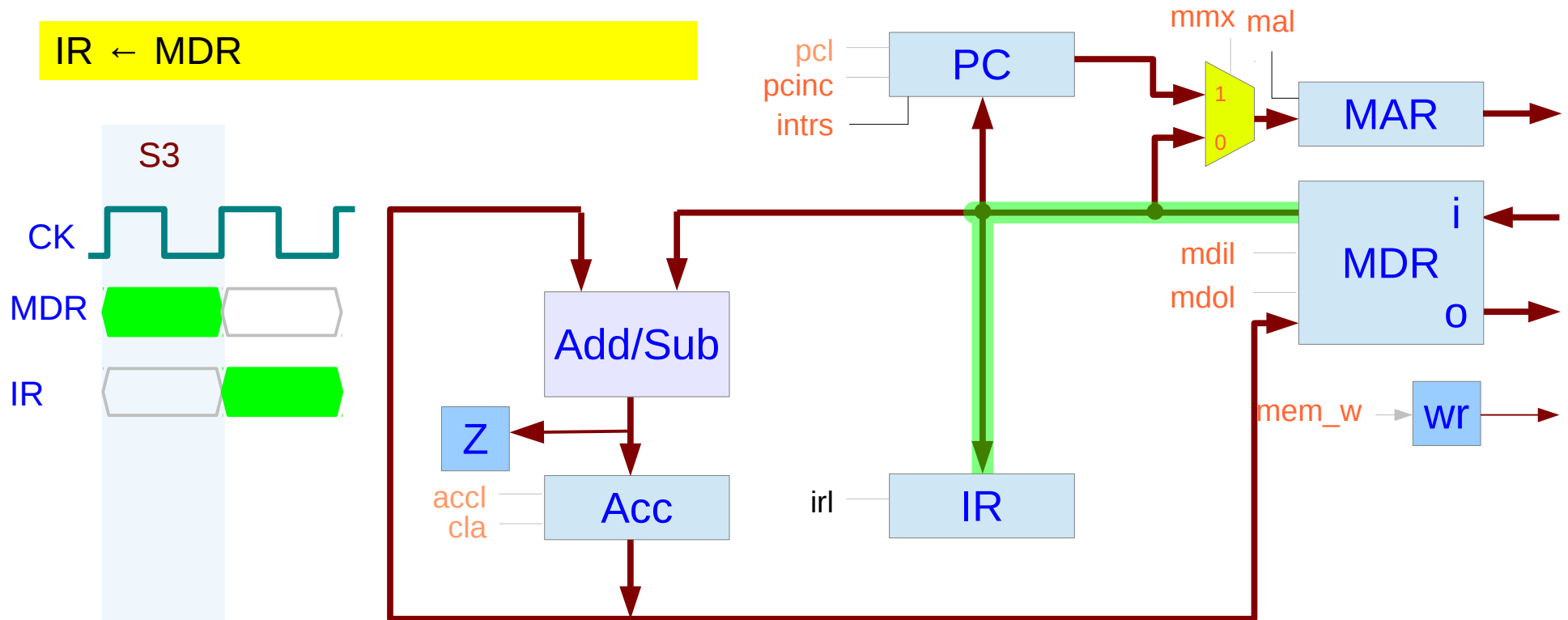
mmx,

mal

Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>



# Data Path (IF, S3)



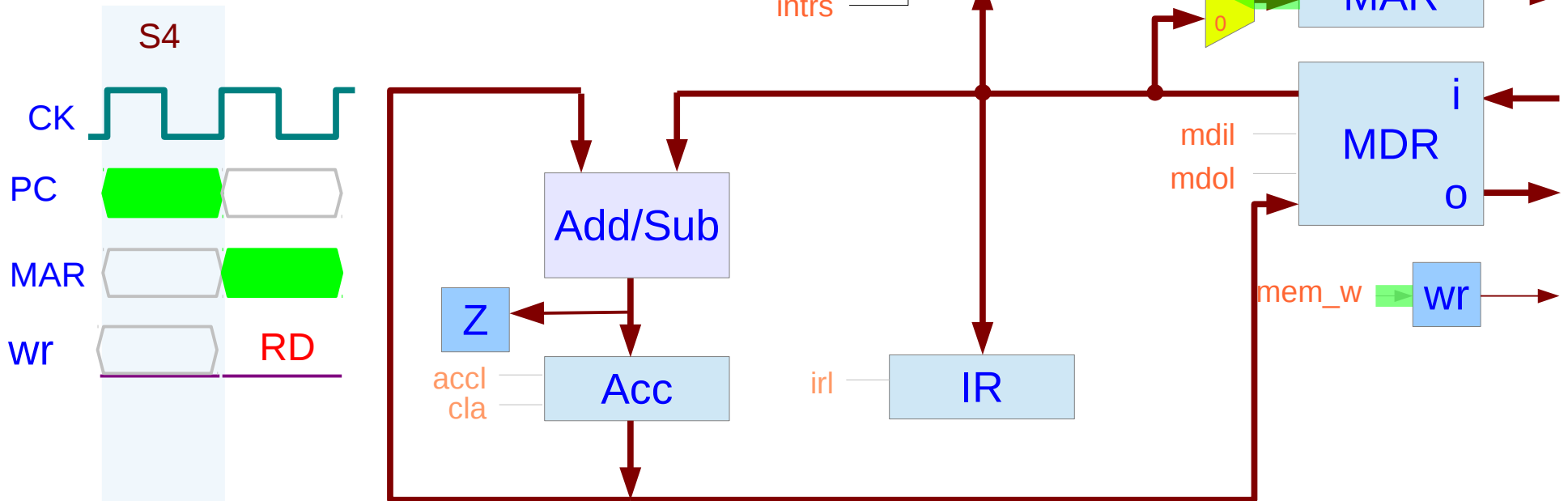
irl

Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>



# Data Path (ADD, S4)

MAR ← PC; MEM\_RD

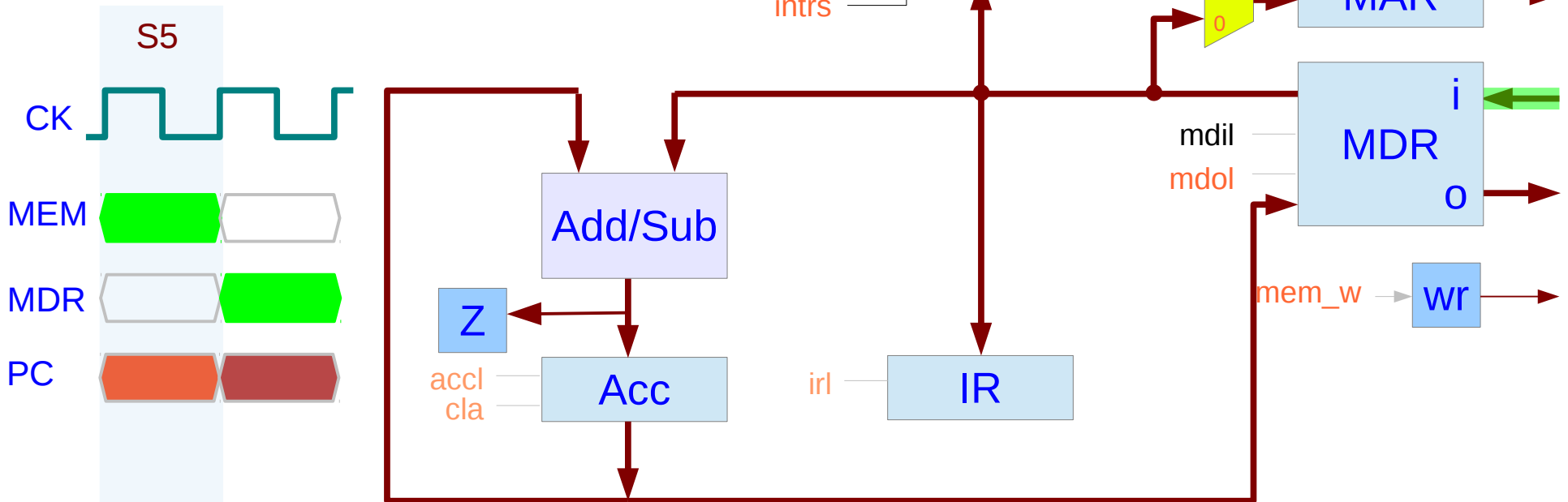


mmx,  
mal

Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>

# Data Path (ADD, S5)

MDR ← MEM; PC ← PC+1



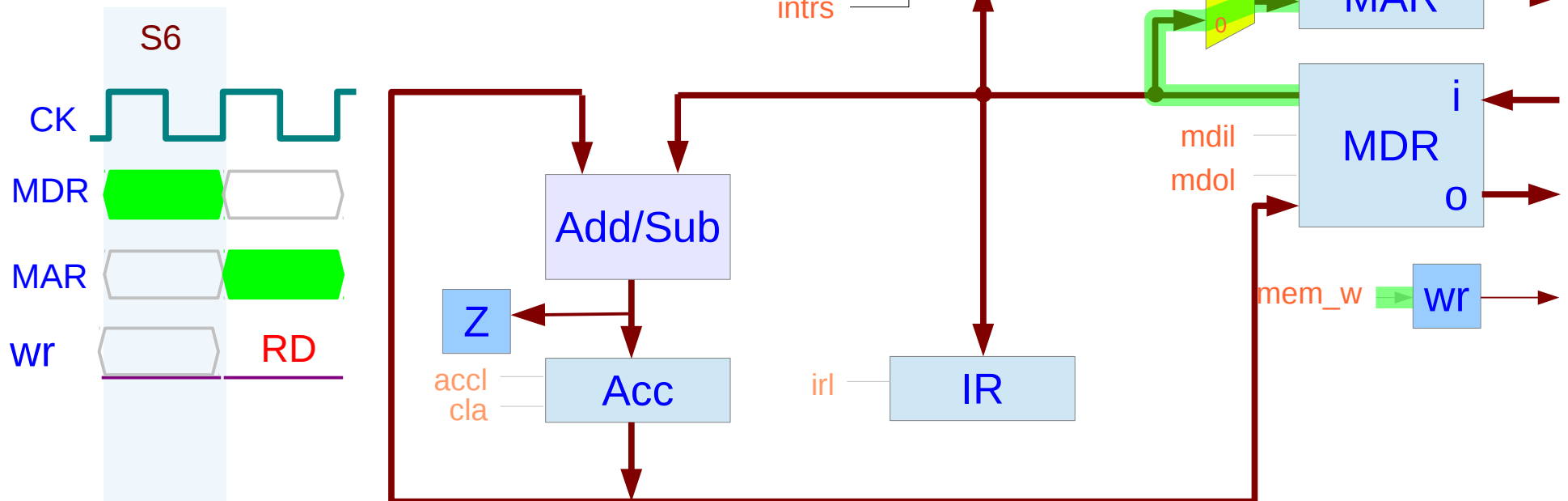
mdil,  
pcinc,

Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>



# Data Path (ADD, S6)

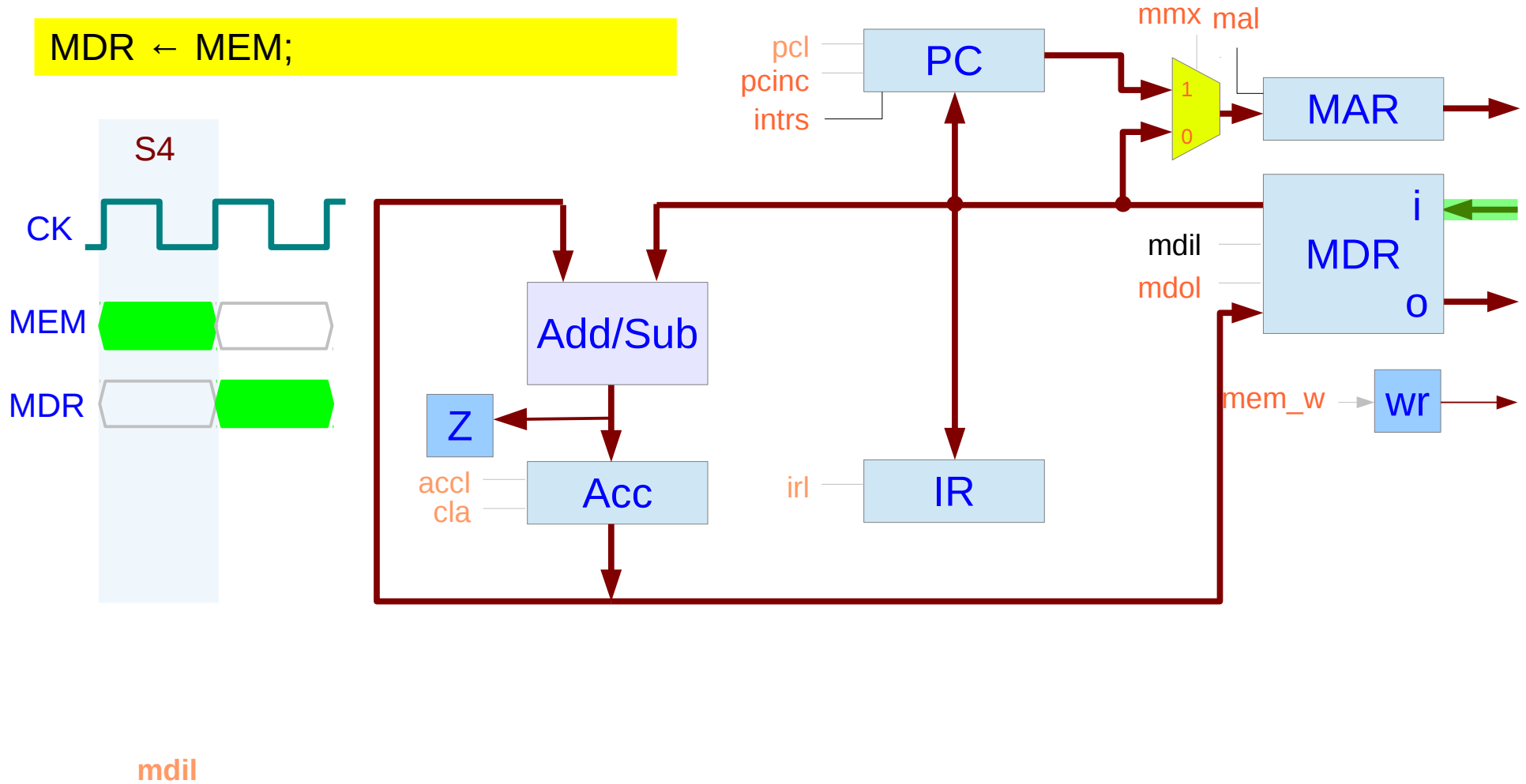
MAR ← MDR; MEM\_RD



mal

Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>

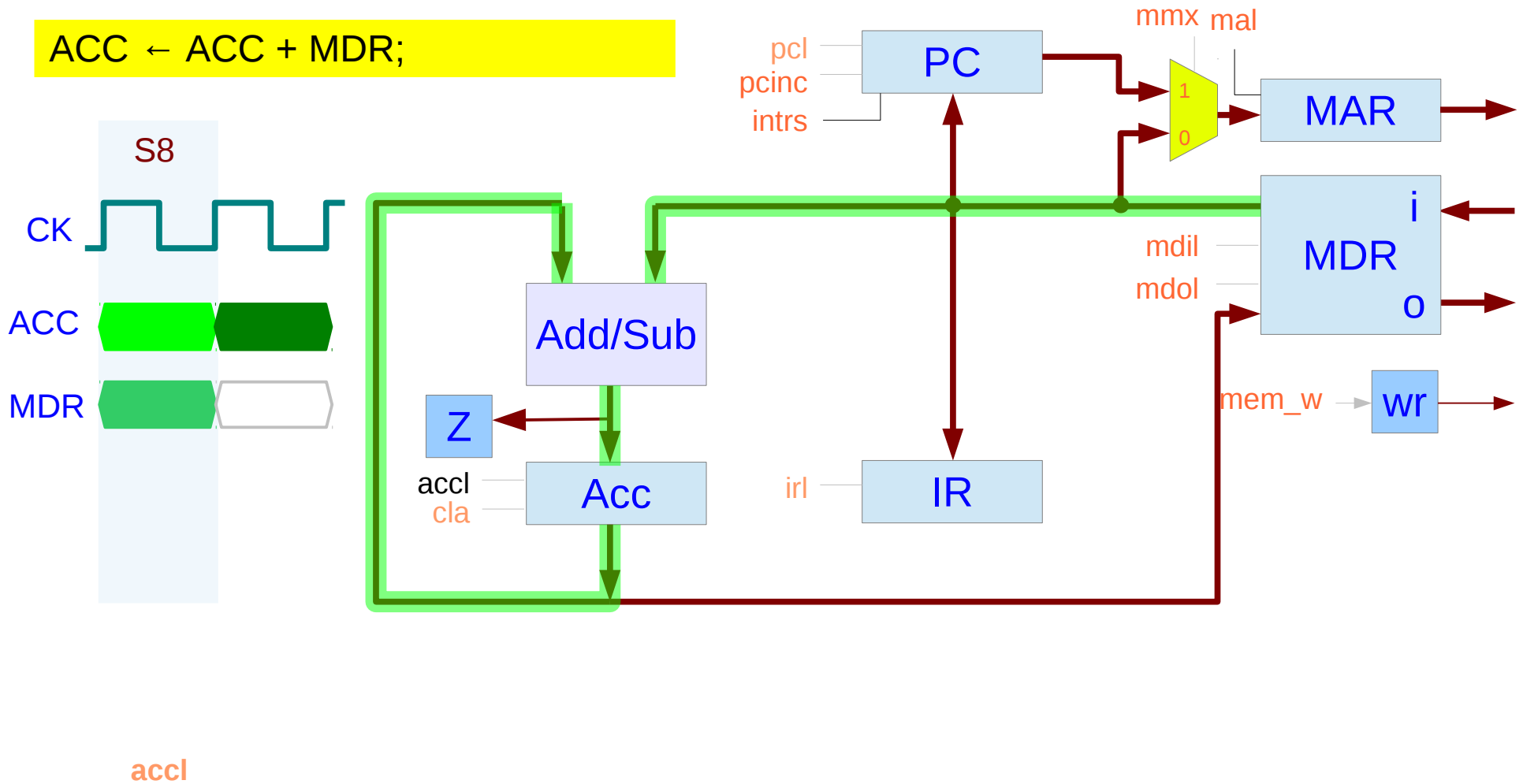
# Data Path (ADD, S7)



Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>

# Data Path (ADD, S8)

ACC ← ACC + MDR;

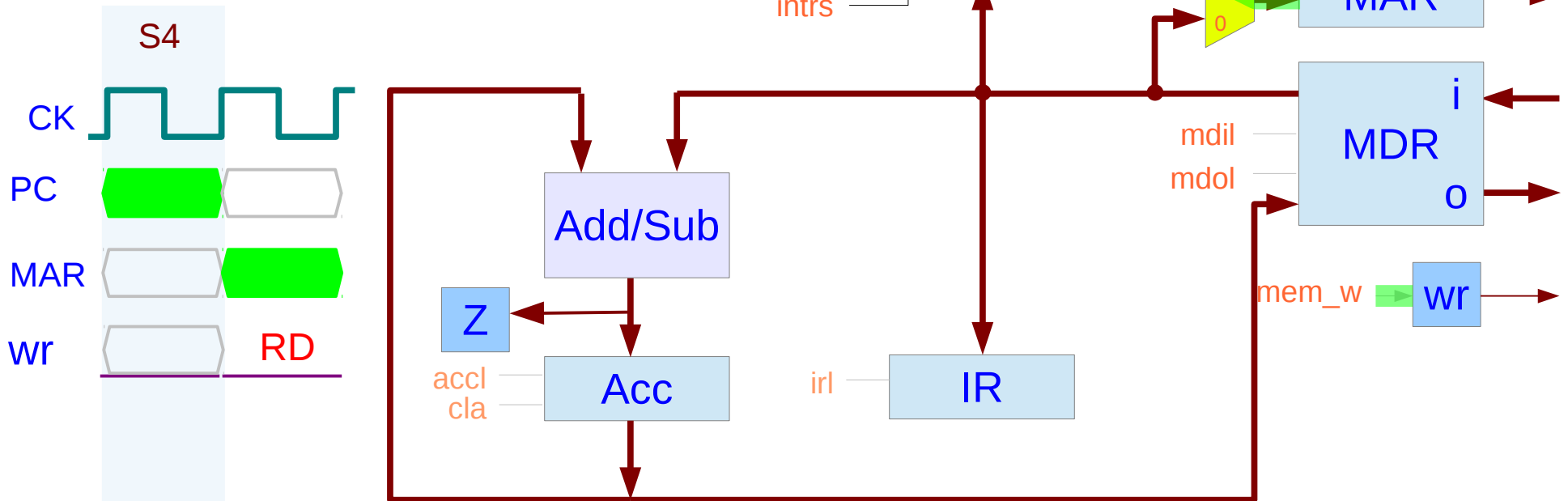


Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>



# Data Path (STR, S4)

MAR ← PC; MEM\_RD

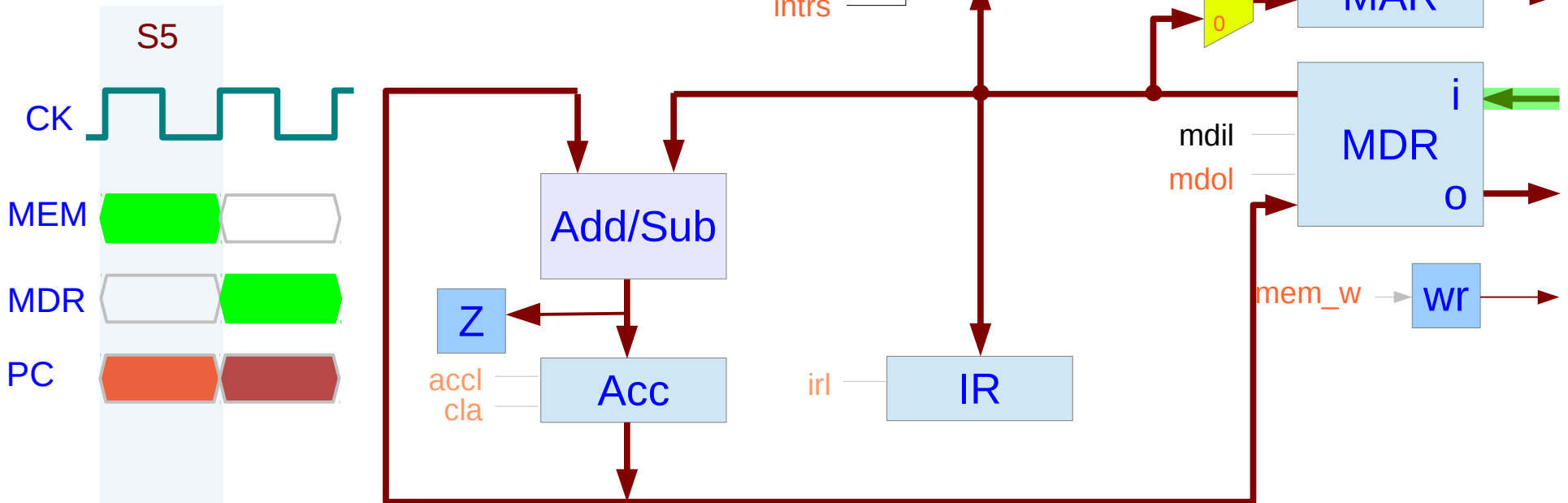


mmx,  
mal

Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>

# Data Path (STR, S5)

MDR ← MEM; PC ← PC + 1

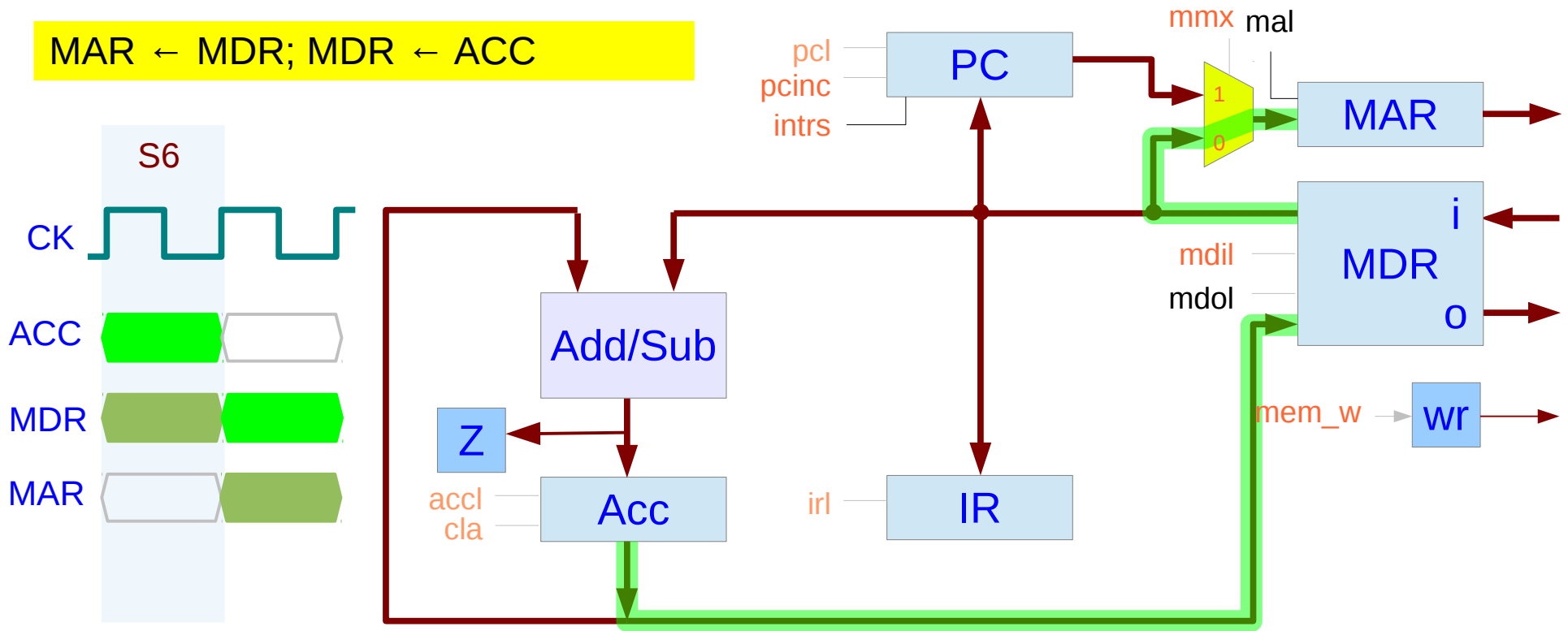


mdil,  
pcinc

Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>

# Data Path (STR, S6)

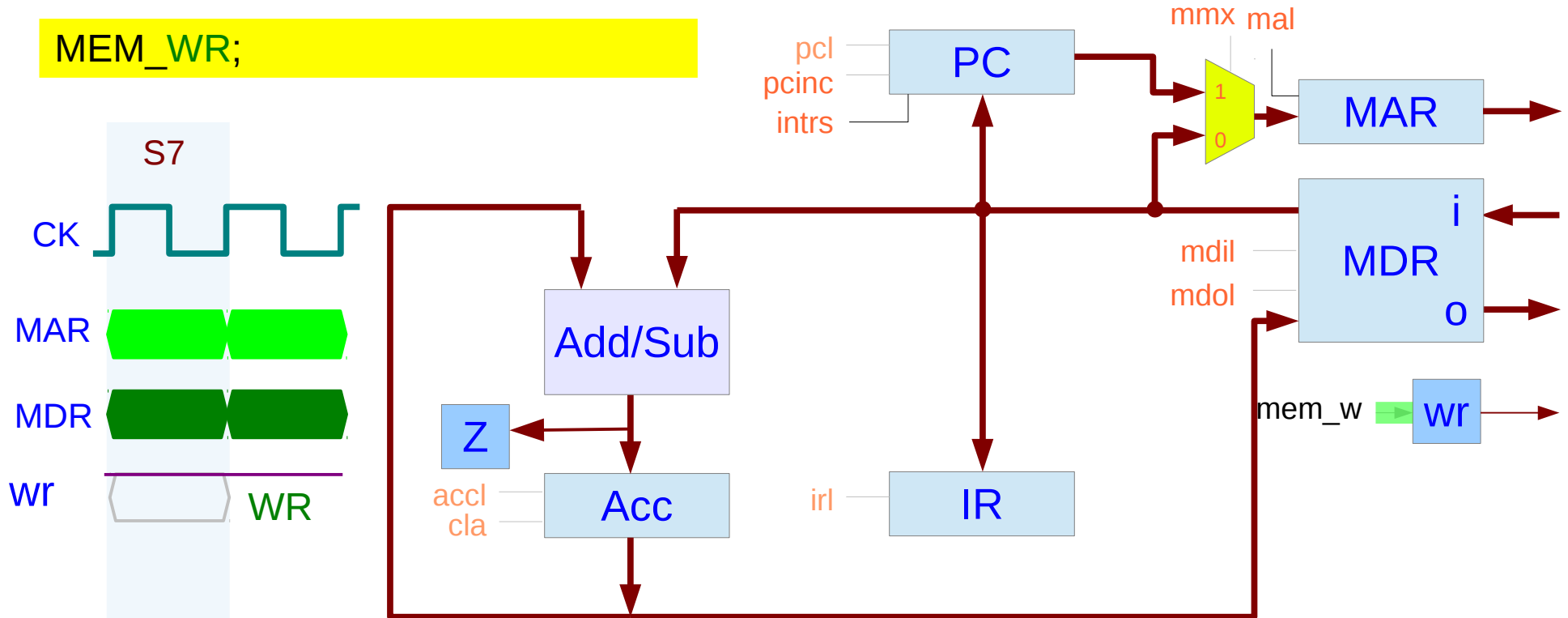
MAR ← MDR; MDR ← ACC



mal,  
mdol

Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>

# Data Path (STR, S7)



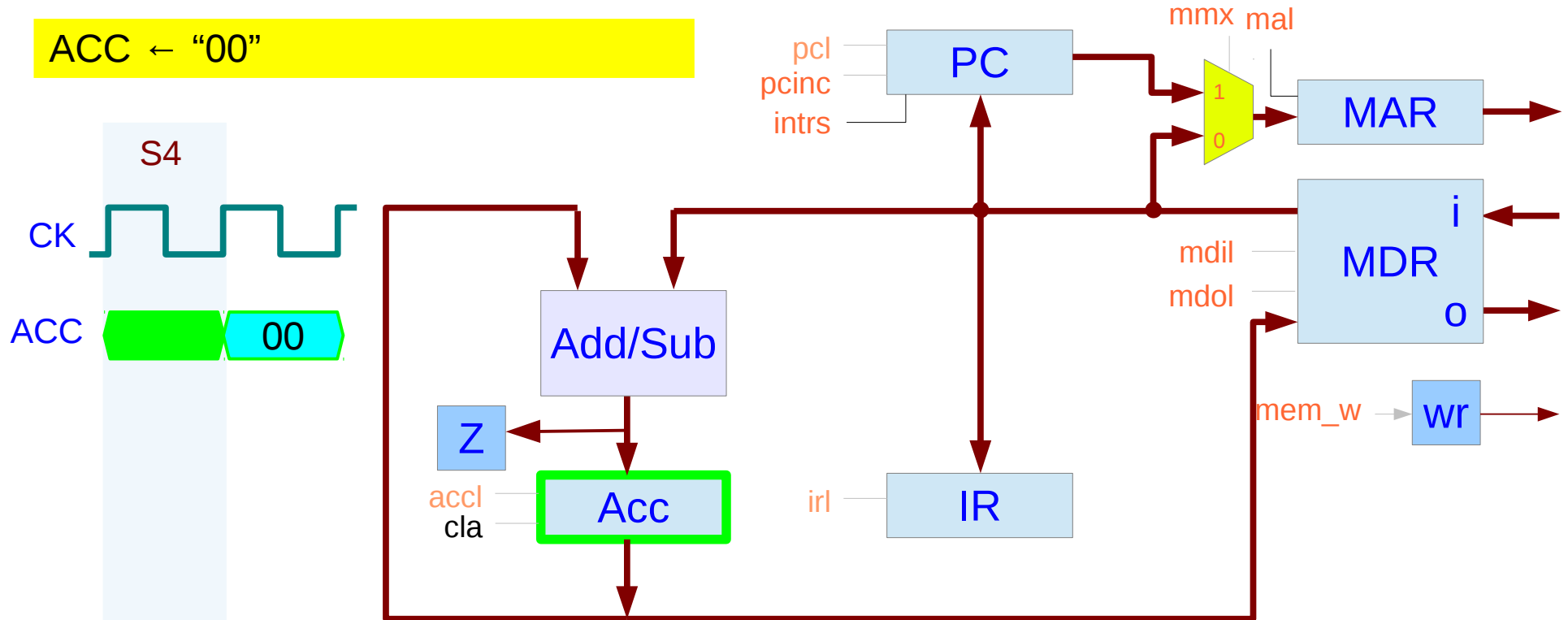
mem\_w

Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>





# Data Path (CLA, S4)



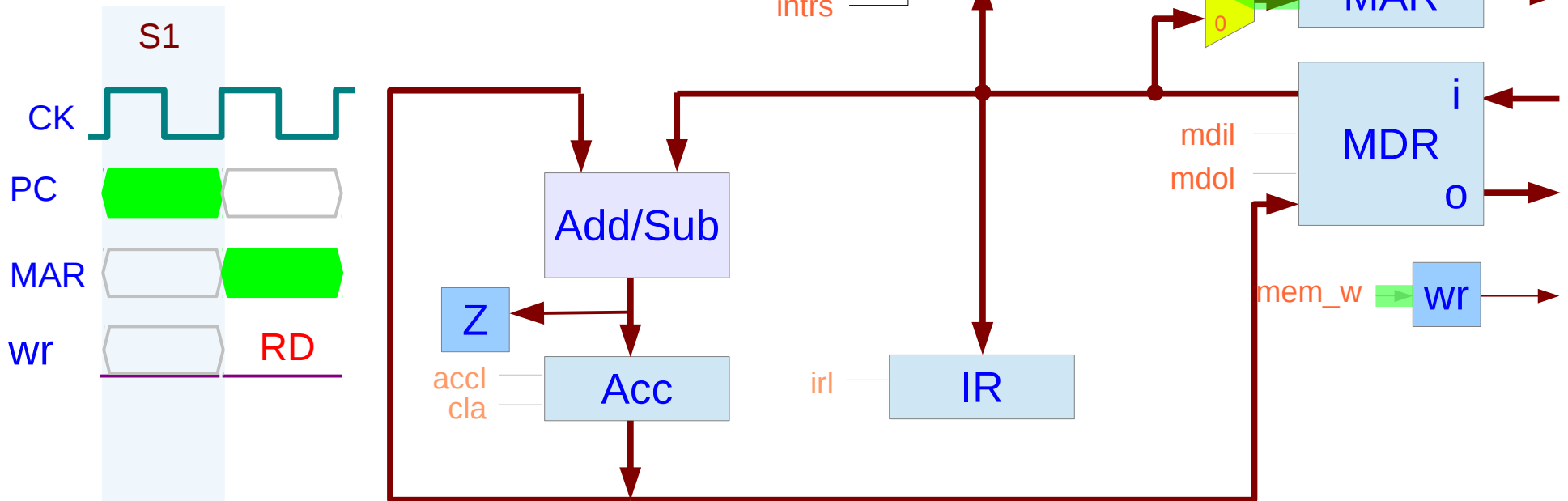
cla

Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>



# Data Path (JNZ, S4)

MAR ← PC; MEM\_RD;

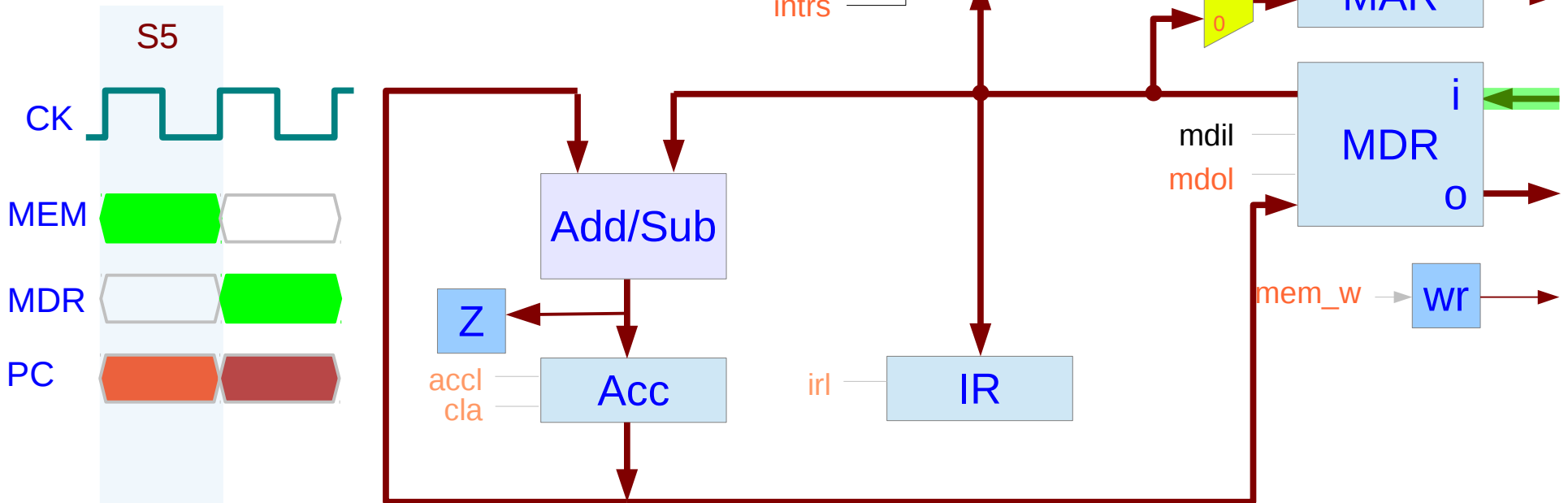


mmx,  
mal

Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>

# Data Path (JNZ, S5)

MDR ← MEM; PC ← PC + 1

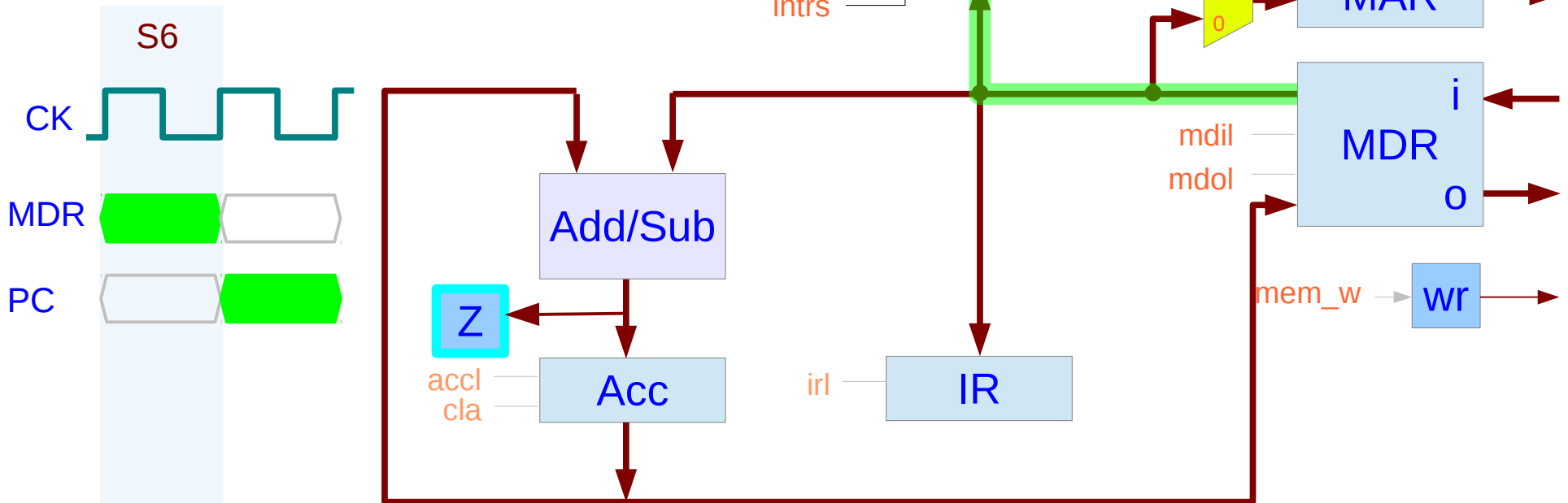


mdil,  
pcinc

Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>

# Data Path (JNZ, S6)

If (Z=='0') PC ← MDR;

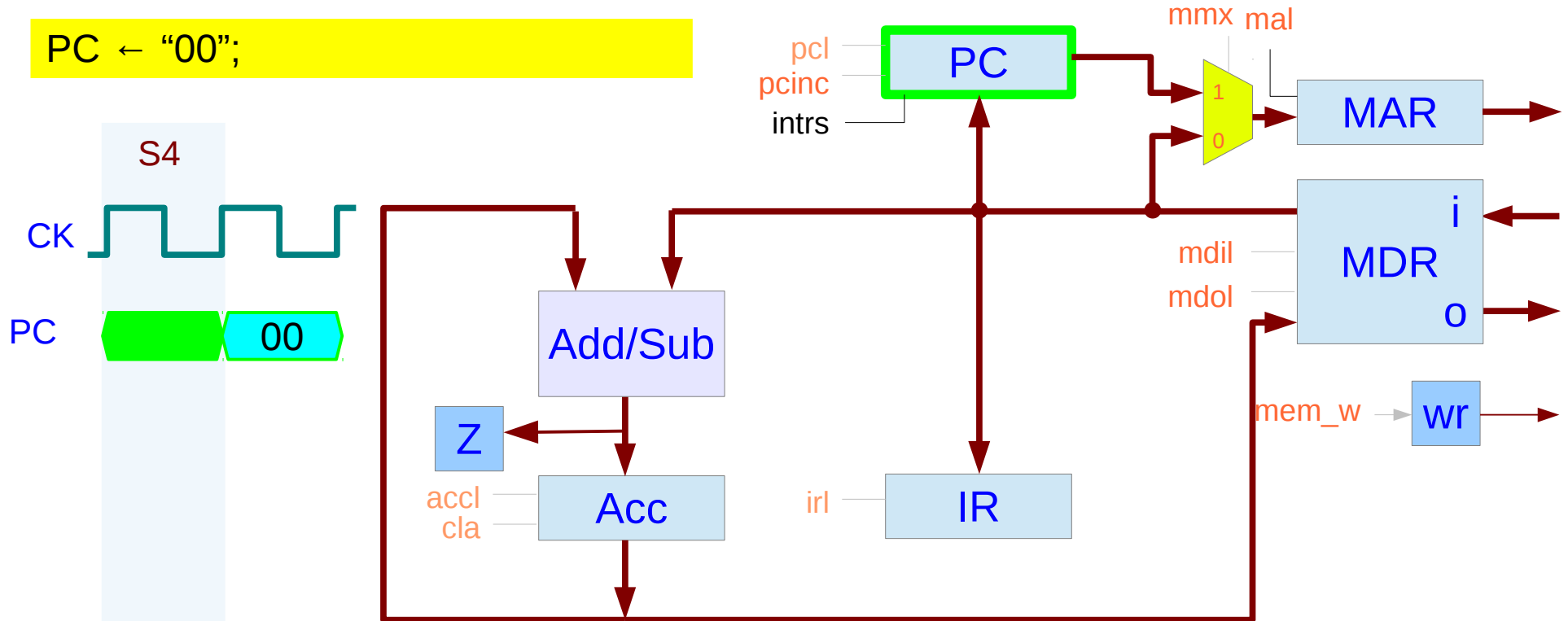


*pcl*

Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>



# Data Path (RST, S4)



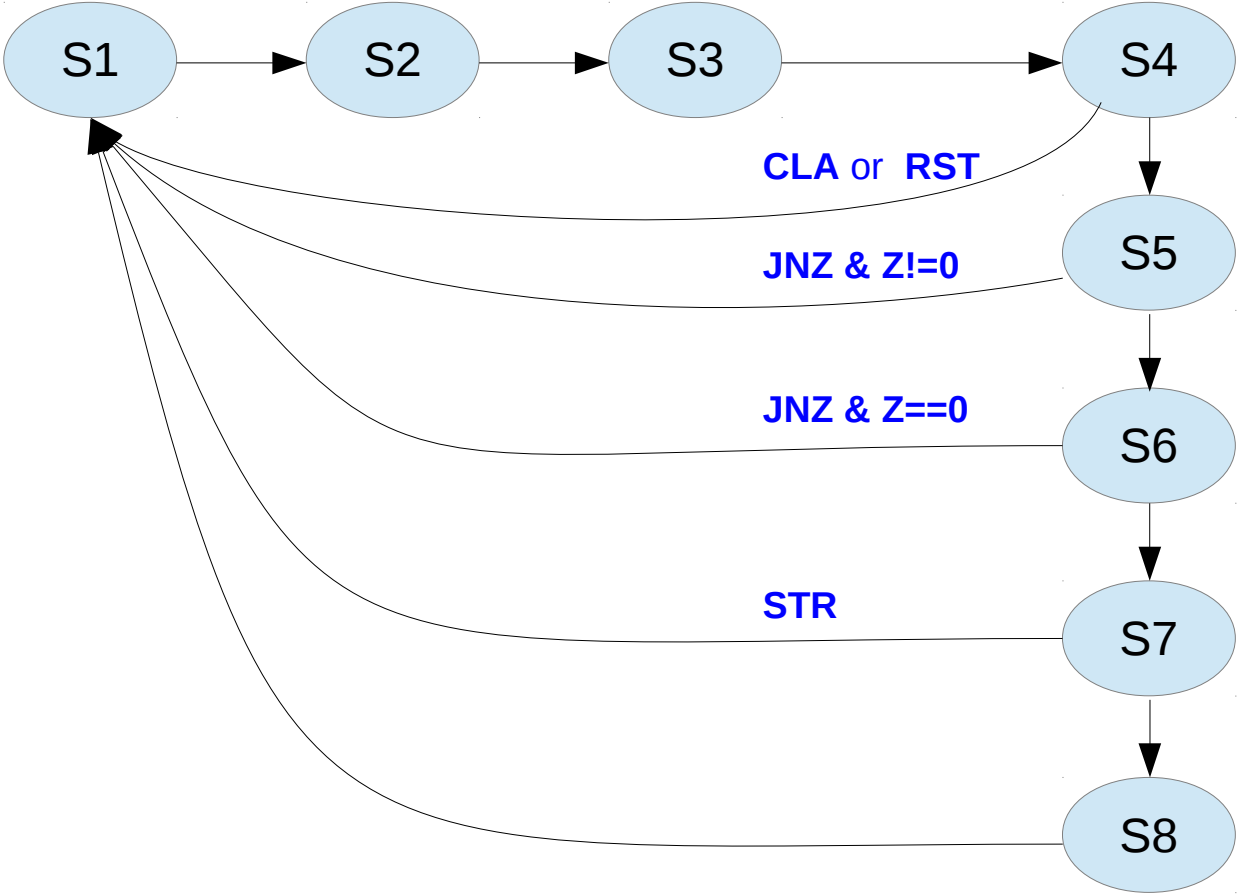
intrs

Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>



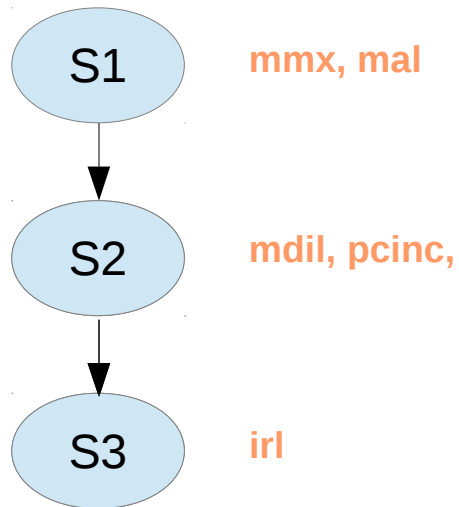


# Control Unit – FSM

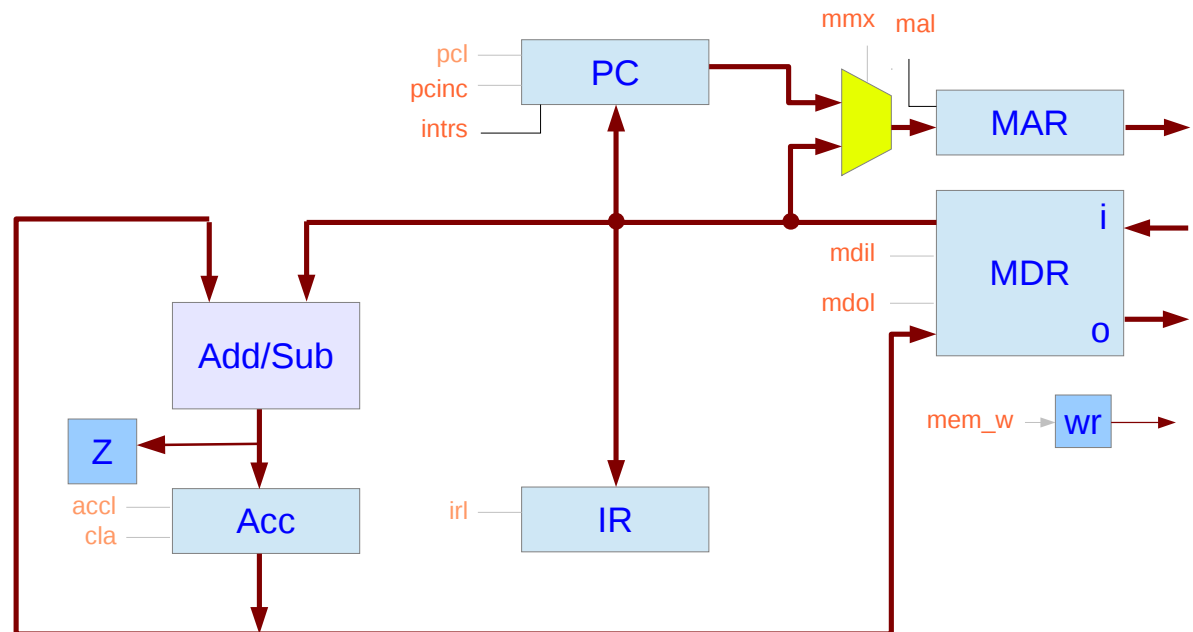


Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>

# Control Signal – IF

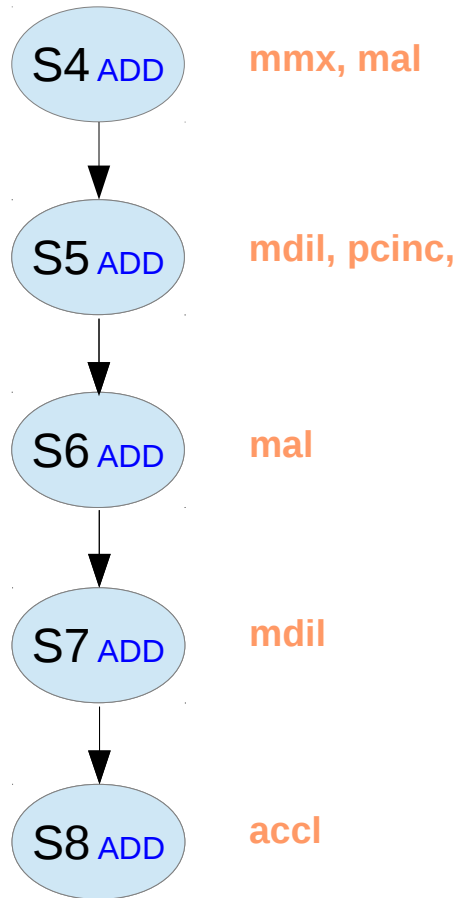


S1 MAR  $\leftarrow$  PC; MEM\_RD;  
S2 MDR  $\leftarrow$  MEM; PC  $\leftarrow$  PC+1;  
S3 IR  $\leftarrow$  MDR

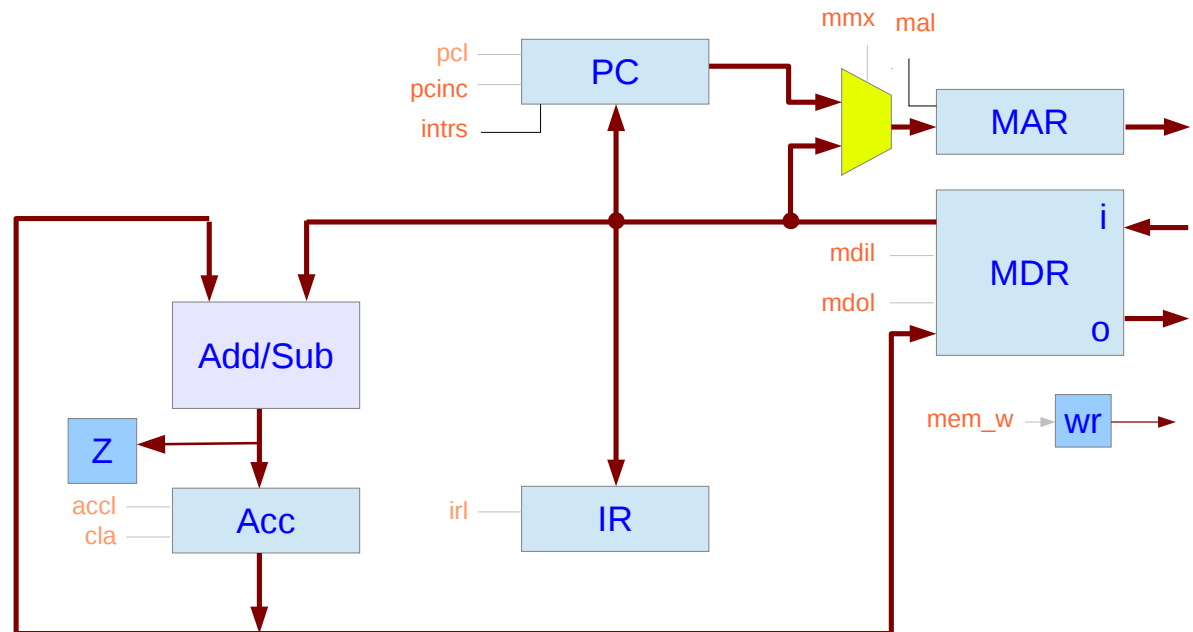


Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>

# Control Signal – ADD

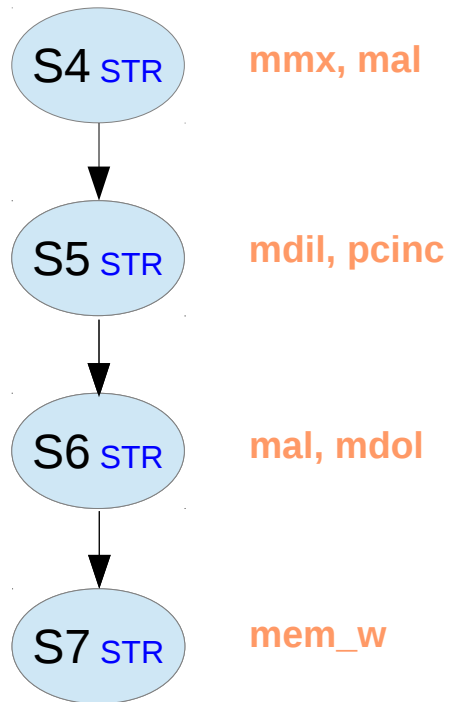


S4    MAR ← PC; MEM\_RD  
 S5    MDR ← MEM; PC ← PC+1  
 S6    MAR ← MDR; MEM\_RD  
 S7    MDR ← MEM;  
 S8    ACC ← ACC + MDR;

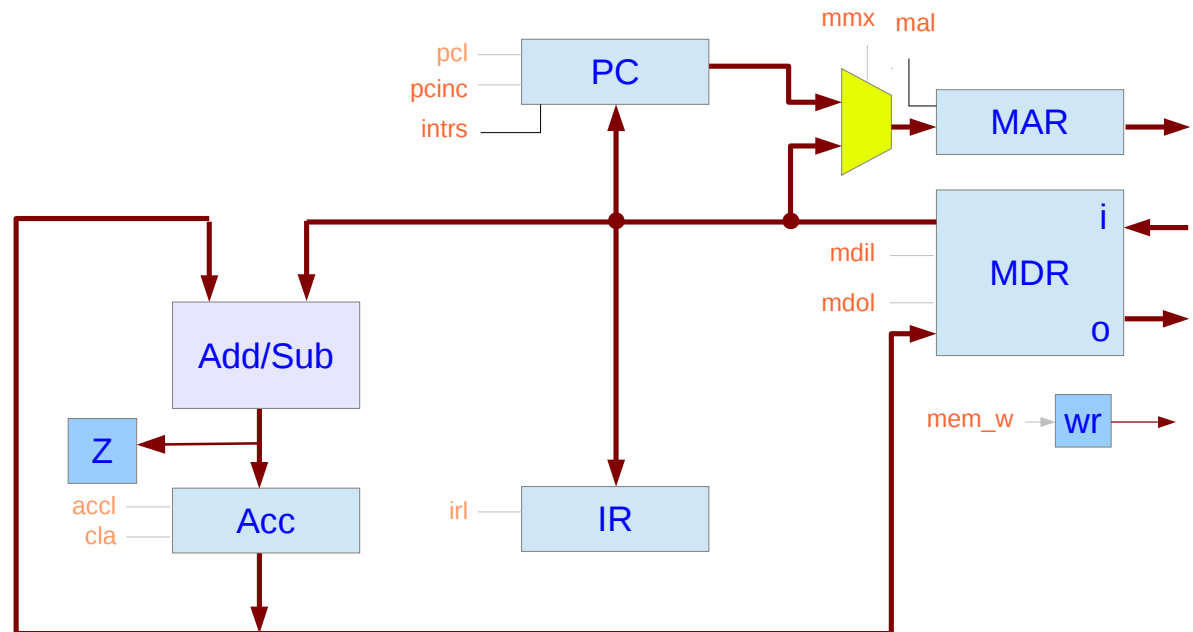


Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>

# Control Signal – STR



S4 MAR  $\leftarrow$  PC; MEM\_RD  
 S5 MDR  $\leftarrow$  MEM; PC  $\leftarrow$  PC + 1  
 S6 MAR  $\leftarrow$  MDR; MDR  $\leftarrow$  ACC  
 S7 MEM\_WR;

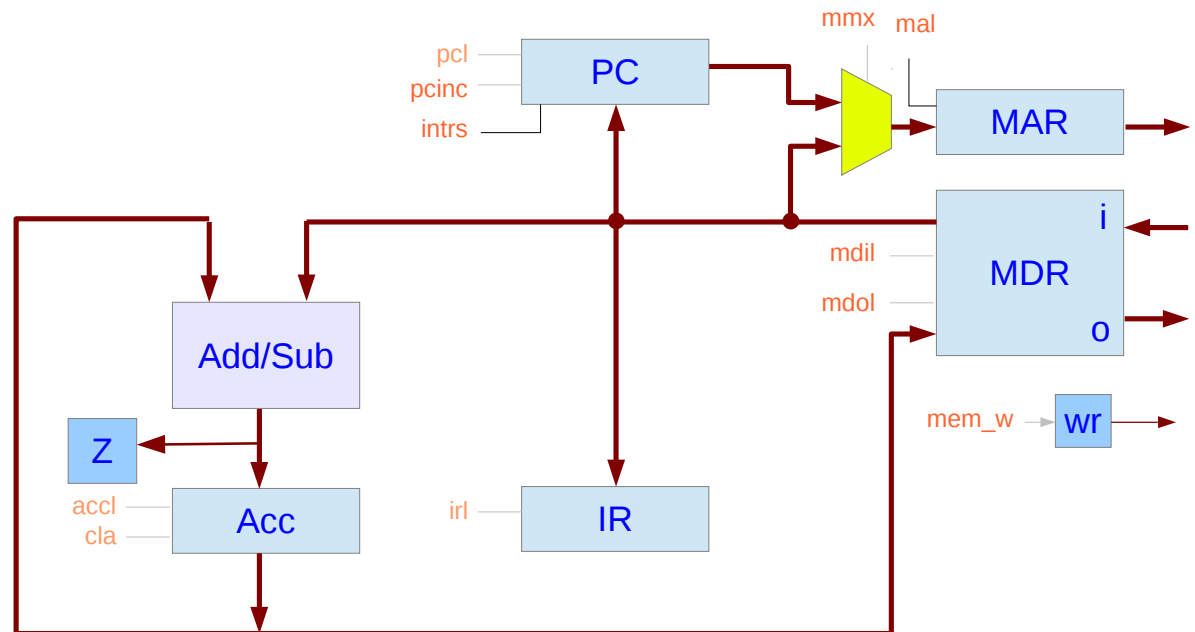


Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>

# Control Signal – CLA

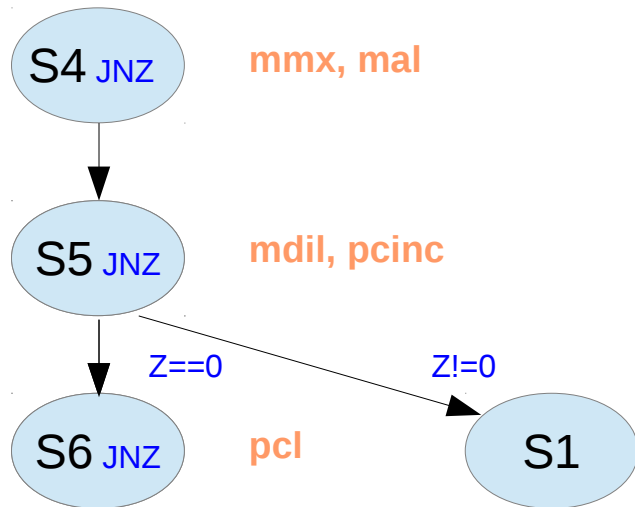
S4 CLA  
cla

S4 ACC ← "00"

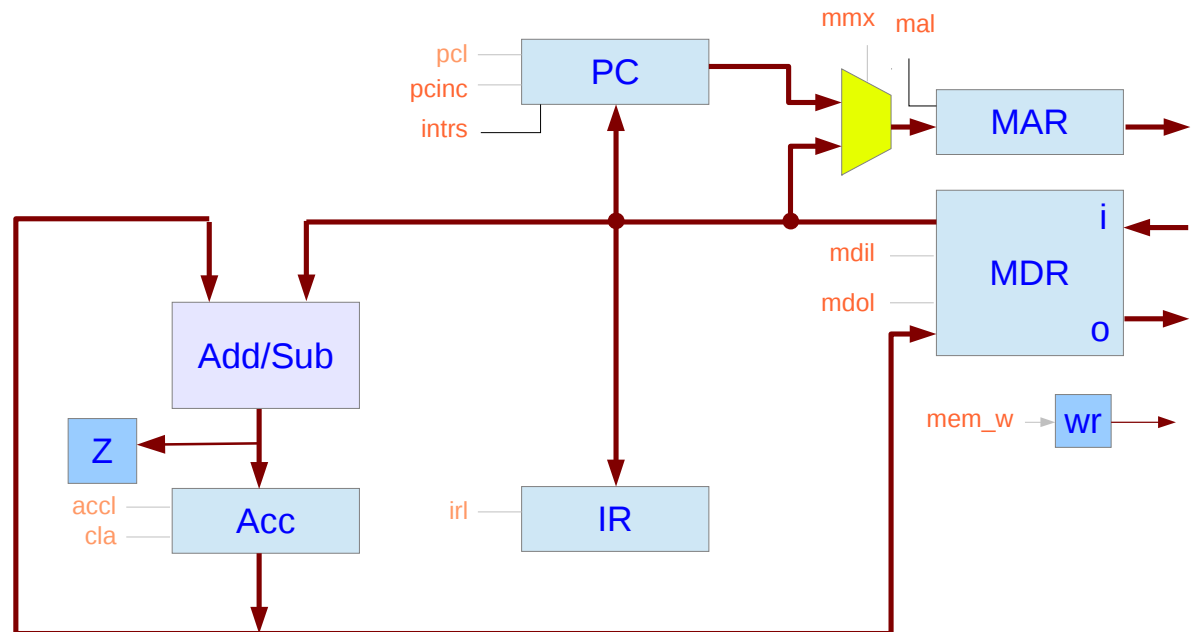


Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>

# Control Signal – JNZ



S4 MAR  $\leftarrow$  PC; MEM\_RD;  
 S5 MDR  $\leftarrow$  MEM; PC  $\leftarrow$  PC + 1  
 S6 If (Z=='0') PC  $\leftarrow$  MDR;



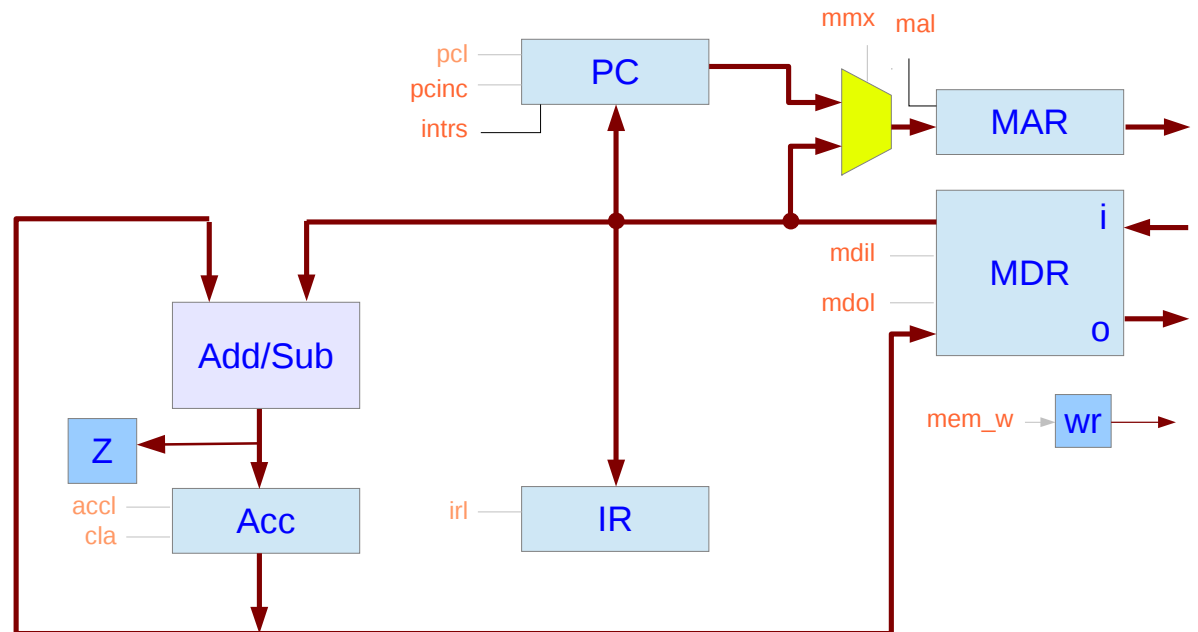
Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>

# Control Signal – RST

S4<sub>RST</sub>

intrs

S4 PC ← "00"



Based on <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>







## References

- [1] <http://en.wikipedia.org/>
- [2] <http://www.ele.uri.edu/Courses/ele306/f01/Tinydoc.pdf>