RAM (1A)

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11/12/13

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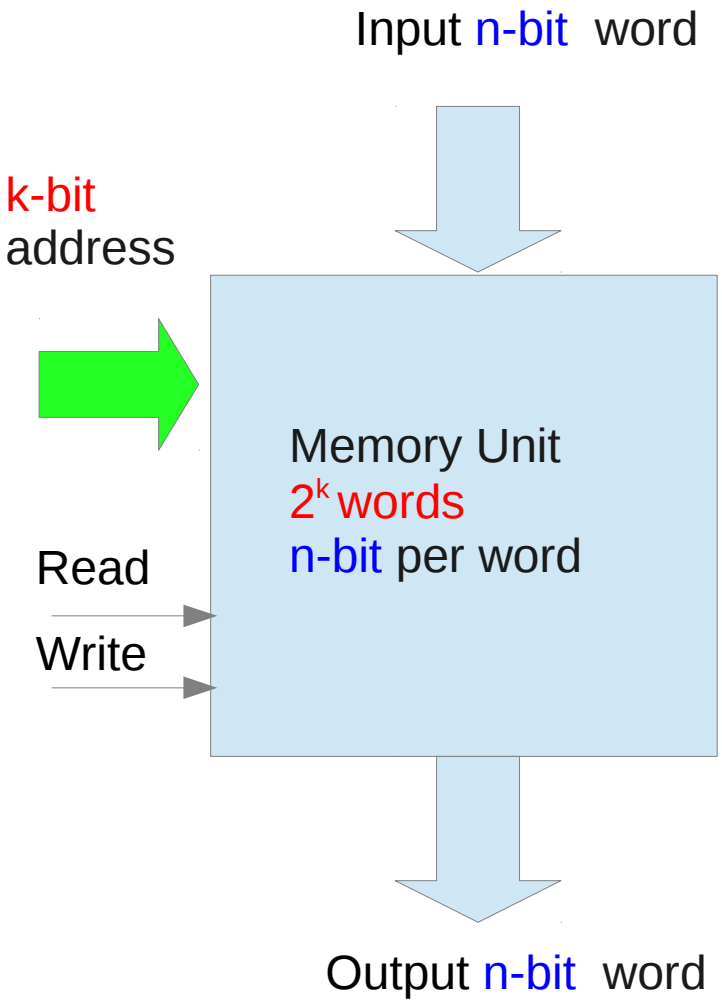
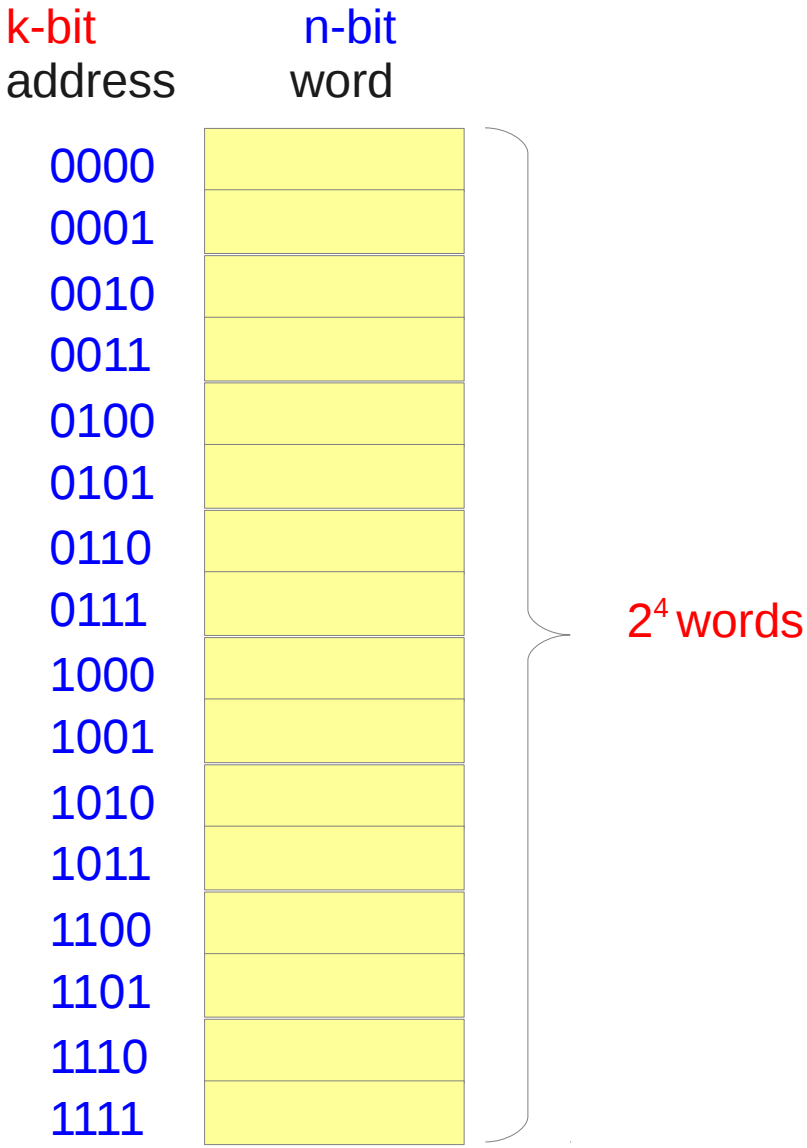
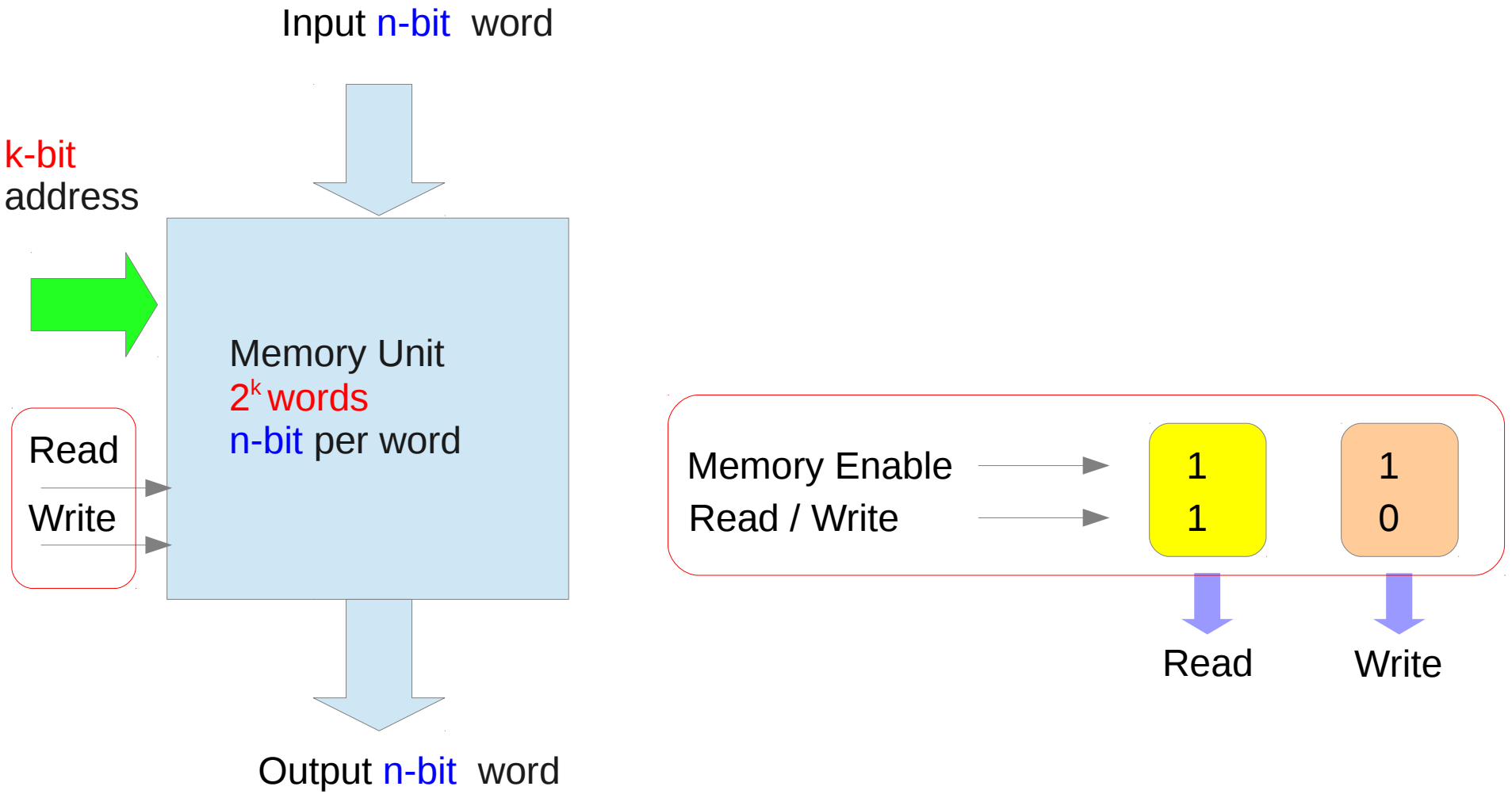
Block Diagram of a Memory Unit

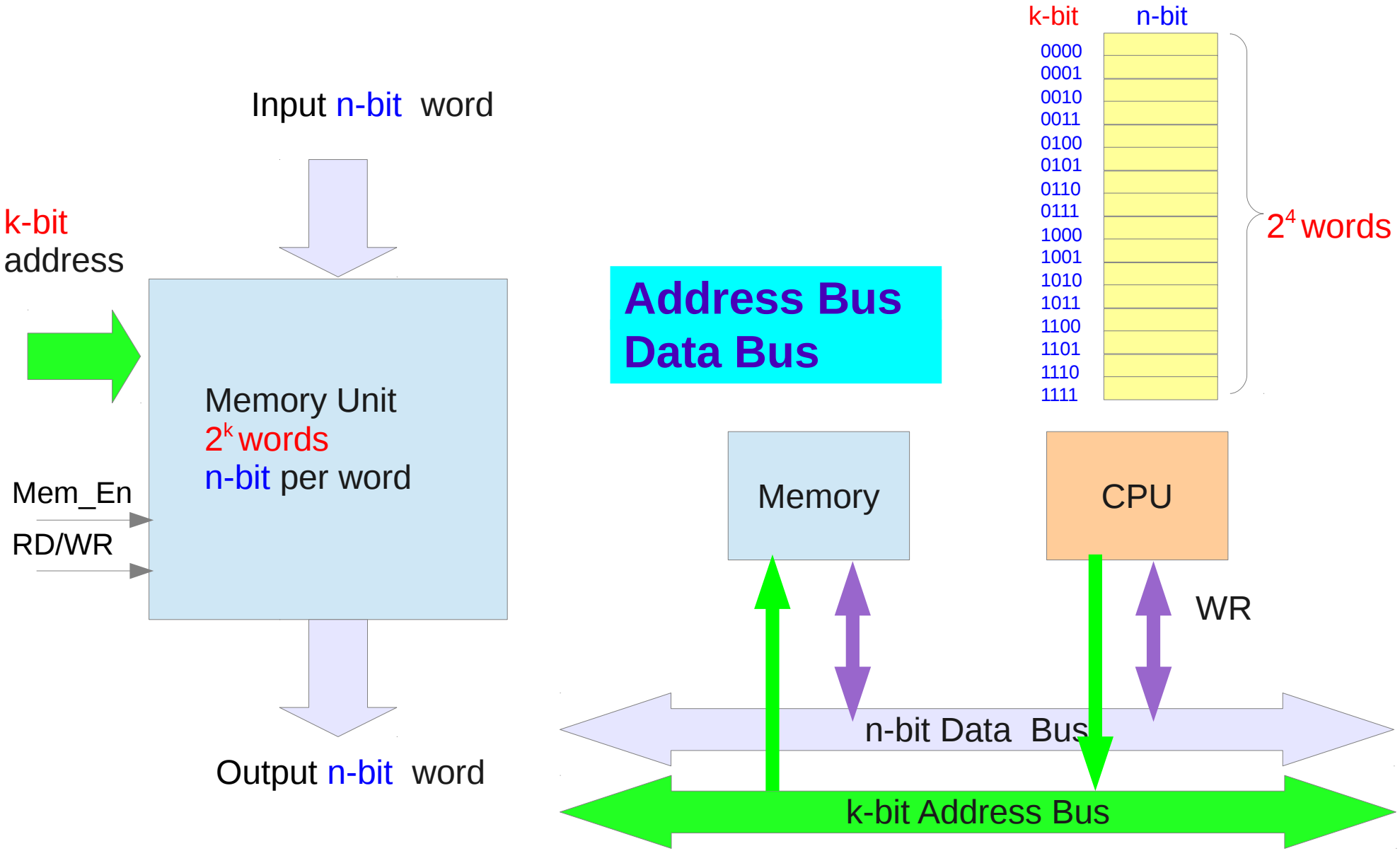




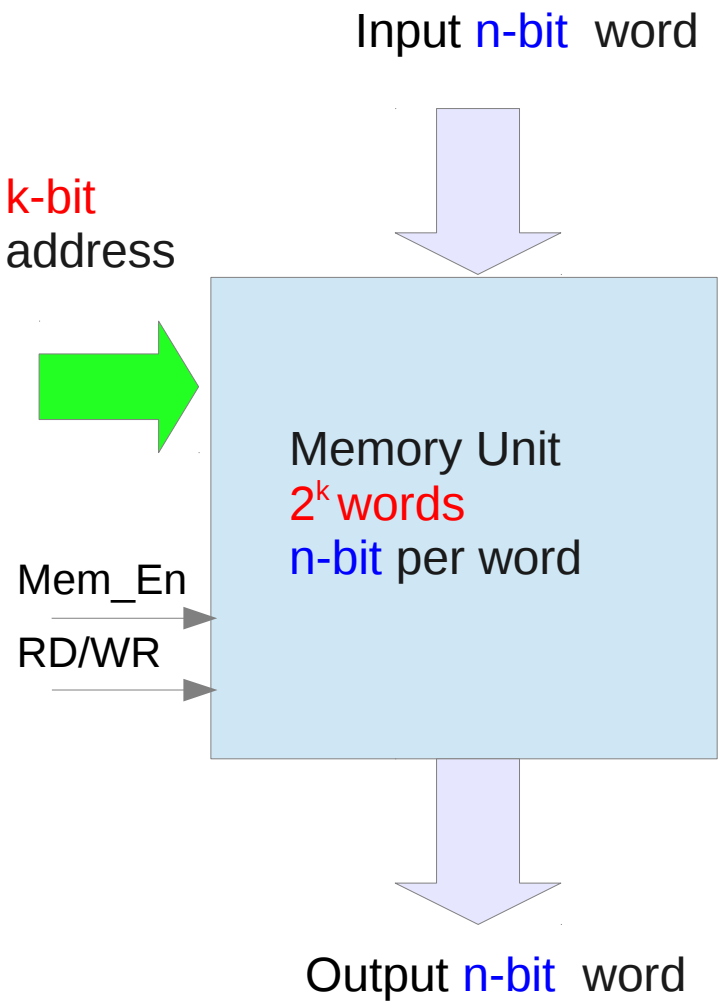
Memory Control Lines

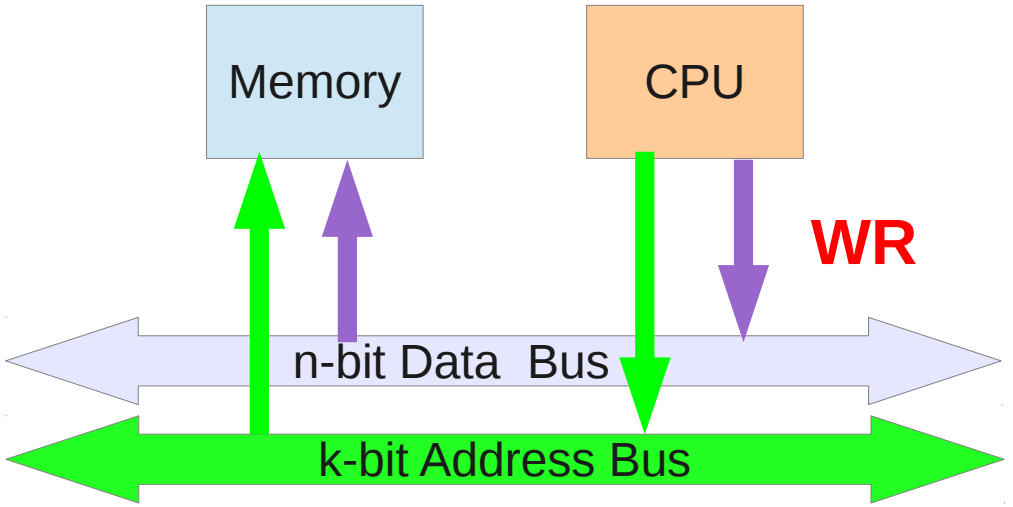


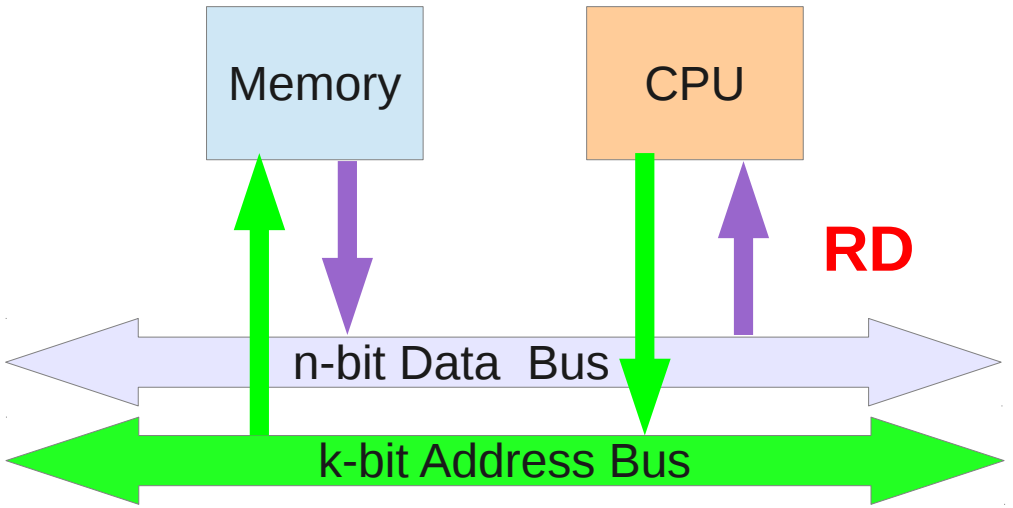
Address & Data Buses



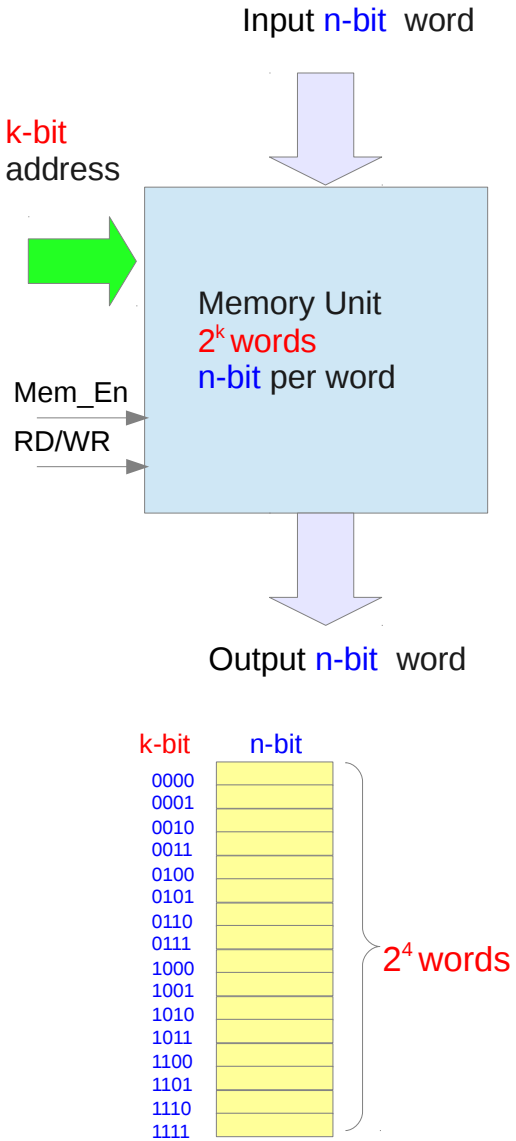
RD & WR Operations

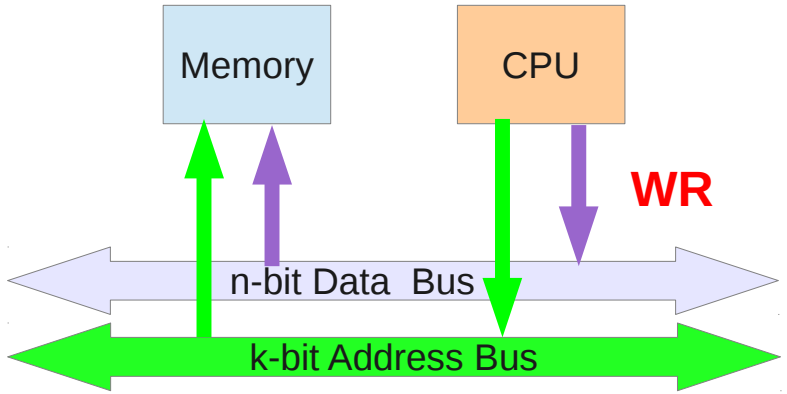


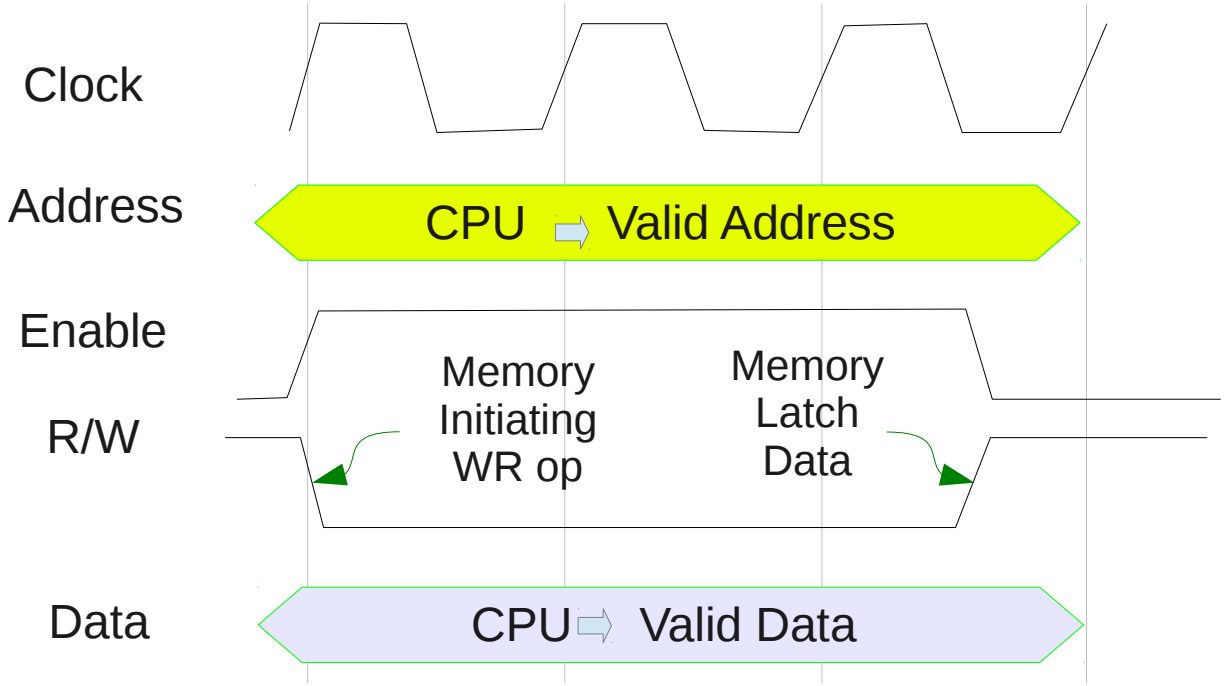




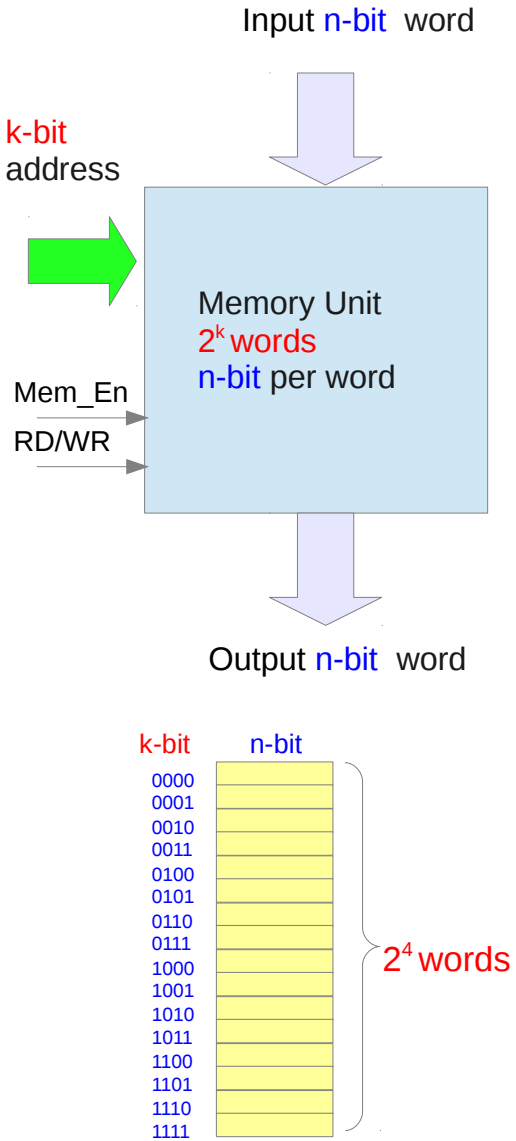
Memory Write Cycle

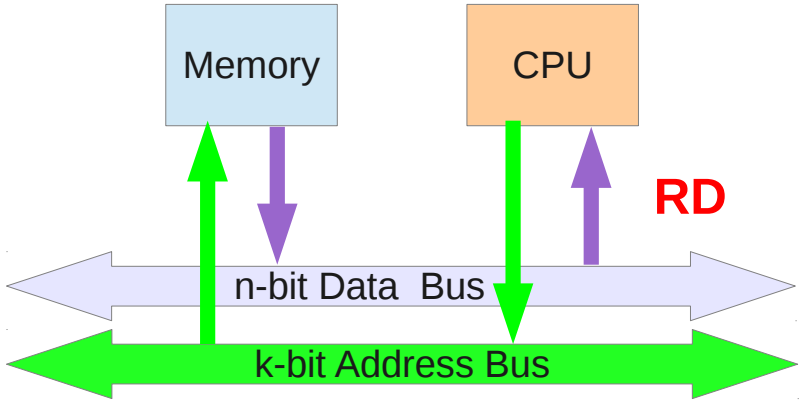


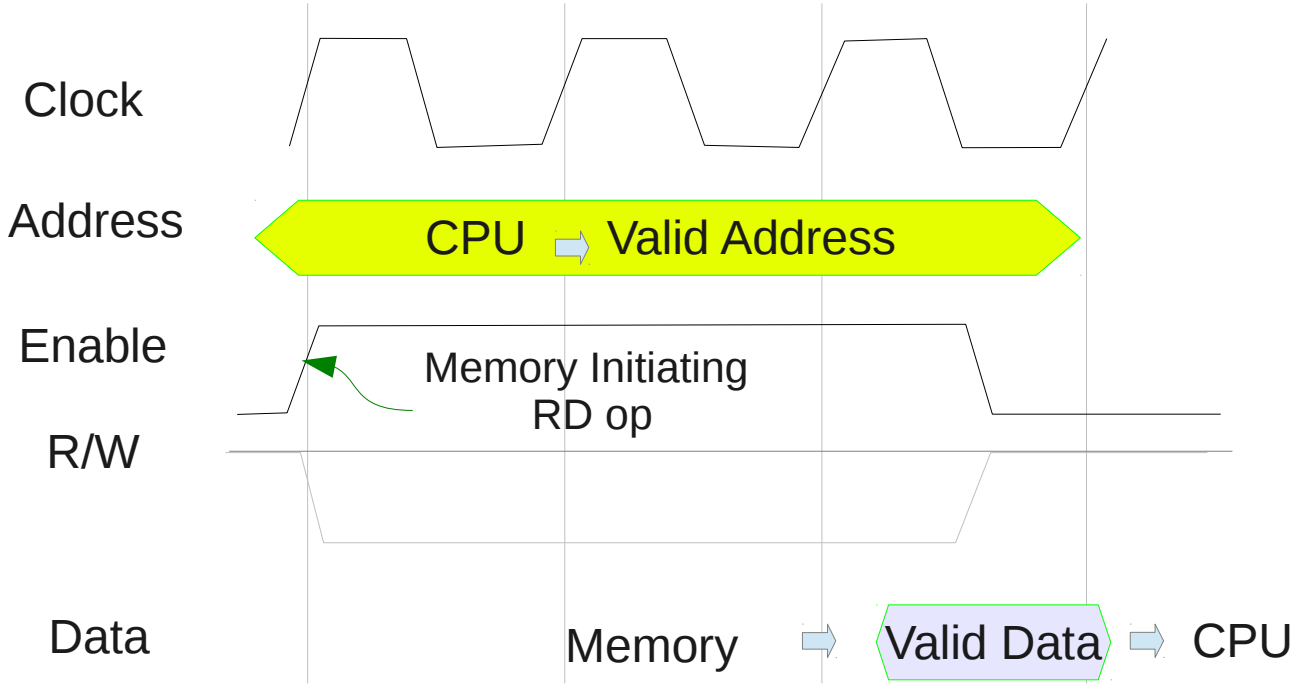




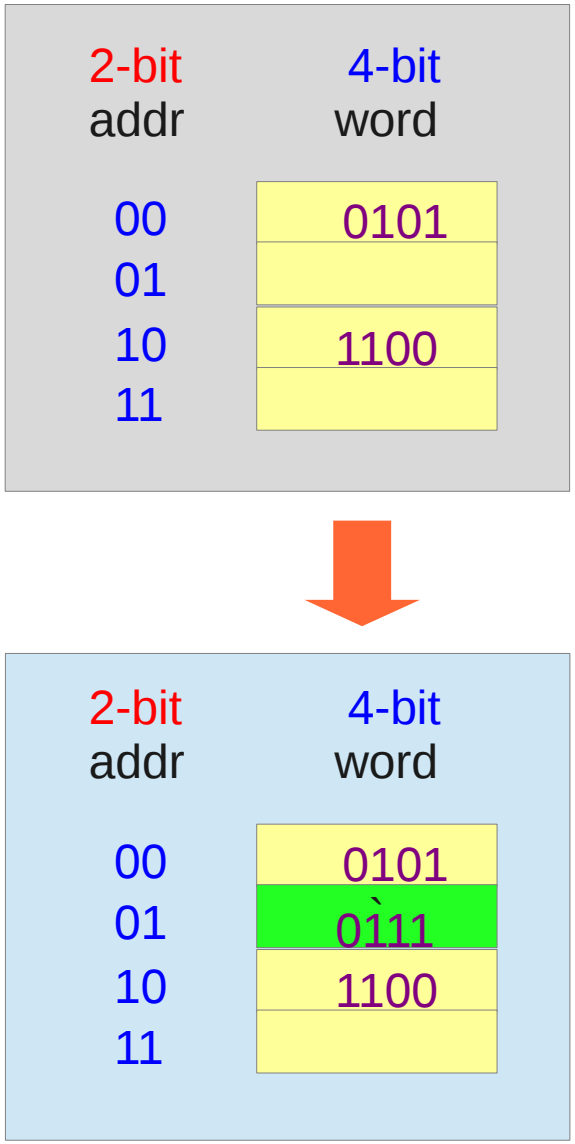
Memory Read Cycle

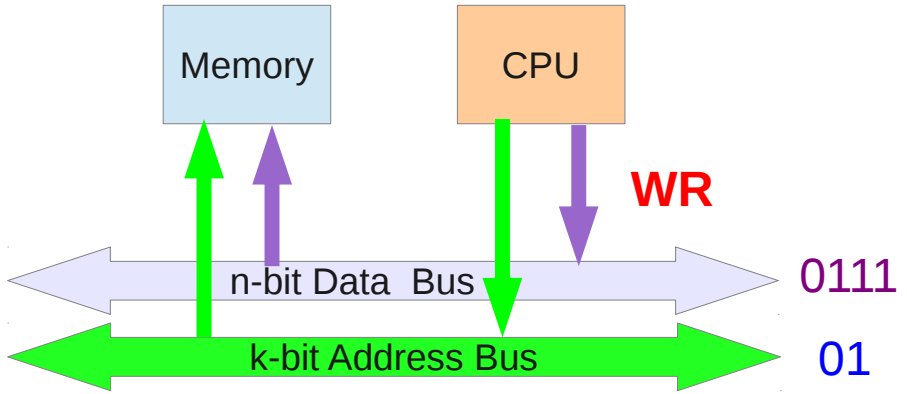


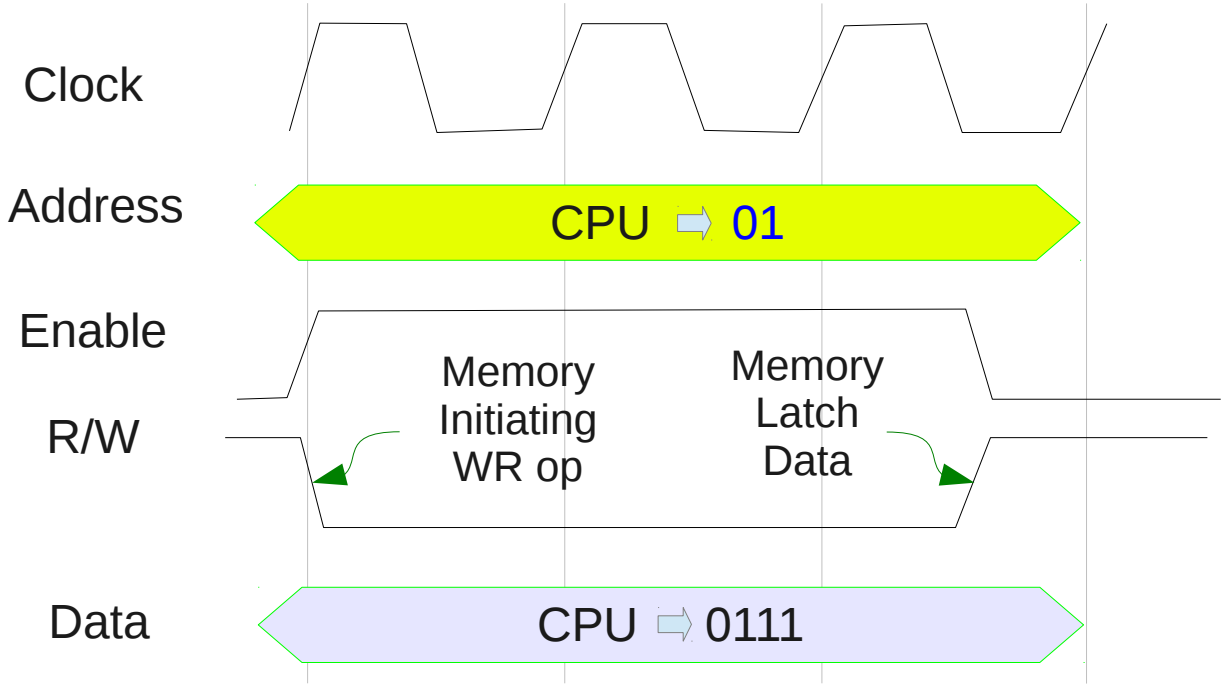




Memory Write Example

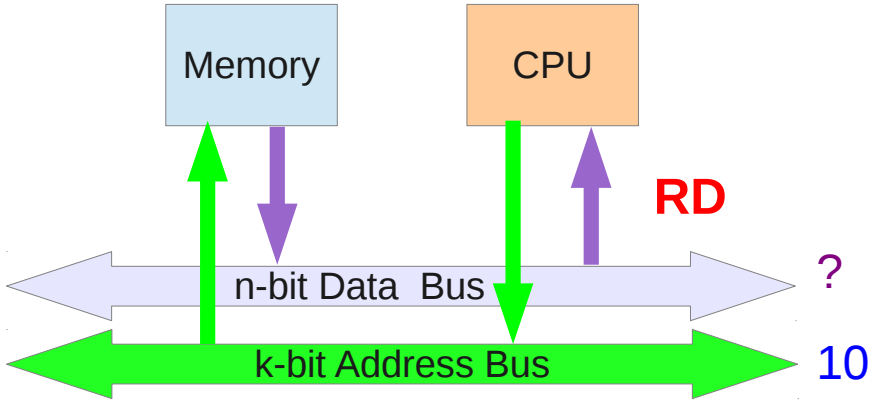


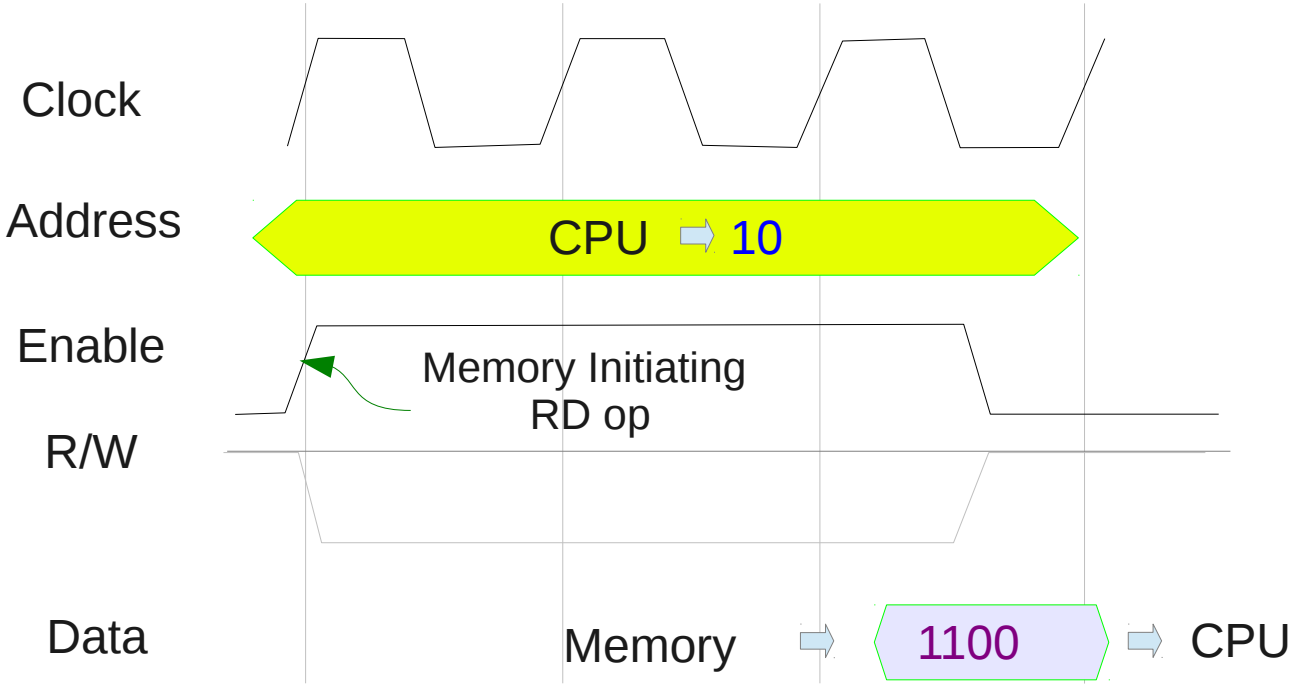




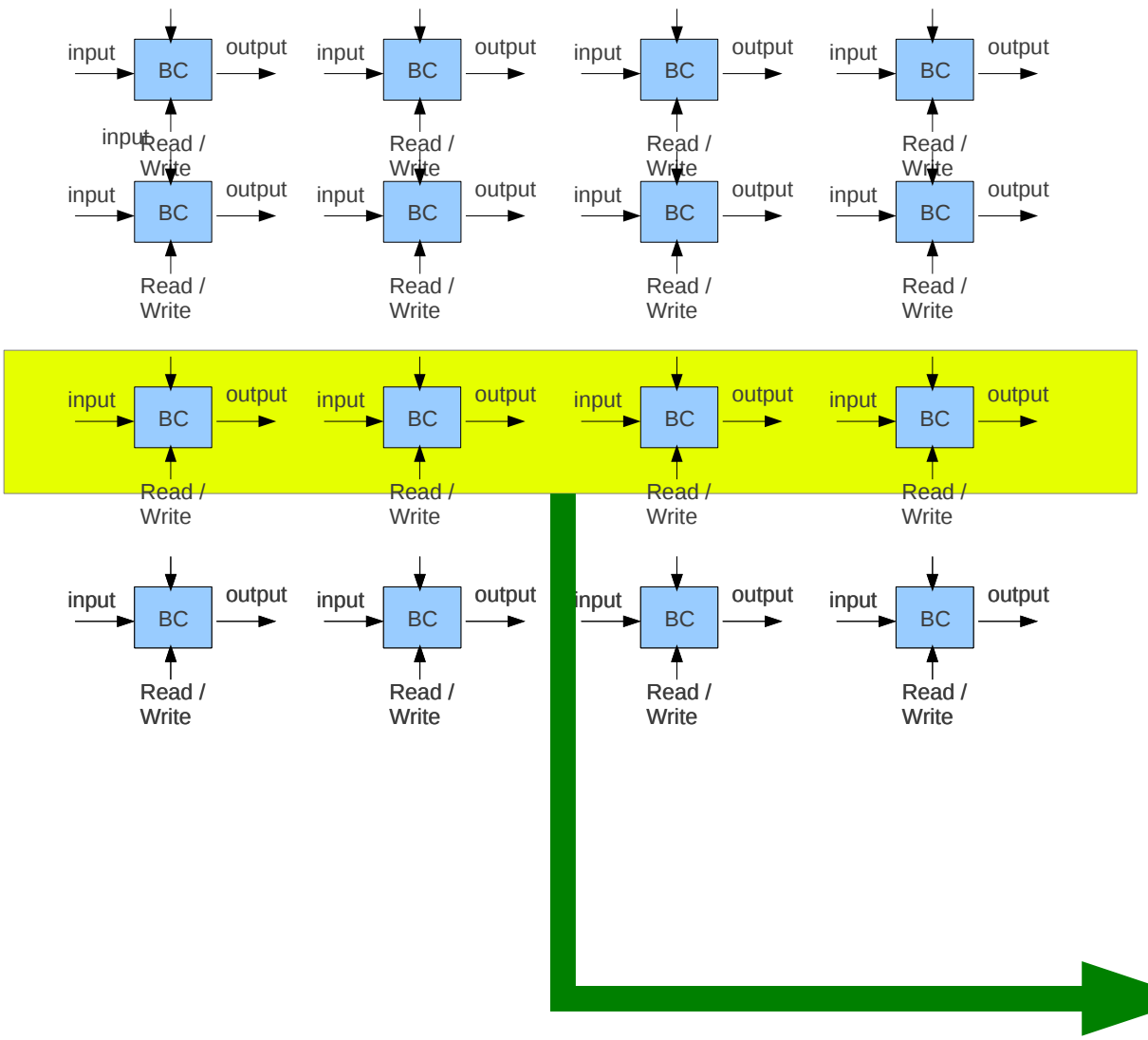
Memory Read Example

2-bit addr	4-bit word
00	0101
01	
10	1100
11	





Selecting a Word



selected 4-bit word

2-bit address

4-bit word

00

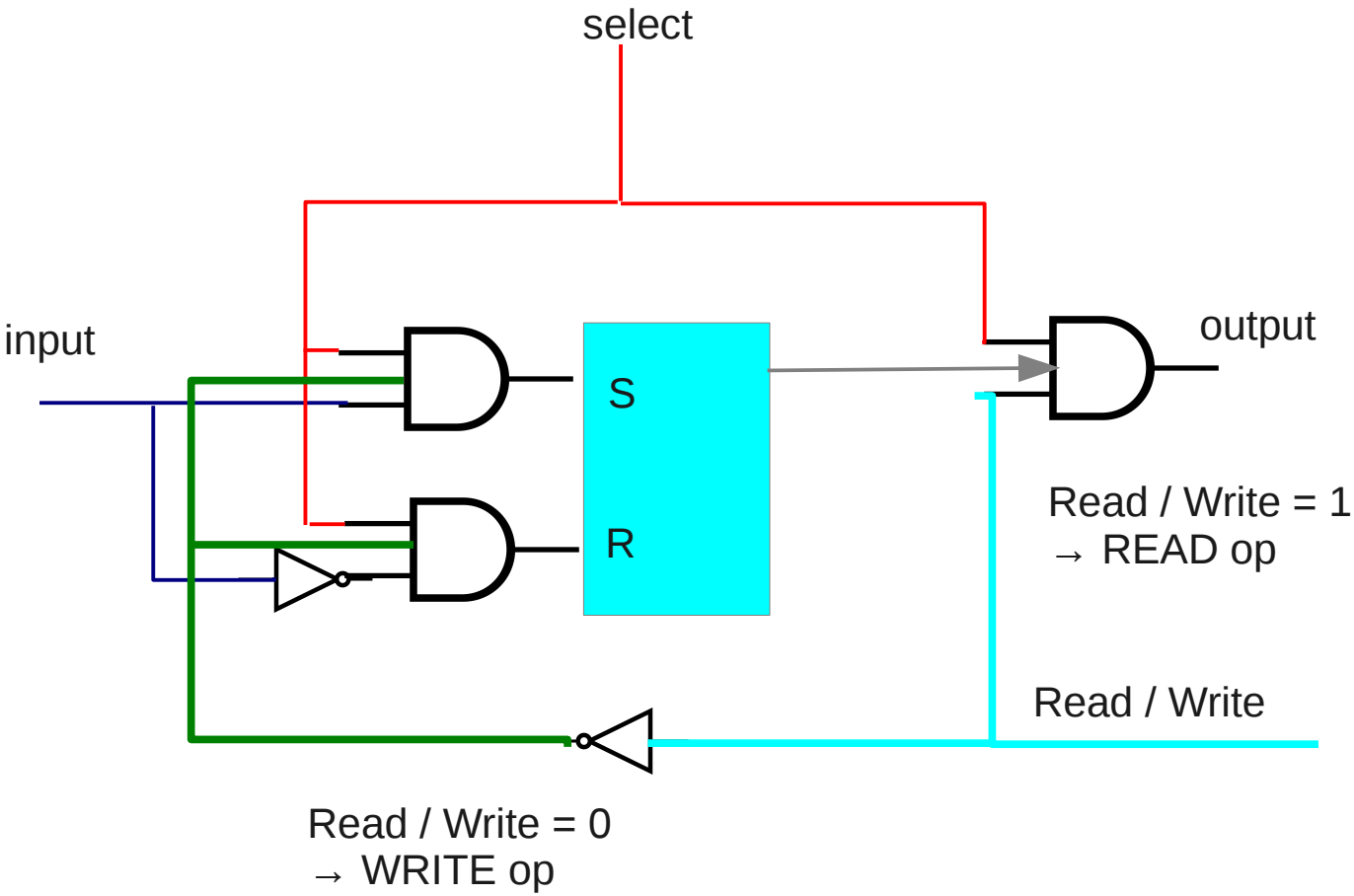
01

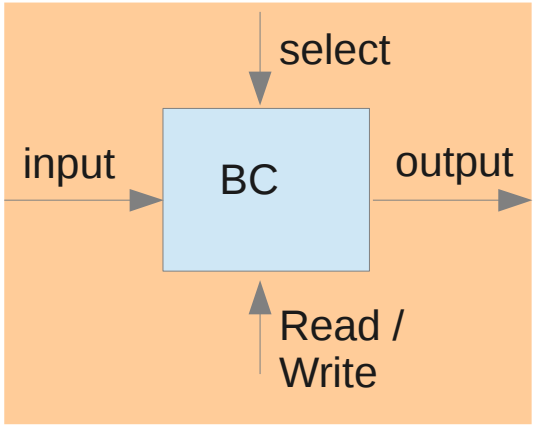
10

11

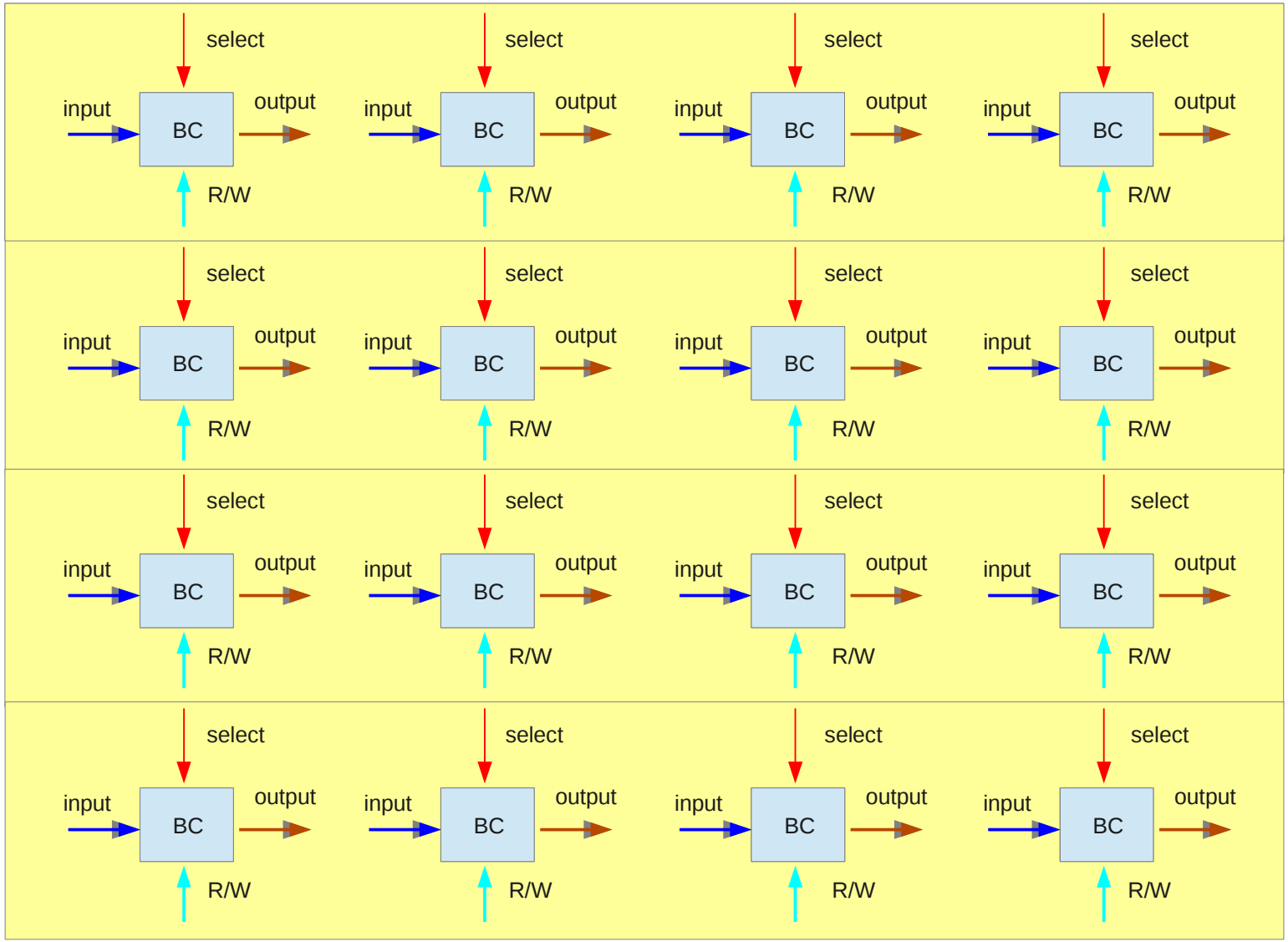
2^4 words

Selecting a Word

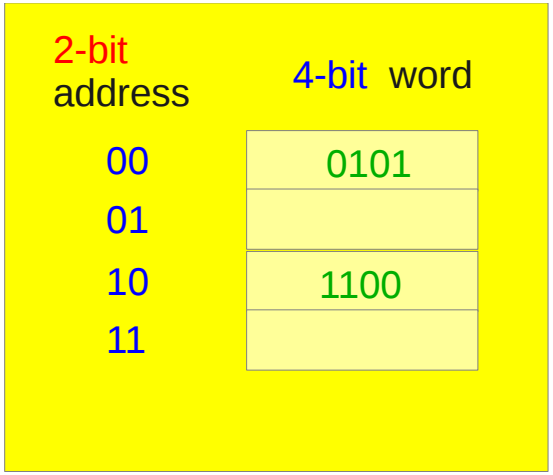


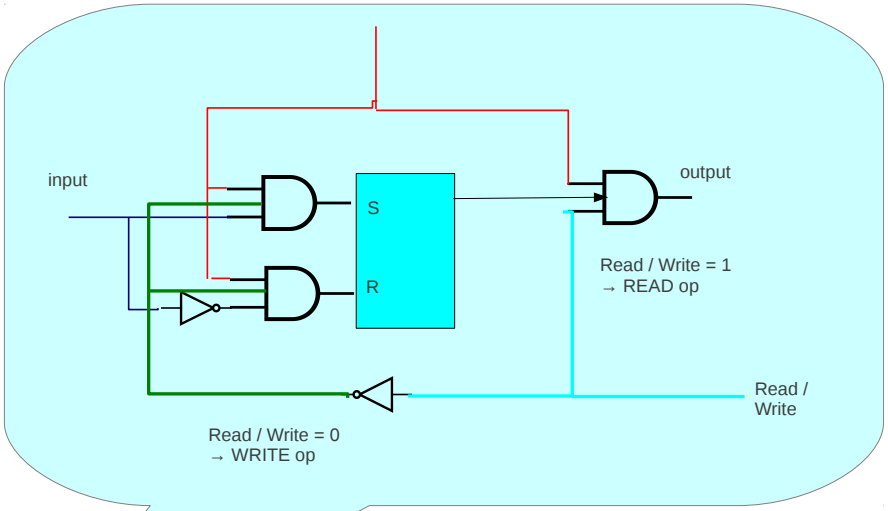


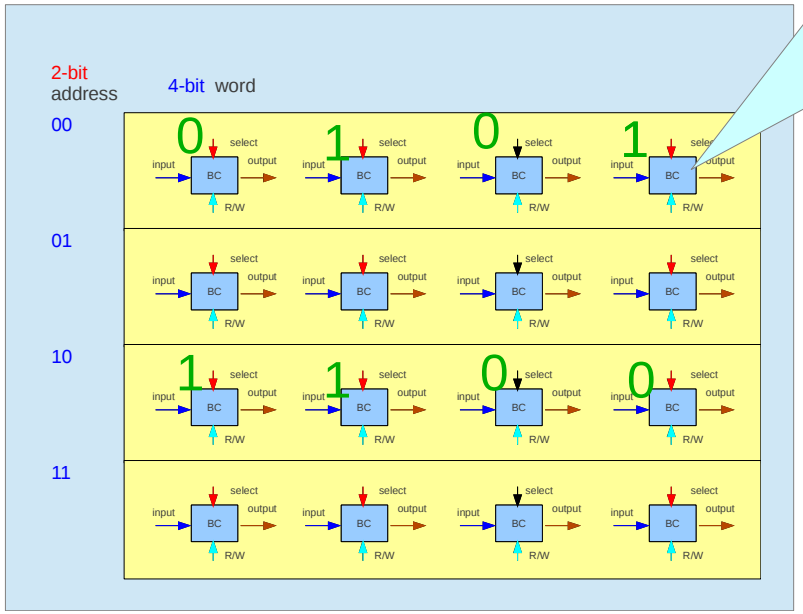
A Memory Map


00
01
10
11
select
input
output
BC
R/W
2-bit
addr
Bit 3
Bit 2
Bit 1
Bit 0
4-bit word

4x4 Memory


2-bit
address
4-bit word
00
01
10
11
0101
1100


input
S
R
output
Read / Write = 1
→ READ op
Read /
Write
Read / Write = 0
→ WRITE op


2-bit
address
4-bit word
00
01
10
11
select
input
output
BC
R/W

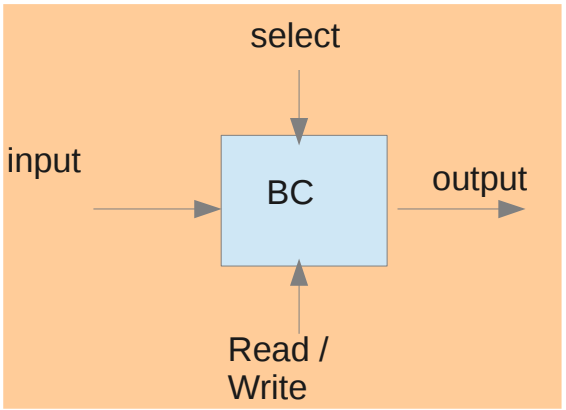
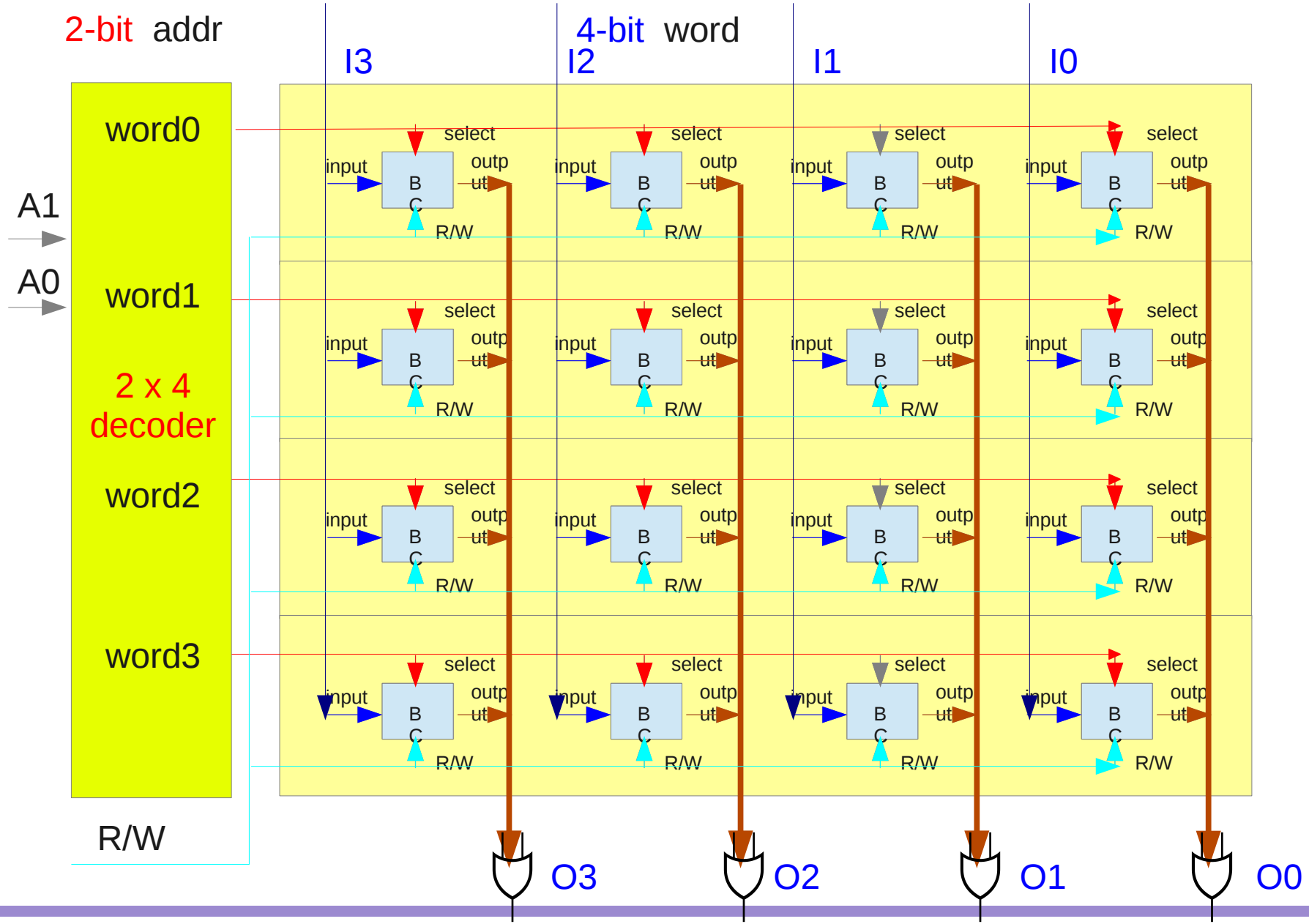
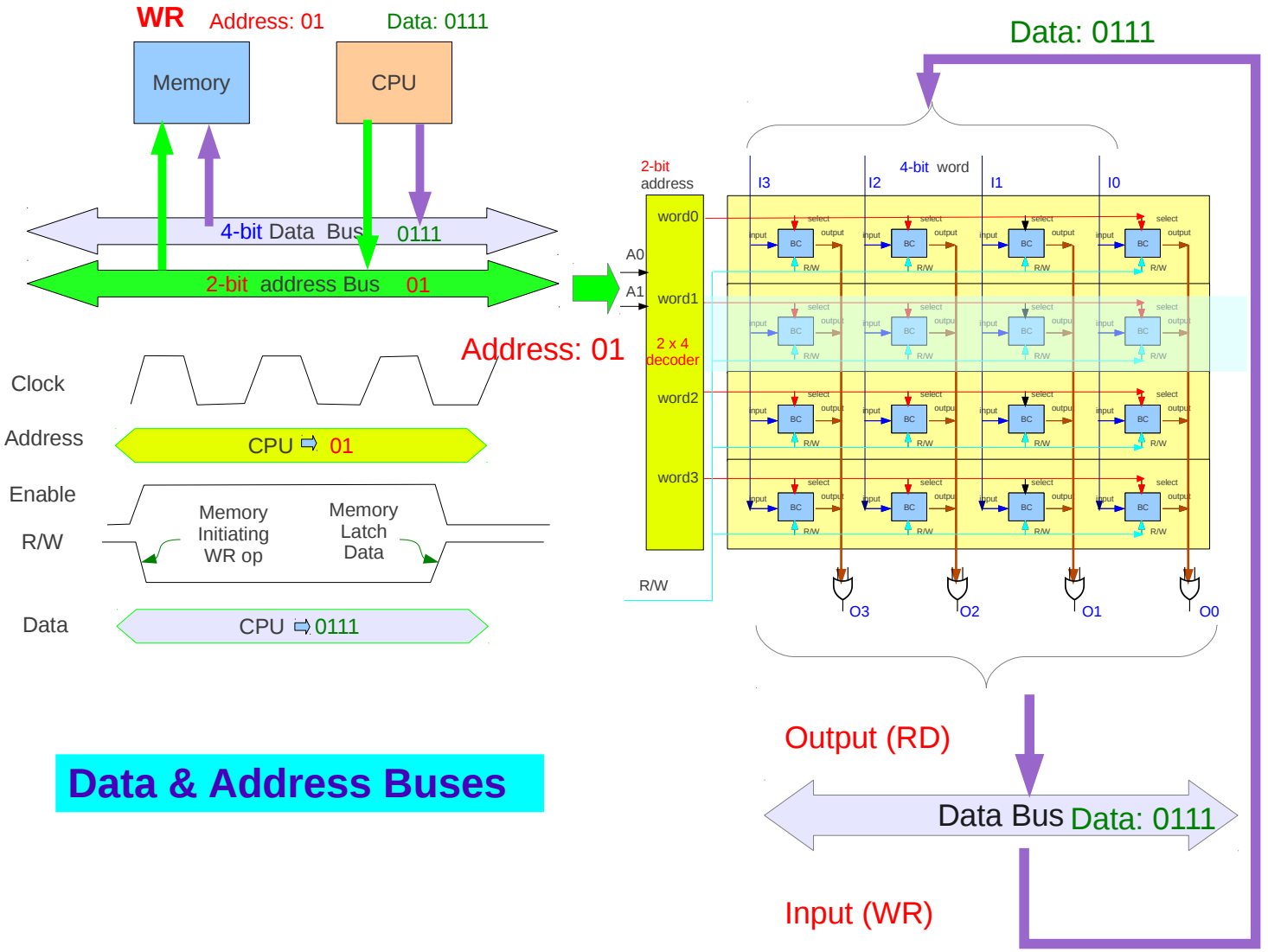

select
input
BC
output
Read /
Write

Diagram for a 4x4 Memory

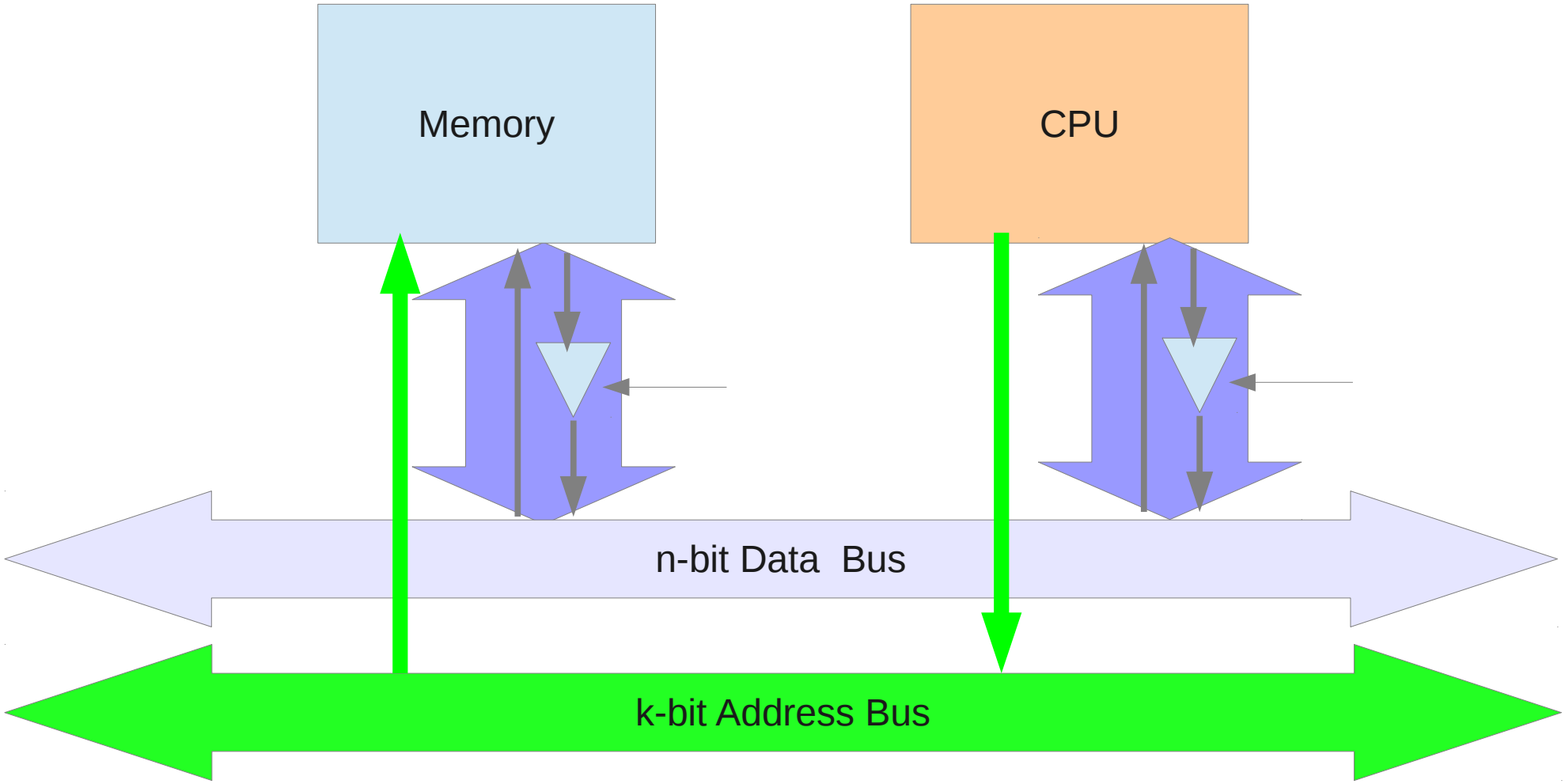


Write Cycle Example for a 4x4 Memory

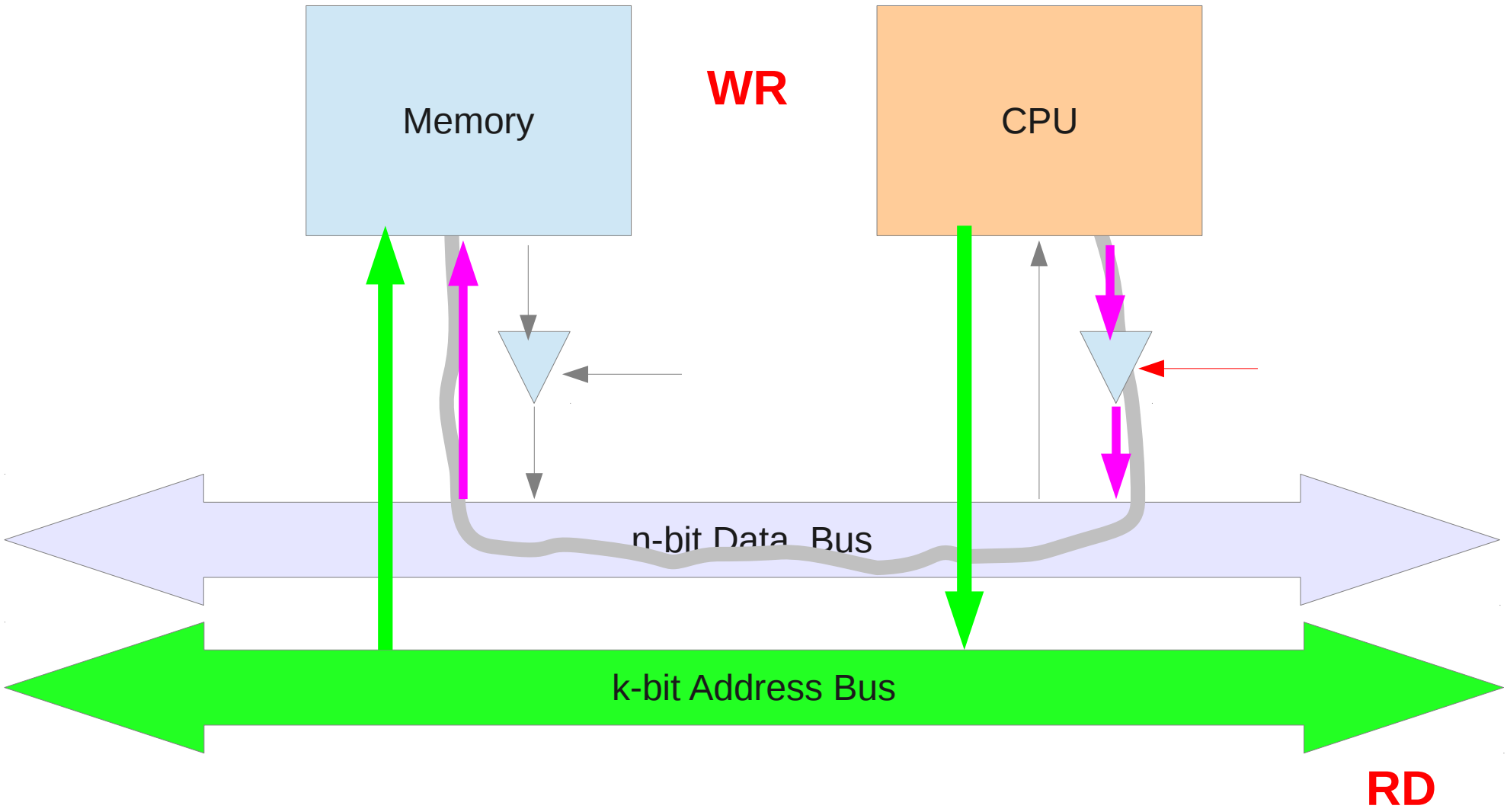


Data & Address Buses

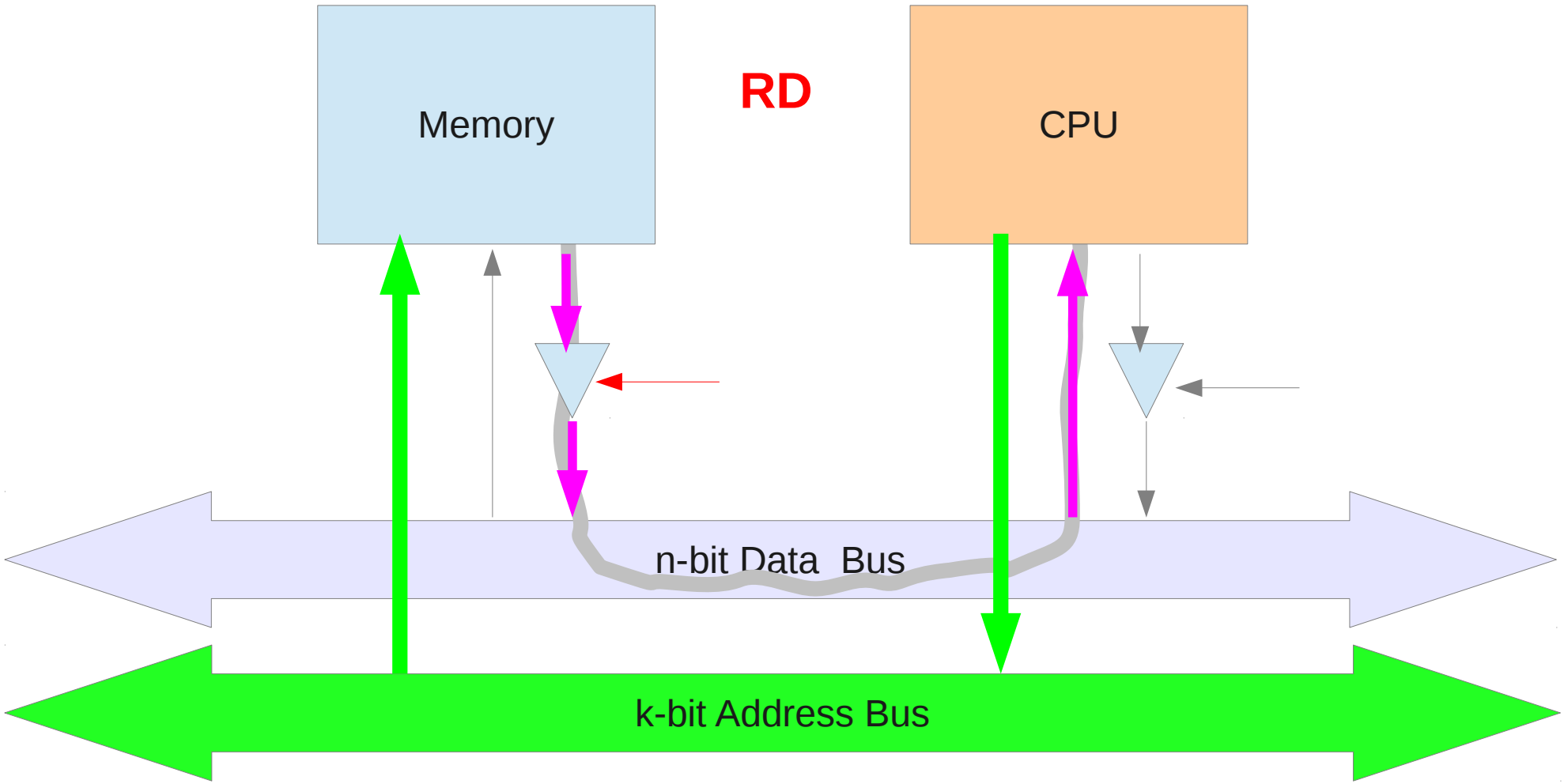
Bi-directional Data Bus



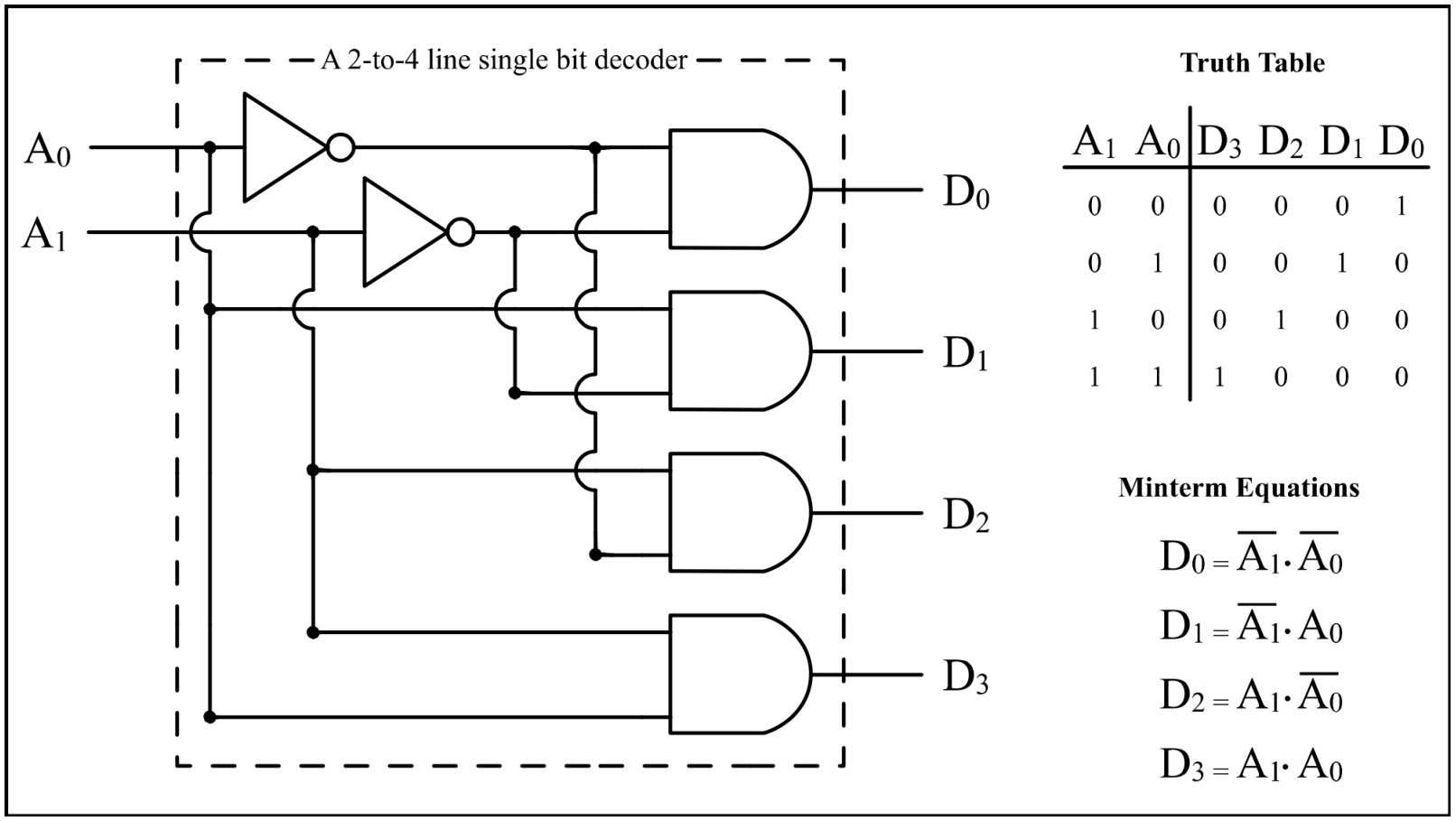
From CPU to Memory



From Memory to CPU



2 to 4 Decoder



Truth Table

A_1	A_0	D_3	D_2	D_1	D_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0

Minterm Equations

$$D_0 = \overline{A_1} \cdot \overline{A_0}$$

$$D_1 = \overline{A_1} \cdot A_0$$

$$D_2 = A_1 \cdot \overline{A_0}$$

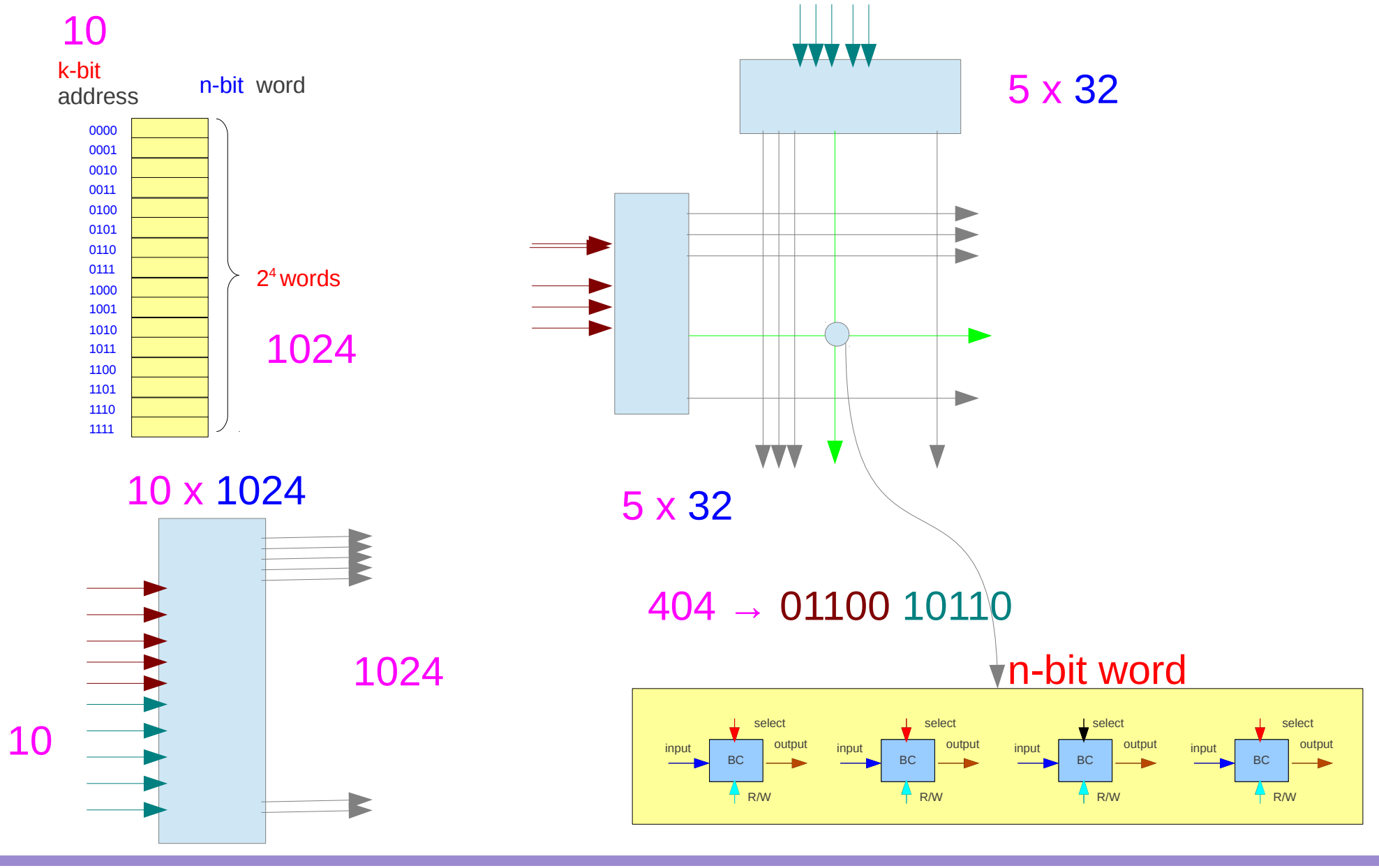
$$D_3 = A_1 \cdot A_0$$

2 x 4 decoder : 4 AND gates

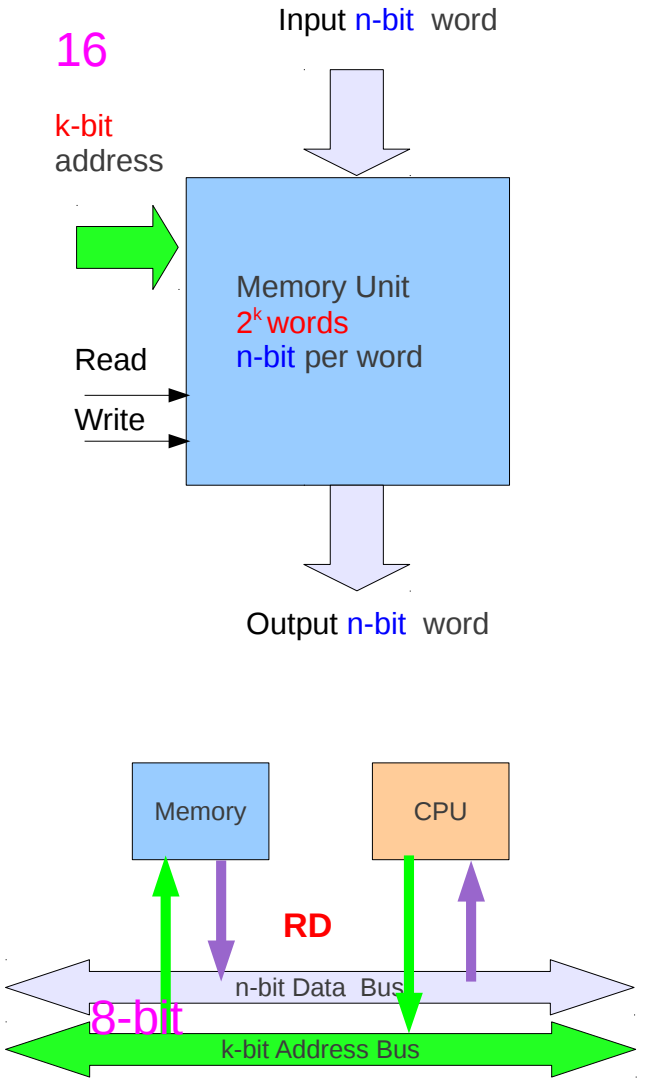
10 x 1024 decoder : 1024 AND gates

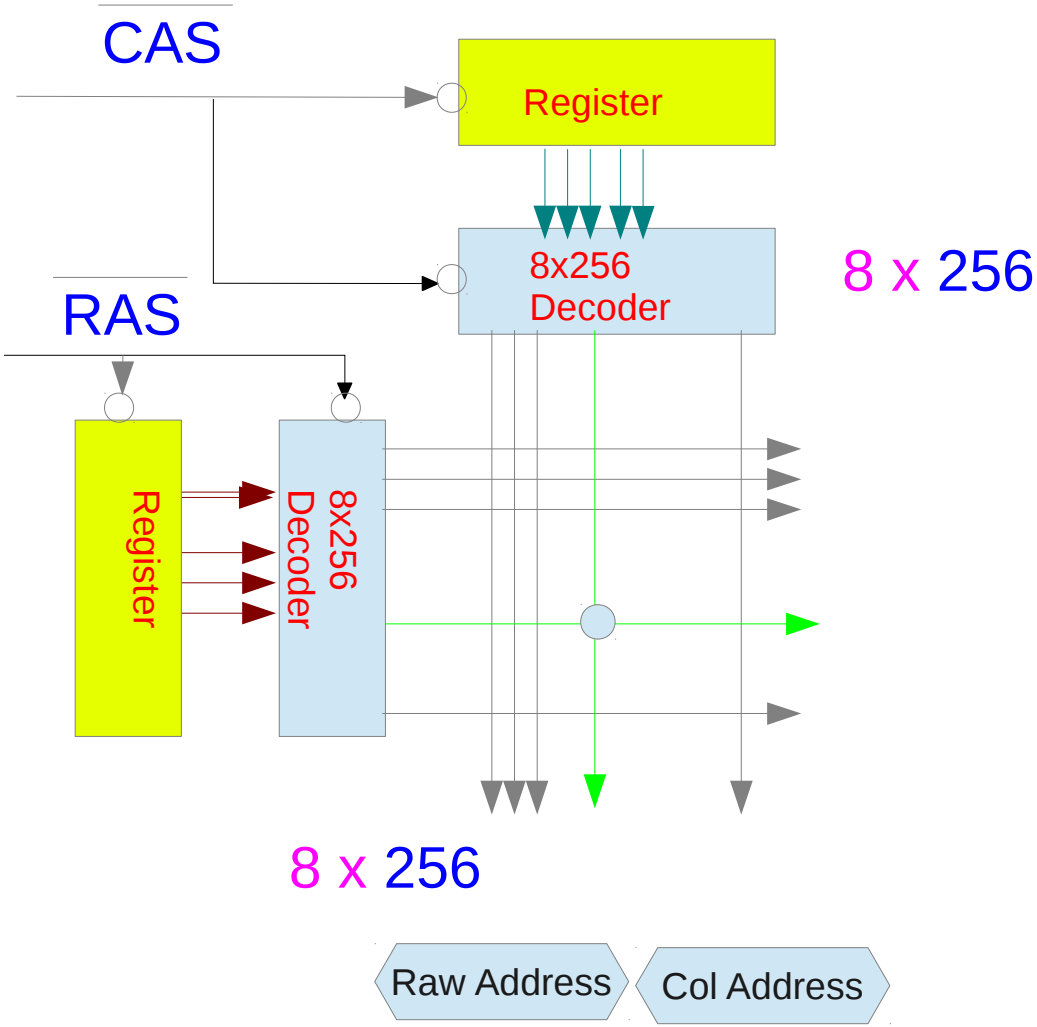
4 x 16 decoder : 16 AND gates

Coincidence Decoder



Time Sharing Address Bus





References

[1] http://en.wikipedia.org/
[2] M. M. Mano, C. R. Kime, “Logic and Computer Design Fundamentals”, 4th ed.
[3] D.M. Harris, S. L. Harris, “Digital Design and Computer Architecture”