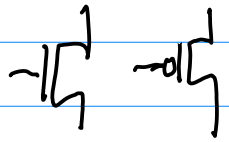
SOC HW #1

20160326

1.5 CMOS combinational circuit Transistor



(a) $Y = A = \bar{\bar{A}}$

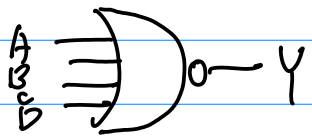
(b) $Y = A\bar{B} + \bar{A}B = A \oplus B$

(c) $Y = \bar{A}\bar{B} + AB = \overline{A \oplus B}$

(d) $Y = AB + BC + AC$

$A, \bar{A}, B, \bar{B}$

1.7 CMOS 4-input NOR



1.19 $A_0, \bar{A_0}, A_1, \bar{A_1}$

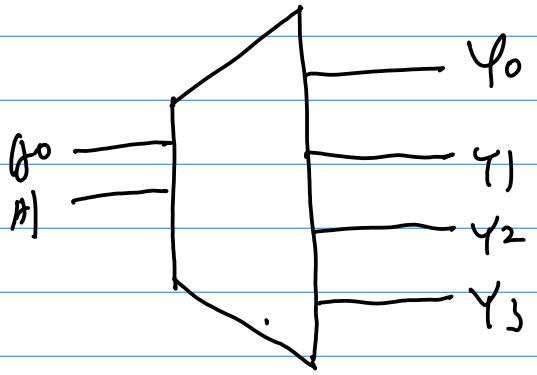
decoder

$Y_0 = \bar{A_1}\,\bar{A_0}$ 0 0

$Y_1 = \bar{A_1}\,A_0$ 0 1

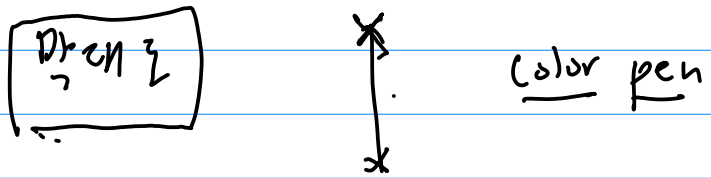
$Y_2 = A_1\,\bar{A_0}$ 1 0

$Y_3 = A_1\,A_0$ 1 1

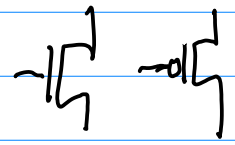


1.2| $\bar{F} = \overline{(A+B) \cdot (C+D)}$

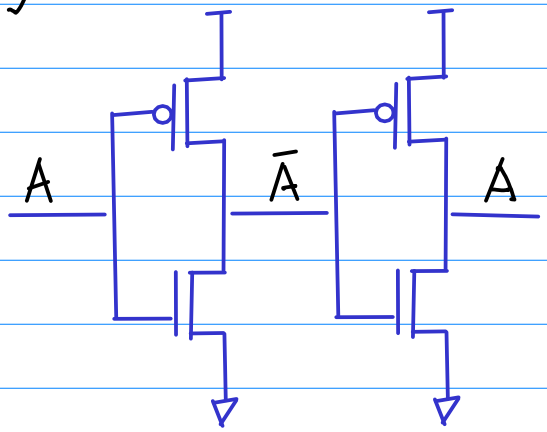
(a) Transistor level schematic

(b) 

1.5 CMOS combinational circuit Transistor

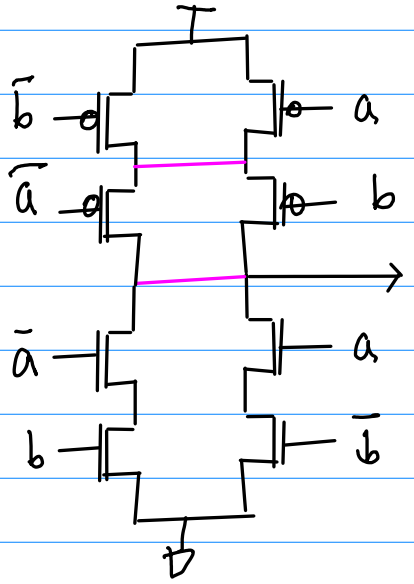


(a) $Y = A = \bar{\bar{A}}$



(b) $Y = A\bar{B} + \bar{A}B = A \oplus B$

XOR (AOI)



$\overline{a \oplus b}$

$(a+\bar{b}) \cdot (\bar{a}+b)$

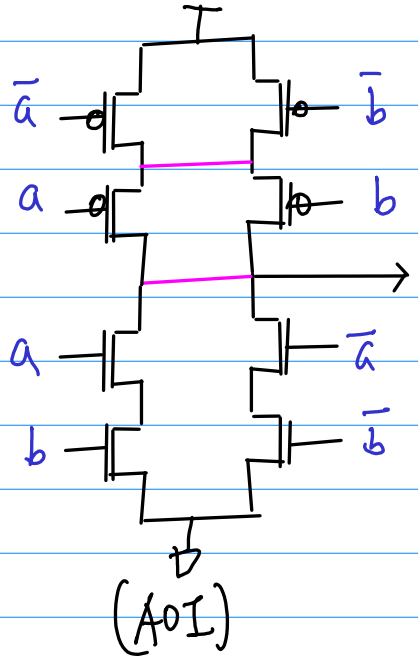
$= 0 + \bar{a}\bar{b} + ab + 0$

$= ab + \bar{a}\bar{b} = \overline{a \oplus b}$

$\bar{a}b + a\bar{b} = a \oplus b$

(c) $Y = \bar{A}\bar{B} + AB = \overline{A \oplus B}$

XNOR (AOI)



(AOI)

$\overline{a \oplus b}$

$(\bar{a}+\bar{b}) \cdot (a+b) = a\bar{b} + \bar{a}$

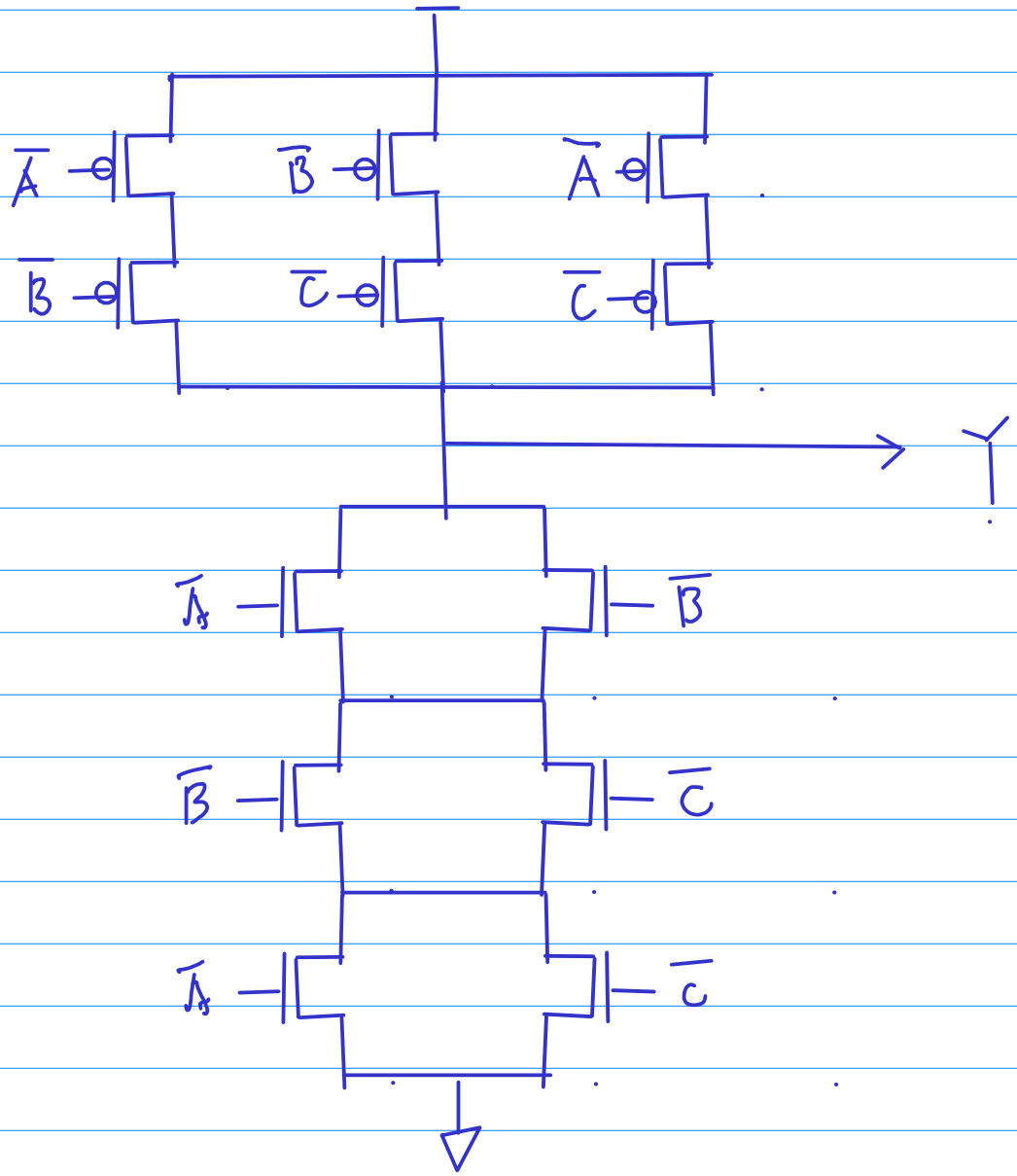
$= a \oplus b$

$ab + \bar{a}\bar{b} = \overline{a \oplus b}$

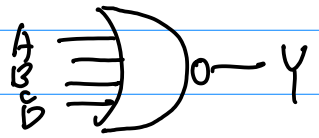
(d) $Y = AB + BC + AC$ pMOS PUN

$\overline{Y} = \overline{AB + BC + AC} = \overline{AB} \cdot \overline{BC} \cdot \overline{AC}$

$= (\overline{A} + \overline{B}) \cdot (\overline{B} + \overline{C}) \cdot (\overline{A} + \overline{C})$ n MOS PDN



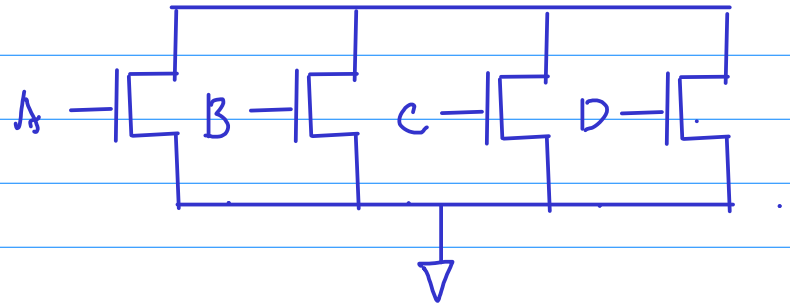
1.7 CMOS 4-input NOR



$$Y = \overline{A+B+C+D}$$

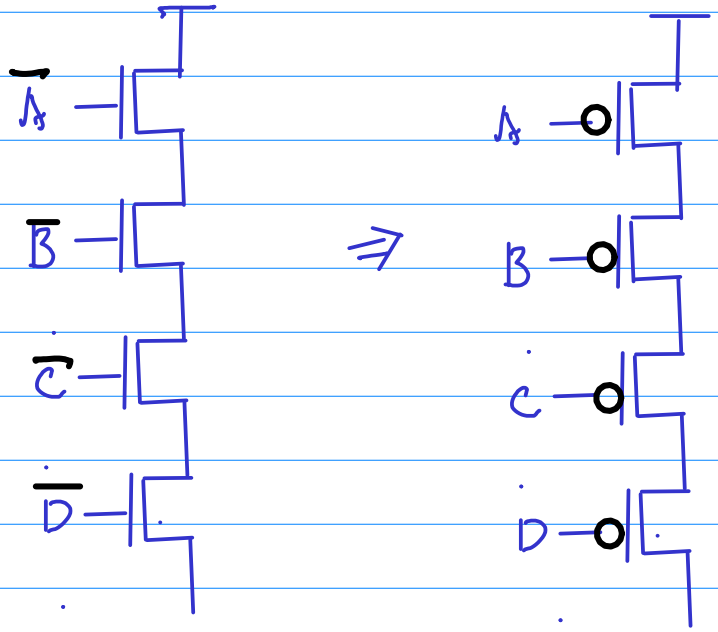
nMOS PDN

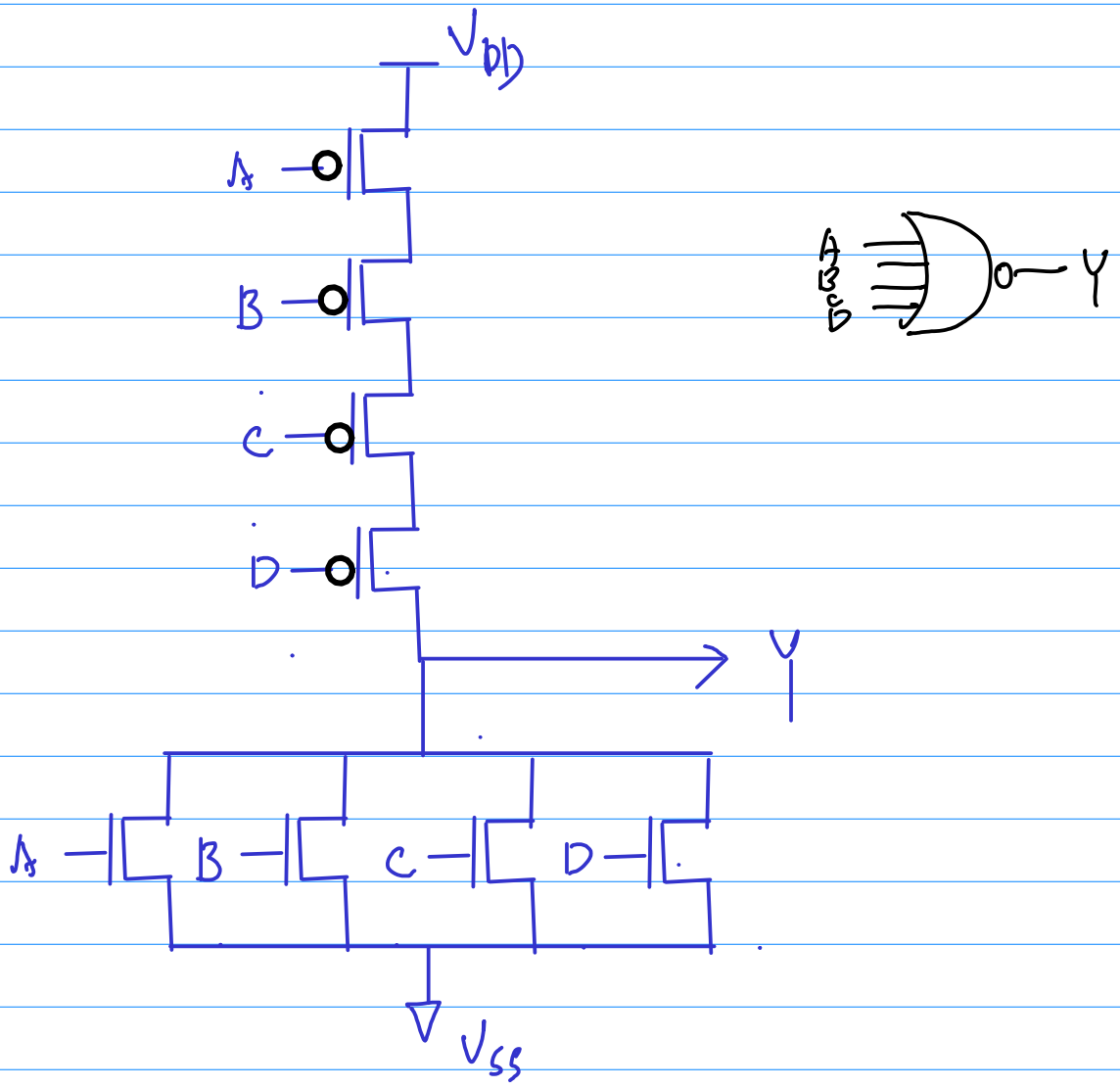
$$\overline{Y} = \overline{\overline{A+B+C+D}} = A+B+C+D$$



pMOS PUN

$$Y = \overline{A+B+C+D} = \overline{A}\cdot\overline{B}\cdot\overline{C}\cdot\overline{D}$$




V_{DD}
A
B
C
D
Y
A
B
C
D
Y
A
B
C
D
V_{SS}

1.19

$A_0, \overline{A_0}, A_1, \overline{A_1}$

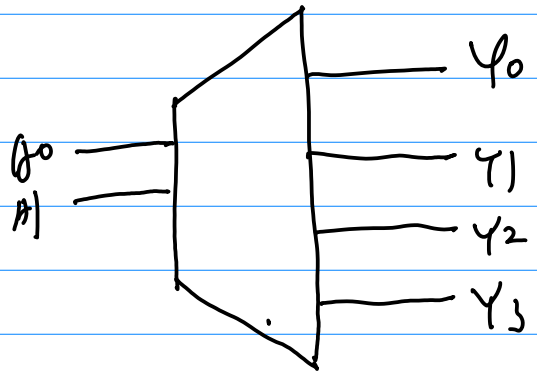
decoder

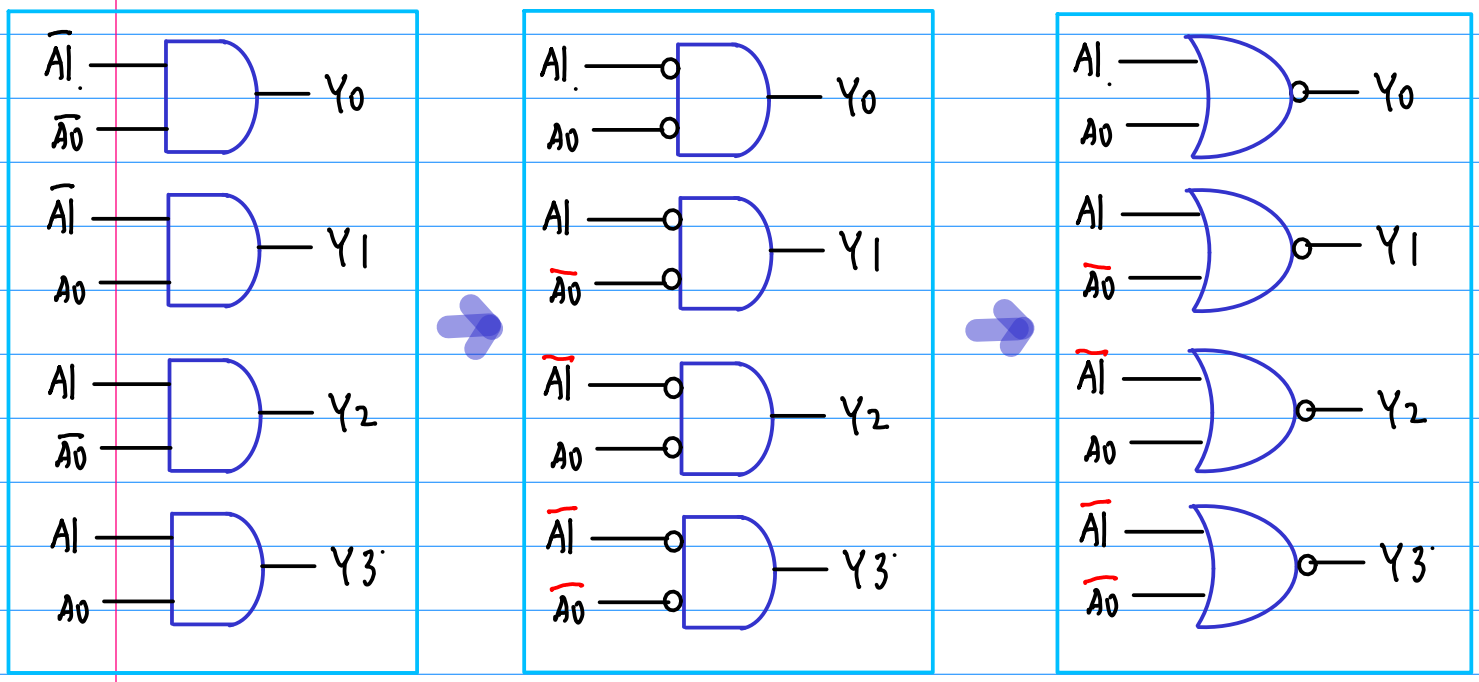
$Y_0 = \overline{A_1}\,\overline{A_0}$ 00

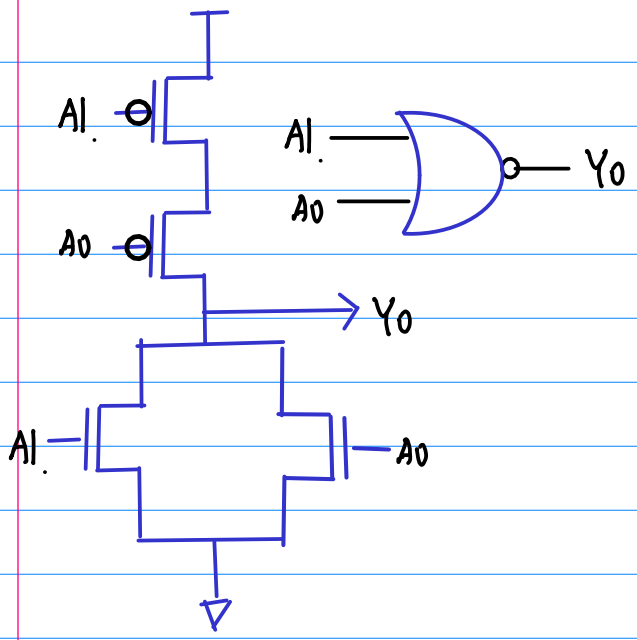
$Y_1 = \overline{A_1} A_0$ 01

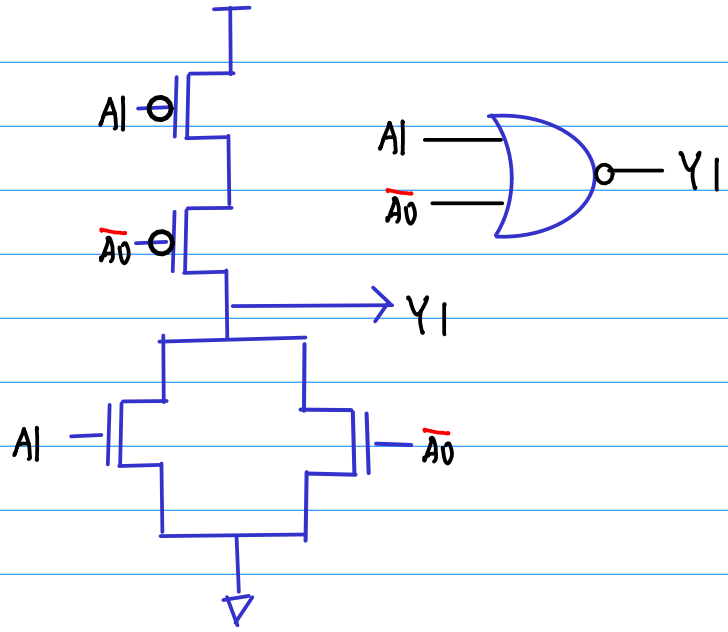
$Y_2 = A_1 \overline{A_0}$ 10

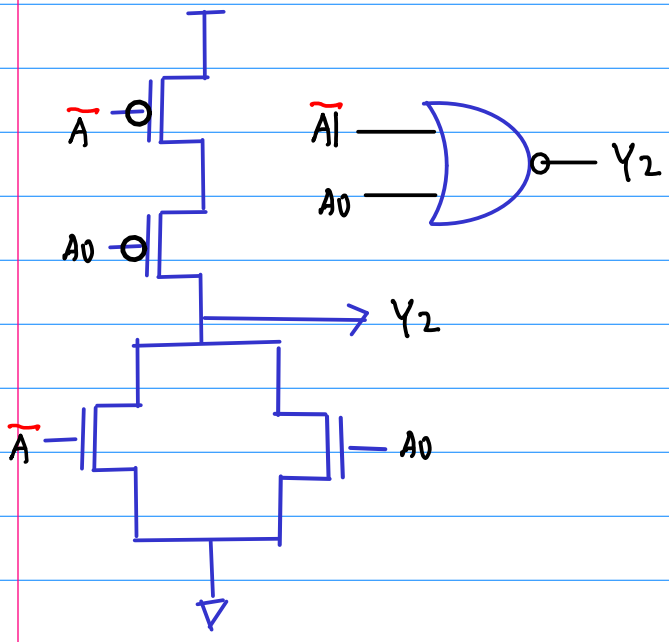
$Y_3 = A_1 A_0$ 11

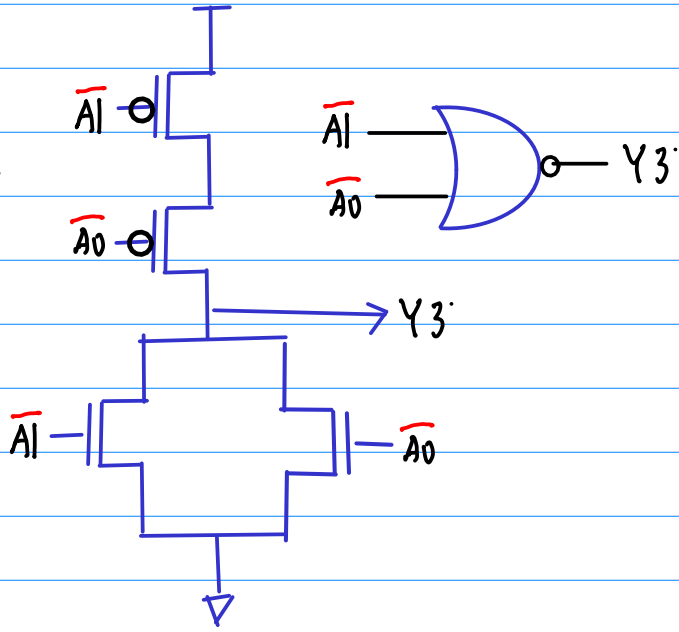





A1
A0
Y0
A1
A0
Y0
A1
A0

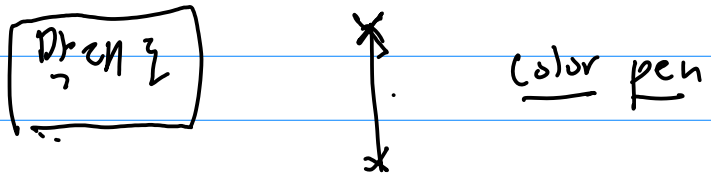

A1
A0
Y1
A1
A0
Y1
A1
A0


A
A0
Y2
A1
A0
Y2
A
A0


A1
A0
Y3
A1
A0
Y3
A1
A0

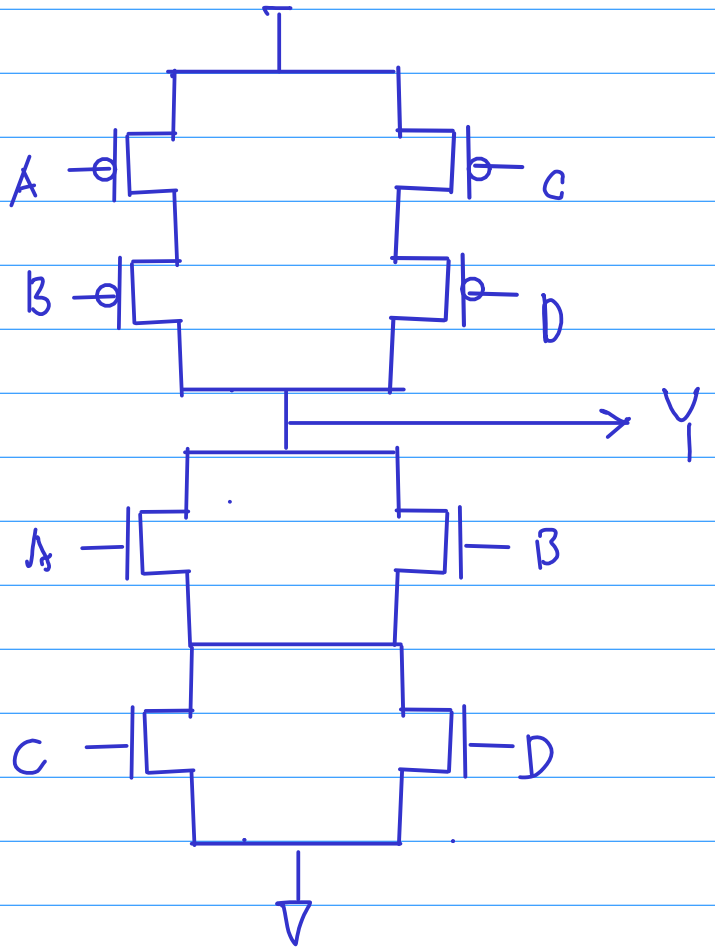
1.2| $\overline{F} = \overline{(A+B)\cdot(C+D)}$

(a) Transistor level schematic

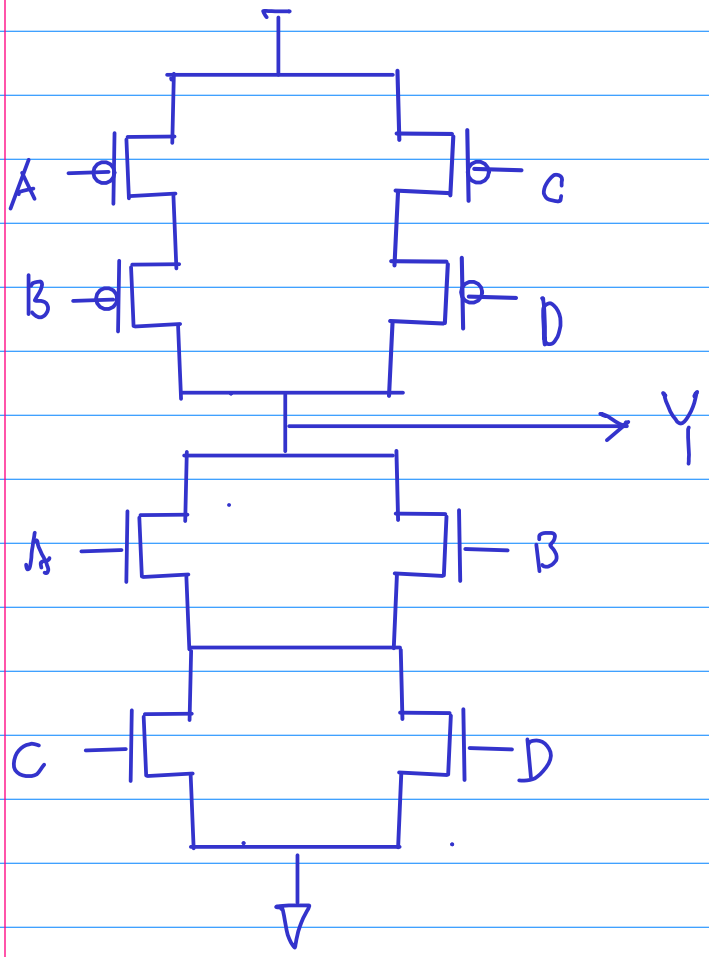
(b) 

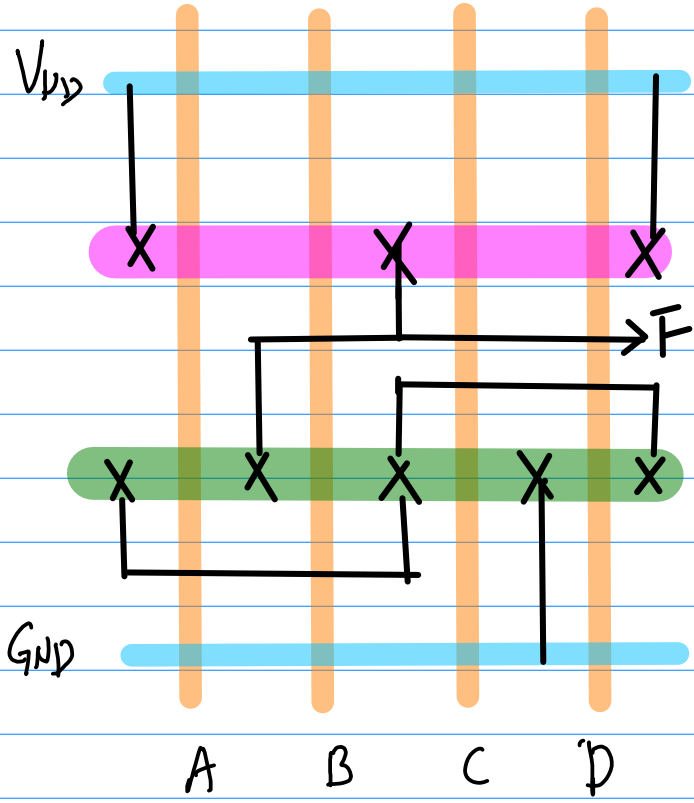
nMOS PDN $\overline{\overline{F}} = \overline{\overline{(A+B)\cdot(C+D)}} = (A+B)\cdot(C+D)$

pMOS PUN $\overline{F} = \overline{(A+B)\cdot(C+D)} = \overline{(A+B)} + \overline{(C+D)} = (\overline{A}\cdot\overline{B}) + (\overline{C}\cdot\overline{D})$

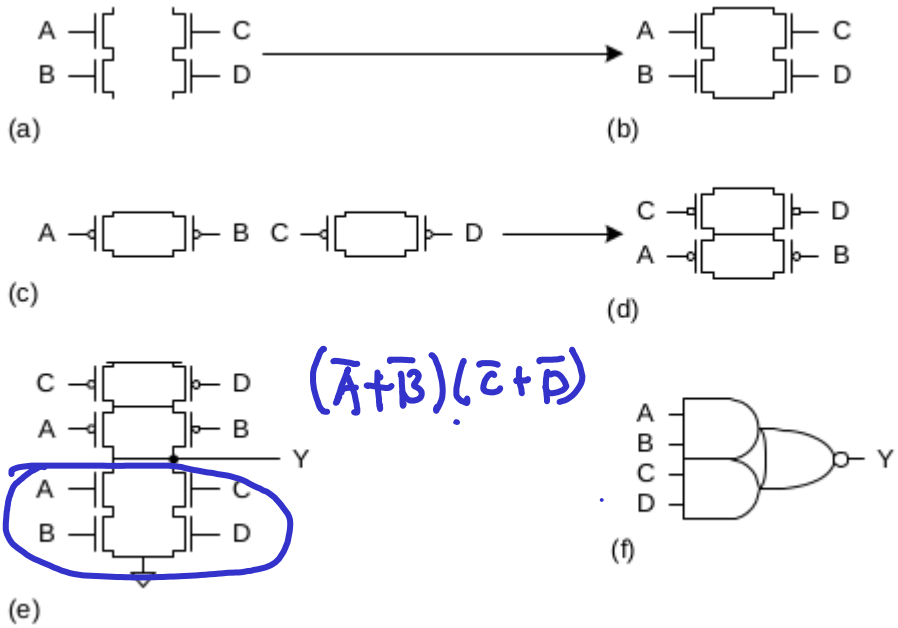


Stick Diagram





(f) Weste's Book



$(A+B)+(C\cdot D)$

$(\bar{C}+\bar{D})\cdot(\bar{A}+\bar{B})$

$(\bar{A}+\bar{B})(\bar{C}+\bar{D})$

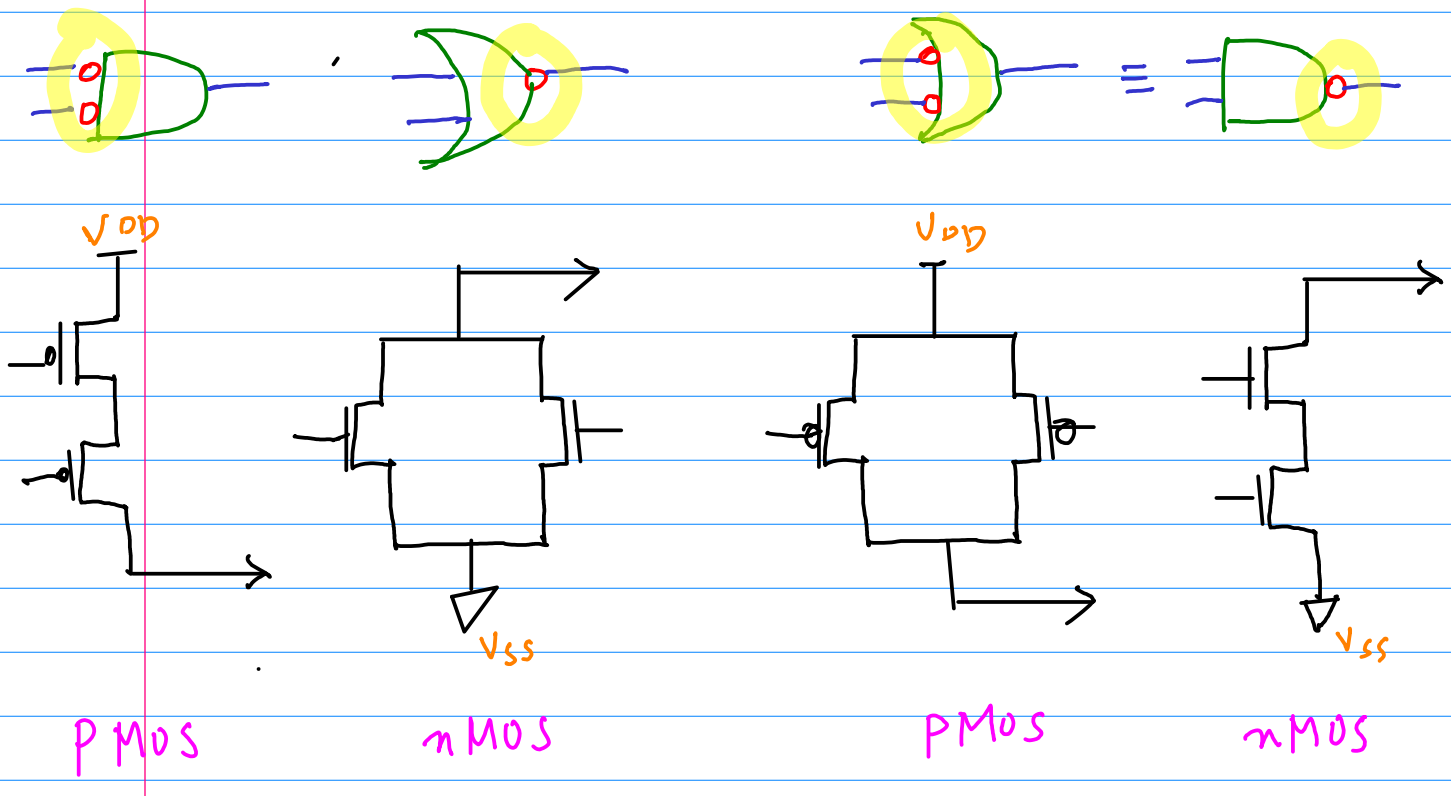
$\overline{AB+CD}$

$\overline{(A+B)+(C\cdot D)}$

$= \overline{A+B}\cdot\overline{C\cdot D}$

$= (\bar{A}+\bar{B})\cdot(\bar{C}+\bar{D})$

Basic nMOS, pMOS Configurations

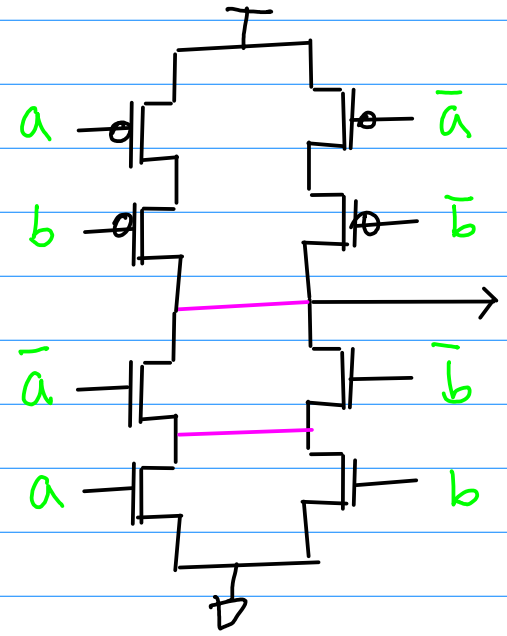


XNOR, XOR using OAI

$$a \oplus b = \bar{a} \cdot b + a \bar{b}$$

$$\overline{a \oplus b} = ab + \bar{a}\bar{b}$$

XNOR (OAI)



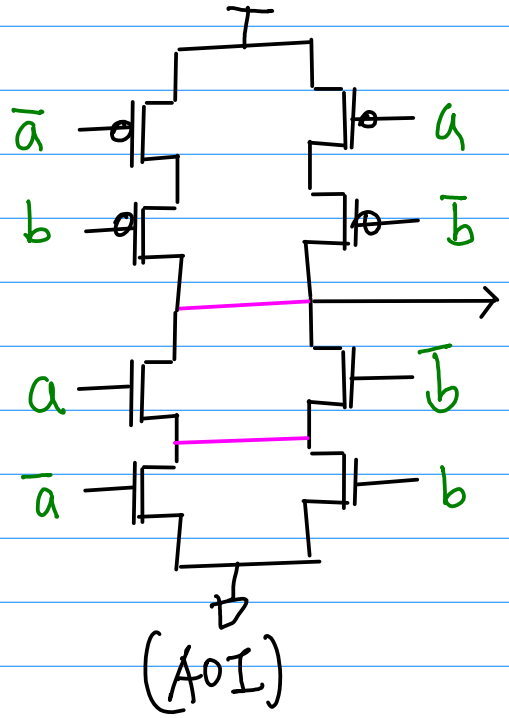
$ab + \bar{a}\bar{b} = \overline{a \oplus b}$

$\overline{a \oplus b}$

$(\bar{a} + \bar{b}) \cdot (a + b)$

$= a\bar{b} + \bar{a}b = a \oplus b$

XOR (OAI)



(AOI)

$\bar{a}b + a\bar{b} = a \oplus b$

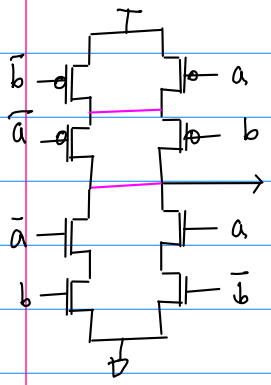
$\overline{a \oplus b}$

$(a + \bar{b}) \cdot (\bar{a} + b)$

$= ab + \bar{a}\bar{b} = \overline{a \oplus b}$

✳ Which one is better?

XNOR (AOI)

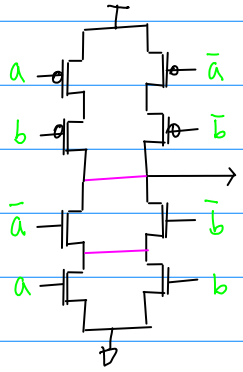


$(a+\bar{b})\cdot(\bar{a}+b)$
$= 0 + \bar{a}\bar{b} + ab + 0$
$= ab + \bar{a}\bar{b} = \overline{a \oplus b}$

$\overline{a \oplus b}$

$\bar{a}b + a\bar{b} = a \oplus b$

XNOR (OAI)

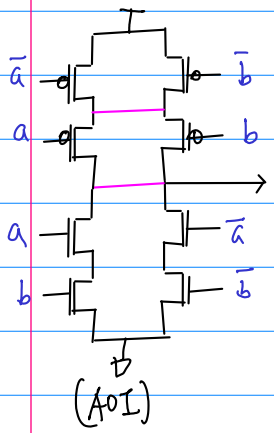


$ab + \bar{a}\bar{b} = \overline{a \oplus b}$

$\overline{a \oplus b}$

$(\bar{a}+\bar{b})\cdot(a+b)$
$= a\bar{b} + \bar{a}b = a \oplus b$

XOR (AOI)

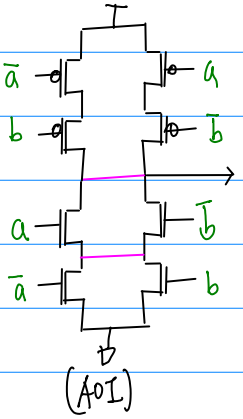


$(\bar{a}+\bar{b})\cdot(a+b) = a\bar{b} + \bar{a}$
$= a \oplus b$

$\overline{a \oplus b}$

$ab + \bar{a}\bar{b} = \overline{a \oplus b}$

XOR (OAI)



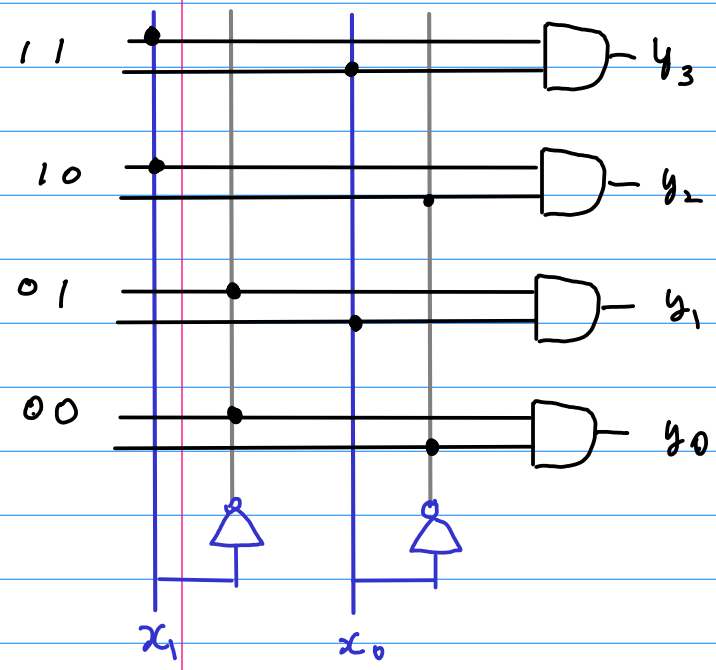
$\bar{a}b + a\bar{b} = a \oplus b$

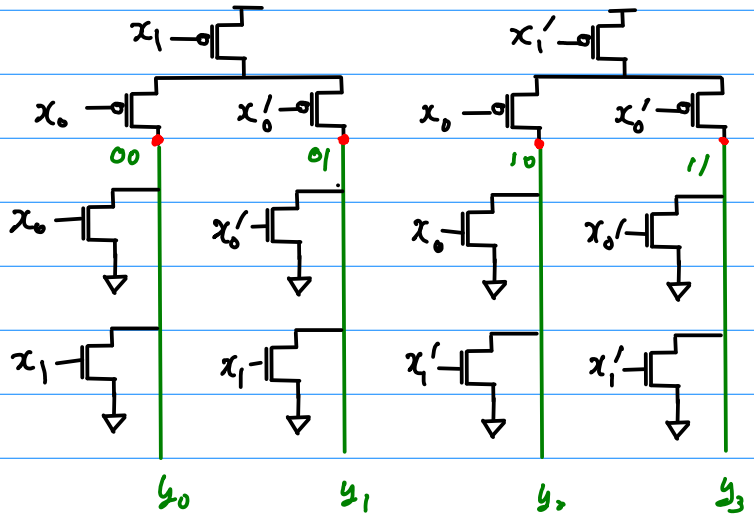
$\overline{a \oplus b}$

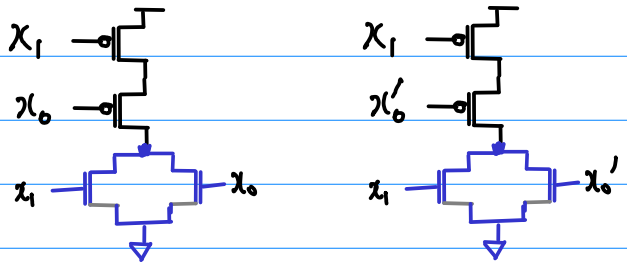
$(a+\bar{b})\cdot(\bar{a}+b)$
$= ab + \bar{a}\bar{b} = \overline{a \oplus b}$

Decoder

x_1	x_0	y_3	y_2	y_1	y_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0







$x_1 x_0$ = 00

all nMOS OFF

$y_0 \rightarrow 1$

$x_1 x_0$ = 01

all nMOS OFF

$y_1 \rightarrow 1$

$x_1 x_0$ = 10

all nMOS OFF

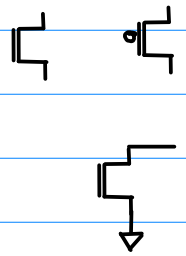
$y_2 \rightarrow 1$

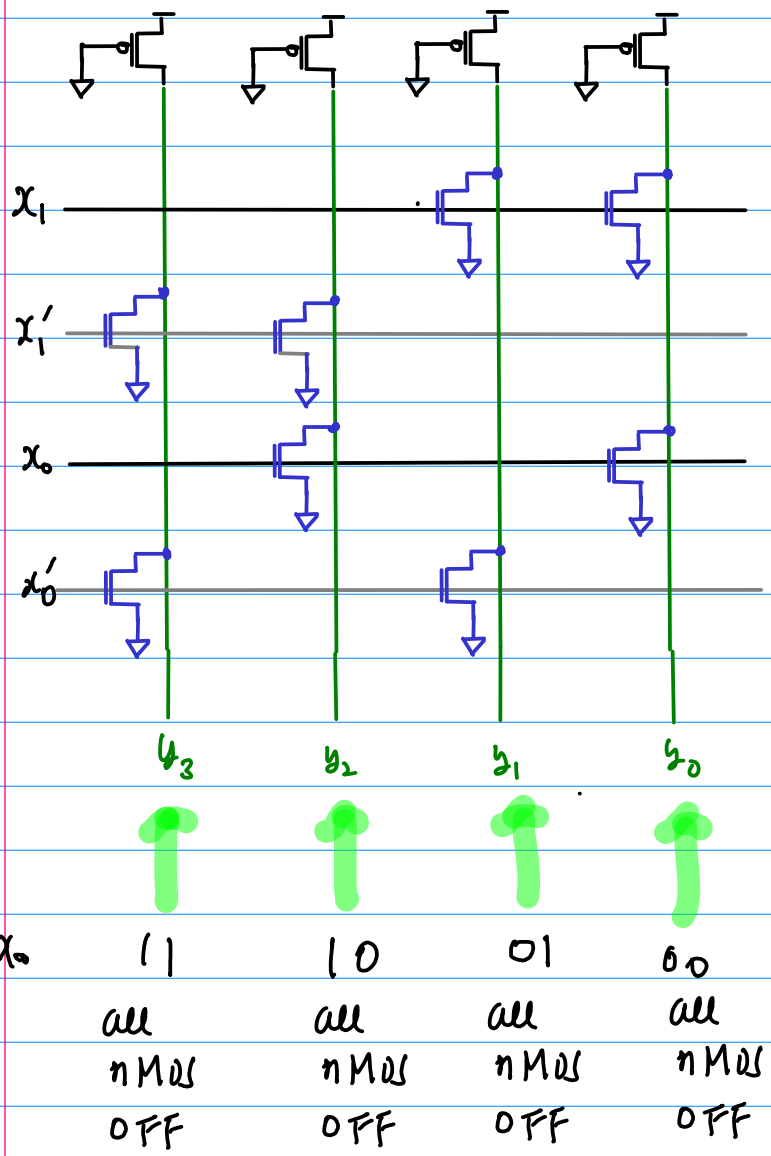
$x_1 x_0$ = 11

all nMOS OFF

$y_3 \rightarrow 1$

x_1	x_0	y_3	y_2	y_1	y_0
0	0	0	0	0	1
0	1	0	0	1	0
1	0	0	1	0	0
1	1	1	0	0	0





x_1x_0	11	10	01	00
	all nMOS OFF	all nMOS OFF	all nMOS OFF	all nMOS OFF