

# RAM Timing(1A)

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# Memory Types

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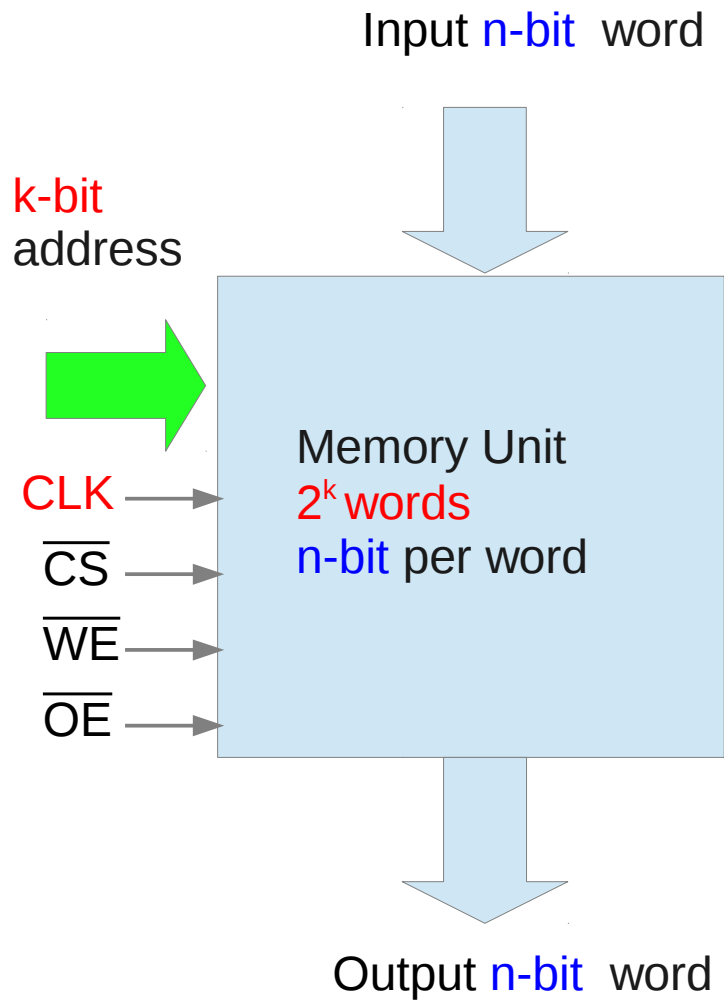
RAM (Random Access Memory)

SRAM (Static RAM) – **Fast**  
Synchronous SRAM  
Asynchronous SRAM

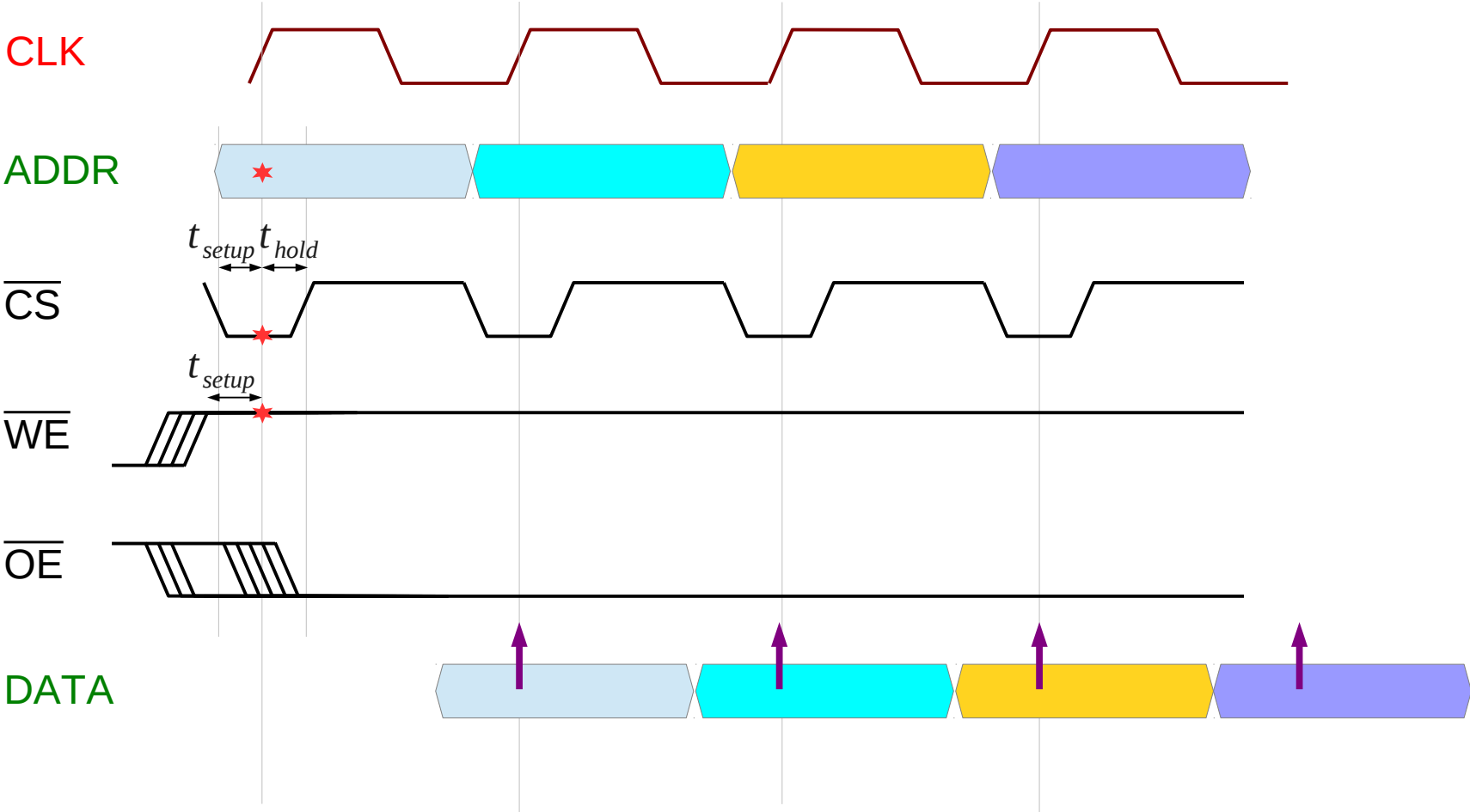
DRAM (Dynamic RAM) – **High Density**

ROM (Read Only Memory)

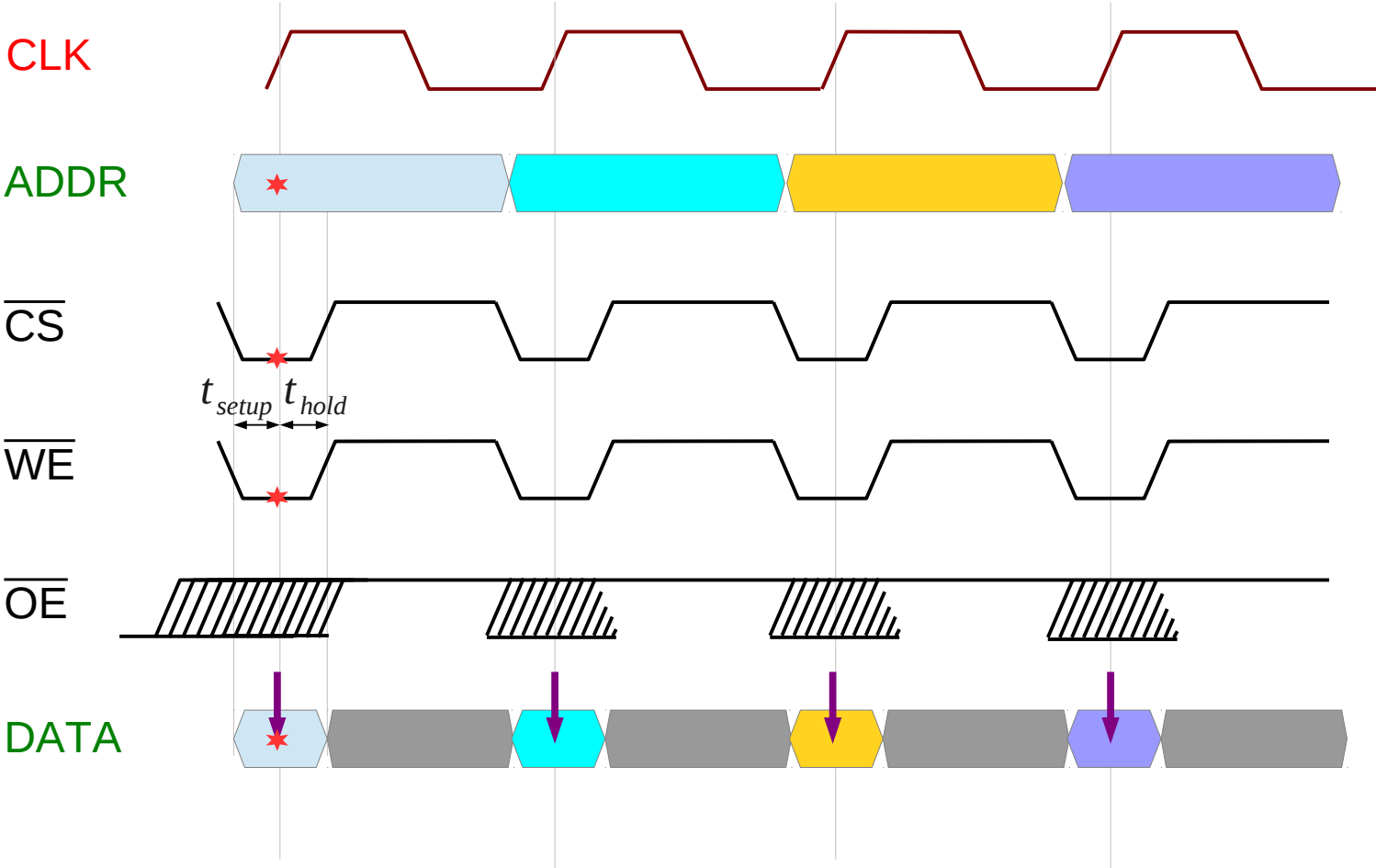
# Synchronous SRAM



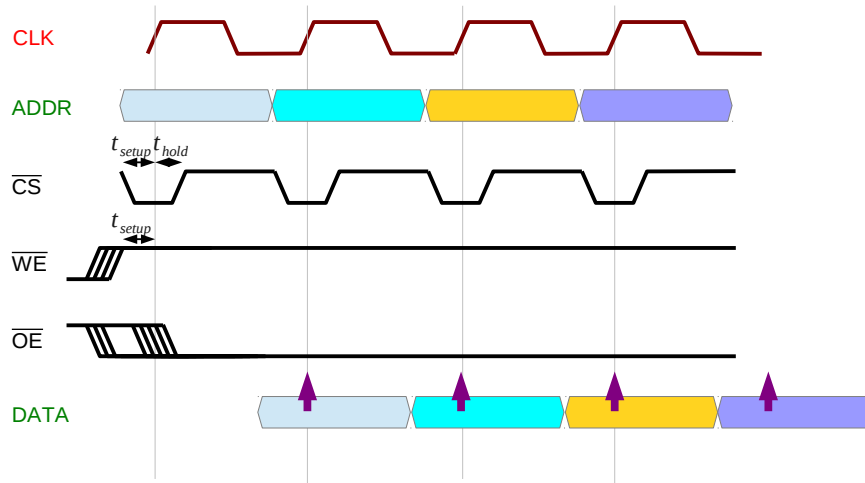
# Synchronous SRAM Read Cycle



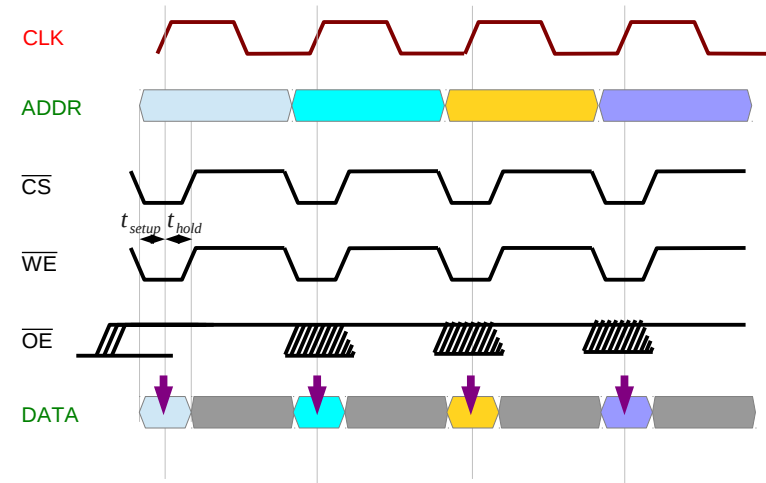
# Synchronous SRAM Write Cycle



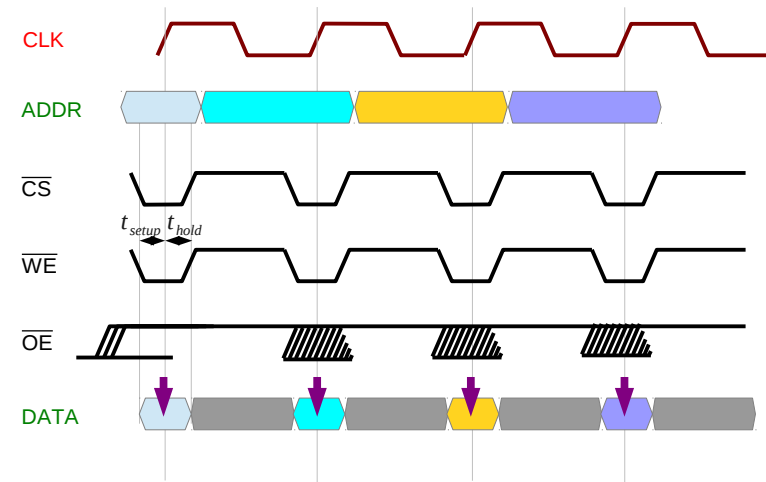
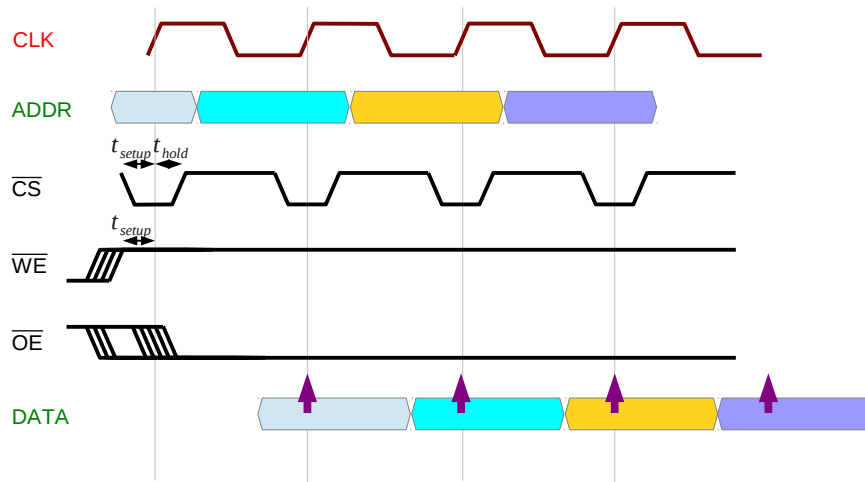
# Synchronous SRAM Cycle



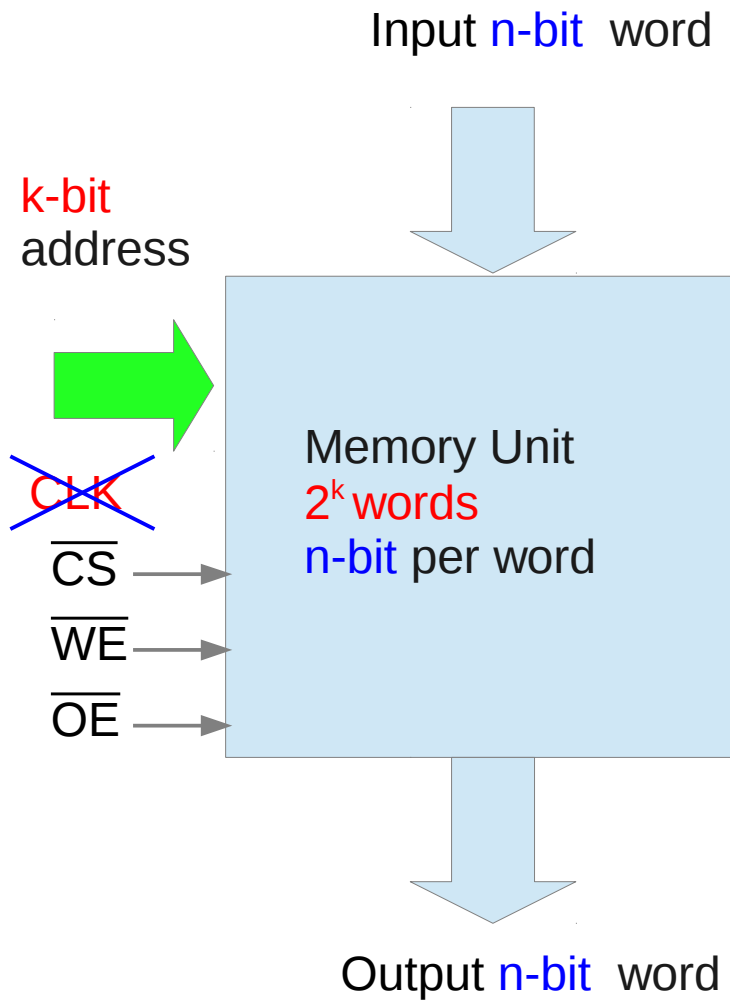
**Sync SRAM RD Cycle**



**Sync SRAM WR Cycle**



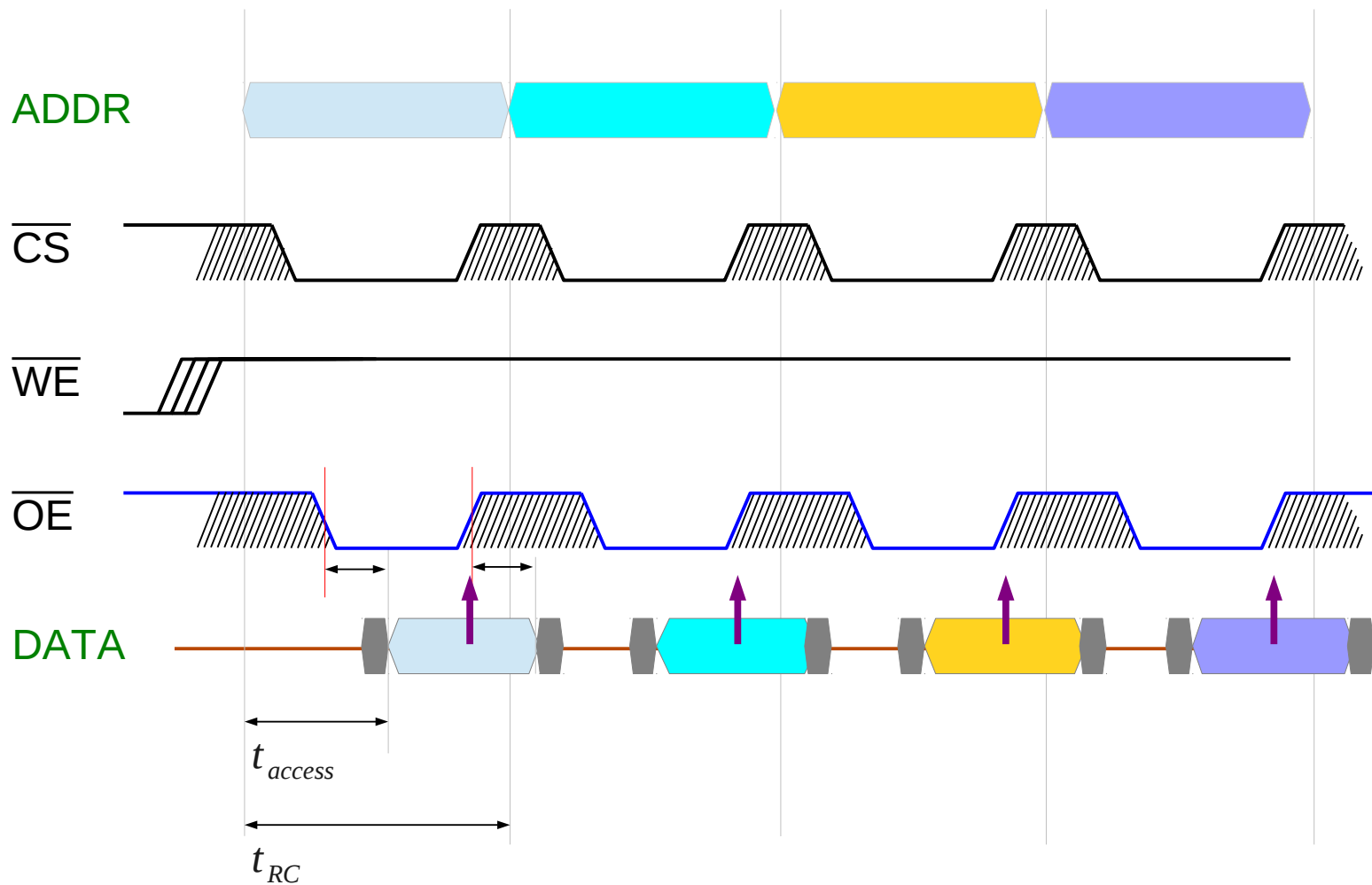
# Asynchronous SRAM





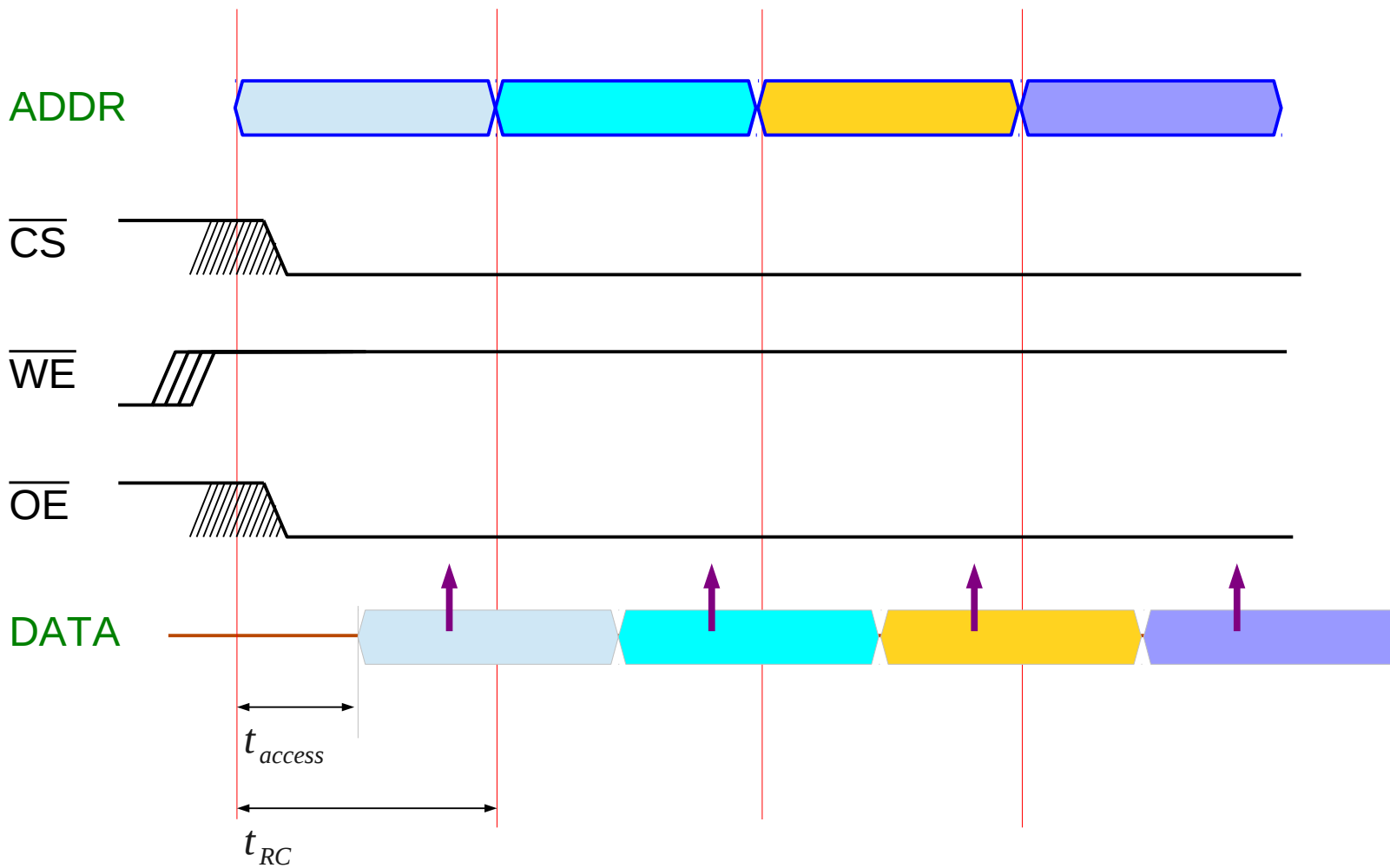
# Asynchronous SRAM Read Cycle

$\overline{\text{OE}}$  Controlled



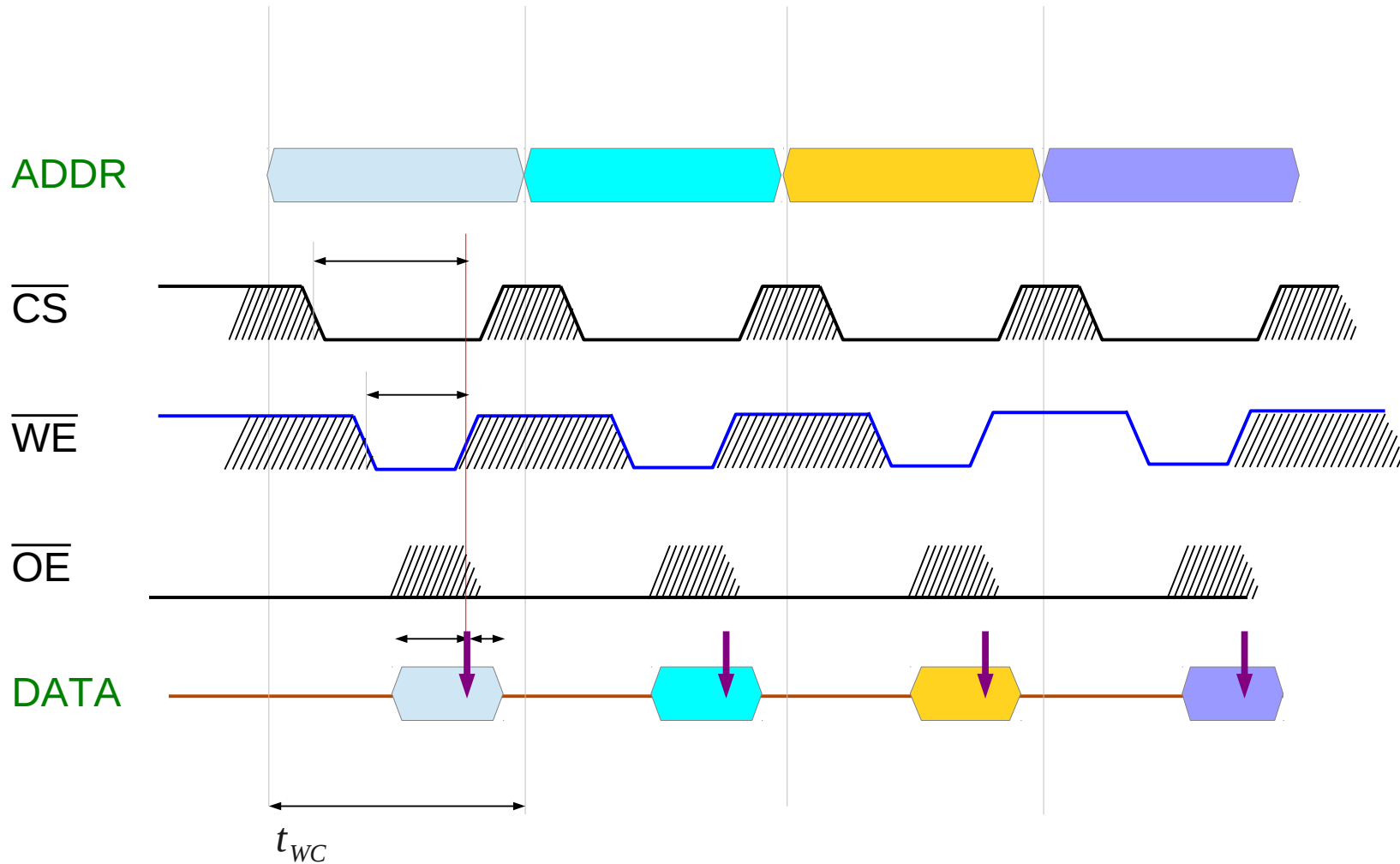
# Asynchronous SRAM Read Cycle

## Address Transition Controlled



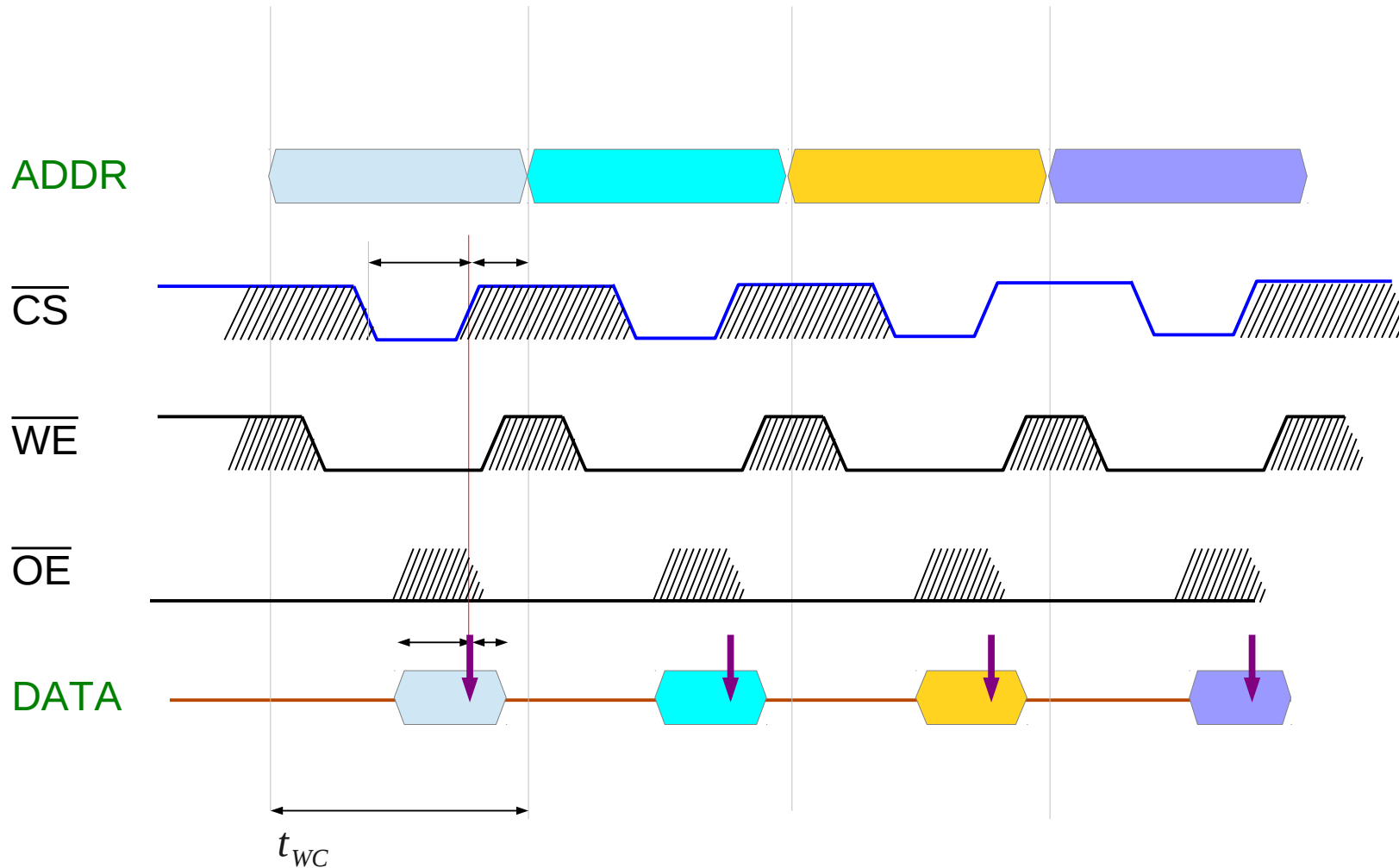
# Asynchronous SRAM Write Cycle

**$\overline{WE}$  Controlled**



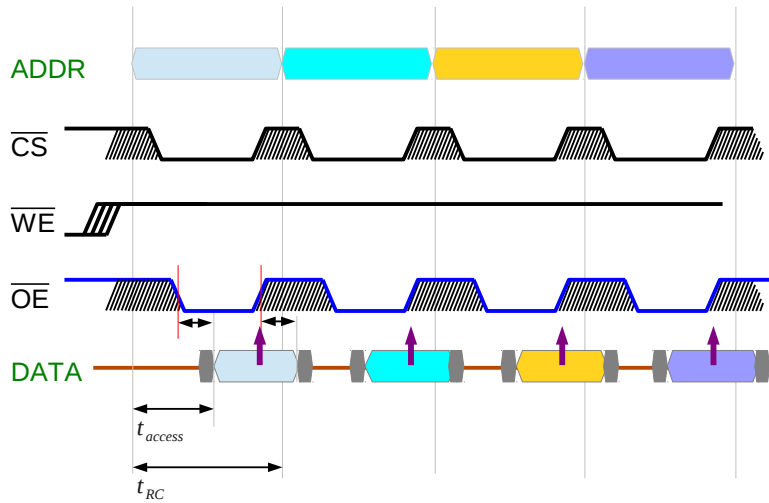
# Asynchronous SRAM Write Cycle

**$\overline{\text{CS}}$  Controlled**

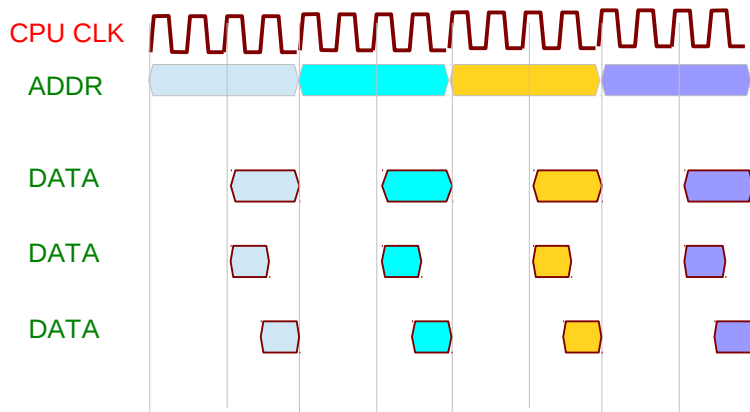


# Asynchronous SRAM Cycle

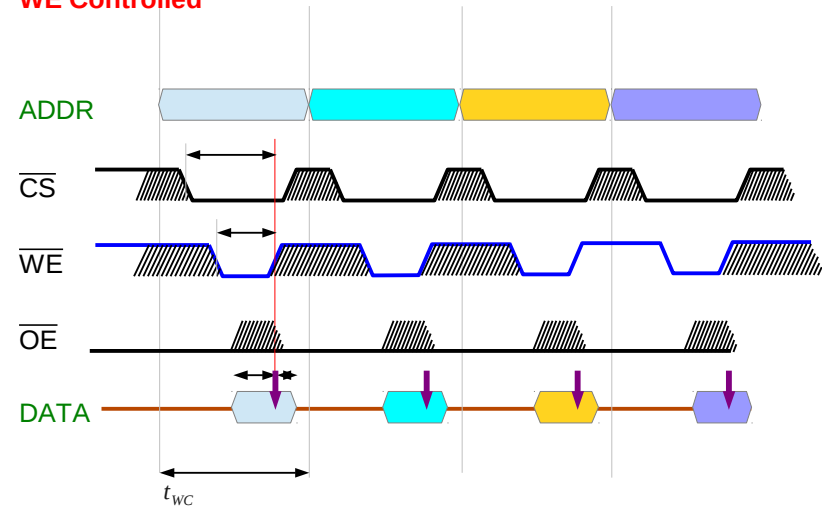
**$\overline{OE}$  Controlled**



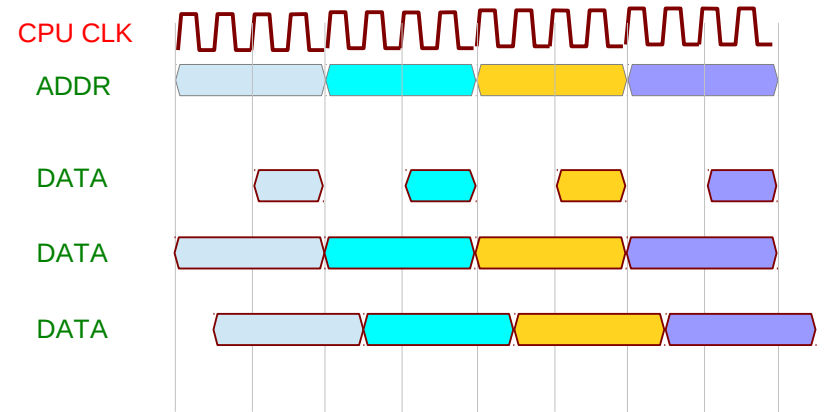
**Async SRAM RD Cycle**



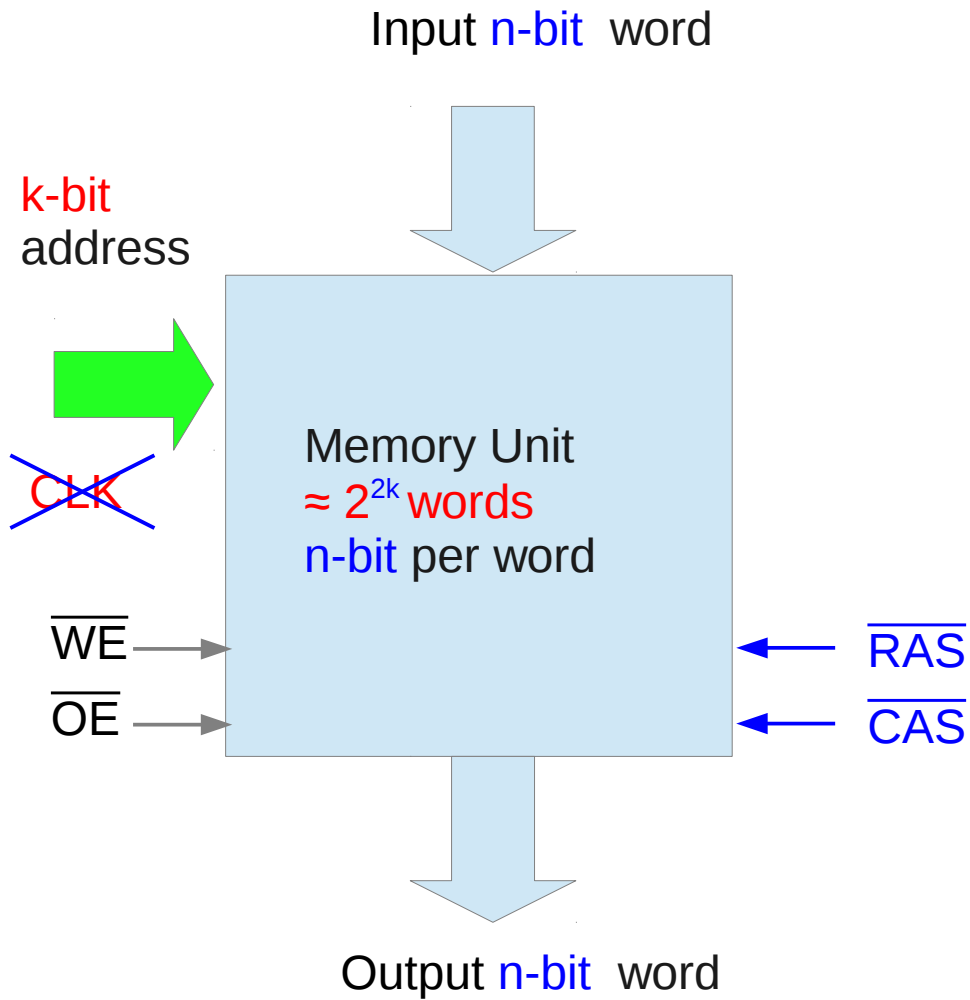
**$\overline{WE}$  Controlled**



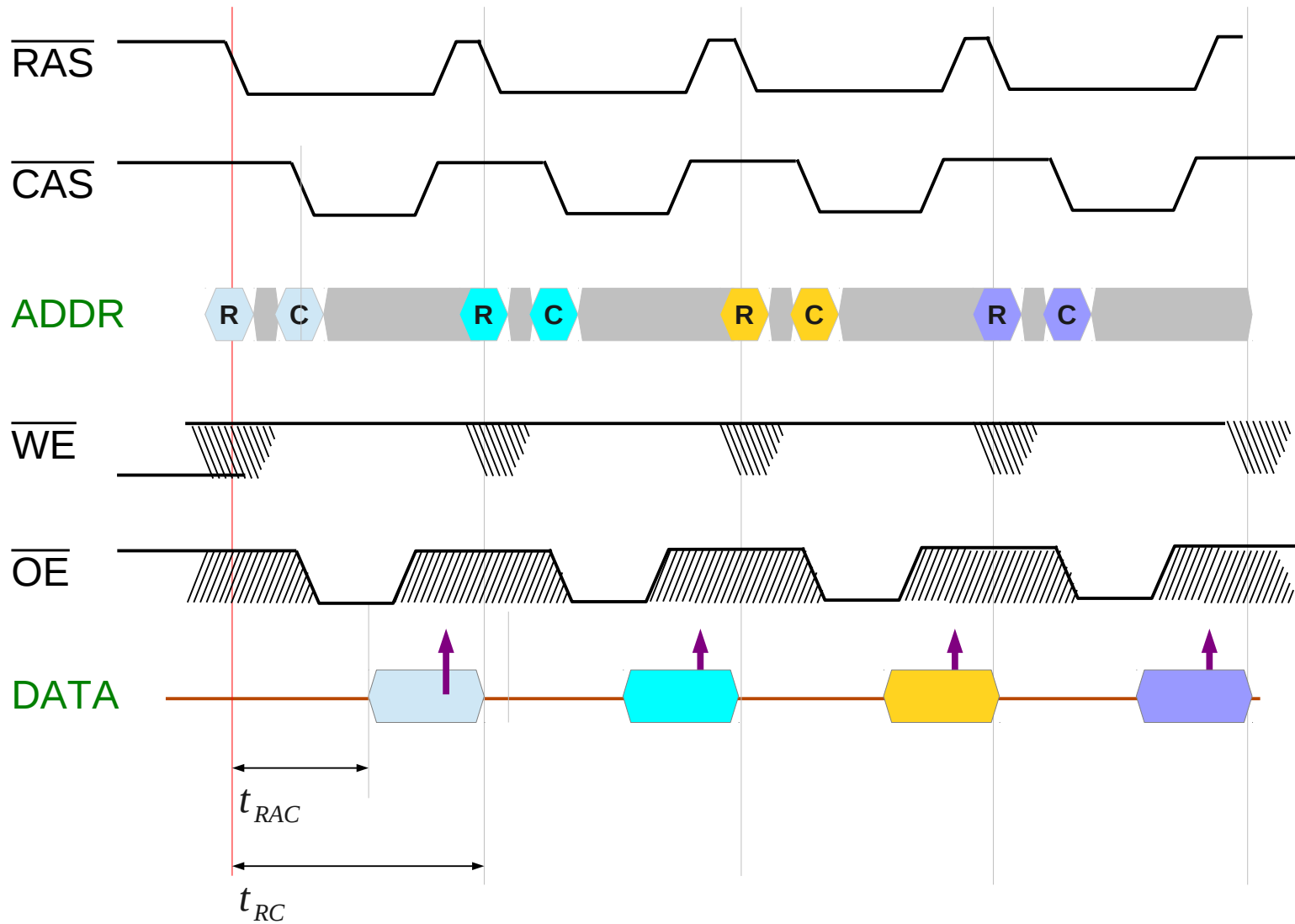
**Async SRAM WR Cycle**



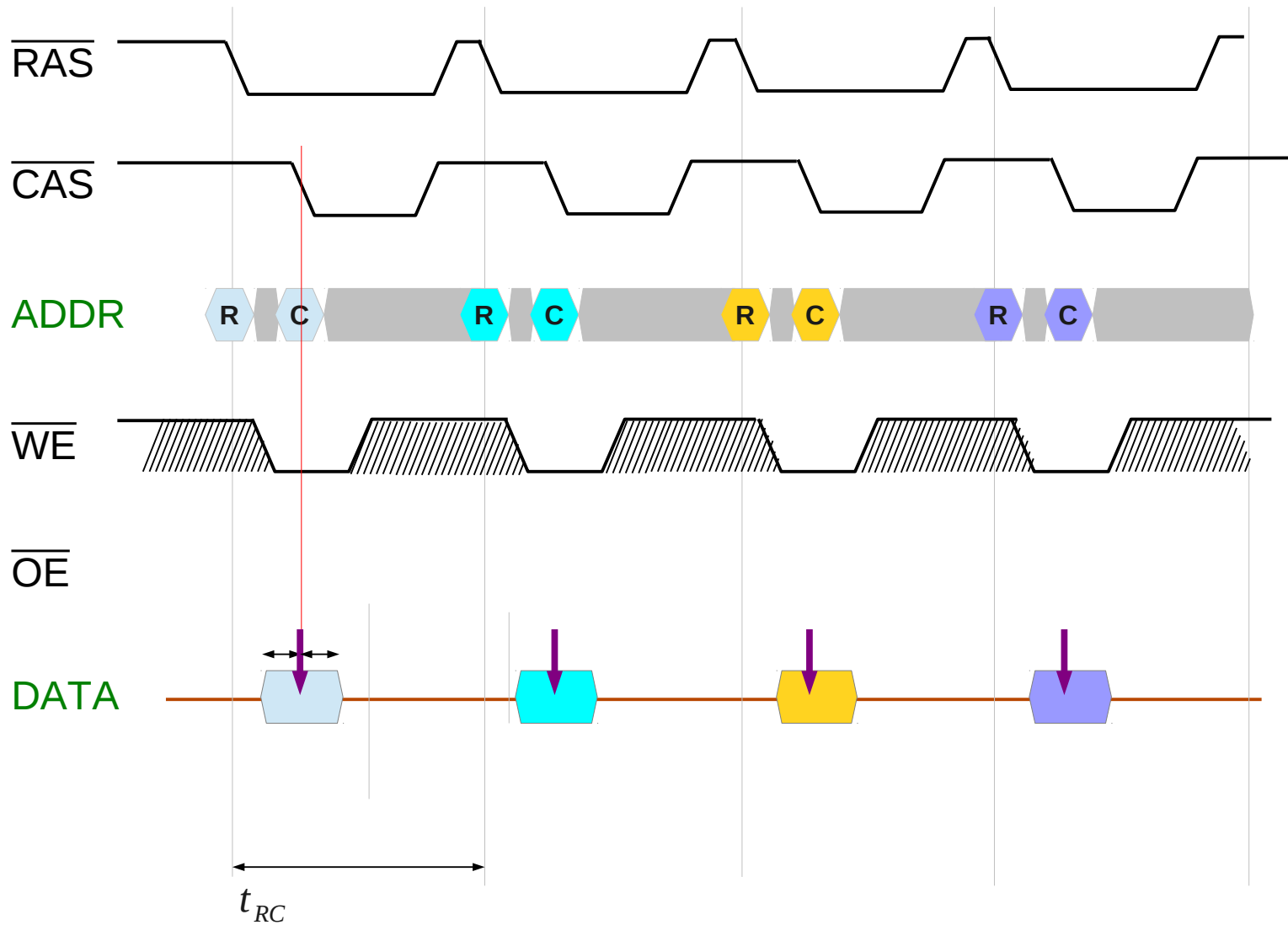
# DRAM



# DRAM Read Cycle



# DRAM Write Cycle





## References

- [1] <http://en.wikipedia.org/>
- [2] M. M. Mano, C. R. Kime, "Logic and Computer Design Fundamentals", 4<sup>th</sup> ed.
- [3] D.M. Harris, S. L. Harris, "Digital Design and Computer Architecture"