RAM Timing(1A)

Please send corrections (or suggestions) to youngwlim@hotmail.com.

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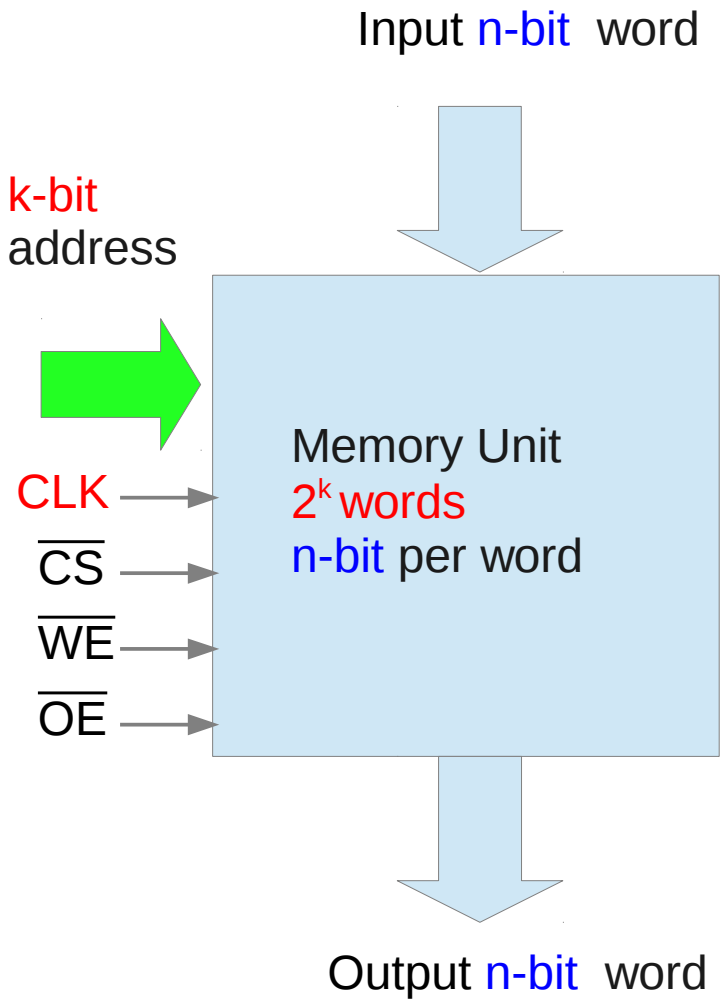
Memory Types

RAM (Random Access Memory)

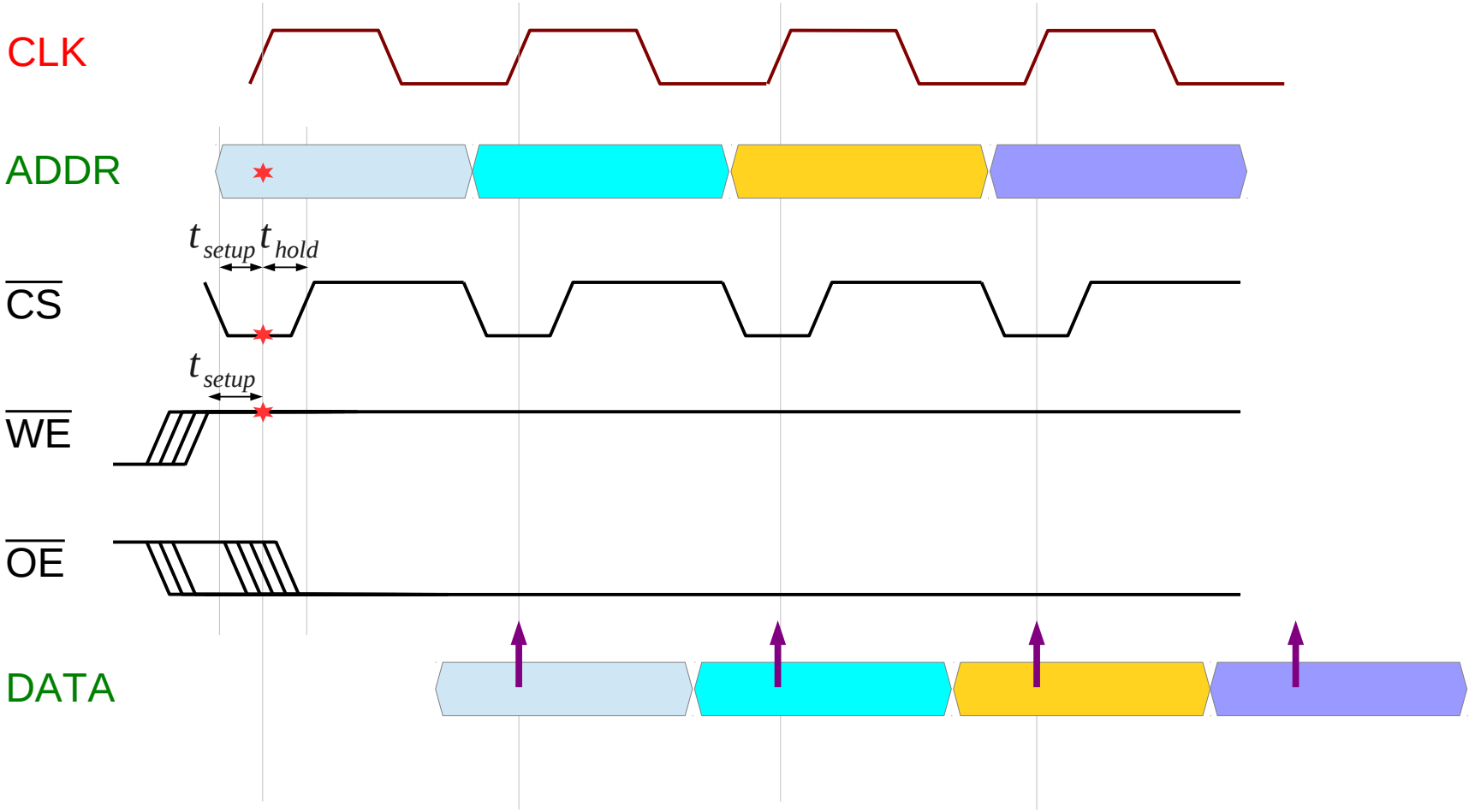
- SRAM (Static RAM) – Fast
  - Synchronous SRAM
  - Asynchronous SRAM
- DRAM (Dynamic RAM) – High Density

ROM (Read Only Memory)

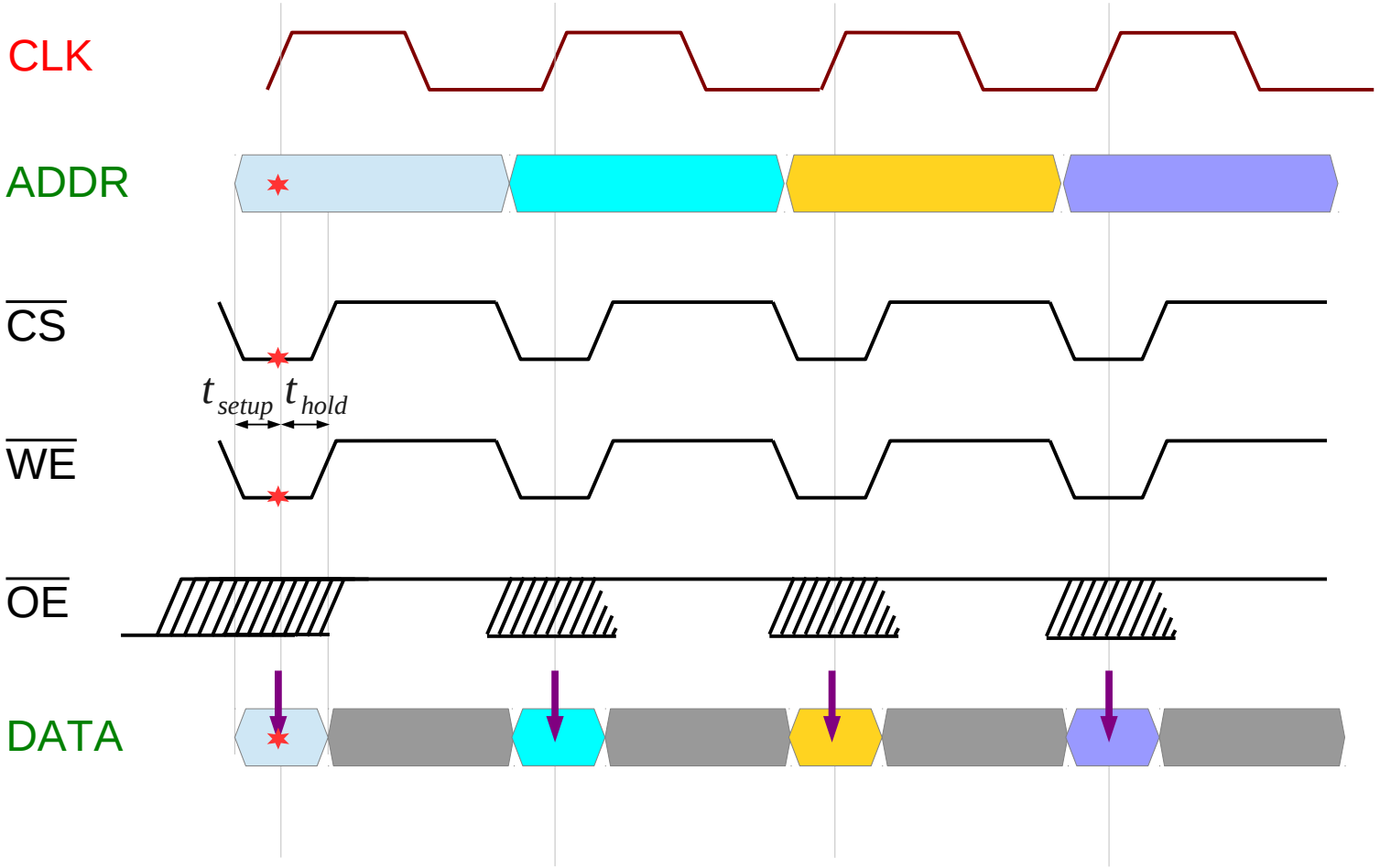
Synchronous SRAM



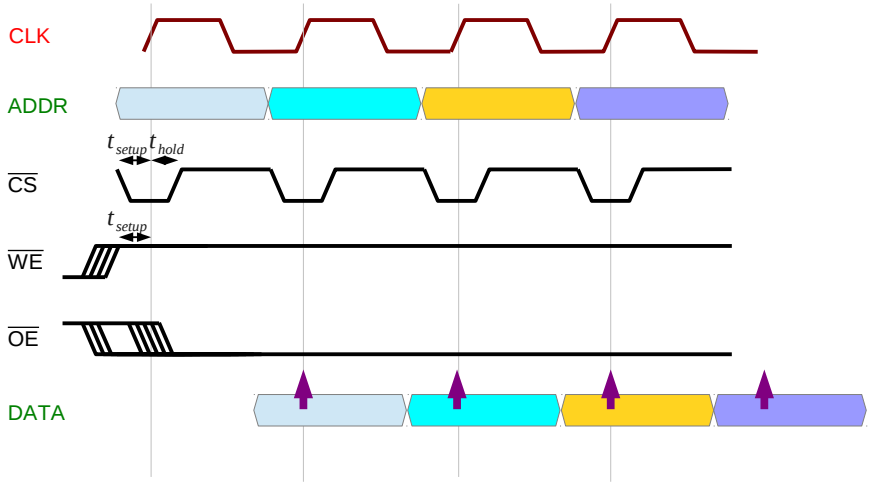
Synchronous SRAM Read Cycle



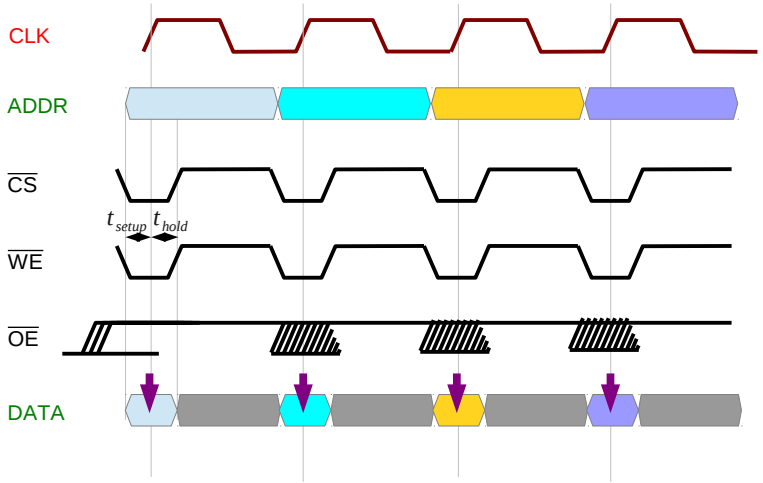
Synchronous SRAM Write Cycle



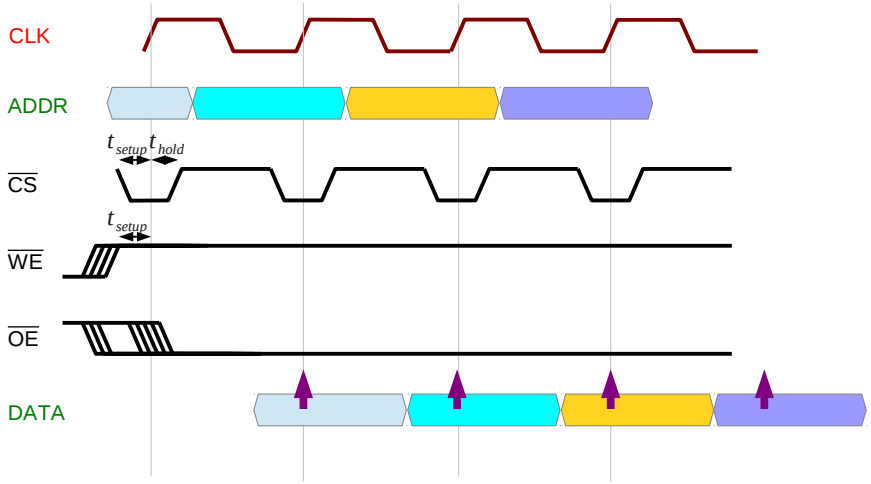
Synchronous SRAM Cycle

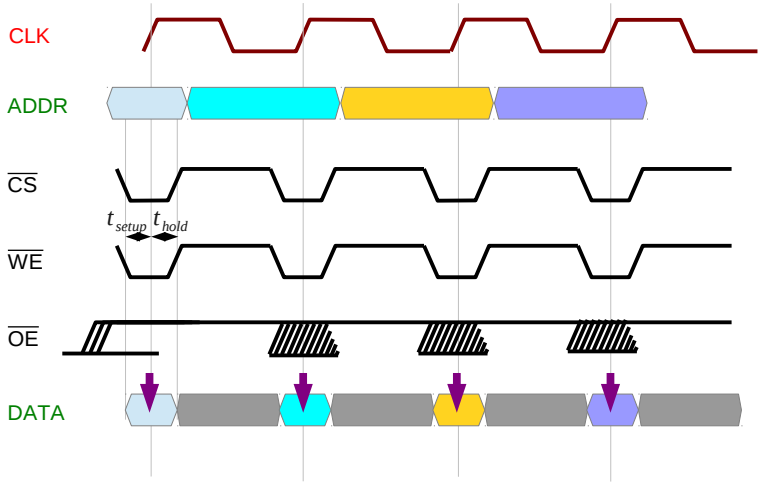


Sync SRAM RD Cycle

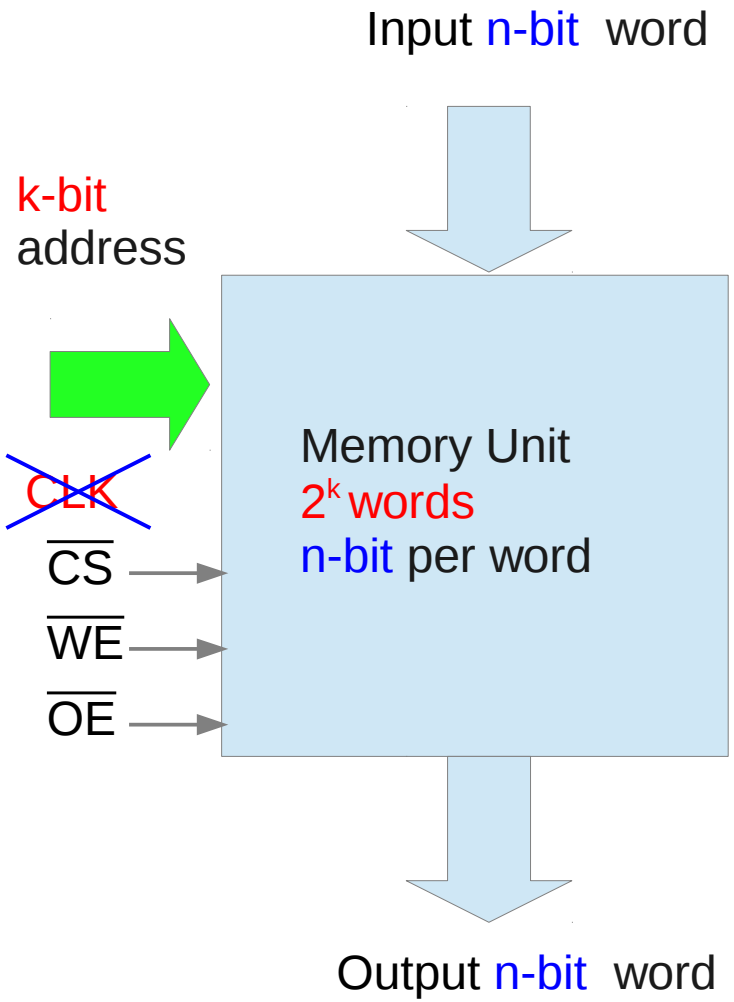


Sync SRAM WR Cycle



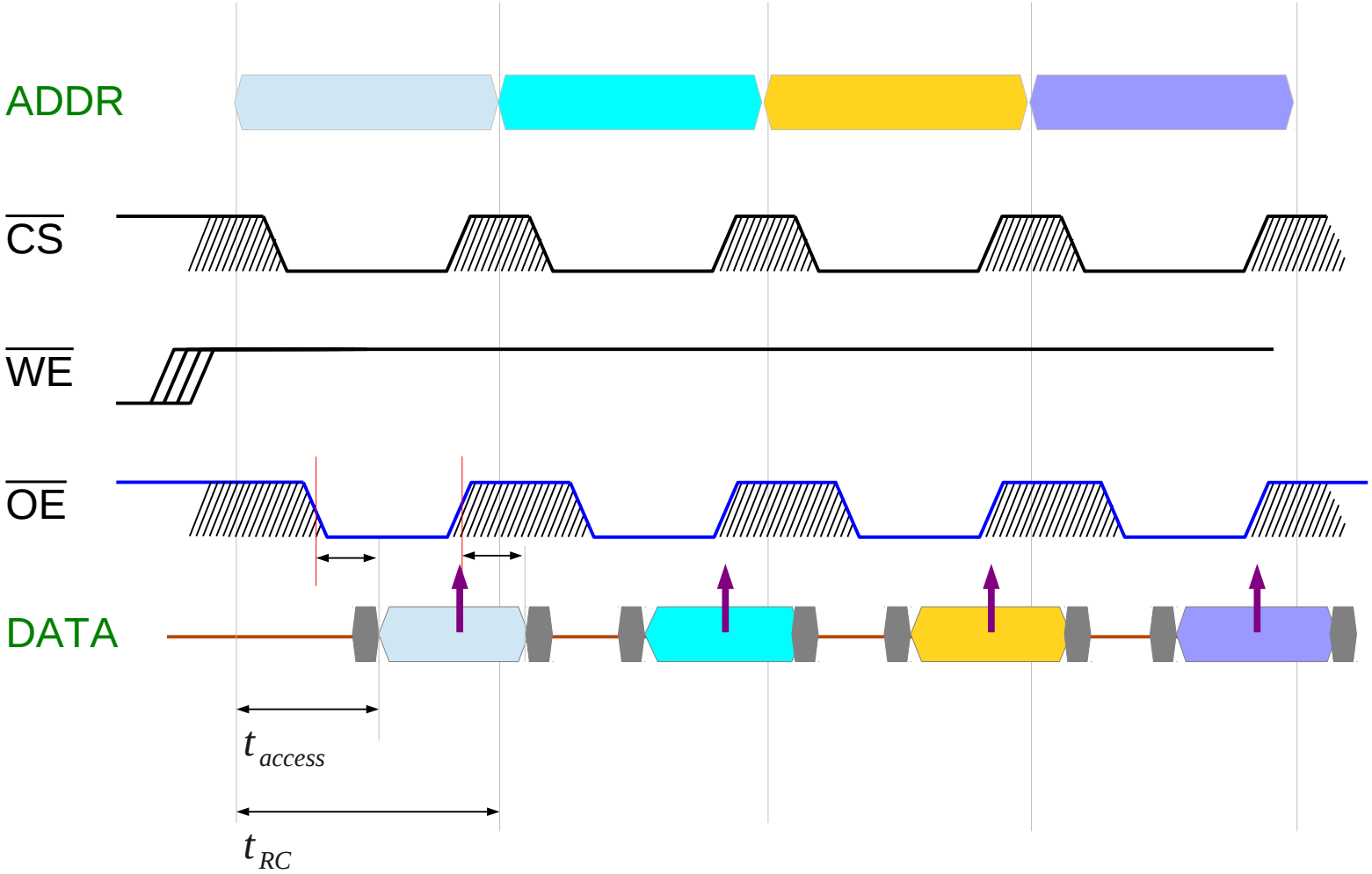


Asynchronous SRAM



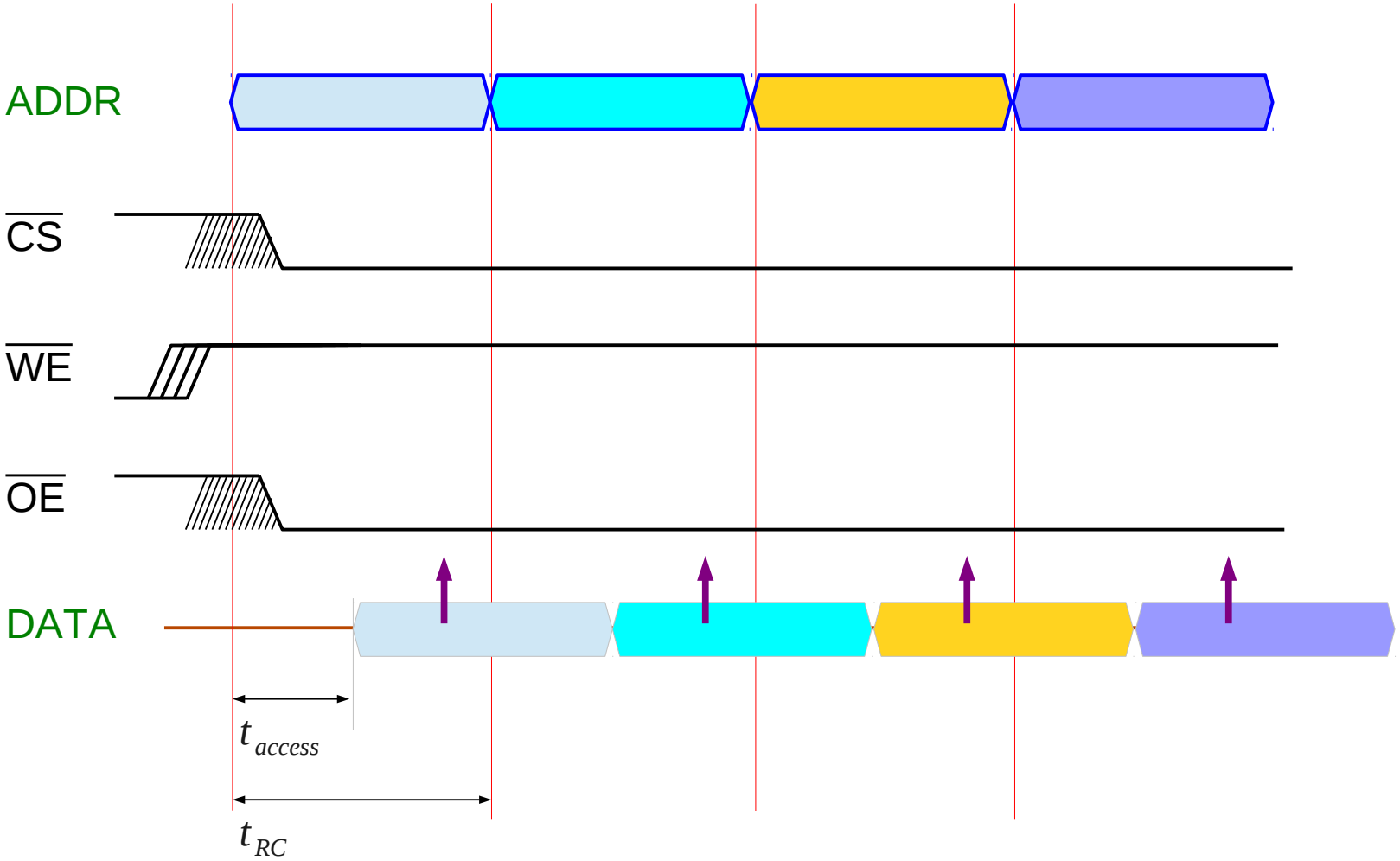
Asynchronous SRAM Read Cycle

$\overline{\text{OE}}$ Controlled



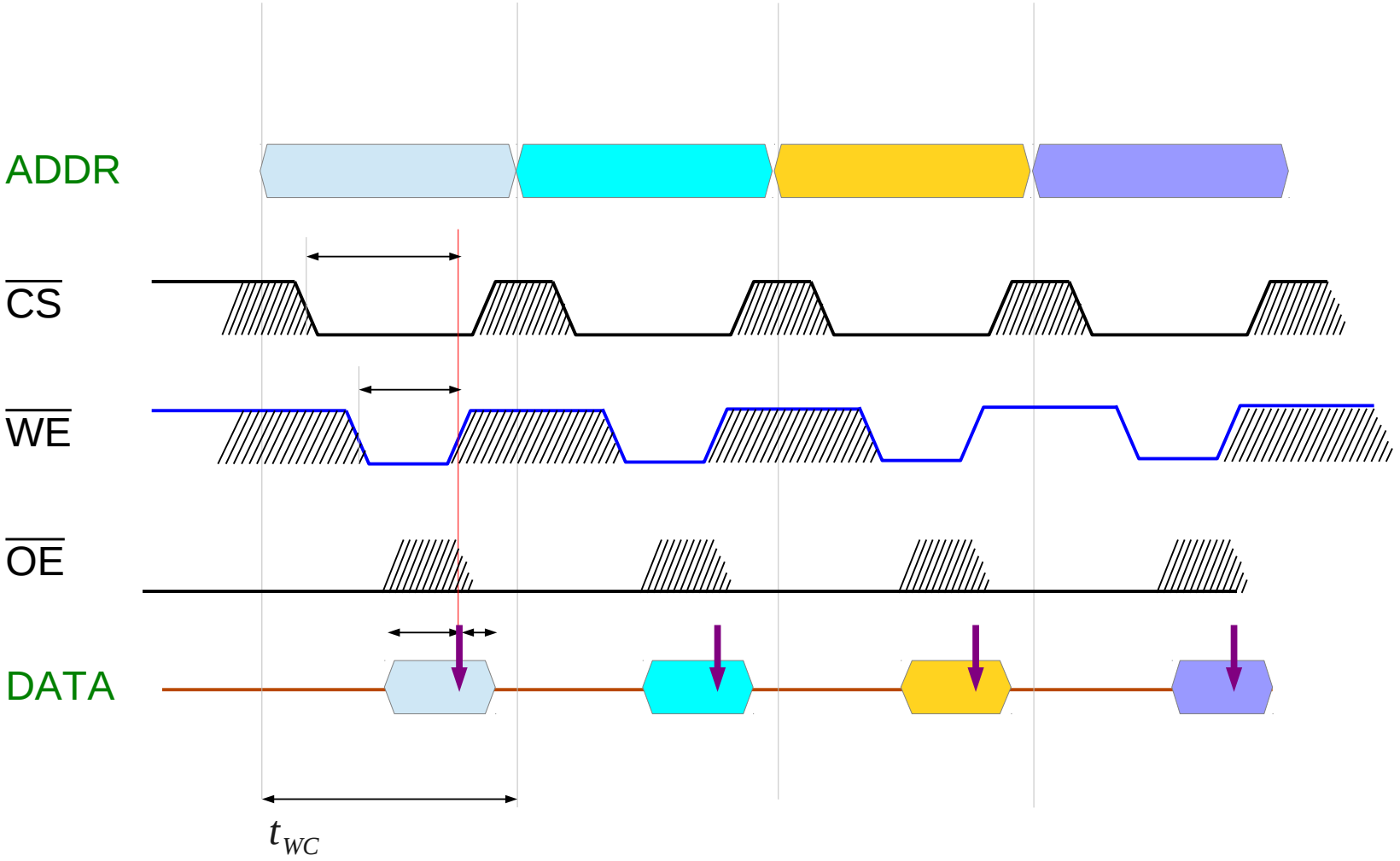
Asynchronous SRAM Read Cycle

Address Transition Controlled



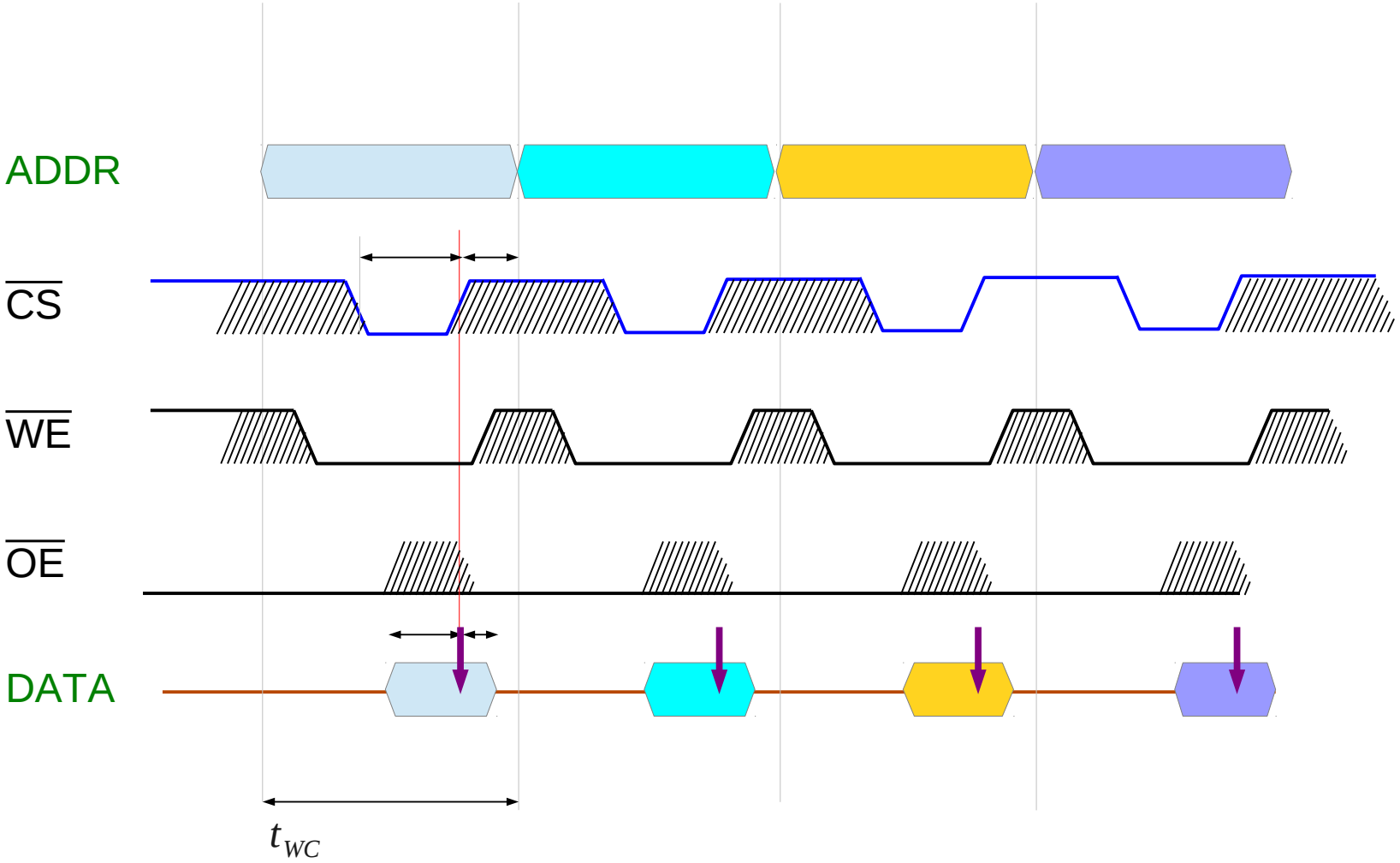
Asynchronous SRAM Write Cycle

$\overline{WE}$ Controlled

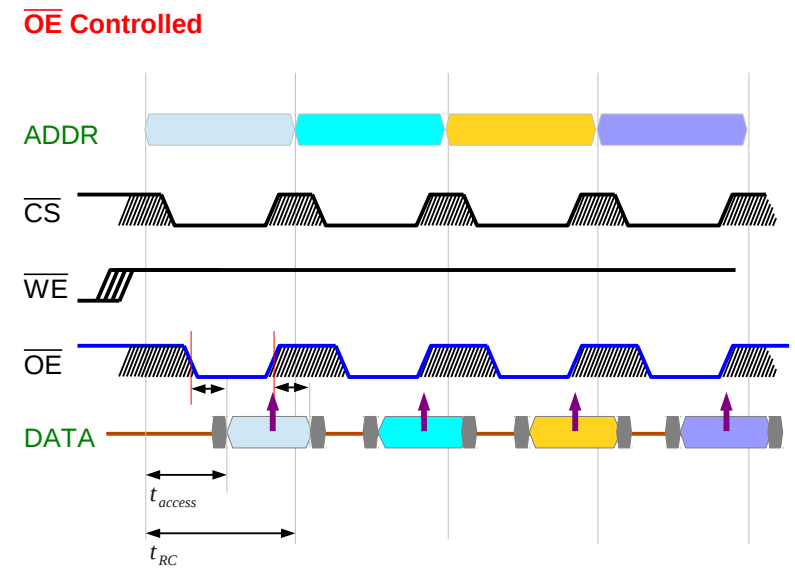


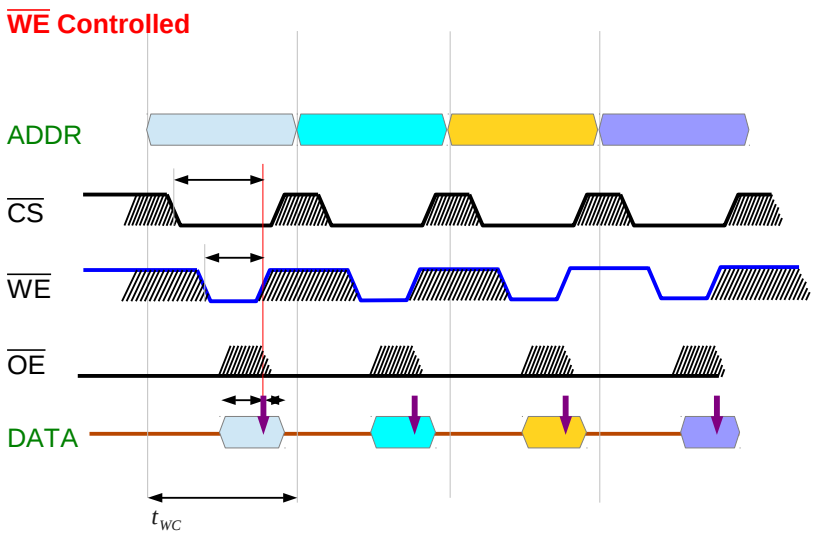
Asynchronous SRAM Write Cycle

$\overline{CS}$ Controlled

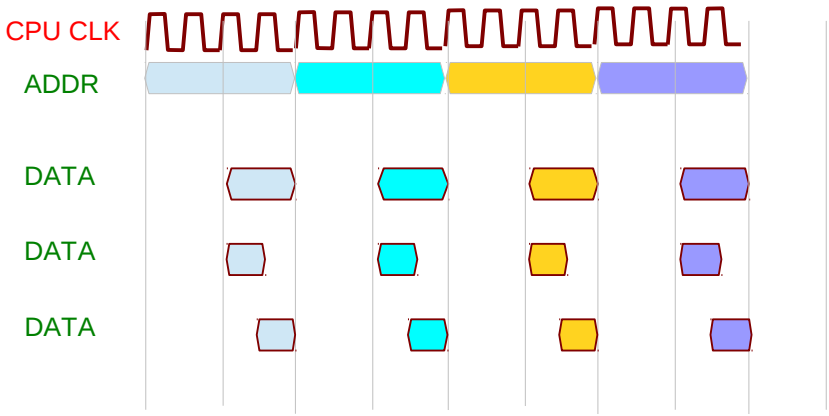


Asynchronous SRAM Cycle

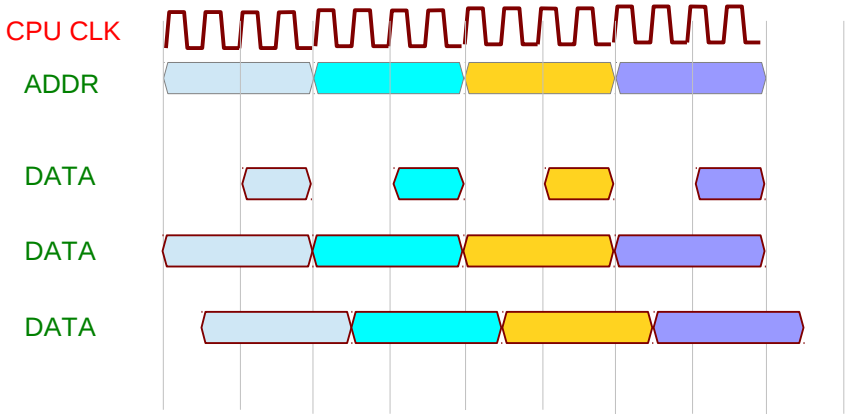




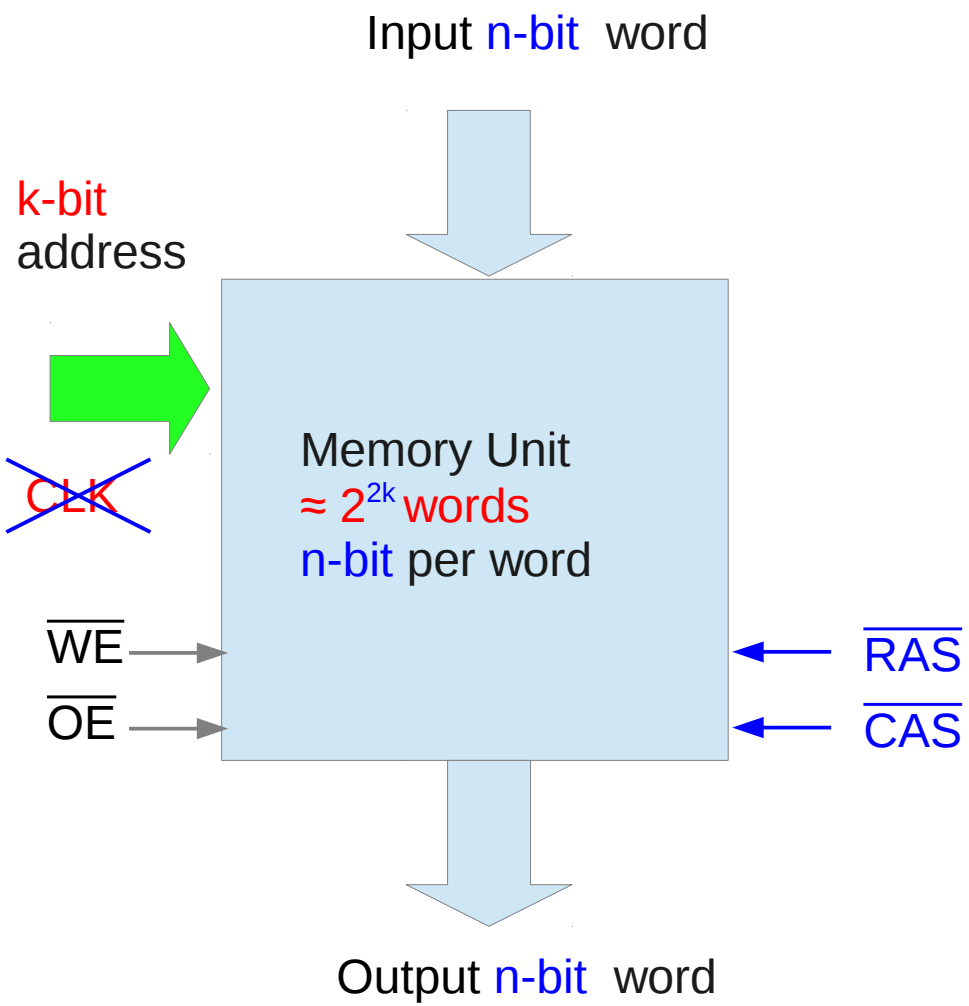
Async SRAM RD Cycle



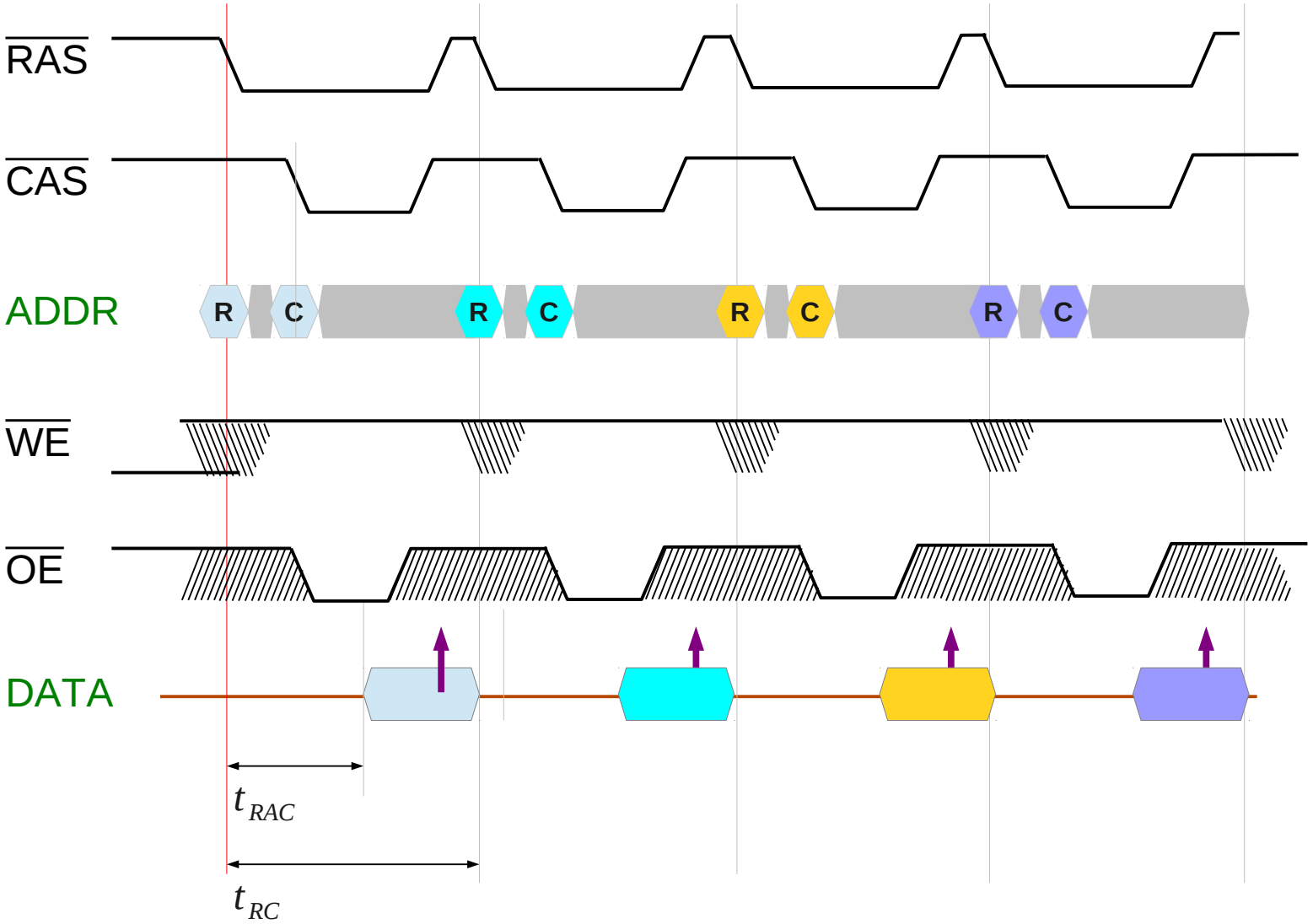
Async SRAM WR Cycle



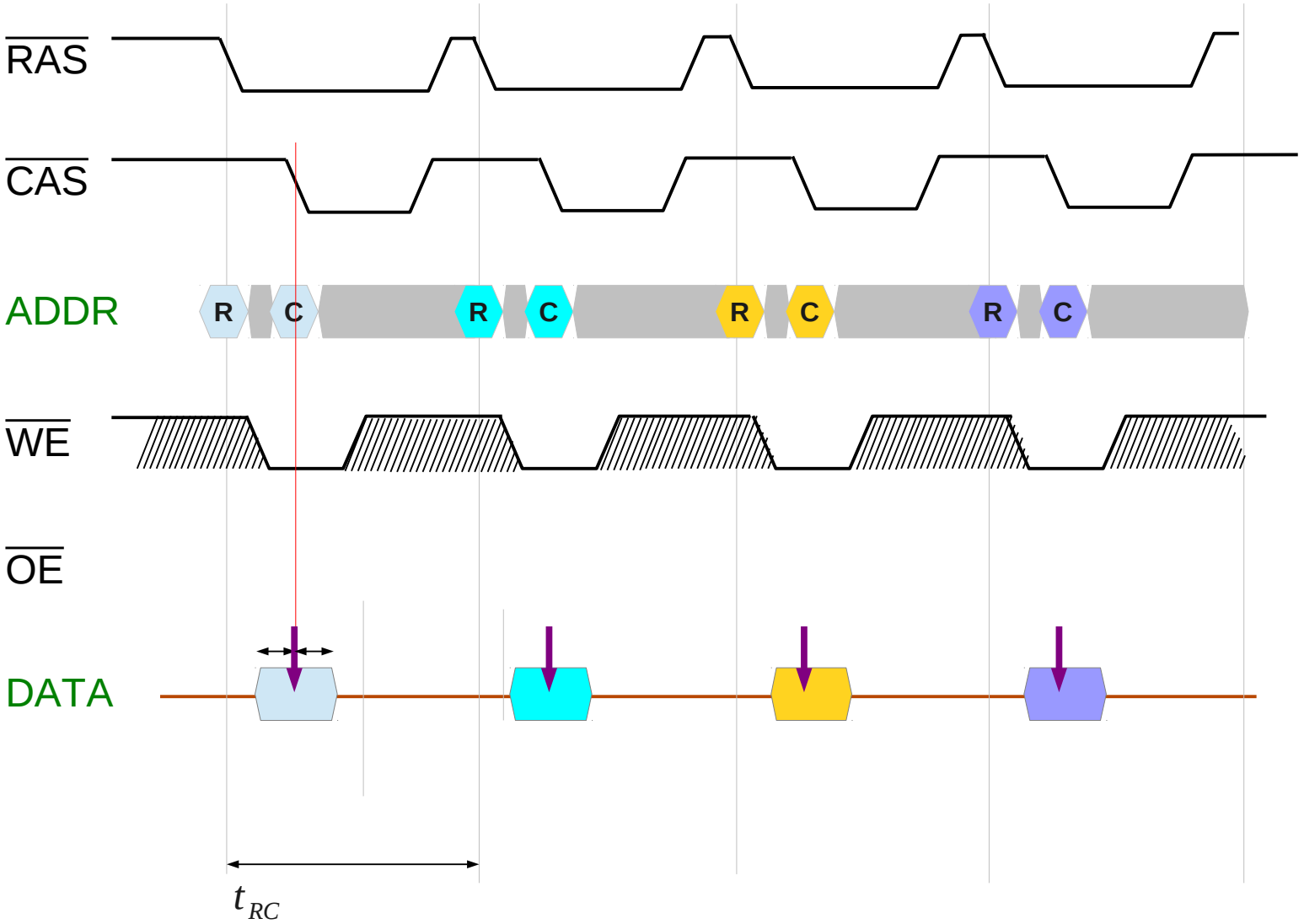
DRAM


Input n-bit word
k-bit
address
CLK
Memory Unit
≈ 2^2k words
n-bit per word
WE
OE
RAS
CAS
Output n-bit word

DRAM Read Cycle



DRAM Write Cycle



References

[1] http://en.wikipedia.org/
[2] M. M. Mano, C. R. Kime, “Logic and Computer Design Fundamentals”, 4th ed.
[3] D.M. Harris, S. L. Harris, “Digital Design and Computer Architecture”