The Necessities in SOC Design

1. Fabrication

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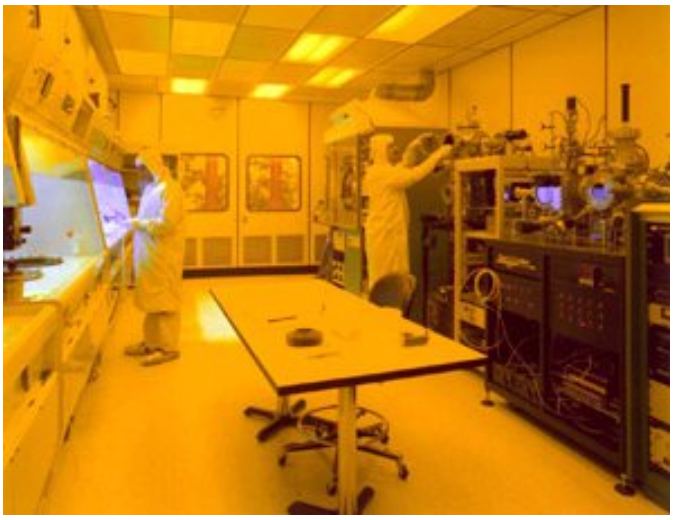
Semiconductor device fabrication

Semiconductor device fabrication is the process used to create the integrated circuits that are present in everyday electrical and electronic devices. It is a multiple-step sequence of photolithographic and chemical processing steps during which electronic circuits are gradually created on a wafer made of pure semiconducting material. Silicon is almost always used, but various compound semiconductors are used for specialized applications.

The entire manufacturing process, from start to packaged chips ready for shipment, takes six to eight weeks and is performed in highly specialized facilities referred to as fabs.

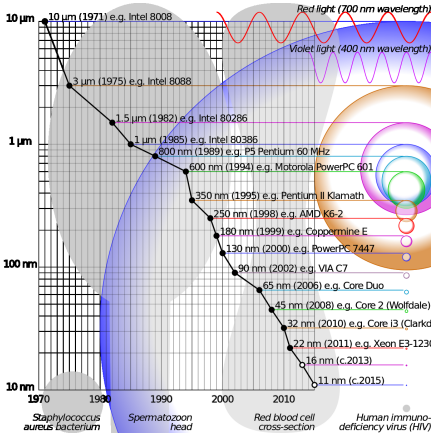


NASA's Glenn Research Center cleanroom.

History

When feature widths were far greater than about 10 micrometres, purity was not the issue that it is today in device manufacturing. As devices became more integrated, cleanrooms became even cleaner. Today, the fabs are pressurized with filtered air to remove even the smallest particles, which could come to rest on the wafers and contribute to defects. The workers in a semiconductor fabrication facility are required to wear cleanroom suits to protect the devices from human contamination.

Semiconductor device manufacturing has spread from Texas and California in the 1960s to the rest of the world, such as Europe, Middle East, and Asia. It is a global business today. The leading semiconductor manufacturers typically have facilities all over the world. Intel, the world's largest manufacturer, has facilities in Europe and Asia as well as the U.S. Other top manufacturers include Taiwan Semiconductor Manufacturing Company (Taiwan), STMicroelectronics (Europe), Analog Devices (US), Integrated Device Technology (US), Atmel (US/Europe), Freescale Semiconductor (US), Samsung (Korea), Texas Instruments (US), IBM (US), GlobalFoundries (Germany, Singapore, future New York fab in construction), Toshiba (Japan), NEC Electronics (Japan), Infineon (Europe, US, Asia), Renesas (Japan), Fujitsu (Japan/US), NXP Semiconductors (Europe and US), Micron Technology (US), Hynix (Korea), and SMIC (China).



Progress of miniaturisation, and comparison of sizes of semiconductor manufacturing process nodes with some microscopic objects and visible light wavelengths.

Wafers

A typical wafer is made out of extremely pure silicon that is grown into mono-crystalline cylindrical ingots (boules) up to 300 mm (slightly less than 12 inches) in diameter using the Czochralski process. These ingots are then sliced into wafers about 0.75 mm thick and polished to obtain a very regular and flat surface.

Once the wafers are prepared, many process steps are necessary to produce the desired semiconductor integrated circuit. In general, the steps can be grouped into two major parts:

- Front-end-of-line (FEOL) processing
- Back-end-of-line (BEOL) processing

Processing

In semiconductor device fabrication, the various processing steps fall into four general categories: deposition, removal, patterning, and modification of electrical properties.

- **Deposition** is any process that grows, coats, or otherwise transfers a material onto the wafer. Available technologies consist of physical vapor deposition (PVD), chemical vapor deposition (CVD), electrochemical deposition (ECD), molecular beam epitaxy (MBE) and more recently, atomic layer deposition (ALD) among others.
- **Removal processes** are any that remove material from the wafer either in bulk or selectively and consist primarily of etch processes, either wet etching or dry etching. Chemical-mechanical planarization (CMP) is also a removal process used between levels.
- **Patterning** covers the series of processes that shape or alter the existing shape of the deposited materials and is generally referred to as lithography. For example, in conventional lithography, the wafer is coated with a chemical called a *photoresist*. The photoresist is exposed by a *stepper*, a machine that focuses, aligns, and moves the mask, exposing select portions of the wafer to short wavelength light. The exposed regions are washed away by a developer solution. After etching or other processing, the remaining photoresist is removed by plasma ashing.
- **Modification of electrical properties** has historically consisted of doping transistor sources and drains originally by diffusion furnaces and later by ion implantation. These doping processes are followed by furnace anneal or in advanced devices, by rapid thermal anneal (RTA) which serve to activate the implanted dopants. Modification of electrical properties now also extends to reduction of dielectric constant in low-k insulating materials via exposure to ultraviolet light in UV processing (UVP).

Modern chips have up to eleven metal levels produced in over 300 sequenced processing steps.

Front-end-of-line (FEOL) processing

FEOL processing refers to the formation of the transistors directly in the silicon. The raw wafer is engineered by the growth of an ultrapure, virtually defect-free silicon layer through epitaxy. In the most advanced logic devices, *prior* to the silicon epitaxy step, tricks are performed to improve the performance of the transistors to be built. One method involves introducing a *straining step* wherein a silicon variant such as silicon-germanium (SiGe) is deposited. Once the epitaxial silicon is deposited, the crystal lattice becomes stretched somewhat, resulting in improved electronic mobility. Another method, called *silicon on insulator* technology involves the insertion of an insulating layer between the raw silicon wafer and the thin layer of subsequent silicon epitaxy. This method results in the creation of transistors with reduced parasitic effects.

Gate oxide and implants

Front-end surface engineering is followed by: growth of the gate dielectric, traditionally silicon dioxide (SiO_2), patterning of the gate, patterning of the source and drain regions, and subsequent implantation or diffusion of dopants to obtain the desired complementary electrical properties. In dynamic random access memory (DRAM) devices, storage capacitors are also fabricated at this time, typically stacked above the access transistor (implementing them as trenches etched deep into the silicon surface was a technique developed by the now defunct DRAM manufacturer Qimonda).

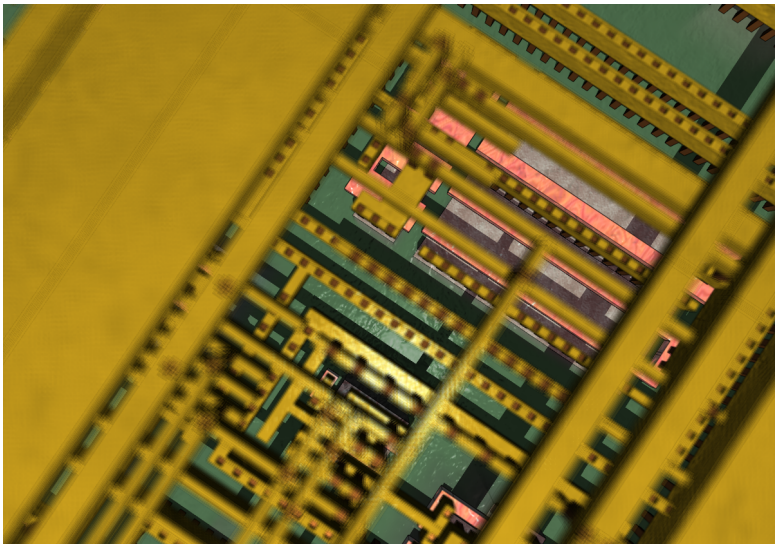
Back-end-of-line (BEOL) processing

Metal layers

Once the various semiconductor devices have been created, they must be interconnected to form the desired electrical circuits. This occurs in a series of wafer processing steps collectively referred to as BEOL (not to be confused with *back end* of chip fabrication which refers to the packaging and testing stages). BEOL processing involves creating metal interconnecting wires that are isolated by dielectric layers. The insulating material was traditionally a form of SiO_2 or a silicate glass, but recently new low dielectric constant materials are being used. These dielectrics presently take the form of SiOC (silicon oxycarbide) and have dielectric constants around 2.7 (compared to 3.9 for SiO_2), although materials with constants as low as 2.2 are being offered to chipmakers.

Interconnect

Historically, the metal wires consisted of aluminium. In this approach to wiring often called *subtractive aluminium*, blanket films of aluminium are deposited first, patterned, and then etched, leaving isolated wires. Dielectric material is then deposited over the exposed wires. The various metal layers are interconnected by etching holes, called *vias*, in the insulating material and depositing tungsten in them with a CVD technique. This approach is still used in the fabrication of many memory chips such as dynamic random access memory (DRAM) as the number of interconnect levels is small, currently no more than four.



Synthetic detail of a standard cell through four layers of planarized copper interconnect, down to the polysilicon (pink), wells (greyish) and substrate (green).

More recently, as the number of interconnect levels for logic has substantially increased due to the large number of transistors that are now interconnected in a modern microprocessor, the timing delay in the wiring has become significant prompting a change in wiring material from aluminium to copper and from the silicon dioxides to newer low-K material. This performance enhancement also comes at a *reduced cost* via damascene processing that eliminates processing steps. As the number of interconnect levels increases, planarization of the previous layers is required to ensure a flat surface prior to subsequent lithography. Without it, the levels would become increasingly crooked and extend outside the depth of focus of available lithography, interfering with the ability to pattern. CMP (chemical-mechanical planarization) is the primary processing method to achieve such planarization although dry

etch back is still sometimes employed if the number of interconnect levels is no more than three.

Wafer test

The highly serialized nature of wafer processing has increased the demand for metrology in between the various processing steps. Wafer test metrology equipment is used to verify that the wafers haven't been damaged by previous processing steps up until testing. If the number of dies—the integrated circuits that will eventually become chips—etched on a wafer exceeds a failure threshold (i.e. too many failed dies on one wafer), the wafer is scrapped rather than investing in further processing.

Device test

Once the front-end process has been completed, the semiconductor devices are subjected to a variety of electrical tests to determine if they function properly. The proportion of devices on the wafer found to perform properly is referred to as the yield.

The fab tests the chips on the wafer with an electronic tester that presses tiny probes against the chip. The machine marks each bad chip with a drop of dye. Currently, electronic dye marking is possible if wafer test data is logged into a central computer database and chips are "binned" (i.e. sorted into virtual bins) according to predetermined test limits. The resulting binning data can be graphed, or logged, on a wafer map to trace manufacturing defects and mark bad chips. This map can be also used during wafer assembly and packaging.

Chips are also tested again after packaging, as the bond wires may be missing, or analog performance may be altered by the package. This is referred to as "final test".

Usually, the fab charges for test time, with prices in the order of cents per second. Test times vary from a few milliseconds to a couple of seconds, and the test software is optimized for reduced test time. Multiple chip (multi-site) testing is also possible, since many testers have the resources to perform most or all of the tests in parallel.

Chips are often designed with "testability features" such as scan chains and "built-in self-test" to speed testing, and reduce test costs. In certain designs that use specialized analog fab processes, wafers are also laser-trimmed during test, to achieve tightly-distributed resistance values as specified by the design.

Good designs try to test and statistically manage *corners*: extremes of silicon behavior caused by operating temperature combined with the extremes of fab processing steps. Most designs cope with more than 64 corners.

Die preparation

Once tested, a wafer is typically reduced in thickness

before the wafer is scored and then broken into individual die -- wafer dicing.

Only the good, unmarked chips go on to be packaged.

Packaging

Plastic or ceramic packaging involves mounting the die, connecting the die pads to the pins on the package, and sealing the die. Tiny wires are used to connect pads to the pins. In the old days, wires were attached by hand, but now purpose-built machines perform the task. Traditionally, the wires to the chips were gold, leading to a "lead frame" (pronounced "leed frame") of copper, that had been plated with solder, a mixture of tin and lead. Lead is poisonous, so lead-free "lead frames" are now mandated by ROHS.

Chip-scale package (CSP) is another packaging technology. A plastic dual in-line package, like most packages, is many times larger than the actual die hidden inside, whereas CSP chips are nearly the size of the die. CSP can be constructed for each die *before* the wafer is diced.[1]

The packaged chips are retested to ensure that they were not damaged during packaging and that the die-to-pin interconnect operation was performed correctly. A laser etches the chip's name and numbers on the package.

List of steps

This is a list of processing techniques that are employed numerous times in a modern electronic device and do not necessarily imply a specific order.

- Wafer processing
  - Wet cleans
  - Photolithography
  - Ion implantation (in which dopants are embedded in the wafer creating regions of increased (or decreased) conductivity)
  - Dry etching
  - Wet etching
  - Plasma ashing
  - Thermal treatments
    - Rapid thermal anneal
    - Furnace anneals
    - Thermal oxidation
  - Chemical vapor deposition (CVD)
  - Physical vapor deposition (PVD)
  - Molecular beam epitaxy (MBE)
  - Electrochemical deposition (ECD). See Electroplating
  - Chemical-mechanical planarization (CMP)
  - Wafer testing (where the electrical performance is verified)
  - Wafer backgrinding (to reduce the thickness of the wafer so the resulting chip can be put into a thin device like a smartcard or PCMCIA card.)
- Die preparation
  - Wafer mounting
  - Die cutting
- IC packaging
  - Die attachment
  - IC bonding
    - Wire bonding
    - Thermosonic bonding
    - Flip chip
    - Wafer bonding
    - Tab bonding
  - IC encapsulation
    - Baking
    - Plating
    - Lasermarking
    - Trim and form
- IC testing

Hazardous materials

Many toxic materials are used in the fabrication process.[2] These include:

- poisonous elemental dopants such as arsenic, antimony and phosphorus
- poisonous compounds like arsine, phosphine and silane
- highly reactive liquids, such as hydrogen peroxide, fuming nitric acid, sulfuric acid and hydrofluoric acid

It is vital that workers not be directly exposed to these dangerous substances. The high degree of automation common in the IC fabrication industry helps to reduce the risks of exposure of this sort. Most fabrication facilities employ exhaust management systems, such as wet scrubbers, combustors, heated absorber cartridges etc., to control the risk to workers and also the environment if these toxic materials are released into the atmosphere.

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Further reading

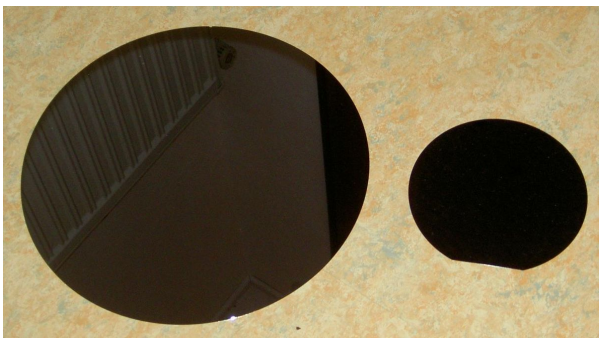
- Kaeslin, Hubert (2008), *Digital Integrated Circuit Design, from VLSI Architectures to CMOS Fabrication*, Cambridge University Press, section 14.2.

External links

- Semiconductor glossary (http://www.semiconductorglossary.com)

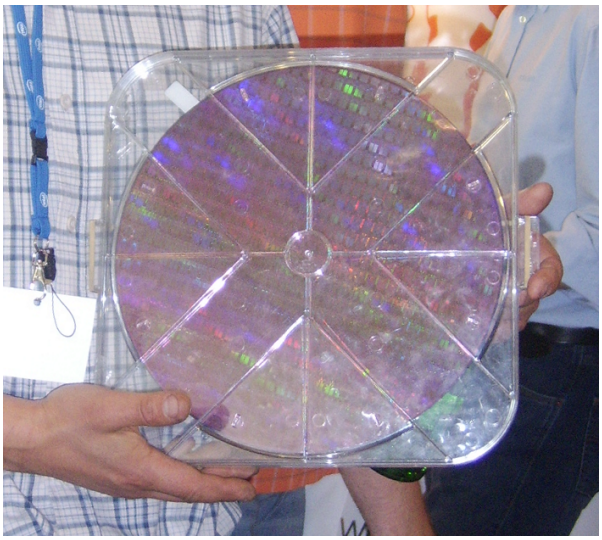
Wafer (electronics)

In electronics, a **wafer** (also called a **slice** or **substrate**[1]) is a thin slice of semiconductor material, such as a silicon crystal, used in the fabrication of integrated circuits and other microdevices. The wafer serves as the substrate for microelectronic devices built in and over the wafer and undergoes many microfabrication process steps such as doping or ion implantation, etching, deposition of various materials, and photolithographic patterning. Finally the individual microcircuits are separated (dicing) and packaged.



Polished 12" and 6" silicon wafers. The flat cut into the right wafer indicates its doping and crystallographic orientation (see below)

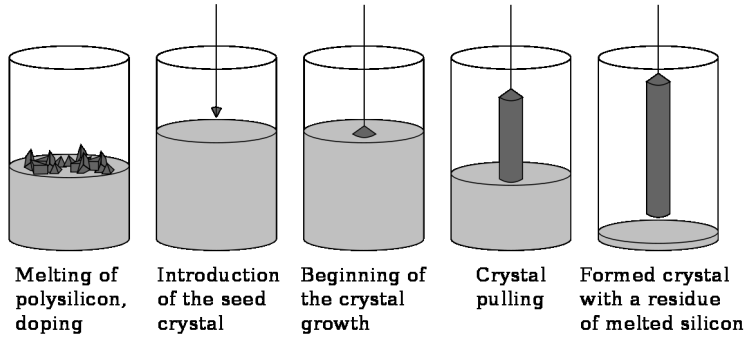
Several types of solar cell are also made from such wafers. On a *solar wafer* a solar cell (usually square) is made from the entire wafer.



VLSI microcircuits fabricated on a 12-inch (300 mm) silicon wafer, before dicing and packaging

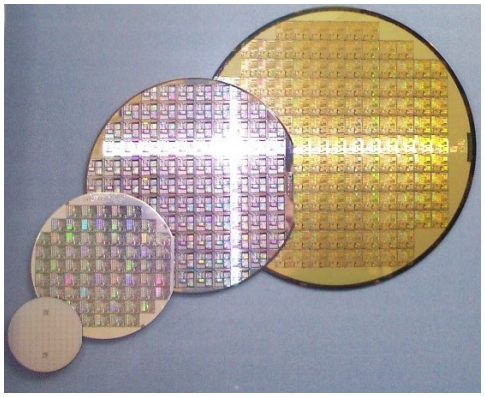
Formation

Wafers are formed of highly pure (99.9999999% purity),[2] nearly defect-free single crystalline material.[3] One process for forming crystalline wafers is known as Czochralski growth invented by the Polish chemist Jan Czochralski. In this process, a cylindrical ingot of high purity monocrystalline semiconductor, such as silicon or germanium, is formed by pulling a seed crystal from a 'melt'.[4][5] Donor impurity atoms, such as boron or phosphorus in the case of silicon, can be added to the molten intrinsic material in precise amounts in order to dope the crystal, thus changing it into n-type or p-type extrinsic semiconductor.



The Czochralski process.

The ingot is then sliced with a wafer saw (wire saw) and polished to form wafers.[6] The size of wafers for photovoltaics is 100–200 mm square and the thickness is 200–300 μm. In the future, 160 μm will be the standard.[7] Electronics use wafer sizes from 100–300 mm diameter. (The largest wafer made has a diameter of 450 mm but is not yet in production.)



2-inch (51 mm), 4-inch (100 mm), 6-inch (150 mm), and 8-inch (200 mm) wafers

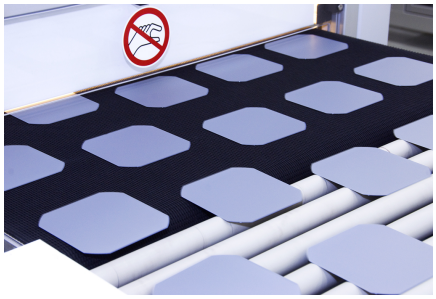
Cleaning, texturing and etching

Wafers are cleaned with weak acids to remove unwanted particles, or repair damage caused during the sawing process. When used for solar cells, the wafers are textured to create a rough surface to increase their efficiency. The generated PSG (phosphosilicate glass) is removed from the edge of the wafer in the etching.[8]

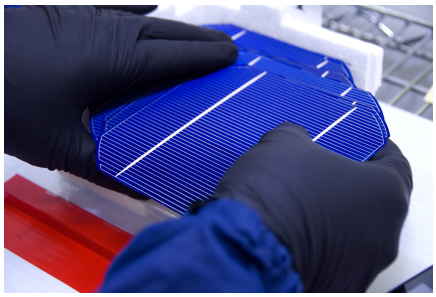
Wafer properties

Standard wafer sizes

Silicon wafers are available in a variety of diameters from 25.4 mm (1 inch) to 300 mm (11.8 inches).[9] Semiconductor fabrication plants (also known as *fabs*) are defined by the diameter of wafers that they are tooled to produce. The diameter has gradually increased to improve throughput and reduce cost with the current state-of-the-art fab considered to be 300 mm (12 inch), with the next standard projected to be 450 mm (18 inch).[10][11] Intel, TSMC and Samsung are separately conducting research to the advent of 450 mm "prototype" (research) fabs by 2012, though serious hurdles remain. Dean Freeman, an analyst with Gartner Inc., predicted that production fabs could emerge sometime between the 2017 and 2019 timeframe,[12] a lot of that will depend on a plethora of new technological breakthroughs and not simply extending current technology.



Solar wafers on the conveyor



Completed solar wafer

- 1-inch (25 mm)
- 2-inch (51 mm). Thickness 275 µm.
- 3-inch (76 mm). Thickness 375 µm.
- 4-inch (100 mm). Thickness 525 µm.
- 5-inch (130 mm) or 125 mm (4.9 inch). Thickness 625 µm.
- 150 mm (5.9 inch, usually referred to as "6 inch"). Thickness 675 µm.
- 200 mm (7.9 inch, usually referred to as "8 inch"). Thickness 725 µm.
- 300 mm (11.8 inch, usually referred to as "12 inch"). Thickness 775 µm.
- 450 mm (17.7 inch, usually referred to as "18 inch"). Thickness 925 µm (expected).[13]

Wafers grown using materials other than silicon will have different thicknesses than a silicon wafer of the same diameter. Wafer thickness is determined by the mechanical strength of the material used; the wafer must be thick enough to support its own weight without cracking during handling.

A unit wafer fabrication step, such as an etch step or a lithography step, can be performed on more chips per wafer as roughly the square of the increase in wafer diameter, while the cost of the unit fabrication step goes up more slowly than the square of the wafer diameter. This is the cost basis for shifting to larger and larger wafer sizes. Conversion to 300 mm wafers from 200 mm wafers began in earnest in 2000, and reduced the price per die about 30-40%.[14] However, this was not without significant problems for the industry.

The next step to 450 mm should accomplish similar productivity gains as the previous size increase. However, machinery needed to handle and process larger wafers results in increased investment costs to build a single factory. There is considerable resistance to moving up to 450 mm by 2012 despite the obvious productivity enhancements, mainly because companies feel it would take too long to recoup their investment.[15] The difficult and costly 300 mm process only accounted for approximately 20% of worldwide capacity on a square inches basis by the end of 2005.[16] The step up to 300 mm required a major change from the past, with fully automated factories using

300 mm wafers versus barely automated factories for the 200 mm wafers. These major investments were undertaken in the economic downturn following the dot-com bubble, resulting in huge resistance to upgrading to 450 mm by the original timeframe.

Other initial technical problems in the ramp up to 300 mm included vibrational effects, gravitational bending (sag), and problems with flatness. Among the new problems in the ramp up to 450 mm are that the crystal ingots will be 3 times heavier (total weight a metric ton) and take 2-4 times longer to cool, and the process time will be double.[17] All told, the development of 450 mm wafers require significant engineering, time, and cost to overcome.

Analytical die count estimation

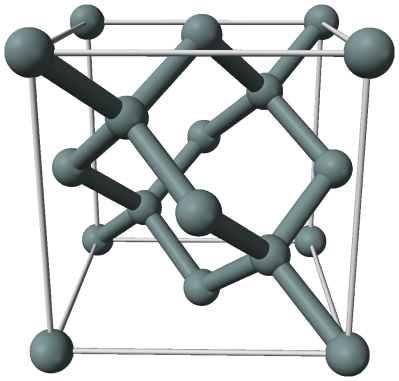
For any given wafer diameter [**d**, *mm*] and target IC size [**S**, mm^2], there is an exact number of integral die pieces that can be sliced out of the wafer. The gross Die Per Wafer [**DPW**] can be estimated by the following expression:

$$DPW = d\pi \left(\frac{d}{4S} - \frac{1}{\sqrt{2S}} \right)$$

Note, that the gross die count does not take into account the die defect loss, various alignment markings and test sites on the wafer.

Crystalline orientation

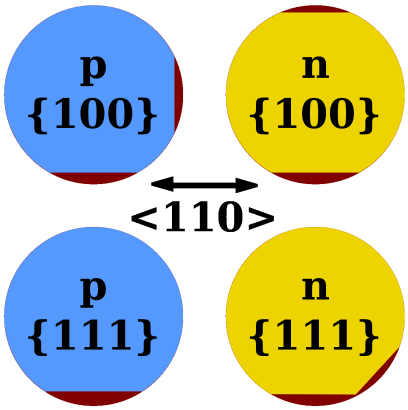
Wafers are grown from crystal having a regular crystal structure, with silicon having a diamond cubic structure with a lattice spacing of 5.430710 Å (0.5430710 nm).[18] When cut into wafers, the surface is aligned in one of several relative directions known as crystal orientations. Orientation is defined by the Miller index with [100] or [111] faces being the most common for silicon.[18] Orientation is important since many of a single crystal's structural and electronic properties are highly anisotropic. Ion implantation depths depend on the wafer's crystal orientation, since each direction offers distinct paths for transport.[19] Wafer cleavage typically occurs only in a few well-defined directions. Scoring the wafer along cleavage planes allows it to be easily diced into individual chips ("dies") so that the billions of individual circuit elements on an average wafer can be separated into many individual circuits.



Diamond Cubic Crystal Structure, Silicon unit cell

Wafer flats and crystallographic orientation notches

Wafers under 200 mm diameter have *flats* cut into one or more sides indicating the crystallographic planes of the wafer (usually the {110} face). In earlier-generation wafers a pair of flats at different angles additionally conveyed the doping type (see illustration for conventions). Wafers of 200 mm diameter and above use a single small notch to convey wafer orientation, with no visual indication of doping type.[20]



Flats can be used to denote doping and crystallographic orientation. Red represents material that has been removed.

Impurity doping

Silicon wafers are generally not 100% pure silicon, but are instead formed with an initial impurity doping concentration between 10^{13} and 10^{16} atoms per cm^3 of boron, phosphorus, arsenic, or antimony which is added to the melt and defines the wafer as either bulk n-type or p-type.[21] However, compared with single-crystal silicon's atomic density of 5×10^{22} atoms per cm^3, this still gives a purity greater than 99.9999%. The wafers can also be initially provided with some interstitial oxygen concentration. Carbon and metallic contamination are kept to a minimum.[22] Transition metals, in particular, must be kept below parts per billion concentrations for electronic applications.[23]

Compound semiconductors

While silicon is the prevalent material for wafers used in the electronics industry, other compound III-V or II-VI materials have also been employed. Gallium arsenide (GaAs), a III-V semiconductor produced via the Czochralski process, is also a common wafer material.[5]

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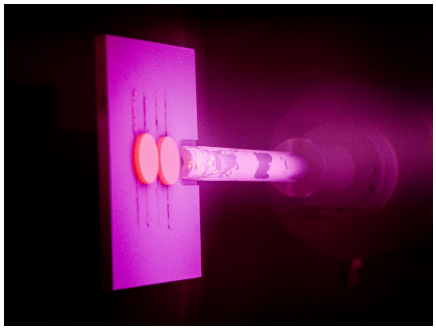
External links

- Everything Wafers (http://www.ee.byu.edu/cleanroom/everything_wafers.phtml) - A guide to semiconductor substrates type, property, cleaving, etching, and fabrication.

Physical vapor deposition

Physical vapor deposition (**PVD**) is a variety of vacuum deposition methods used to deposit thin films by the condensation of a vaporized form of the desired film material onto various workpiece surfaces (e.g., onto semiconductor wafers).



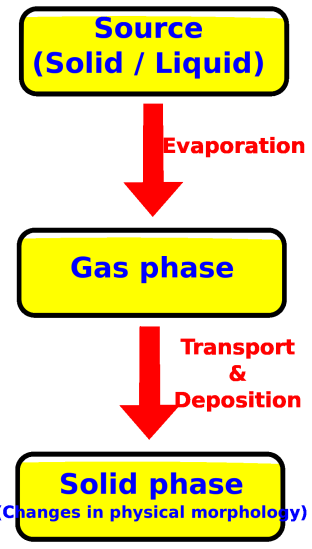
Inside the Plasma Spray-Physical Vapor Deposition, or PS-PVD, ceramic powder is introduced into the plasma flame, which vaporizes it and then condenses it on the (cooler) workpiece to form the ceramic coating.

The coating method involves purely physical processes such as high temperature vacuum evaporation with subsequent condensation, or plasma sputter bombardment rather than involving a chemical reaction at the surface to be coated as in chemical vapor deposition.

The term *physical vapor deposition* originally appeared in the 1966 book *Vapor Deposition* by C. F. Powell, J. H. Oxley and J. M. Blocher Jr., (but Michael Faraday was using PVD to deposit coatings as far back as 1838).

Variants of PVD include, in alphabetical order:

- Cathodic Arc Deposition: In which a high power electric arc discharged at the target (source) material blasts away some into highly ionized vapor to be deposited onto the workpiece.
- Electron beam physical vapor deposition: In which the material to be deposited is heated to a high vapor pressure by electron bombardment in "high" vacuum and is transported by diffusion to be deposited by condensation on the (cooler) workpiece.
- Evaporative deposition: In which the material to be deposited is heated to a high vapor pressure by electrically resistive heating in "low" vacuum.
- Pulsed laser deposition: In which a high power laser ablates material from the target into a vapor.
- Sputter deposition: In which a glow plasma discharge (usually localized around the "target" by a magnet) bombards the material sputtering some away as a vapor for subsequent deposition.



PVD: Process flow diagram

PVD is used in the manufacture of items, including semiconductor devices, aluminized PET film for balloons and snack bags, and coated cutting tools for metalworking. Besides PVD tools for fabrication special smaller tools mainly for scientific purposes have been developed. They mainly serve the purpose of extreme thin films like atomic layers and are used mostly for small substrates. A good example are mini e-beam evaporators which can deposit monolayers of virtually all materials with melting points up to 3500 °C.

The source material is unavoidably also deposited on most other surfaces interior to the vacuum chamber, including the workholders.

Some of the techniques used to measure the physical properties of PVD coatings are:

- Calo tester: coating thickness test
- Nanoindentation: hardness test for thin-film coatings
- Pin on disc tester: wear and friction coefficient test
- Scratch tester: coating adhesion test

Advantages:

• PVD coatings are sometimes harder and more corrosion resistant than coatings applied by the electroplating process. Most coatings have high temperature and good impact strength, excellent abrasion resistance and are so durable that protective topcoats are almost never necessary.

• Ability to utilize virtually any type of inorganic and some organic coating materials on an equally diverse group of substrates and surfaces using a wide variety of finishes.

• More environmentally friendly than traditional coating processes such as electroplating and painting.

• More than one technique can be used to deposit a given film.

Disadvantages:

• Specific technologies can impose constraints; for example, line-of-sight transfer makes coating annular shapes practically impossible.

• Some PVD technologies typically operate at very high temperatures and vacuums, requiring special attention by operating personnel.

• Requires a cooling water system to dissipate large heat loads.

Application: (Reference: Achal Singh SRM-CEL) As mentioned previously, PVD coatings are generally used to improve hardness, wear resistance and oxidation resistance. Thus, such coatings use in a wide range of applications such as: • Aerospace

• Automotive

• Surgical/Medical

• Dies and moulds for all manner of material processing

• Cutting tools

• Fire arms

See thin-film deposition for a more general discussion of this class of manufacturing technique.

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External links

- Society of Vacuum Coaters [1]
- PVD Animation [2]—an animation of a generic PVD sputter tool

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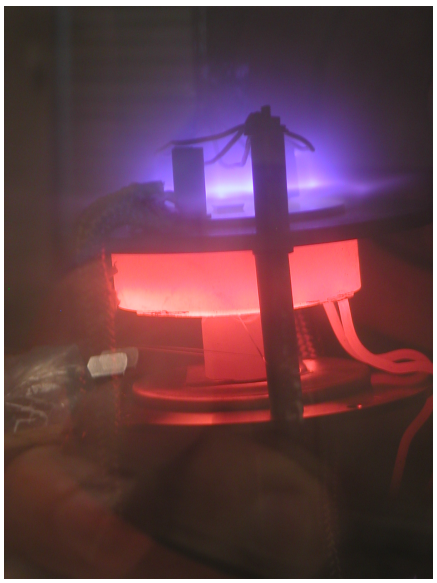
[1] http://www.svc.org/
[2] http://www.syngraphics.com/whatsnew_PVD.html

Chemical vapor deposition

Chemical vapor deposition (CVD) is a chemical process used to produce high-purity, high-performance solid materials. The process is often used in the semiconductor industry to produce thin films. In a typical CVD process, the wafer (substrate) is exposed to one or more volatile precursors, which react and/or decompose on the substrate surface to produce the desired deposit. Frequently, volatile by-products are also produced, which are removed by gas flow through the reaction chamber.

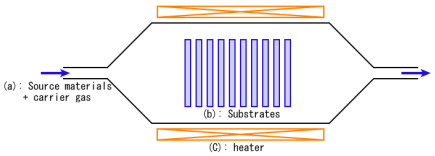
Microfabrication processes widely use CVD to deposit materials in various forms, including: monocrystalline, polycrystalline, amorphous, and epitaxial. These materials include: silicon, carbon fiber, carbon nanofibers, filaments, carbon nanotubes, SiO_2, silicon-germanium, tungsten, silicon carbide, silicon nitride, silicon oxynitride, titanium nitride, and various high-k dielectrics. The CVD process is also used to produce synthetic diamonds.



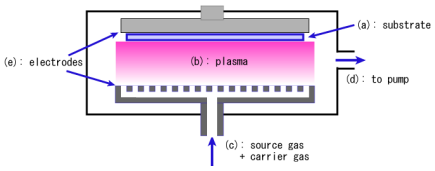
DC plasma (violet) enhances the growth of carbon nanotubes in laboratory-scale PECVD apparatus

Types

CVD is practiced in a variety of formats. These processes generally differ in the means by which chemical reactions are initiated.



Hot-wall thermal CVD (batch operation type)



Plasma assisted CVD

- Classified by operating pressure:
  - *Atmospheric pressure CVD* (APCVD) – CVD process at atmospheric pressure.
  - *Low-pressure CVD* (LPCVD) – CVD process at sub-atmospheric pressures.[1] Reduced pressures tend to reduce unwanted gas-phase reactions and improve film uniformity across the wafer.
  - *Ultrahigh vacuum CVD* (UHVCVD) – CVD process at very low pressure, typically below 10^{-6} Pa (~10^{-8} torr). Note that in other fields, a lower division between high and ultra-high vacuum is common, often 10^{-7} Pa.

Most modern CVD processes are either LPCVD or UHVCVD.

- Classified by physical characteristics of vapor:
  - *Aerosol assisted CVD* (AACVD) – A CVD process in which the precursors are transported to the substrate by means of a liquid/gas aerosol, which can be generated ultrasonically. This technique is suitable for use with non-volatile precursors.
  - *Direct liquid injection CVD* (DLICVD) – A CVD process in which the precursors are in liquid form (liquid or solid dissolved in a convenient solvent). Liquid solutions are injected in a vaporization chamber towards injectors (typically car injectors). The precursor vapors are then transported to the substrate as in classical CVD process. This technique is suitable for use on liquid or solid precursors. High growth rates can be reached using this technique.
- Plasma methods (see also Plasma processing):
  - *Microwave plasma-assisted CVD* (MPCVD)
  - *Plasma-Enhanced CVD* (PECVD) – CVD process that utilizes plasma to enhance chemical reaction rates of the precursors.[2] PECVD processing allows deposition at lower temperatures, which is often critical in the manufacture of semiconductors.
  - *Remote plasma-enhanced CVD* (RPECVD) – Similar to PECVD except that the wafer substrate is not directly in the plasma discharge region. Removing the wafer from the plasma region allows processing temperatures down to room temperature.
- *Atomic layer CVD* (ALCVD) – Deposits successive layers of different substances to produce layered, crystalline films. See Atomic layer epitaxy.
- *Combustion Chemical Vapor Deposition* (CCVD) – Combustion Chemical Vapor Deposition or flame pyrolysis is an open-atmosphere, flame-based technique for depositing high-quality thin films and nanomaterials.
- *Hot wire CVD* (HWCVD) – also known as catalytic CVD (Cat-CVD) or hot filament CVD (HFCVD), this process uses a hot filament to chemically decompose the source gases.[3]
- *Hybrid Physical-Chemical Vapor Deposition* (HPCVD) – This process involves both chemical decomposition of precursor gas and vaporization of a solid source.
- *Metalorganic chemical vapor deposition* (MOCVD) – This CVD process is based on metalorganic precursors.
- *Rapid thermal CVD* (RTCVD) – This CVD process uses heating lamps or other methods to rapidly heat the wafer substrate. Heating only the substrate rather than the gas or chamber walls helps reduce unwanted gas-phase reactions that can lead to particle formation.
- *Vapor phase epitaxy* (VPE)

Uses

CVD is commonly used to deposit conformal films. A variety of applications for such films exist. Gallium arsenide is used in some integrated circuits (ICs). Amorphous polysilicon is used in photovoltaic devices. Certain carbides and nitrides confer wear-resistance.[4]

Commerically important materials prepared by CVD

Polysilicon

Polycrystalline silicon is deposited from trichlorosilane ($SiHCl_3$) or silane (SiH_4), using the following reactions:[5]

$$SiHCl_3 \rightarrow Si + H_2 + HCl$$

$$SiH_4 \rightarrow Si + 2\ H_2$$

This reaction is usually performed in LPCVD systems, with either pure silane feedstock, or a solution of silane with 70–80% nitrogen. Temperatures between 600 and 650 °C and pressures between 25 and 150 Pa yield a growth rate between 10 and 20 nm per minute. An alternative process uses a hydrogen-based solution. The hydrogen reduces the growth rate, but the temperature is raised to 850 or even 1050 °C to compensate. Polysilicon may be grown directly with doping, if gases such as phosphine, arsine or diborane are added to the CVD chamber. Diborane increases the growth rate, but arsine and phosphine decrease it.

Silicon dioxide

Silicon dioxide (usually called simply "oxide" in the semiconductor industry) may be deposited by several different processes. Common source gases include silane and oxygen, dichlorosilane ($SiCl_2H_2$) and nitrous oxide[6] (N_2O), or tetraethylorthosilicate (TEOS; $Si(OC_2H_5)_4$). The reactions are as follows :

$$SiH_4 + O_2 \rightarrow SiO_2 + 2\ H_2$$

$$SiCl_2H_2 + 2\ N_2O \rightarrow SiO_2 + 2\ N_2 + 2\ HCl$$

$$Si(OC_2H_5)_4 \rightarrow SiO_2 + \text{byproducts}$$

The choice of source gas depends on the thermal stability of the substrate; for instance, aluminium is sensitive to high temperature. Silane deposits between 300 and 500 °C, dichlorosilane at around 900 °C, and TEOS between 650 and 750 °C, resulting in a layer of *low- temperature oxide* (LTO). However, silane produces a lower-quality oxide than the other methods (lower dielectric strength, for instance), and it deposits nonconformally. Any of these reactions may be used in LPCVD, but the silane reaction is also done in APCVD. CVD oxide invariably has lower quality than thermal oxide, but thermal oxidation can only be used in the earliest stages of IC manufacturing.

Oxide may also be grown with impurities (alloying or "doping"). This may have two purposes. During further process steps that occur at high temperature, the impurities may diffuse from the oxide into adjacent layers (most notably silicon) and dope them. Oxides containing 5–15% impurities by mass are often used for this purpose. In addition, silicon dioxide alloyed with phosphorus pentoxide ("P-glass") can be used to smooth out uneven surfaces. P-glass softens and reflows at temperatures above 1000 °C. This process requires a phosphorus concentration of at least 6%, but concentrations above 8% can corrode aluminium. Phosphorus is deposited from phosphine gas and oxygen:

$$4\ PH_3 + 5\ O_2 \rightarrow 2\ P_2O_5 + 6\ H_2$$

Glasses containing both boron and phosphorus (borophosphosilicate glass, BPSG) undergo viscous flow at lower temperatures; around 850 °C is achievable with glasses containing around 5 weight % of both constituents, but stability in air can be difficult to achieve. Phosphorus oxide in high concentrations interacts with ambient moisture to produce phosphoric acid. Crystals of BPO_4 can also precipitate from the flowing glass on cooling; these crystals are not readily etched in the standard reactive plasmas used to pattern oxides, and will result in circuit defects in

integrated circuit manufacturing.

Besides these intentional impurities, CVD oxide may contain byproducts of the deposition process. TEOS produces a relatively pure oxide, whereas silane introduces hydrogen impurities, and dichlorosilane introduces chlorine.

Lower temperature deposition of silicon dioxide and doped glasses from TEOS using ozone rather than oxygen has also been explored (350 to 500 °C). Ozone glasses have excellent conformality but tend to be hygroscopic – that is, they absorb water from the air due to the incorporation of silanol (Si-OH) in the glass. Infrared spectroscopy and mechanical strain as a function of temperature are valuable diagnostic tools for diagnosing such problems.

Silicon nitride

Silicon nitride is often used as an insulator and chemical barrier in manufacturing ICs. The following two reactions deposit silicon nitride from the gas phase:

$$3\ SiH_4 + 4\ NH_3 \rightarrow Si_3N_4 + 12\ H_2$$

$$3\ SiCl_2H_2 + 4\ NH_3 \rightarrow Si_3N_4 + 6\ HCl + 6\ H_2$$

Silicon nitride deposited by LPCVD contains up to 8% hydrogen. It also experiences strong tensile stress, which may crack films thicker than 200 nm. However, it has higher resistivity and dielectric strength than most insulators commonly available in microfabrication (10^{16} Ω·cm and 10 MV/cm, respectively).

Another two reactions may be used in plasma to deposit SiNH:

$$2\ SiH_4 + N_2 \rightarrow 2\ SiNH + 3\ H_2$$

$$SiH_4 + NH_3 \rightarrow SiNH + 3\ H_2$$

These films have much less tensile stress, but worse electrical properties (resistivity 10^6 to 10^{15} Ω·cm, and dielectric strength 1 to 5 MV/cm).[7]

Metals

CVD processes for tungsten is achieved from tungsten hexafluoride (WF_6), which may be deposited in two ways:

$$WF_6 \rightarrow W + 3\ F_2$$

$$WF_6 + 3\ H_2 \rightarrow W + 6\ HF$$

Other metals, notably aluminium and copper, can be deposited by CVD. As of 2010, a commercially cost effective CVD process for copper did not exist, although volatile sources exist, such as $Cu(hfac)_2$. Copper is typically deposited by electroplating. Aluminum can be deposited from triisobutylaluminium (TIBAL) and related organoaluminium compounds.

CVD processes for molybdenum, tantalum, titanium, nickel are widely used. These metals can form useful silicides when deposited onto silicon. Mo, Ta and Ti are deposited by LPCVD, from their pentachlorides. Nickel, molybdenum, and tungsten can be deposited at low temperatures from their carbonyl precursors. In general, for an arbitrary metal *M*, the reaction is as follows:

$$2\ MCl_5 + 5\ H_2 \rightarrow 2\ M + 10\ HCl$$

Niobium(V) oxide layers can be produced by the thermal decomposition of niobium(V) ethoxide with the loss of diethyl ether[8][9] according to the equation:

$$2\ Nb(OC_2H_5)_5 \rightarrow Nb_2O_5 + 5\ C_2H_5OC_2H_5$$

Diamond

Colorless gem cut from diamond grown by chemical vapor deposition

CVD can be used to produce a synthetic diamond by creating the circumstances necessary for carbon atoms in a gas to settle on a substrate in crystalline form.

CVD production of diamonds has received a great deal of attention in the materials sciences because it allows many new applications of diamonds that had previously been considered too difficult to make economical. CVD diamond growth typically occurs under low pressure (1–27 kPa; 0.145–3.926 psi; 7.5-203 Torr) and involves feeding varying amounts of gases into a chamber, energizing them and providing conditions for diamond growth on the substrate. The gases always include a carbon source, and typically include hydrogen as well, though the amounts used vary greatly depending on the type of diamond being grown. Energy sources include hot filament, microwave power, and arc discharges, among others. The energy source is intended to generate a plasma in which the gases are broken down and more complex chemistries occur. The actual chemical process for diamond growth is still under study and is complicated by the very wide variety of diamond growth processes used.

Using CVD, films of diamond can be grown over large areas of substrate with control over the properties of the diamond produced. In the past, when high pressure high temperature (HPHT) techniques were used to produce a diamond, the result was typically very small free standing diamonds of varying sizes. With CVD diamond growth areas of greater than fifteen centimeters (six inches) diameter have been achieved and much larger areas are likely to be successfully coated with diamond in the future. Improving this process is key to enabling several important applications.

The growth of diamond directly on a substrate allows the addition of many of diamond's important qualities to other materials. Since diamond has the highest thermal conductivity of any bulk material, layering diamond onto high heat producing electronics (such as optics and transistors) allows the diamond to be used as a heat sink.[10][11] Diamond films are being grown on valve rings, cutting tools, and other objects that benefit from diamond's hardness and exceedingly low wear rate. In each case the diamond growth must be carefully done to achieve the necessary adhesion onto the substrate. Diamond's very high scratch resistance and thermal conductivity, combined with a lower coefficient of thermal expansion than Pyrex glass, a coefficient of friction close to that of Teflon (Polytetrafluoroethylene) and strong lipophilicity would make it a nearly ideal non-stick coating for cookware if large substrate areas could be coated economically.

CVD growth allows one to control the properties of the diamond produced. In the area of diamond growth. The word "diamond" is used as a description of any material primarily made up of sp3 bonded carbon, and there are many different types of diamond included in this. By regulating the processing parameters—especially the gases introduced, but also including the pressure the system is operated under, the temperature of the diamond, and the method of generating plasma—many different materials that can be considered diamond can be made. Single crystal diamond can be made containing various dopants.[12] Polycrystalline diamond consisting of grain sizes from several nanometers to several micrometers can be grown.[10][13] Some polycrystalline diamond grains are surrounded by thin, non-diamond carbon, while others are not. These different factors affect the diamond's hardness, smoothness, conductivity, optical properties and more.

Chalcogenides

Commercially, mercury cadmium telluride is of continuing interest for detection of infrared radiation. Consisting of a alloy of CdTe and HgTe, this material can be prepared from the dimethyl derivatives of the respective elements.

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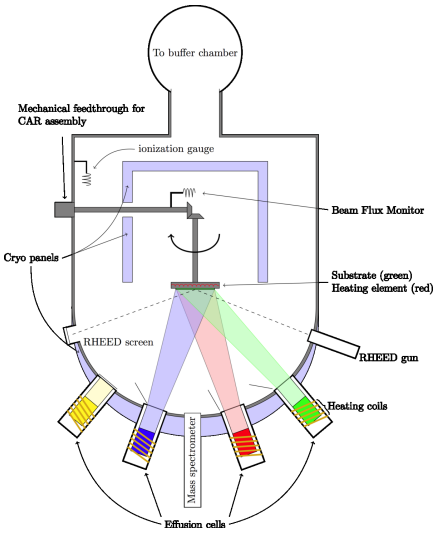
- T. Liu, D. Raabe and S. Zaefferer "A 3D tomographic EBSD analysis of a CVD diamond thin film" Sci. Technol. Adv. Mater. 9 (2008) 035013 (http://dx.doi.org/10.1088/1468-6996/9/3/035013) *free-download*
- Christoph Wild "CVD Diamond Properties and Useful Formula" CVD Diamond Booklet (2008) PDF (http://www.diamond-materials.com/downloads/cvd_diamond_booklet.pdf) *free-download*
- Dennis W. Hess, CHEMICAL VAPOR DEPOSITION OF DIELECTRIC AND METAL FILMS (http://www.dtic.mil/cgi-bin/GetTRDoc?AD=ADA204709#page=74)*free-download* from Electronic Materials and Processing: Proceedings of the First Electronic Materials and Processing Congress held in conjunction with the 1988 World Materials Congress Chicago, Illinois, USA, 24–30 September 1988, Edited by Prabjit Singh (Sponsored by the Electronic Materials and Processing Division of ASM INTERNATIONAL)

External links

- Fundamentals of Chemical Vapor Deposition (http://www.timedomaincvd.com/CVD_Fundamentals/Fundamentals_of_CVD.html), by TimeDomain CVD, Inc.
- Traditional Coating Technologies (http://www.ngimat.com/technology/ccvd.html)
- Chemical vapor deposition with atmospheric plasma (http://www.acxys.com/processes/coating)

Molecular beam epitaxy

Molecular beam epitaxy (MBE) is one of several methods of depositing single crystals. It was invented in the late 1960s at Bell Telephone Laboratories by J. R. Arthur and Alfred Y. Cho.[1] MBE is widely used in the manufacture of semiconductor devices, including transistors for cellular phones and WiFi. Recently, the world's most efficient solar cells have been demonstrated with MBE and are being commercialized.



A simple sketch showing the main components and rough layout and concept of the main chamber in a Molecular Beam Epitaxy system

Method

Molecular beam epitaxy takes place in high vacuum or ultra-high vacuum (10^{-8} Pa). The most important aspect of MBE is the deposition rate (typically less than 3000 nm per hour) allows the films to grow epitaxially. These deposition rates require proportionally better vacuum to achieve the same impurity levels as other deposition techniques. The absence of carrier gases as well as the ultra high vacuum environment result in the highest achievable purity of the grown films.

In solid-source MBE, elements such as gallium and arsenic, in ultra-pure form, are heated in separate quasi-Knudsen effusion cells until they begin to slowly sublime. The gaseous elements then condense on the wafer, where they may react with each other. In the example of gallium and arsenic, single-crystal gallium arsenide is formed. The term "beam" means that evaporated atoms do not interact with each other or vacuum chamber gases until they reach the wafer, due to the long mean free paths of the atoms.

During operation, reflection high energy electron diffraction (RHEED) is often used for monitoring the growth of the crystal layers. A computer controls shutters in front of each furnace, allowing precise control of the thickness of each layer, down to a single layer of atoms. Intricate structures of layers of different materials may be fabricated this way. Such control has allowed the development of structures where the electrons can be confined in space, giving quantum wells or even quantum dots. Such layers are now a critical part of many modern semiconductor devices, including semiconductor lasers and light-emitting diodes.

In systems where the substrate needs to be cooled, the ultra-high vacuum environment within the growth chamber is maintained by a system of cryopumps, and cryopanels, chilled using liquid nitrogen or cold nitrogen gas to a temperature close to 77 Kelvin (−196 degrees Celsius). Cryogenic temperatures act as a sink for impurities in the vacuum, so vacuum levels need to be several orders of magnitude better to deposit films under these conditions. In other systems, the wafers on which the crystals are grown may be mounted on a rotating platter which can be heated to several hundred degrees Celsius during operation.

Molecular beam epitaxy is also used for the deposition of some types of organic semiconductors. In this case, molecules, rather than atoms, are evaporated and deposited onto the wafer. Other variations include gas-source

MBE, which resembles chemical vapor deposition.

Lately molecular beam epitaxy has been used to deposit oxide materials for advanced electronic, magnetic and optical applications. For these purposes, MBE systems have to be modified to incorporate oxygen sources. [2]

ATG instability

The **ATG** (Asaro-Tiller-Grinfeld) instability, also known as the Grinfeld instability, is an elastic instability often encountered during molecular beam epitaxy. If there is a mismatch between the lattice sizes of the growing film and the supporting crystal, elastic energy will be accumulated in the growing film. At some critical height, the free energy of the film can be lowered if the film breaks into isolated islands, where the tension can be relaxed laterally. The critical height depends on Young's moduli, mismatch size, and surface tensions.

Some applications for this instability have been researched, such as the self-assembly of quantum dot. This community uses the name of Stranski–Krastanov growth for ATG.

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External links

- Silicon and germanium nanowires by molecular beam epitaxy (http://www.mpi-halle.mpg.de/department2/research-areas/nanowires-nanoobjects/si-ge-nanowhiskers-by-mbe/abstract/)
- University of Texas MBE group (Primer on MBE growth) (http://lase.mer.utexas.edu/mbe.php)
- Physics of Thin Films: Molecular Beam Epitaxy (class notes) (http://www.uccs.edu/~tchriste/courses/PHYS549/549lectures/mbe.html)

Atomic layer deposition

Atomic layer deposition (ALD) is a thin film deposition technique that is based on the sequential use of a gas phase chemical process. The majority of ALD reactions use two chemicals, typically called precursors. These precursors react with a surface one at a time in a sequential, self-limiting, manner. By exposing the precursors to the growth surface repeatedly, a thin film is deposited.[1]

Introduction

ALD is a self-limiting (the amount of film material deposited in each reaction cycle is constant), sequential surface chemistry that deposits conformal thin-films of materials onto substrates of varying compositions. Due to the characteristics of self-limiting and surface reactions, ALD film growth makes atomic scale deposition control possible. ALD is similar in chemistry to chemical vapor deposition (CVD), except that the ALD reaction breaks the CVD reaction into two half-reactions, keeping the precursor materials separate during the reaction. By keeping the precursors separate throughout the coating process, atomic layer control of film growth can be obtained as fine as ~0.1 Å (10 pm) per cycle. Separation of the precursors is accomplished by pulsing a purge gas (typically nitrogen or argon) after each precursor pulse to remove excess precursor from the process chamber and prevent 'parasitic' CVD deposition on the substrate.

ALD principle was first published under name “Molecular Layering” in the early 1960s by Prof. S.I. Kol’tsov from Leningrad (Lensovet) Technological Institute (LTI). These ALD experiments were conducted under the scientific supervision of corresponding member of the Russian Academy of Sciences Prof. V.B. Aleskovskii. The concept of the ALD process was first proposed by Prof. V.B. Aleskovskii in his Ph.D. thesis published in 1952.[2] [3] [4] It was the work of Dr Tuomo Suntola and coworkers in Finland in mid-1970s that made a scientific idea a true thin film deposition technology and took that into an industrial use and worldwide awareness. After starting with elemental precursors (that is why name ‘atomic’) they were forced to convert to molecular precursors too to expand the materials selection. But as importantly, Suntola and coworkers also developed reactors that enabled the implementation of the ALD technology (at that time called atomic layer epitaxy (ALE)[5] [6] into industrial level in manufacturing of thin film electroluminescent (TFEL) flat-panel displays. These displays served as the original motivation for developing the ALD technology as they require high quality dielectric and luminescent films on large-area substrates, something that was not available at the time being. TFEL display manufacturing was started in mid-1980s and was for a long time the only industrial application of ALD. Interest in ALD has increased in steps in the mid-1990s and 2000s, with the interest focused on silicon-based microelectronics. ALD is considered as one deposition method with the greatest potential for producing very thin, conformal films with control of the thickness and composition of the films possible at the atomic level. A major driving force for the recent interest is the prospective seen for ALD in scaling down microelectronic devices. In 2004, European SEMI award was given to Dr Tuomo Suntola for inventing the ALD technology and introducing it worldwide.

ALD can be used to deposit several types of thin films, including various oxides (e.g. Al_2O_3, TiO_2, SnO_2, ZnO, HfO_2), metal nitrides (e.g. TiN, TaN, WN, NbN), metals (e.g. Ru, Ir, Pt), and metal sulfides (e.g. ZnS).

ALD process

The growth of material layers by ALD consists of repeating the following characteristic four steps:

1. Exposure of the first precursor, typically an organometallic compound.
2. Purge or evacuation of the reaction chamber to remove the non-reacted precursors and the gaseous reaction by-products.
3. Exposure of the second precursor – or another treatment to activate the surface again for the reaction of the first precursor, such as a plasma.[7]
4. Purge or evacuation of the reaction chamber.

Each reaction cycle adds a given amount of material to the surface, referred to as the growth per cycle. To grow a material layer, reaction cycles are repeated as many as required for the desired film thickness. One cycle may take time from 0.5 s to a few seconds and deposit between 0.1 and 3 Å of film thickness. Due to the self-terminating reactions, ALD is a surface-controlled process, where process parameters other than the precursors, substrate, and temperature have little or no influence. And, because of the surface control, ALD-grown films are extremely conformal and uniform in thickness. These thin films can also be used in correlation with other common fabrication methods.

Advantages and limitations

Advantages

Using ALD, film thickness depends only on the number of reaction cycles, which makes the thickness control accurate and simple. Unlike CVD, there is less need of reactant flux homogeneity, which gives large area (large batch and easy scale-up) capability, excellent conformality and reproducibility, and simplifies the use of solid precursors. Also, the growth of different multilayer structures is straight forward. These advantages make the ALD method attractive for microelectronics for manufacturing of future generation integrated circuits. Other advantages of ALD are the wide range of film materials available, high density and low impurity level. Also, lower deposition temperature can be used in order not to affect sensitive substrates.

Limitations

The major limitation of ALD is its slowness; usually only a fraction of a monolayer is deposited in one cycle. Fortunately, the films needed for future-generation ICs are very thin and thus the slowness of ALD is not such an important issue. More recently, commercial ALD tools can achieve cycle times of <5 seconds meaning a 100nm film can be deposited in under an hour. With batch processing this can equate to a high throughput of wafers/minute. New advances in roll-to-roll ALD are allowing even faster throughput.

Although the selection of film materials grown by ALD is wide, many technologically important materials (Si, Ge, Si_3N_4, several multi-component oxides, certain metals) cannot currently be deposited by ALD in a cost-effective way.

ALD is a chemical technique and thus there is always a risk of residues being left from the precursors. The impurity content of the films depends on the completeness of the reactions. In typical oxide processes where metal halides of alkyl compounds are used together with water as precursors, impurities found in the films are at the 0.1-1 atom % level.

ALD in microelectronics

In microelectronics, ALD is studied as a potential technique to deposit high-*k* (high permittivity) gate oxides, high-*k* memory capacitor dielectrics, ferroelectrics, and metals and nitrides for electrodes and interconnects. In high-*k* gate oxides, where the control of ultra thin films is essential, ALD is only likely to come in to wider use at the 45 nm technology. In metallizations, conformal films are required; currently it is expected that ALD will be used in mainstream production at the 65 nm node. In dynamic random access memories (DRAMs), the conformality requirements are even higher and ALD is the only method that can be used when feature sizes become smaller than 100 nm.[8]

Gate oxides

Deposition of the high-*k* oxides Al_2O_3, ZrO_2, and HfO_2 has been one of the most widely examined areas of ALD. The motivation for high-*k* oxides comes from the problem of high tunneling current through the commonly used SiO_2 gate dielectric in metal-oxide-semiconductor field-effect transistors (MOSFETs) when it is downscaled to a thickness of 1.0 nm and below. With the high-*k* oxide, a thicker gate dielectric can be made for the required capacitance density, thus the tunneling current can be reduced through the structure.

Intel Corporation has reported using ALD to deposit high-*k* gate dielectric for its 45 nm CMOS technology.[9]

DRAM capacitors

The development of dynamic random access memory (DRAM) capacitor dielectrics has been similar to that of gate dielectrics: SiO_2 has been widely used in the industry thus far, but it is likely to be phased out in the near future as the scale of devices are decreased. The requirements for the downscaled DRAM capacitors are good conformality and permittivity values above 200, thus the candidate materials are different from those explored for MOSFET gate dielectrics. (For example, Al_2O_3, ZrO_2, and HfO_2) The most extensively studied candidate has been $(Ba,Sr)TiO_3$. ALD is a very promising method, which can satisfy the high conformal requirements of DRAM applications. A permittivity of 180 was measured for $SrTiO_3$ and 165 for $BaTiO_3$ when films thicker than 200 nm were post-deposition annealed, but when the film thickness was decreased to 50 nm, the permittivity decreased to only 100.[10]

Transition-metal nitrides

Transition-metal nitrides, such as TiN and TaN find potential use both as metal barriers and as gate metals. Metal barriers are used in modern Cu-based chips to avoid diffusion of Cu into the surrounding materials, such as insulators and the silicon substrate, and also, to prevent Cu contamination by elements diffusing from the insulators by surrounding every Cu interconnection with a layer of metal barriers. The metal barriers have strict demands: they should be pure; dense; conductive; conformal; thin; have good adhesion towards metals and insulators. The requirements concerning process technique can be fulfilled by ALD. The most studied ALD nitride is TiN which is deposited from $TiCl_4$ and NH_3.[11]

Metal films

Motivations of an interest in metal ALD are:

1. Cu interconnects and W plugs, or at least Cu seed layers for Cu electrodeposition and W seeds for W CVD,
2. transition-metal nitrides (e.g. TiN, TaN, WN) for Cu interconnect barriers
3. noble metals for ferroelectric random access memory (FRAM) and DRAM capacitor electrodes
4. high- and low-work function metals for dual-gate MOSFETs.

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- Journal articles discussing ALD (http://ald.colorado.edu/J_Phys_Chem_100.pdf) (http://link.aip.org/link/?JAPIAU/97/121301/1) (http://avspublications.org/jvsta/resource/1/jvtad6/v29/i5/p050801_s1) (http://jes.ecsdl.org/content/157/7/P66.abstract?sid=5799daa8-334d-4c05-bec1-0408a7b7d104) (http://avspublications.org/jvsta/resource/1/jvtad6/v30/i1/p01A133_s1)
- Academic researchers specializing in ALD (http://chem.wayne.edu/faculty/winter/) (http://www.chem.harvard.edu/groups/gordon/) (http://www.colorado.edu/chem/people/georges.html) (http://phys.tue.nl/pmp/) (http://www.cmbe.engr.uconn.edu/profile_willis_brian.html)
- Major conferences dedicated to ALD (http://www.phys.tue.nl/ALD2008/)
- ALD Animation (http://www.youtube.com/watch?v=9p2wwOTpCCI)

Etching (microfabrication)

Etching is used in microfabrication to chemically remove layers from the surface of a wafer during manufacturing. Etching is a critically important process module, and every wafer undergoes many etching steps before it is complete.

For many etch steps, part of the wafer is protected from the etchant by a "masking" material which resists etching. In some cases, the masking material is a photoresist which has been patterned using photolithography. Other situations require a more durable mask, such as silicon nitride.

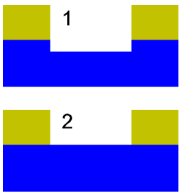
Etching tanks used to perform Piranha, Hydrofluoric acid or RCA clean on 4-inch wafer batches at LAAS technological facility in Toulouse, France

Figures of merit

If the etch is intended to make a cavity in a material, the depth of the cavity may be controlled approximately using the etching time and the known etch rate. More often, though, etching must entirely remove the top layer of a multilayer structure, without damaging the underlying or masking layers. The etching system's ability to do this depends on the ratio of etch rates in the two materials (*selectivity*).

Some etches undercut the masking layer and form cavities with sloping sidewalls. The distance of undercutting is called *bias*. Etchants with large bias are called *isotropic*, because they erode the substrate equally in all directions. Modern processes greatly prefer anisotropic etches, because they produce sharp, well-controlled features.

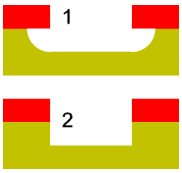
Selectivity



Yellow: layer to be removed; blue: layer to remain

1. A poorly selective etch removes the top layer, but also attacks the underlying material.
2. A highly selective etch leaves the underlying material unharmed.

Isotropy



Red: masking layer; yellow: layer to be removed

1. A perfectly isotropic etch produces round sidewalls.
2. A perfectly anisotropic etch produces vertical sidewalls.

Etching media and technology

The two fundamental types of etchants are liquid-phase ("wet") and plasma-phase ("dry"). Each of these exists in several varieties.

Wet etching

The first etching processes used liquid-phase ("wet") etchants. The wafer can be immersed in a bath of etchant, which must be agitated to achieve good process control. For instance, buffered hydrofluoric acid (BHF) is used commonly to etch silicon dioxide over a silicon substrate.

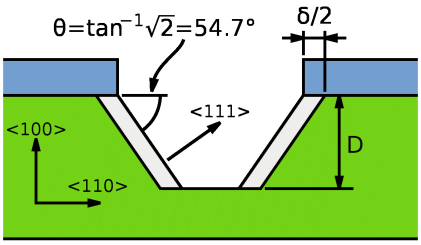
Different specialised etchants can be used to characterise the surface etched.

Wet etchants are usually isotropic, which leads to large bias when etching thick films. They also require the disposal of large amounts of toxic waste. For these reasons, they are seldom used in state-of-the-art processes. However, the photographic developer used for photoresist resembles wet etching.

As an alternative to immersion, single wafer machines use the Bernoulli principle to employ a gas (usually, pure nitrogen) to cushion and protect one side of the wafer while etchant is applied to the other side. It can be done to either the front side or back side. The etch chemistry is dispensed on the top side when in the machine and the bottom side is not affected. This etch method is particularly effective just before "backend" processing (BEOL), where wafers are normally very much thinner after wafer backgrinding, and very sensitive to thermal or mechanical stress. Etching a thin layer of even a few micrometres will remove microcracks produced during backgrinding resulting in the wafer having dramatically increased strength and flexibility without breaking.

Anisotropic wet etching (Orientation dependent etching)

Some wet etchants etch crystalline materials at very different rates depending upon which crystal face is exposed. In single-crystal materials (e.g. silicon wafers), this effect can allow very high anisotropy, as shown in the figure.



An anisotropic wet etch on a silicon wafer creates a cavity with a trapezoidal cross-section. The bottom of the cavity is a {100} plane (see Miller indices), and the sides are {111} planes. The blue material is an etch mask, and the green material is silicon.

Several anisotropic wet etchants are available for silicon, all of them hot aqueous caustics. For instance, potassium hydroxide (KOH) displays an etch rate selectivity 400 times higher in <100> crystal directions than in <111> directions. EDP (an aqueous solution of ethylene diamine and pyrocatechol), displays a <100>/<111> selectivity of 17X, does not etch silicon dioxide as KOH does, and also displays high selectivity between lightly doped and heavily boron-doped (p-type) silicon. Use of these etchants on wafers that already contain CMOS integrated circuits requires protecting the circuitry. KOH may introduce mobile potassium ions into silicon dioxide, and EDP is highly corrosive and carcinogenic, so care is required in their use. Tetramethylammonium hydroxide (TMAH) presents a safer alternative than EDP, with a 37X selectivity between {100} and {111} planes in silicon.

Etching a (100) silicon surface through a rectangular hole in a masking material, for example a hole in a layer of silicon nitride, creates a pit with flat sloping {111}-oriented sidewalls and a flat (100)-oriented bottom. The {111}-oriented sidewalls have an angle to the surface of the wafer of:

$$\tan^{-1}\sqrt{2} = 54.7^\circ$$

If the etching is continued "to completion", i.e. until the flat bottom disappears, the pit becomes a trench with a V-shaped cross section. If the original rectangle was a perfect square, the pit when etched to completion displays a pyramidal shape.

The undercut, δ, under an edge of the masking material is given by:

$$\delta = \frac{\sqrt{6}D}{S} = \frac{\sqrt{6}R_{100}T}{R_{100}/R_{111}} = \sqrt{6}TR_{111},$$

where R_{xxx} is the etch rate in the <xxx> direction, T is the etch time, D is the etch depth and S is the anisotropy of the material and etchant.

Different etchants have different anisotropies. Below is a table of common anisotropic etchants for silicon:

Etchant	Operating temp (°C)	R_{100} (μm/min)	$S=R_{100}/R_{111}$	Mask materials
Ethylenediamine pyrocatechol (EDP)[1]	110	0.47	17	SiO_2, Si_3N_4, Au, Cr, Ag, Cu
Potassium hydroxide/Isopropyl alcohol (KOH/IPA)	50	1.0	400	Si_3N_4, SiO_2 (etches at 2.8 nm/min)
Tetramethylammonium hydroxide (TMAH)[2]	80	0.6	37	Si_3N_4, SiO_2

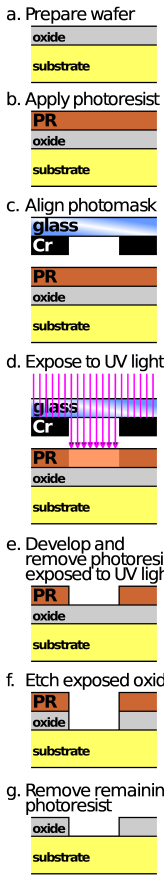
Plasma etching

Modern VLSI processes avoid wet etching, and use *plasma etching* instead. Plasma etchers can operate in several modes by adjusting the parameters of the plasma. Ordinary plasma etching operates between 0.1 and 5 Torr. (This unit of pressure, commonly used in vacuum engineering, equals approximately 133.3 pascals.) The plasma produces energetic free radicals, neutrally charged, that react at the surface of the wafer. Since neutral particles attack the wafer from all angles, this process is isotropic.

Plasma etching can be isotropic, i.e., exhibiting a lateral undercut rate on a patterned surface approximately the same as its downward etch rate, or can be anisotropic, i.e., exhibiting a smaller lateral undercut rate than its downward etch rate. Such anisotropy is maximized in deep reactive ion etching. The use of the term anisotropy for plasma etching should not be conflated with the use of the same term when referring to orientation-dependent etching.

The source gas for the plasma usually contains small molecules rich in chlorine or fluorine. For instance, carbon tetrachloride (CCl_4) etches silicon and aluminium, and trifluoromethane etches silicon dioxide and silicon nitride. A plasma containing oxygen is used to oxidize ("ash") photoresist and facilitate its removal.

Ion milling, or *sputter etching*, uses lower pressures, often as low as 10^{-4} Torr (10 mPa). It bombards the wafer with energetic ions of noble gases, often Ar^+, which knock atoms from the substrate by transferring momentum. Because the etching is performed by ions, which approach the wafer approximately from one direction, this process is highly anisotropic. On the other hand, it tends to display poor selectivity. *Reactive-ion etching* (RIE) operates under conditions intermediate between sputter and plasma etching (between 10^{-3} and 10^{-1} Torr). *Deep reactive-ion etching* (DRIE) modifies the RIE technique to produce deep, narrow features.



Simplified illustration of dry etching using positive photoresist during a photolithography process in semiconductor microfabrication. Note: Not to scale.

Common etch processes used in microfabrication

Etchants for common microfabrication materials

Material to be etched	Wet etchants	Plasma etchants
Aluminium (Al)	80% phosphoric acid (H_3PO_4) + 5% acetic acid + 5% nitric acid (HNO_3) + 10% water (H_2O) at 35–45 °C[3]	Cl_2, CCl_4, $SiCl_4$, BCl_3[4]
Indium tin oxide [ITO] (In_2O_3:SnO_2)	Hydrochloric acid (HCl) + nitric acid (HNO_3) + water (H_2O) (1:0.1:1) at 40 °C[5]	
Chromium (Cr)	• "Chrome etch": ceric ammonium nitrate ($(NH_4)_2Ce(NO_3)_6$) + nitric acid (HNO_3)[6] • Hydrochloric acid (HCl)[6]	
Gallium Arsenide (GaAs)	• Hydrochloric Acid (HCl) • Citric Acid diluted ($C_6H_8O_7$: H_2O, 1 : 1) + Hydrogen Peroxide (H_2O_2)+ Water (H_2O)	• Cl_2, CCl_4, $SiCl_4$, BCl_3, CCl_2F_2
Gold (Au)	Aqua regia	
Molybdenum (Mo)		CF_4[4]
Organic residues and photoresist	Piranha etch: sulfuric acid (H_2SO_4) + hydrogen peroxide (H_2O_2)	O_2 (ashing)
Platinum (Pt)	Aqua regia	
Silicon (Si)	• Nitric acid (HNO_3) + hydrofluoric acid (HF)[3] • Potassium hydroxide (KOH) • Ethylenediamine pyrocatechol (EDP) • Tetramethylammonium hydroxide (TMAH)	• CF_4, SF_6, NF_3[4] • Cl_2, CCl_2F_2[4]
Silicon dioxide (SiO_2)	• Hydrofluoric acid (HF)[3] • Buffered oxide etch [BOE]: ammonium fluoride (NH_4F) and hydrofluoric acid (HF)[3]	CF_4, SF_6, NF_3[4]
Silicon nitride (Si_3N_4)	• 85% Phosphoric acid (H_3PO_4) at 180 °C[3] (Requires SiO_2 etch mask)	CF_4, SF_6, NF_3,[4] CHF_3
Tantalum (Ta)		CF_4[4]
Titanium (Ti)	Hydrofluoric acid (HF)[3]	BCl_3[7]
Titanium nitride (TiN)	• Nitric acid (HNO_3) + hydrofluoric acid (HF) • SC1 • Buffered HF (bHF)	
Tungsten (W)	• Nitric acid (HNO_3) + hydrofluoric acid (HF) • Hydrogen Peroxide (H_2O_2)	• CF_4[4] • SF_6

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External links

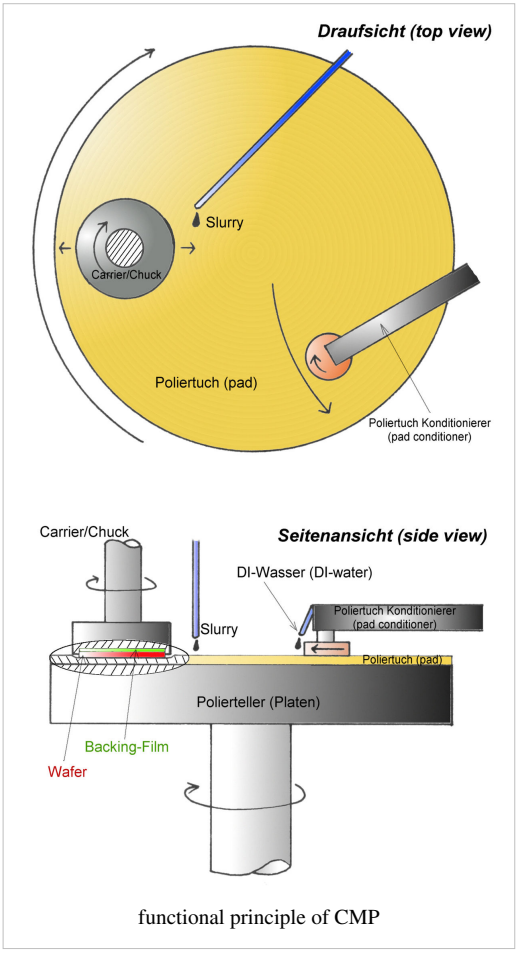
- BYU Cleanroom Chemical Etching (http://www.cleanroom.byu.edu/wet_etch.phtml)
- Technology of wet etching (http://www.crystec.com/jwawete.htm) of silicon and semiconductor wafers.
- Technology of dry etching (http://www.crystec.com/trietche.htm) or plasma etching of silicon and semiconductor wafers.

Chemical-mechanical planarization

Chemical Mechanical Polishing/Planarization is a process of smoothing surfaces with the combination of chemical and mechanical forces. It can be thought of as a hybrid of chemical etching and free abrasive polishing.

Description

The process uses an abrasive and corrosive chemical slurry (commonly a colloid) in conjunction with a polishing pad and retaining ring, typically of a greater diameter than the wafer. The pad and wafer are pressed together by a dynamic polishing head and held in place by a plastic retaining ring. The dynamic polishing head is rotated with different axes of rotation (i.e., not concentric). This removes material and tends to even out any irregular topography, making the wafer flat or planar. This may be necessary in order to set up the wafer for the formation of additional circuit elements. For example, this might be necessary in order to bring the entire surface within the depth of field of a photolithography system, or to selectively remove material based on its position. Typical depth-of-field requirements are down to Angstrom levels for the latest 22 nm technology.



functional principle of CMP

Working Principles

Typical CMP tools, such as the ones seen on the right, consist of a rotating and extremely flat platen which is covered by a pad. The wafer that is being polished is mounted upside-down in a carrier/spindle on a backing film. The retaining ring (Figure 1) keeps the wafer in the correct horizontal position. During the process of loading and unloading the wafer onto the tool, the wafer is held by vacuum by the carrier to prevent unwanted particles from building up on the wafer surface. A slurry introduction mechanism deposits the slurry on the pad, this is represented by the slurry supply in Figure 1. Both the platen and the carrier are then rotated and the carrier is kept oscillating as well; this can be better seen in the top view of Figure 2. A downward pressure/down force is applied to the carrier, pushing it against the pad; typically the down force is an average force, but local pressure is needed for the removal mechanisms. Down force depends on the contact area which, in turn, is dependent on the structures of both the wafer and the pad. Typically the pads have a roughness of 50 µm; contact is made by asperities (which typically are the high points on the wafer) and, as a result, the contact area is only a fraction of the wafer area. In CMP, the mechanical properties of the wafer itself must be considered too. If the wafer has a slightly bowed structure, the pressure will be greater on the edges than it would on the center, which causes non-uniform polishing. In order to compensate for the wafer bow, pressure can be applied to the wafer's backside which, in turn, will equalize the centre-edge differences. The pads used in the CMP tool should be rigid in order to uniformly polish the wafer surface. However, these rigid pads must be kept in alignment with the wafer at all times. Therefore, real pads are often just stacks of soft and hard materials that conform to wafer topography to some extent. Generally, these pads are made from porous polymeric materials with a pore size

between 30-50 μm, are consumed in the process, and must be regularly reconditioned. In most cases the pads are very much proprietary, and are usually referred to by their trademark names rather than their chemical or other properties.

Usage in semiconductor fabrication

Before about 1990 CMP was looked on as too "dirty" to be included in high-precision fabrication processes, since abrasion tends to create particles and the abrasives themselves are not without impurities. Since that time, the integrated circuit industry has moved from aluminium to copper conductors. This required the development of an *additive patterning* process, which relies on the unique abilities of CMP to remove material in a planar and uniform fashion and to stop repeatably at the interface between copper and oxide insulating layers (see Copper-based chips for details). Adoption of this process has made CMP processing much more widespread. In addition to aluminum and copper, CMP processes have been developed for polishing tungsten, silicon dioxide, and (recently) carbon nanotubes.[1]

Limitations of CMP

There are currently several limitations of CMP that appear during the polishing process requiring optimization of a new technology. In particular, an improvement in wafer metrology is required. In addition, it was discovered that the CMP process has several potential defects including stress cracking, delaminating at weak interfaces, and corrosive attacks from slurry chemicals. The oxide polishing process, which is the oldest and most used in today's industry, has one problem: a lack of end points requires blind polishing, making it hard to determine when the desired amount of material has been removed or the desired degree of planarization has been obtained. If the oxide layer has not been sufficiently thinned and/or the desired degree of planarity has not been achieved during this process, then (theoretically) the wafer can be repolished, but in a practical sense this is unattractive in production and is to be avoided if at all possible. If the oxide thickness is too thin or too non-uniform, then the wafer must be reworked, an even less attractive process and one that is likely to fail. Obviously, this method is time-consuming and costly since technicians have to be more attentive while performing this process.

Application

Shallow trench isolation (STI), a process used to fabricate semiconductor devices, is a technique used to enhance the isolation between devices and active areas. Moreover, STI has a higher degree of planarity making it essential in photolithographic applications, depth of focus budget by decreasing minimum line width. To planarize shallow trenches, a common method should be used such as the combination of resist etching-back (REB) and chemical mechanical polishing (CMP). This process comes in a sequence pattern as follows. First, the isolation trench pattern is transferred to the silicon wafer. Oxide is deposited on the wafer in the shape of trenches. A photo mask, composed of silicon nitride, is patterned on the top of this sacrificial oxide. A second layer is added to the wafer to create a planar surface. After that, the silicon is thermally oxidized, so the oxide grows in regions where there is no Si3N4 and the growth is between 0.5 and 1.0 μm thick. Since the oxidizing species such as water or oxygen are unable to diffuse through the mask, the nitride prevents the oxidation. Next, the etching process is used to etch the wafer and leave a small amount of oxide in the active areas. In the end, CMP is used to polish the SiO_2 overburden with an oxide on the active area.

References

[1] Awano,Y.: (2006), "Carbon Nanotube (CNT) Via Interconnect Technologies: Low temperature CVD growth and chemical mechanical planarization for vertically aligned CNTs". *Proc. 2006 ICPT*, 10

External links

- "CMP, chemical mechanical planarization, polishing equipment", by Crystec Technology Trading GmbH obtained from: http://www.crystec.com/alpovere.htm
- "Chemical Mechanical Planarization", by Dr. Wang Zengfeng, Dr. Yin Ling, Ng Sum Huan, and Teo Phaik Luan obtained from: http://maltiel-consulting.com/CMP-Chemical-mechanical_planarization_maltiel_semiconductor.pdf

Books

- Silicon processing for the VLSI Era — Vol. IV *Deep-submicron Process Technology* — S Wolf, 2002, ISBN 978-0-9616721-7-1, Chapter 8 "Chemical mechanical polishing" pp. 313—432

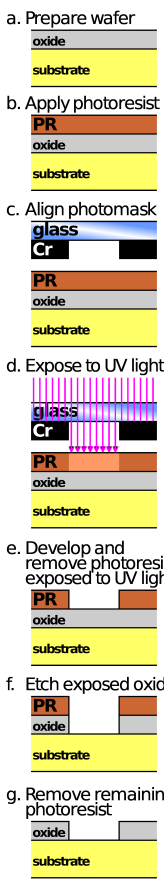
Photolithography

Photolithography (also termed "optical lithography" or "UV lithography") is a process used in microfabrication to pattern parts of a thin film or the bulk of a substrate. It uses light to transfer a geometric pattern from a photomask to a light-sensitive chemical "photoresist", or simply "resist," on the substrate. A series of chemical treatments then either engraves the exposure pattern into, or enables deposition of a new material in the desired pattern upon, the material underneath the photo resist. For example, in complex integrated circuits, a modern CMOS wafer will go through the photolithographic cycle up to 50 times.

Photolithography shares some fundamental principles with photography in that the pattern in the etching resist is created by exposing it to light, either directly (without using a mask) or with a projected image using an optical mask. This procedure is comparable to a high precision version of the method used to make printed circuit boards. Subsequent stages in the process have more in common with etching than with lithographic printing. It is used because it can create extremely small patterns (down to a few tens of nanometers in size), it affords exact control over the shape and size of the objects it creates, and because it can create patterns over an entire surface cost-effectively. Its main disadvantages are that it requires a flat substrate to start with, it is not very effective at creating shapes that are not flat, and it can require extremely clean operating conditions.

Basic procedure

A single iteration of photolithography combines several steps in sequence. Modern cleanrooms use automated, robotic wafer track systems to coordinate the process. The procedure described here omits some advanced treatments, such as thinning agents or edge-bead removal.[1]



Simplified illustration of dry etching using positive photoresist during a photolithography process in semiconductor microfabrication (not to scale).

Cleaning

If organic or inorganic contaminations are present on the wafer surface, they are usually removed by wet chemical treatment, e.g. the RCA clean procedure based on solutions containing hydrogen peroxide.

Preparation

The wafer is initially heated to a temperature sufficient to drive off any moisture that may be present on the wafer surface. Wafers that have been in storage must be chemically cleaned to remove contamination. A liquid or gaseous "adhesion promoter", such as Bis(trimethylsilyl)amine ("hexamethyldisilazane", HMDS), is applied to promote adhesion of the photoresist to the wafer. The surface layer of silicon dioxide on the wafer reacts with HMDS to form tri-methylated silicon-dioxide, a highly water repellent layer not unlike the layer of wax on a car's paint. This water repellent layer prevents the aqueous developer from penetrating between the photoresist layer and the wafer's surface, thus preventing so-called lifting of small photoresist structures in the (developing) pattern.

Photoresist application

The wafer is covered with photoresist by spin coating. A viscous, liquid solution of photoresist is dispensed onto the wafer, and the wafer is spun rapidly to produce a uniformly thick layer. The spin coating typically runs at 1200 to 4800 rpm for 30 to 60 seconds, and produces a layer between 0.5 and 2.5 micrometres thick. The spin coating process results in a uniform thin layer, usually with uniformity of within 5 to 10 nanometres. This uniformity can be explained by detailed fluid-mechanical modelling, which shows that the resist moves much faster at the top of the layer than at the bottom, where viscous forces bind the resist to the wafer surface. Thus, the top layer of resist is quickly ejected from the wafer's edge while the bottom layer still creeps slowly radially along the wafer. In this way, any 'bump' or 'ridge' of resist is removed, leaving a very flat layer. Final thickness is also determined by the evaporation of liquid solvents from the resist. For very small, dense features (<125 or so nm), lower resist thicknesses (<0.5 micrometres) are needed to overcome collapse effects at high aspect ratios; typical aspect ratios are <4:1.

The photo resist-coated wafer is then prebaked to drive off excess photoresist solvent, typically at 90 to 100 °C for 30 to 60 seconds on a hotplate.

Exposure and developing

After prebaking, the photoresist is exposed to a pattern of intense light. The exposure to light causes a chemical change that allows some of the photoresist to be removed by a special solution, called "developer" by analogy with photographic developer. Positive photoresist, the most common type, becomes soluble in the developer when exposed; with negative photoresist, unexposed regions are soluble in the developer. To learn more about the process of exposure and development of positive resist, see Ralph Dammel, "Diazonaphtoquinone-based resists", SPIE Optical Engineering Press, Vol TT11 (1993).

A post-exposure bake (PEB) is performed before developing, typically to help reduce standing wave phenomena caused by the destructive and constructive interference patterns of the incident light. In deep ultraviolet lithography, chemically amplified resist (CAR) chemistry is used. This process is much more sensitive to PEB time, temperature, and delay, as most of the "exposure" reaction (creating acid, making the polymer soluble in the basic developer) actually occurs in the PEB.[2]

The develop chemistry is delivered on a spinner, much like photoresist. Developers originally often contained sodium hydroxide (NaOH). However, sodium is considered an extremely undesirable contaminant in MOSFET fabrication because it degrades the insulating properties of gate oxides (specifically, sodium ions can migrate in and out of the gate, changing the threshold voltage of the transistor and making it harder or easier to turn the transistor on over time). Metal-ion-free developers such as tetramethylammonium hydroxide (TMAH) are now used.

The resulting wafer is then "hard-baked" if a non-chemically amplified resist was used, typically at 120 to 180 °C for 20 to 30 minutes. The hard bake solidifies the remaining photoresist, to make a more durable protecting layer in future ion implantation, wet chemical etching, or plasma etching.

Etching

In etching, a liquid ("wet") or plasma ("dry") chemical agent removes the uppermost layer of the substrate in the areas that are not protected by photoresist. In semiconductor fabrication, dry etching techniques are generally used, as they can be made anisotropic, in order to avoid significant undercutting of the photoresist pattern. This is essential when the width of the features to be defined is similar to or less than the thickness of the material being etched (i.e. when the aspect ratio approaches unity). Wet etch processes are generally isotropic in nature, which is often indispensable for microelectromechanical systems, where suspended structures must be "released" from the underlying layer.

The development of low-defectivity anisotropic dry-etch process has enabled the ever-smaller features defined photolithographically in the resist to be transferred to the substrate material.

Photoresist removal

After a photoresist is no longer needed, it must be removed from the substrate. This usually requires a liquid "resist stripper", which chemically alters the resist so that it no longer adheres to the substrate. Alternatively, photoresist may be removed by a plasma containing oxygen, which oxidizes it. This process is called ashing, and resembles dry etching.

Exposure ("printing") systems

Exposure systems typically produce an image on the wafer using a photomask. The light shines through the photomask, which blocks it in some areas and lets it pass in others. (Maskless lithography projects a precise beam directly onto the wafer without using a mask, but it is not widely used in commercial processes.) Exposure systems may be classified by the optics that transfer the image from the mask to the wafer.

The wafer track portion of an aligner that uses 365 nm ultraviolet light

Contact and proximity

A contact printer, the simplest exposure system, puts a photomask in direct contact with the wafer and exposes it to a uniform light. A proximity printer puts a small gap between the photomask and wafer. In both cases, the mask covers the entire wafer, and simultaneously patterns every die.

Contact printing is liable to damage both the mask and the wafer, and this was the primary reason it was abandoned for high volume production. Both contact and proximity lithography require the light intensity to be uniform across an entire wafer, and the mask to align precisely to features already on the wafer. As modern processes use increasingly large wafers, these conditions become increasingly difficult.

Research and prototyping processes often use contact or proximity lithography, because it uses inexpensive hardware and can achieve high optical resolution. The resolution in proximity lithography is approximately the square root of the product of the wavelength and the gap distance. Hence, except for projection lithography (see below), contact printing offers the best resolution, because its gap distance is approximately zero (neglecting the thickness of the photoresist itself). In addition, nanoimprint lithography may revive interest in this familiar technique, especially since the cost of ownership is expected to be low; however, the shortcomings of contact printing discussed above remain as challenges.

Projection

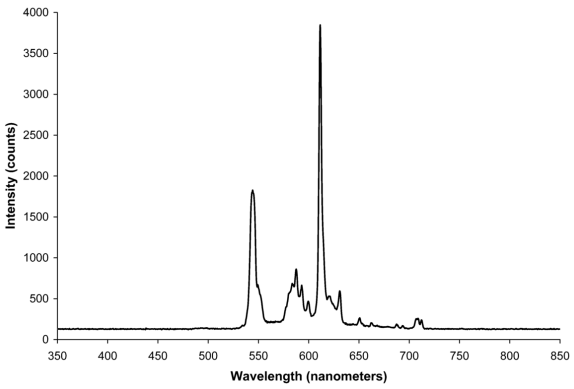
Very-large-scale integration (VLSI) lithography uses projection systems. Unlike contact or proximity masks, which cover an entire wafer, projection masks (known as "reticles") show only one die or an array of dice (known as a "field"). Projection exposure systems (steppers or scanners) project the mask onto the wafer many times to create the complete pattern.

Photomasks

The image for the mask originates from a computerized data file. This data file is converted to a series of polygons and written onto a square fused quartz substrate covered with a layer of chromium using a photolithographic process. A laser beam (laser writer) or a beam of electrons (e-beam writer) is used to expose the pattern defined by the data file and travels over the surface of the substrate in either a vector or raster scan manner. Where the photoresist on the mask is exposed, the chrome can be etched away, leaving a clear path for the illumination light in the stepper/scanner system to travel through.

Resolution in projection systems

The ability to project a clear image of a small feature onto the wafer is limited by the wavelength of the light that is used, and the ability of the reduction lens system to capture enough diffraction orders from the illuminated mask. Current state-of-the-art photolithography tools use deep ultraviolet (DUV) light from excimer lasers with wavelengths of 248 and 193 nm (the dominant lithography technology today is thus also called "excimer laser lithography"), which allow minimum feature sizes down to 50 nm. Excimer laser lithography has thus played a critical role in the continued advance of the so-called Moore's Law for the last 20 years (see below[3]).



The filtered fluorescent lighting in photolithography cleanrooms contains no ultraviolet or blue light in order to avoid exposing photoresists. The spectrum of light emitted by such fixtures gives virtually all such spaces a bright yellow color.

The minimum feature size that a projection system can print is given approximately by:

$$CD = k_1 \cdot \frac{\lambda}{NA}$$

where

CD is the **minimum feature size** (also called the **critical dimension**, *target design rule*). It is also common to write 2 *times* the *half-pitch*.

k_1 (commonly called *k1 factor*) is a coefficient that encapsulates process-related factors, and typically equals 0.4 for production. The minimum feature size can be reduced by decreasing this coefficient through Computational lithography.

λ is the wavelength of light used

NA is the numerical aperture of the lens as seen from the wafer

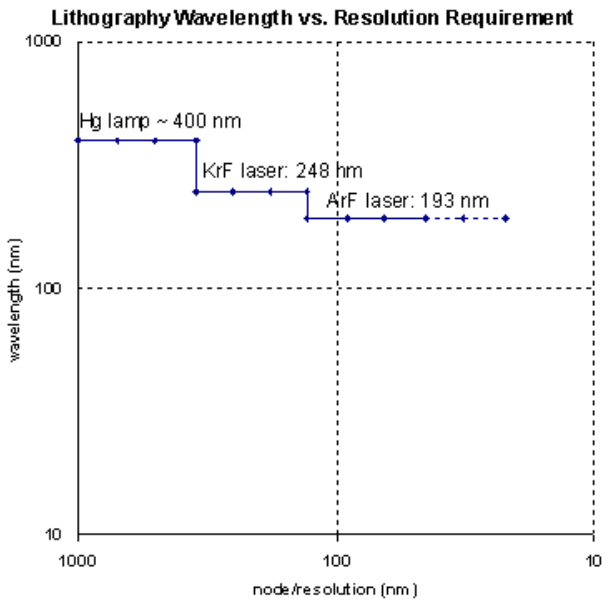
According to this equation, minimum feature sizes can be decreased by decreasing the wavelength, and increasing the numerical aperture (to achieve a tighter focused beam and a smaller spot size). However, this design method runs into a competing constraint. In modern systems, the depth of focus is also a concern:

$$D_F = k_2 \cdot \frac{\lambda}{NA^2}$$

Here, k_2 is another process-related coefficient. The depth of focus restricts the thickness of the photoresist and the depth of the topography on the wafer. Chemical mechanical polishing is often used to flatten topography before high-resolution lithographic steps.

Light sources

Historically, photolithography has used ultraviolet light from gas-discharge lamps using mercury, sometimes in combination with noble gases such as xenon. These lamps produce light across a broad spectrum with several strong peaks in the ultraviolet range. This spectrum is filtered to select a single spectral line. From the early 1960s through the mid-1980s, Hg lamps had been used in lithography for their spectral lines at 436 nm ("g-line"), 405 nm ("h-line") and 365 nm ("i-line"). However, with the semiconductor industry's need for both higher resolution (to produce denser and faster chips) and higher throughput (for lower costs), the lamp-based lithography tools were no longer able to meet the industry's requirements.



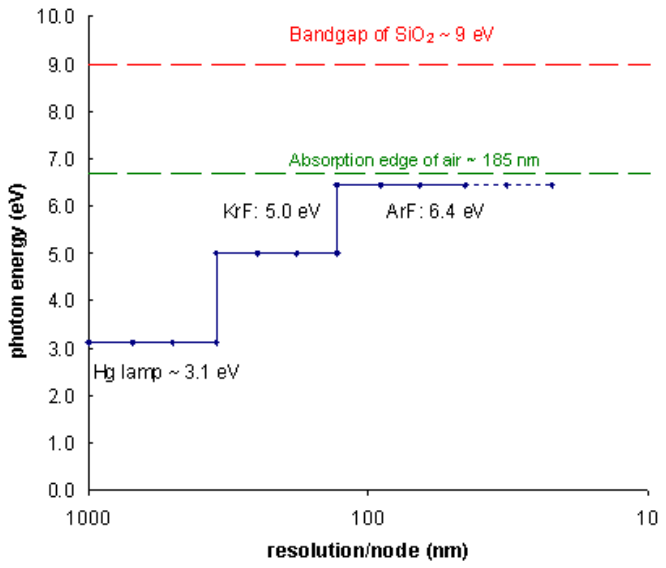
One of the evolutionary paths of lithography has been the use of shorter wavelengths. It is worth noting that the same light source may be used for several technology generations.

This challenge was overcome when in a pioneering development in 1982, excimer laser lithography was proposed and demonstrated at I.B.M. by Kanti Jain,[4][5][6][7] and now excimer laser lithography machines (steppers and scanners) are the primary tools used worldwide in microelectronics production. With phenomenal advances made in tool technology in the last two decades, it is the semiconductor industry view[3] that excimer laser lithography has been a crucial factor in the continued advance of Moore's Law, enabling minimum features sizes in chip manufacturing to shrink from 0.5 micrometer in 1990 to 45 nanometers and below in 2010. This trend is expected to continue into this decade for even denser chips, with minimum features approaching 10

nanometers. From an even broader scientific and technological perspective, in the 50-year history of the laser since its first demonstration in 1960, the invention and development of excimer laser lithography has been highlighted as one of the major milestones.[8][9][10]

The commonly used deep ultraviolet excimer lasers in lithography systems are the Krypton fluoride laser at 248-nm wavelength and the argon fluoride laser at 193-nm wavelength. The primary manufacturers of excimer laser light sources in the 1980s were Lambda Physik (now part of Coherent, Inc.) and Lumonics, but since the mid-1990s Cymer Inc. has become the dominant supplier of excimer laser sources to the lithography equipment manufacturers. Generally, an excimer laser is designed to operate with a specific gas mixture; therefore, changing wavelength is not a trivial matter, as the method of generating the new wavelength is completely different, and the absorption characteristics of materials change. For example, air begins to absorb significantly around the 193 nm wavelength; moving to sub-193 nm wavelengths would require installing vacuum pump and purge equipment on the lithography tools (a significant challenge). Furthermore, insulating materials such as silicon dioxide (SiO_2), when exposed to photons with energy greater than the band gap, release free electrons and holes which subsequently cause adverse charging.

Optical lithography has been extended to feature sizes below 50 nm using the 193 nm ArF excimer laser and liquid immersion techniques. Also termed immersion lithography, this enables the use of optics with numerical apertures exceeding 1.0. The liquid used is typically ultra-pure, deionised water, which provides for a refractive index above that of the usual air gap between the lens and the wafer surface. The water is continually circulated to eliminate thermally-induced distortions. Water will only allow *NA*'s of up to ~1.4, but materials with higher refractive indices will allow the effective *NA* to be increased further.



Changing the lithography wavelength is significantly limited by absorption. Air absorbs below ~ 185 nm.

Experimental tools using the 157 nm wavelength from the F2 excimer laser in a manner similar to current exposure systems have been built. These were once targeted to succeed 193 nm lithography at the 65 nm feature size node but have now all but been eliminated by the introduction of immersion lithography. This was due to persistent technical problems with the 157 nm technology and economic considerations that provided strong incentives for the continued use of 193 nm excimer laser lithography technology. High-index immersion lithography is the newest extension of 193 nm lithography to be considered. In 2006, features less than 30 nm were demonstrated by IBM using this technique.[11]

An option, especially if and when wavelengths continue to decrease to extreme UV or X-ray, is the free-electron laser (or one might say xaser for an X-ray device). These can produce high quality beams at arbitrary wavelengths.

Experimental methods

Photolithography has been defeating predictions of its demise for many years. For instance, by the early 1980s, many in the semiconductor industry had come to believe that features smaller than 1 micrometer could not be printed optically. Modern techniques using excimer laser lithography already print features with dimensions a fraction of the wavelength of light used - an amazing optical feat. New tricks such as immersion lithography, dual-tone resist and multiple patterning continue to improve the resolution of 193 nm lithography. Meanwhile, current research is exploring alternatives to conventional UV, such as electron beam lithography, X-ray lithography, extreme ultraviolet lithography and ion projection lithography.

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[8] American Physical Society / Lasers / History / Timeline; http://www.laserfest.org/lasers/history/timeline.cfm

[9] SPIE / Advancing the Laser / 50 Years and into the Future; http://spie.org/Documents/AboutSPIE/SPIE%20Laser%20Luminaries.pdf

[10] U.K. Engineering & Physical Sciences Research Council / Lasers in Our Lives / 50 Years of Impact; http://www.stfc.ac.uk/Resources/PDF/Lasers50_final1.pdf

[11] Hand, Aaron. "High-Index Lenses Push Immersion Beyond 32 nm" (http://www.reed-electronics.com/semiconductor/article/CA6319061). .

External links

- BYU Photolithography Resources (http://www.ee.byu.edu/cleanroom/lithography.phtml)
- Semiconductor Lithography (http://www.lithoguru.com/scientist/lithobasics.html) — Overview of lithography
- Optical Lithography Introduction (http://www.research.ibm.com/journal/rd/411/chiu.html) — IBM site with lithography-related articles
- Immersion Lithography Article (http://sst.pennnet.com/Articles/Article_Display.cfm?Section=ARCHI&Subsection=Display&ARTICLE_ID=205024&p=28) — Shows how depth-of-focus is increased with immersion lithography
- Photolithography Equipment (http://www.imtecacculine.com)- UV Light Shields & Information
- Photo Etching Experts (http://microphoto.net)

Photoresist

A **photoresist** is a light-sensitive material used in several industrial processes, such as photolithography and photoengraving to form a patterned coating on a surface.

Photoresist categories

The main properties characterizing the photoresist types are:

Tone

Photoresists are classified into two groups: positive resists and negative resists.

- A *positive resist* is a type of photoresist in which the portion of the photoresist that is exposed to light becomes soluble to the photoresist developer. The portion of the photoresist that is unexposed remains insoluble to the photoresist developer.
- A *negative resist* is a type of photoresist in which the portion of the photoresist that is exposed to light becomes insoluble to the photoresist developer. The unexposed portion of the photoresist is dissolved by the photoresist developer.

Differences between tone types[1]

Characteristic	Positive	Negative
Adhesion to Silicon	Fair	Excellent
Relative Cost	More Expensive	Less Expensive
Developer Base	Aqueous	Organic
Minimum Feature	0.5 μm and below	± 2 μm
Step Coverage	Better	Lower
Wet Chemical Resistance	Fair	Excellent

Note: This table is based on generalizations which are generally accepted in the MEMS fabrication industry.

Developing light wavelength

The most important light types include UV, DUV, and the g and I lines having wavelength of 436nm and 365nm respectively of a mercury-vapor lamp.

This particular parameter is closely related to the thickness of the applied photoresist, with thinner layers corresponding to shorter wavelengths, permitting a reduced aspect ratio and a reduced minimum feature size. This is important in microelectronics and especially the ITRS reduction in minimum feature size. Intel has semiconductor fabrication facilities currently operating at the 22 nanometer node.

Chemicals Used

Different chemicals may be used for permanently giving the material the desired property variations:

- Poly(methyl methacrylate) (PMMA)
- Poly(methyl glutarimide) (PMGI)
- Phenol formaldehyde resin (DNQ/Novolac)
- SU-8

The above materials are all applied as a liquid and, generally, spin-coated to ensure uniformity of thickness.

- Dry film – stands alone amongst the other types in that the coating already exists as a uniform thickness, semi-solid film coated onto a polyester substrate and the user applies that substrate to the workpiece in question by lamination.

Applications

- **Fabrication of printed circuit boards**. This can be done by applying photoresist, exposing to the image, and then etching using iron chloride, cupric chloride or an alkaline ammonia etching solution to remove the copperclad substrate.
- **Sand carving**. Sand blasting of materials is done after a photolithographically printed pattern has been applied as a mask.
- **Microelectronics** This application, mainly applied to silicon wafers/silicon integrated circuits is the most developed of the technologies and the most specialized in the field.
- **Patterning and etching of substrates**. This includes specialty photonics materials, MEMS, glass printed circuit boards, and other micropatterning tasks. Photoresist tends not to be etched by solutions with a pH greater than 3.[2]

Other aspects of photoresist technologies

Absorption at UV and shorter wavelengths

Photoresists are most commonly used at wavelengths in the ultraviolet spectrum or shorter (<400 nm). For example, diazonaphthoquinone (DNQ) absorbs strongly from approximately 300 nm to 450 nm. The absorption bands can be assigned to n-π* (S_0–S_1) and π-π* (S_1–S_2) transitions in the DNQ molecule.[3] In the deep ultraviolet (DUV) spectrum, the π-π* electronic transition in benzene [4] or carbon double-bond chromophores [5] appears at around 200 nm. Due to the appearance of more possible absorption transitions involving larger energy differences, the absorption tends to increase with shorter wavelength, or larger photon energy. Photons with energies exceeding the ionization potential of the photoresist (can be as low as 5 eV in condensed solutions)[6] can also release electrons which are capable of additional exposure of the photoresist. From about 5 eV to about 20 eV, photoionization of outer "valence band" electrons is the main absorption mechanism.[7] Above 20 eV, inner electron ionization and Auger transitions become more important. Photon absorption begins to decrease as the X-ray region is approached, as fewer Auger transitions between deep atomic levels are allowed for the higher photon energy. The absorbed energy can drive further reactions and ultimately dissipates as heat. This is associated with the outgassing and contamination from the photoresist.

Electron-beam exposure

Photoresists can also be exposed by electron beams, producing the same results as exposure by light. The main difference is that while photons are absorbed, depositing all their energy at once, electrons deposit their energy gradually, and scatter within the photoresist during this process. As with high-energy wavelengths, many transitions are excited by electron beams, and heating and outgassing are still a concern. The dissociation energy for a C-C bond is 3.6 eV. Secondary electrons generated by primary ionizing radiation have energies sufficient to dissociate this bond, causing scission. In addition, the low-energy electrons have a longer photoresist interaction time due to their lower speed; essentially the electron has to be at rest with respect to the molecule in order to react most strongly via dissociative electron attachment, where the electron comes to rest at the molecule, depositing all its kinetic energy.[8] The resulting scission breaks the original polymer into segments of lower molecular weight, which are more readily dissolved in a solvent, or else releases other chemical species (acids) which catalyze further scission reactions (see the discussion on chemically amplified resists below).

It is not common to select photoresists for electron-beam exposure. Electron beam lithography usually relies on resists dedicated specifically to electron-beam exposure.

DNQ-Novolac photoresist

One very common positive photoresist used with the I, G and H-lines from a mercury-vapor lamp is based on a mixture of diazonaphthoquinone (DNQ) and novolac resin (a phenol formaldehyde resin). DNQ inhibits the dissolution of the novolac resin, but upon exposure to light, the dissolution rate increases even beyond that of pure novolac. The mechanism by which unexposed DNQ inhibits novolac dissolution is not well understood, but is believed to be related to hydrogen bonding (or more exactly diazocoupling in the unexposed region). DNQ-novolac resists are developed by dissolution in a basic solution (usually 0.26N tetramethylammonium hydroxide (TMAH) in water).

Negative photoresist

Contrary to past types, current negative photoresists tend to exhibit better adhesion to various substrates such as Si, GaAs, InP and glass, as well as metals, including Au, Cu and Al, compared to positive-tone photoresists. Additionally, the current generation of G, H and I-line negative-tone photoresists exhibit higher temperature resistance over positive resists.

One very common negative photoresist is based on epoxy-based polymer. The common product name is SU-8 photoresist, and it was originally invented by IBM, but is now sold by Microchem and Gersteltec. One unique property of SU-8 is that it is very difficult to strip. As such, it is often used in applications where a permanent resist pattern (one that is not strippable, and can even be used in harsh temperature and pressure environments) is needed for a device.[9]

DUV photoresist

Deep ultraviolet (DUV) resists are typically polyhydroxystyrene-based polymers with a photoacid generator providing the solubility change. However, this material does not experience the diazocoupling. The combined benzene-chromophore and DNQ-novolac absorption mechanisms lead to stronger absorption by DNQ-novolac photoresists in the DUV, requiring a much larger amount of light for sufficient exposure. The strong DUV absorption results in diminished photoresist sensitivity.

Chemical amplification

Photoresists used in production for DUV and shorter wavelengths require the use of **chemical amplification** to increase the sensitivity to the exposure energy. This is done in order to combat the larger absorption at shorter wavelengths. Chemical amplification is also often used in electron-beam exposures to increase the sensitivity to the exposure dose. In the process, acids released by the exposure radiation diffuse during the post-exposure bake step. These acids render surrounding polymer soluble in developer. A single acid molecule can catalyze many such 'deprotection' reactions; hence, fewer photons or electrons are needed.[10] Acid diffusion is important not only to increase photoresist sensitivity and throughput, but also to limit line edge roughness due to shot noise statistics.[11] However, the acid diffusion length is itself a potential resolution limiter. In addition, too much diffusion reduces chemical contrast, leading again to more roughness.[11]

The following reactions are an example of commercial chemically amplified photoresists in use today:

- photoacid generator + hν (193 nm) → acid cation + sulfonate anion [12]
- sulfonate anion + hν (193 nm) → e^- + sulfonate[13]
- e^- + photoacid generator → e^- + acid cation + sulfonate anion [12]

The e^- represents a solvated electron, or a freed electron that may react with other constituents of the solution. It typically travels a distance on the order of many nanometers before being contained;[14][15] such a large travel distance is consistent with the release of electrons through thick oxide in UV EPROM in response to ultraviolet light. This parasitic exposure would degrade the resolution of the photoresist; for 193 nm the optical resolution is the limiting factor anyway, but for electron beam lithography or EUVL it is the electron range that determines the resolution rather than the optics.

Some common photoresists

Dan Daly states that Shipley, acquired by Rohm and Haas, and Hoechst, now called AZ Electronic Materials, are two producers of microelectronic chemicals. Common products include Hoechst AZ 4620, Hoechst AZ 4562, Shipley 1400-17, Shipley 1400-27, Shipley 1400-37, and Shipley Microposit Developer. The resists mentioned are, generally, applied in a relatively thick layer—approximately 120 nm to 10 μm—and are used in the manufacture of microlens arrays. Microelectronic resists, presumably, utilize specialized products depending upon process objectives and design constraints. The general mechanism of exposure for these photoresists proceeds with the decomposition of diazoquinone, i.e. the evolution of nitrogen gas and the production of carbenes.

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External links

- A list of some commercially available photoresists (http://www.smartfabgroup.com/photoresists.php)

Stepper

A **stepper** is a device used in the manufacture of integrated circuits (ICs) that is similar in operation to a slide projector or a photographic enlarger. Steppers are an essential part of the complex process, called photolithography, that creates millions of microscopic circuit elements on the surface of tiny chips of silicon. These chips form the heart of ICs such as computer processors, memory chips, and many other devices.

An i-line stepper at Cornell NanoScale Science and Technology Facility. (Photo taken under inactinic light.

The stepper's role in photolithography

Elements of the circuit to be created on the IC are reproduced in a pattern of transparent and opaque areas on the surface of a quartz plate called a photomask or reticle. The stepper passes light through the reticle, forming an image of the reticle pattern. The image is focused and reduced by a lens, and projected onto the surface of a silicon wafer that is coated with a photosensitive material called photoresist.

After exposure in the stepper, the coated wafer is developed like photographic film, causing the photoresist to dissolve in certain areas according to the amount of light the areas received during exposure. These areas of photoresist and no photoresist reproduce the pattern on the reticle. The developed wafer is then exposed to acids or other chemicals. The acid etches away the silicon in the parts of the wafer that are no longer protected by the photoresist coating. The other chemicals are used to change the electrical characteristics of the silicon in the bare areas. The wafer is then cleaned, recoated with photoresist, then passed through the stepper again in a process that creates the circuit on the silicon, layer by layer. The entire process is called photolithography or photo engineering.

When the wafer is processed in the stepper, the pattern on the reticle (which may contain a number of individual chip patterns) is exposed repeatedly across the surface of the wafer in a grid. The stepper gets its name from the fact that it moves or "steps" the wafer from one shot location to another. This is accomplished by moving the wafer back and forth and left and right under the lens of the stepper. Previous generations of photolithographic equipment would expose the entire wafer, all at once; a stepper, working on a limited area, is capable of higher resolution.

As of 2008, the most detailed patterns in semiconductor device fabrication are transferred using a type of stepper called a scanner, which moves the wafer and reticle with respect to each other during the exposure, as a way of increasing the size of the exposed area and increasing the imaging performance of the lens.

Basic operation

The silicon wafers are coated with photoresist, and placed in a cassette or "boat" that holds a number of wafers. This is then placed in a part of the stepper called the **wafer loader**, usually located at the lower front of the stepper.

A robot in the wafer loader picks up one of the wafers from the cassette and loads it onto the **wafer stage** where it is aligned to enable another, finer alignment process that will occur later on.

The pattern of the circuitry for each chip is contained in a pattern etched in chrome on the reticle, which is a plate of transparent quartz. A typical reticle used in steppers is 6 inches square and has a usable area of 104mm by 132mm.

A variety of reticles, each appropriate for one stage in the process, are contained in a rack in the **reticle loader**, usually located at the upper front of the stepper. Before the wafer is exposed a reticle is loaded onto the **reticle stage** by a robot, where it is also very precisely aligned. Since the same reticle can be used to expose many wafers, it is loaded once before a series of wafers is exposed, and is realigned periodically.

Once the wafer and reticle are in place and aligned, the wafer stage, which is moved very precisely in the X and Y directions (front to back and left to right) by worm screws or linear motors, carries the wafer so that the first of the many patterns (or "shots") to be exposed on it is located below the lens, directly under the reticle.

Although the wafer is aligned after it is placed on the wafer stage, this alignment is not sufficient to ensure that the layer of circuitry to be printed onto the wafer exactly overlays previous layers already there. Therefore each shot is aligned using special alignment marks that are located in the pattern for each final IC chip. Once this fine alignment is completed, the shot is exposed by light from the stepper's **illumination system** that passes through the reticle, through a **reduction lens**, and on to the surface of the wafer. A process program or "recipe" determines the length of the exposure, the reticle used, as well as other factors that affect the exposure.

Each shot located in a grid pattern on the wafer and is exposed in turn as the wafer is stepped back and forth under the lens. When all shots on the wafer are exposed, the wafer is unloaded by the wafer loader robot, and another wafer takes its place on the stage. The exposed wafer is eventually moved to a developer where the photoresist on its surface is exposed to developing chemicals that wash away areas of the photoresist, based on whether or not they were exposed to the light passing through the reticle. The developed surface is then subjected to other processes of photolithography.

Major subassemblies

A typical stepper has the following subassemblies: wafer loader, wafer stage, wafer alignment system, reticle loader, reticle stage, reticle alignment system, reduction lens, and illumination system. Process programs for each layer printed on the wafer are executed by a control system centering on a computer that stores the process program, reads it, and communicates with the various subassemblies of the stepper in carrying out the program's instructions. The components of the stepper are contained in a sealed chamber that is maintained at a precise temperature to prevent distortions in the printed patterns that might be caused by expansion or contraction of the wafer due to temperature variations. The chamber also contains other systems that support the process, such as air conditioning, power supplies, control boards for the various electrical components, and others.

Illumination and the challenges of improving resolution

The greatest limitation on the ability to produce increasingly finer lines on the surface of the wafer has been the wavelength of the light used in the exposure system. As the required lines have become narrower and narrower, illumination sources producing light with progressively shorter wavelengths have been put into service in steppers and scanners.

The ability of an exposure system, such as a stepper, to resolve narrow lines is limited by the wavelength of the light used for illumination, the ability of the lens to capture light (or actually orders of diffraction) coming at increasingly wider angles (called numerical aperture or N.A.), and various improvements in the process itself. This is expressed by the following equation:

$$\mathrm{CD} = k\frac{\lambda}{\mathrm{NA}}$$

CD is the critical dimension, or finest line resolvable, k is a coefficient expressing process-related factors, λ is the wavelength of the light, and NA is the numerical aperture. Decreasing the wavelength of the light in the illumination system increases the resolving power of the stepper.

Twenty years ago, the ultraviolet "g-line" (436 nm) of the mercury spectrum was used to create lines in the 750 nm range in steppers that employed mercury lamps as their illumination source. Several years later systems employing the "i-line" (365 nm) from mercury lamps were introduced to create lines as low as 350 nm. As the desired line widths approached and eventually became narrower than the wavelength of the light used to create them, a variety of resolution enhancement techniques were developed to make this possible, such as phase shifting reticles and various techniques for manipulating the angles of the exposure light in order to maximize the resolving power of the lens.

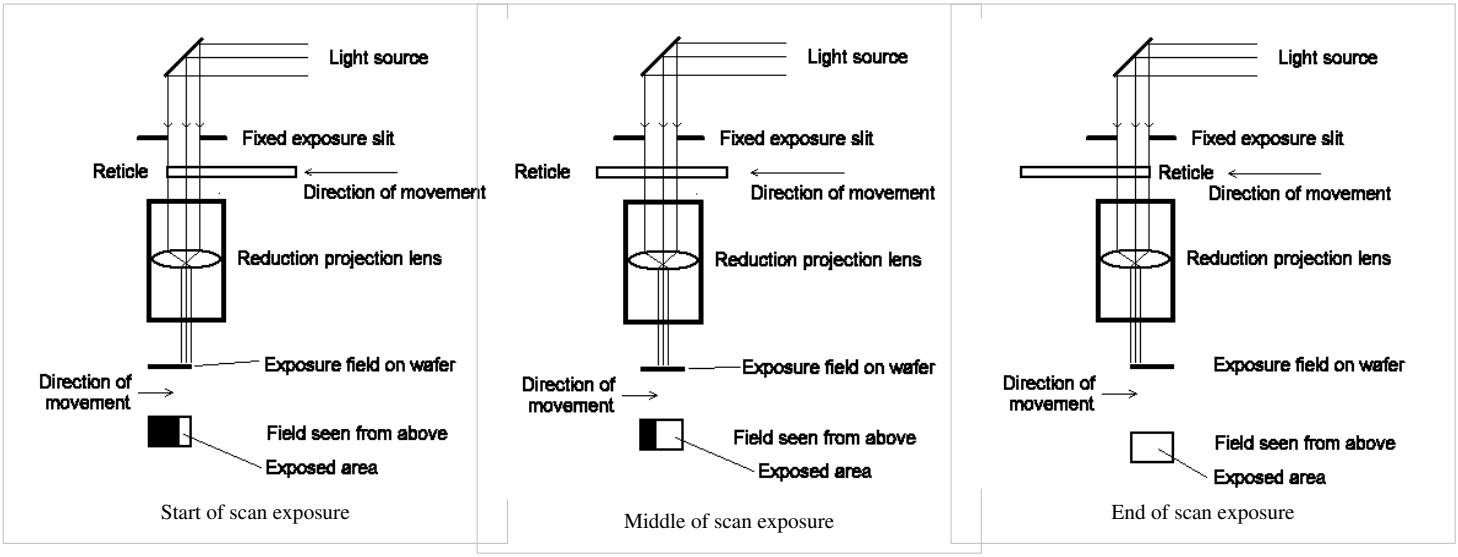
Eventually however, the desired line widths became narrower than what was possible using mercury lamps, and near the middle of the last decade, the semiconductor industry moved towards steppers that employed krypton-fluoride (KrF) excimer lasers producing 248 nm light. Such systems are currently being used to produce lines in the 110 nm range. Lines as low as 32 nm are being resolved by production-capable steppers using argon-fluoride (ArF) excimer lasers that emit light with a wavelength of 193 nm. Although fluoride (F2) lasers are available that produce 157 nm light, they are not practical because of their low power and because they quickly degrade the materials used to make the lenses in the stepper.

Since practical light sources with wavelengths narrower than these lasers have not been available, manufacturers have sought to improve resolution by reducing the process coefficient k. This is done by further improving techniques for manipulating the light as it passes through the illumination system and the reticle, as well as improving techniques for processing the wafer before and after exposure. Manufacturers have also introduced ever larger and more expensive lenses as a means of increasing the numerical aperture. However, these techniques are approaching their practical limit, and line widths in the 45 nm range appear to be near the best that can be achieved with conventional design.

Ultimately, other sources of illumination will have to be put to use, such as electron beams, x-rays or similar sources of electromagnetic energy with wavelengths much shorter than visible light. However, in order to delay as long as possible the vast expense and difficulty of adopting a whole new type of illumination technology, manufacturers have turned to a technique, previously used in microscopes, for increasing the numerical aperture of the lens by allowing the light to pass through water instead of air. This method, called immersion lithography, is the current cutting edge of practical production technology. It works because numerical aperture is a function of the maximum angle of light that can enter the lens and the refractive index of the medium through which the light passes. When water is employed as the medium, it greatly increases numerical aperture, since it has a refractive index of 1.44 at 193 nm, while air has an index of 1. Current production machines employing this technology are capable of resolving lines in the 32 nm range,[1] and may eventually be able to achieve lines of 30 nm.

Scanners

Modern scanners are steppers that increase the length of the area exposed in each shot (the exposure field) by moving the reticle stage and wafer stage in opposite directions to each other during the exposure. Instead of exposing the entire field at once, the exposure is made through an "exposure slit" that is as wide as the exposure field, but only a fraction of its length (such as a 9x25 mm slit for a 35x25 mm field). The image from the exposure slit is scanned across the exposure area.



There are several benefits to this technique. The field can be exposed with a lesser reduction of size from the reticle to the wafer (such as 4x reduction on a scanner, compared with 5x reduction on a stepper), while allowing a field size much larger than that which can be exposed with a typical stepper. Also the optical properties of the projection lens can be optimized in the area through which the image of the projection slit passes, while optical aberrations can be ignored outside of this area, because they will not affect the exposed area on the wafer.

Successful scanning requires extremely precise synchronization between the moving reticle and wafer stages during the exposure. Accomplishing this presents many technological challenges.

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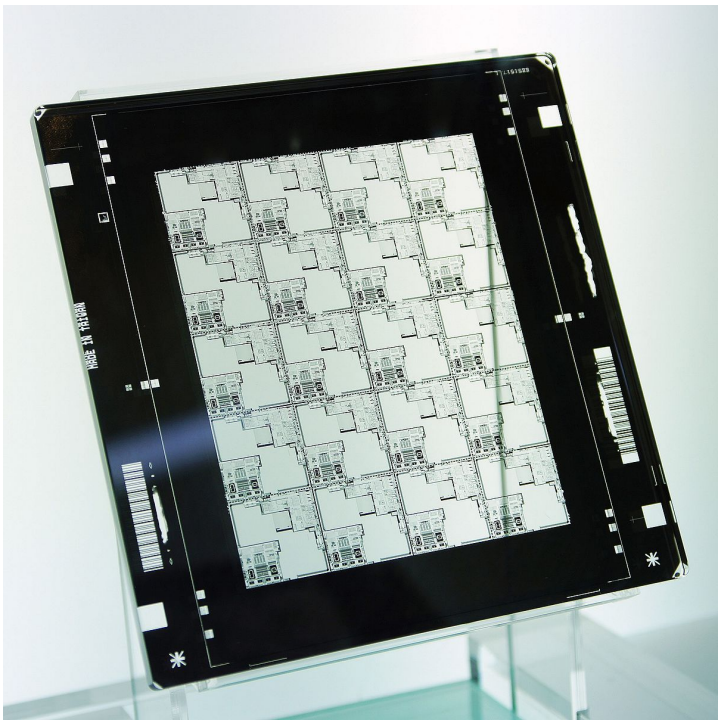
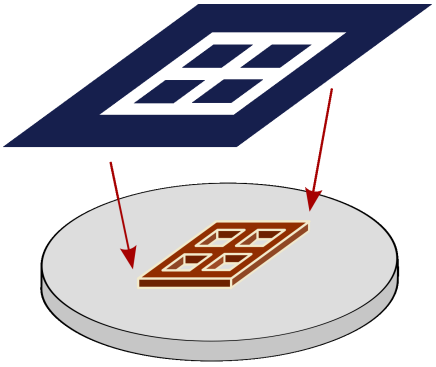
Photomask

A **photomask** is an opaque plate with holes or transparencies that allow light to shine through in a defined pattern. They are commonly used in photolithography.

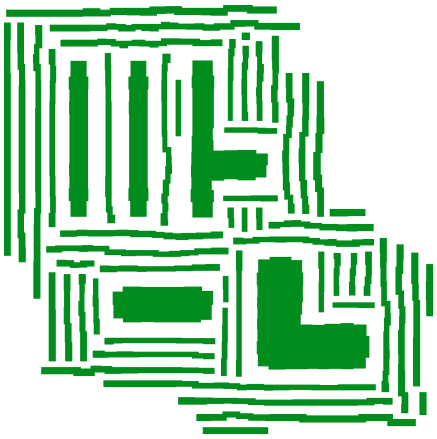


a photomask



A schematic illustration of a photomask (top) and an integrated circuit created using that mask (bottom).

Overview



The above is an actual photomask. The thicker lines are the integrated circuit that is desired to be printed on the wafer. The thinner lines are assists that do not print themselves, but help the integrated circuit print better out-of-focus. The zig-zag appearance of the photomask is because optical proximity correction was applied to it to create a better print.

Lithographic photomasks are typically transparent fused silica blanks covered with a pattern defined with a chrome metal-absorbing film. Photomasks are used at wavelengths of 365 nm, 248 nm, and 193 nm. Photomasks have also been developed for other forms of radiation such as 157 nm, 13.5 nm (EUV), X-ray, electrons, and ions; but these require entirely new materials for the substrate and the pattern film.

A set of photomasks, each defining a pattern layer in integrated circuit fabrication, is fed into a photolithography stepper or scanner, and individually selected for exposure. In double patterning techniques, a photomask would correspond to a subset of the layer pattern.

In photolithography for the mass production of integrated circuit devices, the more correct term is usually **photoreticle** or simply **reticle**. In the case of a photomask, there is a one-to-one correspondence between the mask pattern and the wafer pattern. This was the standard for the 1:1 mask aligners that were succeeded by steppers and scanners with reduction optics. As used in steppers and scanners, the reticle commonly contains only one layer of the chip. (However, some photolithography fabrications utilize reticles with more than one layer patterned onto the same mask). The pattern is projected and shrunk by four or five times onto the wafer surface. To achieve complete wafer coverage, the wafer is repeatedly "stepped" from position to position under the optical column until full exposure is achieved.

Features 150 nm or below in size generally require phase-shifting to enhance the image quality to acceptable values. This can be achieved in many ways. The two most common methods are to use an attenuated phase-shifting background film on the mask to increase the contrast of small intensity peaks, or to etch the exposed quartz so that the edge between the etched and unetched areas can be used to image nearly zero intensity. In the second case, unwanted edges would need to be trimmed out with another exposure. The former method is *attenuated phase-shifting*, and is often considered a weak enhancement, requiring special illumination for the most enhancement, while the latter method is known as *alternating-aperture phase-shifting*, and is the most popular strong enhancement technique.

As leading-edge semiconductor features shrink, photomask features that are 4× larger must inevitably shrink as well. This could pose challenges since the absorber film will need to become thinner, and hence less opaque.[1] A recent study by IMEC has found that thinner absorbers degrade image contrast and therefore contribute to line-edge roughness, using state-of-the-art photolithography tools.[2] One possibility is to eliminate absorbers altogether and use "chromeless" masks, relying solely on phase-shifting for imaging.

The emergence of immersion lithography has a strong impact on photomask requirements. The commonly used attenuated phase-shifting mask is more sensitive to the higher incidence angles applied in "hyper-NA" lithography, due to the longer optical path through the patterned film.[3]

Mask Error Enhancement Factor

Leading-edge photomasks (pre-corrected) images of the final chip patterns magnified by 4 times. This magnification factor has been a key benefit in reducing pattern sensitivity to imaging errors. However, as features continue to shrink, two trends come into play: the first is that the mask error factor begins to exceed one, i.e., the dimension error on the wafer may be more than 1/4 the dimension error on the mask,[4] and the second is that the mask feature is becoming smaller, and the dimension tolerance is approaching a few nanometers. For example, a 25 nm wafer pattern should correspond to a 100 nm mask pattern, but the wafer tolerance could be 1.25 nm (5% spec), which translates into 5 nm on the photomask. The variation of electron beam scattering in directly writing the photomask pattern can easily well exceed this.[5][6]

Pellicles

Particle contamination can be a significant problem in semiconductor manufacturing. A photomask is protected from particles by a pellicle – a thin transparent film stretched over a frame that is glued over one side of the photomask. The pellicle is far enough away from the mask patterns so that moderate-to-small sized particles that land on the pellicle will be too far out of focus to print. Although they are designed to keep particles away, pellicles become a part of the imaging system and their optical properties need to be taken into account.[7]

Leading commercial photomask manufacturers

The SPIE Annual Conference, Photomask Technology reports the SEMATECH Mask Industry Assessment which includes current industry analysis and the results of their annual photomask manufacturers survey. The following companies are listed in order of their global market share (2009 info):[8]

- Infinite Graphics Incorporated
- Dai Nippon Printing
- Toppan Photomasks
- Photronics Inc
- Hoya Corporation
- Taiwan Mask Corporation
- Compugraphics Photomask Solutions
- Nippon Filcon

Major chipmakers such as Intel, Globalfoundries, IBM, NEC, TSMC, Samsung, and Micron Technology, have their own large maskmaking facilities or joint ventures with the abovementioned companies.

The cost to set up a modern 45 nm process mask shop is $200–500 million, a very high threshold for entering this market. The purchase price of a photomask can range from $1,000 to $100,000 for a single high-end phase-shift mask. As many as 30 masks (of varying price) may be required to form a complete mask set.

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Plasma ashing

In semiconductor manufacturing **plasma ashing** is the process of removing the photoresist from an etched wafer. Using a plasma source, a monatomic reactive species is generated. Oxygen or fluorine are the most common reactive species. The reactive species combines with the photoresist to form ash which is removed with a vacuum pump.

Typically, monatomic (single atom) oxygen plasma is created by exposing oxygen gas at a low pressure (O_2) to high power radio waves, which ionise it. This process is done under vacuum in order to create a plasma. As the plasma is formed, many free radicals are created which could damage the wafer. Newer, smaller circuitry is increasingly susceptible to these particles. Originally, plasma was generated in the process chamber, but as the need to get rid of free radicals has increased, many machines now use a downstream plasma configuration, where plasma is formed remotely and the desired particles are channeled to the wafer. This allows electrically charged particles time to recombine before they reach the wafer surface, and prevents damage to the wafer surface.

Two forms of **plasma ashing** are typically performed on wafers. High temperature ashing, or stripping, is performed to remove as much photo resist as possible, while the "descum" process is used to remove residual photo resist in trenches. The main difference between the two processes is the temperature the wafer is exposed to while in an ashing chamber.

Monatomic oxygen is electrically neutral and although it does recombine during the channeling, it does so at a slower rate than the positively or negatively charged free radicals, which attract one another. This means that when all of the free radicals have recombined, there is still a portion of the active species available for process. Because a large portion of the active species is lost to recombination, process times may take longer. To some extent, these longer process times can be mitigated by increasing the temperature of the reaction area.

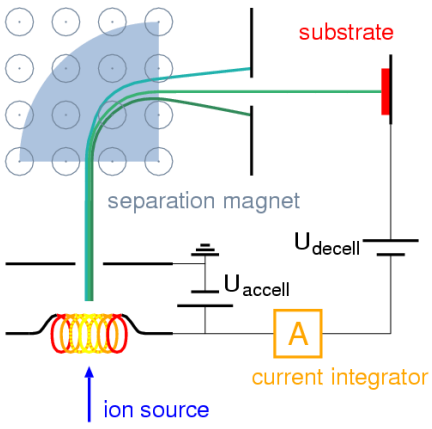
Ion implantation

Ion implantation is a materials engineering process by which ions of a material are accelerated in an electrical field and impacted into a solid. This process is used to change the physical, chemical, or electrical properties of the solid. Ion implantation is used in semiconductor device fabrication and in metal finishing, as well as various applications in materials science research. The ions alter the elemental composition of the target, if the ions differ in composition from the target, stop in the target and stay there. They also cause much chemical and physical change in the target by transferring their energy and momentum to the electrons and atomic nuclei of the target material. This causes a structural change, in that the crystal structure of the target can be damaged or even destroyed by the energetic collision cascades. Because the ions have masses comparable to those of the target atoms, they knock the target atoms out of place more than electron beams do. If the ion energy is sufficiently high (usually tens of MeV) to overcome the coulomb barrier, there can even be a small amount of nuclear transmutation.

An ion implantation system at LAAS technological facility in Toulouse, France.

General principle

Ion implantation equipment typically consists of an ion source, where ions of the desired element are produced, an accelerator, where the ions are electrostatically accelerated to a high energy, and a target chamber, where the ions impinge on a target, which is the material to be implanted. Thus ion implantation is a special case of particle radiation. Each ion is typically a single atom or molecule, and thus the actual amount of material implanted in the target is the integral over time of the ion current. This amount is called the dose. The currents supplied by implanters are typically small (microamperes), and thus the dose which can be implanted in a reasonable amount of time is small. Therefore, ion implantation finds application in cases where the amount of chemical change required is small.



Ion implantation setup with mass separator

Typical ion energies are in the range of 10 to 500 keV (1,600 to 80,000 aJ). Energies in the range 1 to 10 keV (160 to 1,600 aJ) can be used, but result in a penetration of only a few nanometers or less. Energies lower than this result in

very little damage to the target, and fall under the designation ion beam deposition. Higher energies can also be used: accelerators capable of 5 MeV (800,000 aJ) are common. However, there is often great structural damage to the target, and because the depth distribution is broad (Bragg peak), the net composition change at any point in the target will be small.

The energy of the ions, as well as the ion species and the composition of the target determine the depth of penetration of the ions in the solid: A monoenergetic ion beam will generally have a broad depth distribution. The average penetration depth is called the range of the ions. Under typical circumstances ion ranges will be between 10 nanometers and 1 micrometer. Thus, ion implantation is especially useful in cases where the chemical or structural change is desired to be near the surface of the target. Ions gradually lose their energy as they travel through the solid, both from occasional collisions with target atoms (which cause abrupt energy transfers) and from a mild drag from overlap of electron orbitals, which is a continuous process. The loss of ion energy in the target is called stopping and can be simulated with the binary collision approximation method.

Application in semiconductor device fabrication

Doping

The introduction of dopants in a semiconductor is the most common application of ion implantation. Dopant ions such as boron, phosphorus or arsenic are generally created from a gas source, so that the purity of the source can be very high. These gases tend to be very hazardous. When implanted in a semiconductor, each dopant atom can create a charge carrier in the semiconductor after annealing. A hole can be created for a p-type dopant, and an electron for an n-type dopant. This modifies the conductivity of the semiconductor in its vicinity. The technique is used, for example, for adjusting the threshold of a MOSFET.

Ion implantation was developed as a method of producing the p-n junction of photovoltaic devices in the late 1970s and early 1980s,[1] along with the use of pulsed-electron beam for rapid annealing,[2] although it has not to date been used for commercial production.

Silicon on insulator

One prominent method for preparing silicon on insulator (SOI) substrates from conventional silicon substrates is the *SIMOX* (**S**eparation by **IM**plantation of **OX**ygen) process, wherein a buried high dose oxygen implant is converted to silicon oxide by a high temperature annealing process.

Mesotaxy

Mesotaxy is the term for the growth of a crystallographically matching phase underneath the surface of the host crystal (compare to epitaxy, which is the growth of the matching phase on the surface of a substrate). In this process, ions are implanted at a high enough energy and dose into a material to create a layer of a second phase, and the temperature is controlled so that the crystal structure of the target is not destroyed. The crystal orientation of the layer can be engineered to match that of the target, even though the exact crystal structure and lattice constant may be very different. For example, after the implantation of nickel ions into a silicon wafer, a layer of nickel silicide can be grown in which the crystal orientation of the silicide matches that of the silicon.

Application in metal finishing

Tool steel toughening

Nitrogen or other ions can be implanted into a tool steel target (drill bits, for example). The structural change caused by the implantation produces a surface compression in the steel, which prevents crack propagation and thus makes the material more resistant to fracture. The chemical change can also make the tool more resistant to corrosion.

Surface finishing

In some applications, for example prosthetic devices such as artificial joints, it is desired to have surfaces very resistant to both chemical corrosion and wear due to friction. Ion implantation is used in such cases to engineer the surfaces of such devices for more reliable performance. As in the case of tool steels, the surface modification caused by ion implantation includes both a surface compression which prevents crack propagation and an alloying of the surface to make it more chemically resistant to corrosion.

Other applications

Ion beam mixing

Ion implantation can be used to achieve ion beam mixing, i.e. mixing up atoms of different elements at an interface. This may be useful for achieving graded interfaces or strengthening adhesion between layers of immiscible materials.

Problems with ion implantation

Crystallographic damage

Each individual ion produces many point defects in the target crystal on impact such as vacancies and interstitials. Vacancies are crystal lattice points unoccupied by an atom: in this case the ion collides with a target atom, resulting in transfer of a significant amount of energy to the target atom such that it leaves its crystal site. This target atom then itself becomes a projectile in the solid, and can cause successive collision events. Interstitials result when such atoms (or the original ion itself) come to rest in the solid, but find no vacant space in the lattice to reside. These point defects can migrate and cluster with each other, resulting in dislocation loops and other defects.

Damage recovery

Because ion implantation causes damage to the crystal structure of the target which is often unwanted, ion implantation processing is often followed by a thermal annealing. This can be referred to as damage recovery.

Amorphization

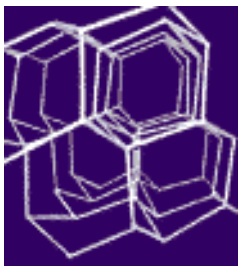
The amount of crystallographic damage can be enough to completely amorphize the surface of the target: i.e. it can become an amorphous solid (such a solid produced from a melt is called a glass). In some cases, complete amorphization of a target is preferable to a highly defective crystal: An amorphized film can be regrown at a lower temperature than required to anneal a highly damaged crystal.

Sputtering

Some of the collision events result in atoms being ejected (sputtered) from the surface, and thus ion implantation will slowly etch away a surface. The effect is only appreciable for very large doses.

Ion channelling

If there is a crystallographic structure to the target, and especially in semiconductor substrates where the crystal structure is more open, particular crystallographic directions offer much lower stopping than other directions. The result is that the range of an ion can be much longer if the ion travels exactly along a particular direction, for example the <110> direction in silicon and other diamond cubic materials. This effect is called *ion channelling*, and, like all the channelling effects, is highly nonlinear, with small variations from perfect orientation resulting in extreme differences in implantation depth. For this reason, most implantation is carried out a few degrees off-axis, where tiny alignment errors will have more predictable effects.



A diamond cubic crystal viewed from the <110> direction, showing hexagonal ion channels.

Ion channelling can be used directly in Rutherford backscattering and related techniques as an analytical method to determine the amount and depth profile of damage in crystalline thin film materials.

Hazardous Materials Note

In the ion implantation semiconductor fabrication process of wafers, it is important for the workers to minimize their exposure to the toxic materials are used in the ion implanter process. Such hazardous elements, solid source and gasses are used, such as arsine and phosphine. For this reason, the semiconductor fabrication facilities are highly automated, and may feature negative pressure gas bottles safe delivery system (SDS). Other elements may include antimony, arsenic, phosphorus, and boron. Residue of these elements show up when the machine is opened to atmosphere, and can also be accumulated and found concentrated in the vacuum pumps hardware. It is important not to expose yourself to these carcinogenic, corrosive, flammable, and toxic elements. Many overlapping safety protocols must be used when handling these deadly compounds. Use safety, and read MSDSs.

High Voltage Safety

High voltage power supplies in ion implantation equipment can pose a risk of electrocution. In addition, high-energy atomic collisions can generate X-rays and, in some cases, other ionizing radiation and radionuclides. Operators and maintenance personnel should learn and follow the safety advice of the manufacturer and/or the institution responsible for the equipment. Prior to entry to high voltage area, terminal components must be grounded using a grounding stick. Next, power supplies should be locked in the off state and tagged to prevent unauthorized energizing.

Other types of particle accelerator, such as radio frequency linear particle accelerators and laser wakefield plasma accelerators have their own hazards.

Manufacturers of Ion Implantation Equipment

- Advanced Ion Beam Technology [3]
- Axcelis Technologies [4]
- Complete Ions [5]
- Facilitation Centre for Industrial Plasma Technologies [6]
- Global Technologies, R&D equipment and Service [7]
- Ion Beam Services [8]
- Nissin Ion Equipment [9]
- SemEquip [10]
- SEN Corporation [11]
- Tokyo Electron Limited [12]
- Ulvac Technologies [13]
- Varian Semiconductor Equipment [14]

References

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[2] G. Landis et al., "Apparatus and Technique for Pulsed Electron Beam Annealing for Solar Cell Production," *Proc. 15th IEEE Photovoltaic Specialists Conf.,* Orlando FL; 976-980 (1981).

[3] http://www.aibt-inc.com

[4] http://www.axcelis.com

[5] http://www.completeions.com

[6] http://www.plasmaindia.com

[7] http://www.global-technologies.fr

[8] http://www.ion-beam-services.com

[9] http://www.nissin-ion.co.jp

[10] http://www.semequip.com

[11] http://www.senova.co.jp/english/index.html

[12] http://www.tel.com/eng/about/index.htm

[13] http://www.ulvac.com

[14] http://www.vsea.com

External links

- SEMI (http://www.semi.org) -- a semiconductor standards clearinghouse and trade organization
- Ion Implantation (http://www.casetechnology.com/implant.html)
- James Ziegler's code for simulating ion implantation. (http://www.srim.org)
- (http://www.centrotherm.de)

Furnace anneal

Furnace annealing is a process used in semiconductor device fabrication which consist of heating multiple semiconductor wafers in order to affect their electrical properties. Heat treatments are designed for different effects. Wafers can be heated in order to activate dopants, change film to film or film to wafer substrate interfaces, densify deposited films, change states of grown films, repair damage from implants, move dopants or drive dopants from one film into another or from a film into the wafer substrate.

Furnace anneals may be integrated into other furnace processing steps, such as oxidations, or may be processed on their own.

Furnace anneals are performed by equipment especially built to heat semiconductor wafers. Furnaces are capable of processing lots of wafers at a time but each process can last between several hours and a day.

Increasingly, furnace anneals are being supplanted by Rapid Thermal Anneal (RTA) or Rapid Thermal Processing (RTP). The reason for this is the relatively long thermal cycles of furnaces causes dopants that are being activated, especially boron, to diffuse farther than is intended. RTP or RTA fixes this by having thermal cycles for each wafer that is of the order of minutes rather than hours for furnace anneals.

Equipment

- Koyo Thermo Systems [1] annealing furnaces for semiconductor, solar, display and electronic applications
- Kokusai [2] Vertron, Zestone, and ALDINNA

References

[1] http://www.crystec.com/kllprode.htm
[2] http://www.ksec.com

Rapid thermal processing

Rapid Thermal Processing (or **RTP**) refers to a semiconductor manufacturing process which heats silicon wafers to high temperatures (up to 1,200 °C or greater) on a timescale of several seconds or less. During cooling, however, wafer temperatures must be brought down slowly so they do not break due to thermal shock. Such rapid heating rates are often attained by high intensity lamps or lasers. These processes are used for a wide variety of applications in semiconductor manufacturing including dopant activation, thermal oxidation, metal reflow and chemical vapor deposition.

Temperature Control

One of the key challenges in rapid thermal processing is accurate measurement and control of the wafer temperature. Monitoring the ambient with a thermocouple has only recently become feasible, in that the high temperature ramp rates prevent the wafer from coming to thermal equilibrium with the process chamber. One temperature control strategy involves *in situ* pyrometry to effect real time control.Used for melting iron for welding purposes.

Rapid thermal anneal

Rapid thermal anneal (RTA) is a subset of Rapid Thermal Processing. It is a process used in semiconductor device fabrication which consists of heating a single wafer at a time in order to affect its electrical properties. Unique heat treatments are designed for different effects. Wafers can be heated in order to activate dopants, change film-to-film or film-to-wafer substrate interfaces, densify deposited films, change states of grown films, repair damage from ion implantation, move dopants or drive dopants from one film into another or from a film into the wafer substrate.

Rapid thermal anneals are performed by equipment that heats a single wafer at a time using either lamp based heating, a hot chuck, or a hot plate that a wafer is brought near. Unlike furnace anneals they are short in duration, processing each wafer in several minutes.

To achieve short time annealing time trade off is made in temperature and process uniformity, temperature measurement and control and wafer stress as well as throughput.

Recently, RTP-like processing has found applications in another rapidly growing field — solar cell fabrication. RTP-like processing, in which an increase in the temperature of the semiconductor sample is produced by the absorption of the optical flux, is now used for a host of solar cell fabrication steps, including phosphorus diffusion for N/P junction formation and impurity gettering, hydrogen diffusion for impurity and defect passivation, and formation of screen-printed contacts using Ag-ink for the front and Al-ink for back contacts, respectively.

External links

- IEEE RTP Conference Homepage [1]
- History of RTP [2]
- Semiconductor International article on RTP technology [3]
- Rapid Thermal Anneal applications and components [4]
- Equipment of RTP [5]
- [6]

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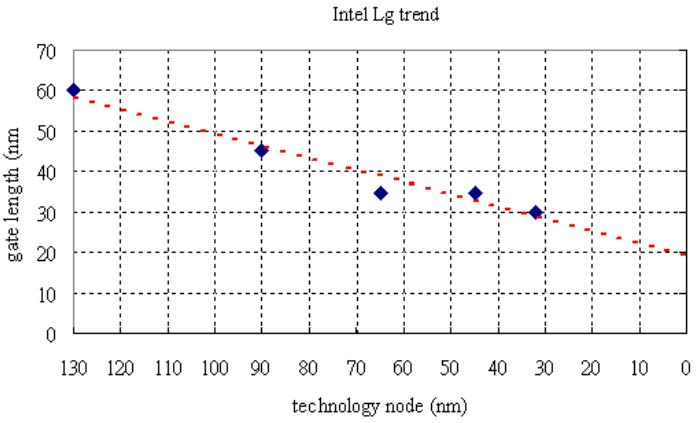
[1] http://www.ieee-rtp.org/
[2] http://www.ieee-rtp.org/archiv/rtp_history.pdf
[3] http://www.reed-electronics.com/semiconductor/article/CA338200
[4] http://www.articleworld.org/index.php/Rapid_thermal_anneal
[5] http://www.allwin21.com/
[6] http://www.allwin21.com/upload/image/AccuThermo.gif

Front end of line

The **front-end-of-line** (**FEOL**) is the first portion of IC fabrication where the individual devices (transistors, capacitors, resistors, etc.) are patterned in the semiconductor.[1] FEOL generally covers everything up to (but not including) the deposition of metal interconnect layers.



MOSFET scaling: Trend of Intel CPU transistor gate length

FEOL contains all processes of CMOS fabrication needed to form fully isolated CMOS elements:

1. Selecting the type of wafer to be used; Chemical-mechanical planarization and cleaning of the wafer.
2. Shallow trench isolation (STI) (or LOCOS in early processes, with feature size > 0.25 μm)
3. Well formation
4. Gate module formation
5. Source and drain module formation

References

[1] Karen A. Reinhardt and Werner Kern (2008). *Handbook of Silicon Wafer Cleaning Technology* (http://books.google.com/books?id=UPaD8JUCKr0C&pg=PA202) (2nd ed.). William Andrew. p. 202. ISBN 978-0-8155-1554-8. .

Further reading

- "CMOS: Circuit Design, Layout, and Simulation" Wiley-IEEE, 2010. ISBN 978-0-470-88132-3. pages 177-178 (http://books.google.com/books?id=kxYhNrOKuJQC&pg=PA177&dq=FEOL) (Chapter 7.2 CMOS Process Integration); pages 180-199 (7.2.1 Frontend-of-the-line integration)

Back end of line

The **back end of line** (**BEOL**) is the second portion of IC fabrication where the individual devices (transistors, capacitors, resistors, etc.) get interconnected with wiring on the wafer.[1] BEOL generally begins when the first layer of metal is deposited on the wafer. BEOL includes contacts, insulating layers (dielectrics), metal levels, and bonding sites for chip-to-package connections.

After the last FEOL step, there is a wafer with isolated transistors (without any wires). In BEOL part of fabrication stage contacts (pads), interconnect wires, vias and dielectric structures are formed. For modern IC process, more than 10 metal layers can be added in the BEOL.

The process used to form DRAM capacitors creates a rough and hilly surface, which makes it difficult to add metal interconnect layers and still maintain good yield. In 1998, state-of-the-art DRAM processes had 4 metal layers, while state-of-the-art logic processes had 7 metal layers. [2]

As of 2002, 5 or 6 layers of metal interconnect are common.[3]

As of 2009, typical DRAM devices (1 Gbit) use 3 layers of metal interconnect, tungsten on the first layer and aluminum on the higher layers.[4][5]

As of 2011, many gate arrays are available with a 3-layer interconnect.[6] Many power ICs and analog ICs use a 3-layer interconnect.[7]

The top-most layers of a chip have the thickest and widest and most widely-separated metal layers, which make the wires on those layers have the least resistance and smallest RC time delay, so they are used for power distribution and clock distribution. The bottom-most metal layers of the chip, closest to the transistors, have thin, narrow, tightly-packed wires, used only for local interconnect. Adding layers can potentially improve performance, but adding layers also reduces yield and increases manufacturing cost. [8]

All the chips decoded by the Visual6502 project have only one or two metal layers, including the RCA 1802, the 6800, the 6502, the 8086, the 6809, the 68000, etc.[9]

Many microprocessors were designed with two metal interconnect layers, both of them aluminum, including the 1987 CVAX and the 1989 Rigel.

Many high-performance microprocessors were designed with 3 metal interconnect layers, all of them aluminum. Those included several processors using the CMOS-3 process, including the 1992 Alpha 21064; and processors using the CMOS-6 process, including the 1996 StrongARM.

The AMD Athlon Thunderbird has 6 interconnect layers, the AMD Athlon Palomino has 7 interconnect layers, the AMD Athlon Thoroughbred A has 8 interconnect layers, and the AMD Athlon Thoroughbred B has 9 interconnect layers.[10] The Intel Xeon Dunnington has nine copper interconnect layers.[11]

Steps of the BEOL:

1. Silicidation of source and drain regions and the polysilicon region.
2. Adding a dielectric (first, lower layer is Pre-Metal dielectric, PMD - to isolate metal from silicon and polysilicon), CMP processing it
3. Make holes in PMD, make a contacts in them.
4. Add metal layer 1
5. Add a second dielectric (this time it is Intra-Metal dielectric)
6. Make vias through dielectric to connect lower metal with higher metal. Vias filled by Metal CVD process.

   Repeat steps 4-6 to get all metal layers.
7. Add final passivation layer to protect the microchip

Before 1998, practically all chips used aluminum for the metal interconnection layers. [12] The four metals with the highest electrical conductivity are silver with the highest conductivity, then copper, then gold, then aluminum.

As of 2011, many commercial processes support 2 or 3 metal layers; the most layers supported on a commercial process is 11 layers, and 12 layers are expected to be supported soon.[13]

After BEOL there is a "back-end process" (also called post-fab), which is done not in the cleanroom, often by a different company. It includes wafer test, wafer backgrinding, die separation, die tests, IC packaging and final test.

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[10] Frank Völkel. "New CPUs, Old Boards: Athlon XP 2800+ Starting From KT333". 2002. (http://www.tomshardware.com/reviews/amd-travels-time,525-7.html)

[11] (http://ieeexplore.ieee.org/xpl/freeabs_all.jsp?arnumber=4977312)

[12] "Copper Interconnect Architecture" (http://www.pctechguide.com/cpu-architecture/copper-interconnect-architecture)

[13] "IC Knowledge Cost and Price Model Supported Process List" (http://www.icknowledge.com/our_products/Processes1108.pdf)

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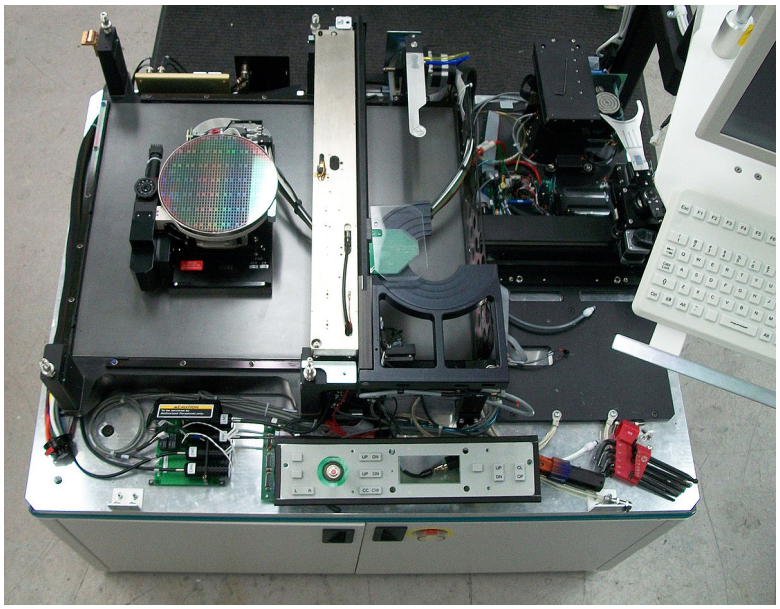
- Silicon VLSI Technology: Fundamentals, Practice, and Modeling. Prentice Hall 2000, ISBN 0-13-085037-3 Chapter 11 "Back End Technology" pages 681-786
- "CMOS: Circuit Design, Layout, and Simulation" Wiley-IEEE, 2010. ISBN 978-0-470-88132-3. (http://books.google.com/books?hl=en&lr=&id=N0XgLh2d2pkC) pages 177-179 (Chapter 7.2 CMOS Process Integration); pages 199-208 (7.2.2 Backend-of-the-line Integration)

Wafer testing

Wafer testing is a step performed during semiconductor device fabrication. During this step, performed before a wafer is sent to die preparation, all individual integrated circuits that are present on the wafer are tested for functional defects by applying special test patterns to them. The wafer testing is performed by a piece of test equipment called a wafer prober. The process of wafer testing can be referred to in several ways: Wafer Sort (WS), Wafer Final Test (WFT), Electronic Die Sort (EDS) and Circuit Probe (CP) are probably the most common. [1]

Wafer prober

A wafer prober is a machine used to test integrated circuits. For electrical testing a set of microscopic contacts or probes called a probe card are held in place whilst the wafer, vacuum-mounted on a wafer chuck, is moved into electrical contact. When a die (or array of dice) have been electrically tested the prober moves the wafer to the next die (or array) and the next test can start. The wafer prober is usually responsible for loading and unloading the wafers from their carrier (or cassette) and is equipped with automatic pattern recognition optics capable of aligning the wafer with sufficient accuracy to ensure accurate registration between the contact pads on the wafer and the tips of the probes.



8-inch semiconductor wafer prober, shown with cover panels, tester and probe card elements removed.

For today's multi-die packages such as stacked chip-scale package (SCSP) or System in Package (SiP) – the development of non-contact (RF) probes for identification of known tested die (KTD) and known good die (KGD) are critical to increasing overall system yield.

The wafer prober also exercises any test circuitry on the wafer scribe lines. Some companies get most of their information about device performance from these scribe line test structures.[2][3][4]

When all test patterns pass for a specific die, its position is remembered for later use during IC packaging. Sometimes a die has internal spare resources available for repairing (i.e. flash memory IC); if it does not pass some test patterns these spare resources can be used. If redundancy of failed die is not possible the die is considered faulty and is discarded. Non-passing circuits are typically marked with a small dot of ink in the middle of the die, or the information of passing/non-passing is stored in a file, named a wafermap. This map categorizes the passing and non-passing dies by making use of bins. A bin is then defined as a good or bad die. This wafermap is then sent to the die attachment process which then only picks up the passing circuits by selecting the bin number of good dies. The process where no ink dot is used to mark the bad dies is named substrate mapping. When ink dots are used, vision systems on subsequent die handling equipment can disqualify the die by recognizing the ink dot.

In some very specific cases, a die that passes some but not all test patterns can still be used as a product, typically with limited functionality. The most common example of this is a microprocessor for which only one part of the on-die cache memory is functional. In this case, the processor can sometimes still be sold as a lower cost part with a

smaller amount of memory and thus lower performance. Additionally when bad dies have been identified, the die from the bad bin can be used by production personnel for assembly line setup.

The contents of all test patterns and the sequence by which they are applied to an integrated circuit are called the test program.

After IC packaging, a packaged chip will be tested again during the IC testing phase, usually with the same or very similar test patterns. For this reason, one might think that wafer testing is an unnecessary, redundant step. In reality this is not usually the case, since the removal of defective dies saves the considerable cost of packaging faulty devices. However, when the production yield is so high that wafer testing is more expensive than the packaging cost of defect devices, the wafer testing step can be skipped altogether and dies will undergo blind assembly.

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[4] *Design for Manufacturability And Statistical Design: A Constructive Approach*, by Michael Orshansky, Sani Nassif, Duane Boning 2007. ISBN 0-387-30928-4 ISBN 978-0-387-30928-6 (http://books.google.com/books?id=sZ-NPuM-ScYC&pg=PA84&lpg=PA84&dq=scribe+line+test+structures&source=bl&ots=uH52TiBixk&sig=LSHJm1EkcT07D-mysd8d419NyH8&hl=en&ei=-fyLSqrbJ5PclAf99ty7CA&sa=X&oi=book_result&ct=result&resnum=10#v=onepage&q=scribe line test structures&f=false) p. 84

Wafer backgrinding

Wafer backgrinding is a semiconductor device fabrication step during which wafer thickness is reduced to allow for stacking and high density packaging of integrated circuits (IC).

ICs are being produced on semiconductor wafers that undergo a multitude of processing steps. The silicon wafers predominantly being used today have diameters of 20 and 30 cm. They are roughly 750 µm thick to ensure a minimum of mechanical stability and to avoid warping during high-temperature processing steps.

Smartcards, USB memory sticks, smartphones, handheld music players, and other ultra compact electronic products would not be feasible in their present form without minimizing the size of their various components along all dimensions. The backside of the wafers are thus ground prior to wafer dicing (where the individual microchips are being singulated). Wafers thinned down to 75 to 50 µm are common today.[1]

Prior to grinding wafers are commonly laminated with UV curable back grinding tape. UV curable back grinding tapes ensure against wafer surface damage during back grinding and prevent wafer surface contamination caused by infiltration of grinding fluid and/or debris. [2]

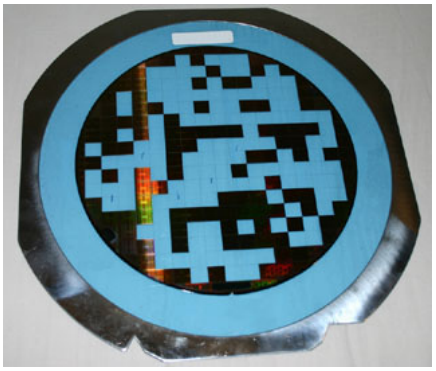
The process is also known as 'Backlap'[3] or 'Wafer thinning'.[4]

References

[1] International Technology (http://www.itrs.net) Roadmap for Semiconductors 2009 edition, page 12-53.
[2] BG Tape (http://www.lintec-usa.com/bg_hogo.cfm), by LINTEC of AMERICA
[3] Introduction to Semiconductor Technology (http://www.st.com/stonline/books/pdf/docs/5038.pdf), by ST Micro-electronics, page 6.
[4] Wafer Backgrind (http://www.siliconfareast.com/backgrind.htm) at Silicon Far East.

Die preparation

Die preparation is a step of semiconductor device fabrication during which a wafer is prepared for IC packaging and IC testing. The process of die preparation typically consists of 2 steps: wafer mounting and wafer dicing.



Wafer glued on blue tape and cut into pieces

Wafer mounting

Wafer mounting is a step that is performed during the die preparation of a wafer as part of the process of semiconductor fabrication. During this step, the wafer is mounted on a plastic tape that is attached to a ring. Wafer mounting is performed right before the wafer is cut into separate dies. The adhesive film on which the wafer is mounted ensures that the individual dies remain firmly in place during 'dicing', as the process of cutting the wafer is called.

The picture on the right shows a 300 mm wafer after it was mounted and diced. The blue plastic is the adhesive tape. The wafer is the round disc in the middle. In this case, a large number of dies were already removed.

Semiconductor-die cutting

In the manufacturing of micro-electronic devices, **die cutting**, **dicing** or **singulation** is a process of reducing a wafer containing multiple identical integrated circuits to individual dies each containing one of those circuits.

During this process, a wafer with up to thousands of circuits is cut into rectangular pieces, each called a die. In between those functional parts of the circuits, a thin non-functional spacing is foreseen where a saw can safely cut the wafer without damaging the circuits. This spacing is called *scribe line* or *saw street*. The width of the scribe is very small, typically around 100 μm. A very thin and accurate saw is therefore needed to cut the wafer into pieces. Usually the dicing is performed with a water-cooled circular saw with diamond-tipped teeth.

Types of blades

The most common make up of blade used is either a metal or resin bond containing abrasive grit of natural or more commonly synthetic diamond, or borazon in various forms. Alternatively, the bond and grit may be applied as a coating to a metal former. See diamond tools.

Further reading

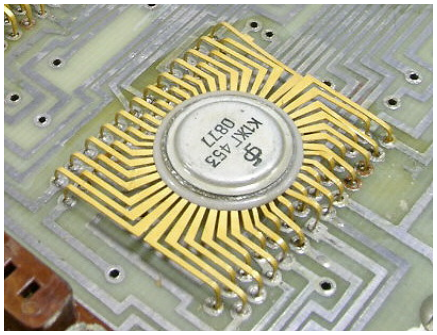
- Kaeslin, Hubert (2008), *Digital Integrated Circuit Design, from VLSI Architectures to CMOS Fabrication*, Cambridge University Press, section 11.4.

Integrated circuit packaging

In electronics manufacturing, **integrated circuit packaging** is the final stage of semiconductor device fabrication, in which the tiny block of semiconducting material is encased in a supporting case that prevents physical damage and corrosion. The case, known as a "package", supports the electrical contacts which connect the device to a circuit board.

In the integrated circuit industry it is called simply **packaging** and sometimes **semiconductor device assembly**, or simply **assembly**. Sometimes it is called **encapsulation** or **seal**. The packaging stage is followed by testing of the integrated circuit.

The term is sometimes confused with electronic packaging, which is the mounting and interconnecting of integrated circuits (and other components) onto printed-circuit boards.

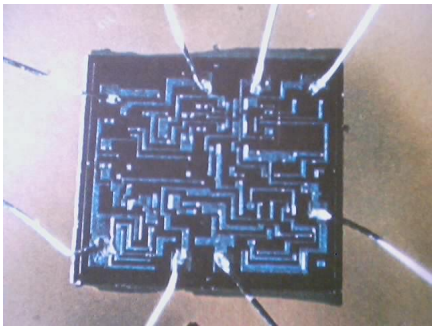


Early USSR made integrated circuit. The tiny block of semiconducting material (the "die"), is enclosed inside the round, metallic case (the "package").

Approaches

The earliest integrated circuits were packaged in ceramic flat packs, which the military used for many years for their reliability and small size. Commercial circuit packaging quickly moved to the dual in-line package (DIP), first in ceramic and later in plastic. In the 1980s VLSI pin counts exceeded the practical limit for DIP packaging, leading to pin grid array (PGA) and leadless chip carrier (LCC) packages. Surface

mount packaging appeared in the early 1980s and became popular in the late 1980s, using finer lead pitch with leads formed as either gull-wing or J-lead, as exemplified by small-outline integrated circuit — a carrier which occupies an area about 30 – 50% less than an equivalent DIP, with a typical thickness that is 70% less. This package has "gull wing" leads protruding from the two long sides and a lead spacing of 0.050 inches.



A small-scale integrated circuit die, with bond wires attached. In the **packaging** stage, the bond wires are attached to the die and connected to the external electrical contacts.

An *area array package* places the interconnection terminals on the surface area, providing a greater number of connections than where only the outer perimeter is used. The first chip package of this kind was a ceramic pin grid array.[1] The plastic ball grid array is the most commonly used.[2]

In the late 1990s, plastic quad flat pack(PQFP) and thin small-outline packages (TSOP) became the most common for high pin count devices, though PGA packages are still often used for microprocessors. Intel and AMD transitioned in the 2000s from PGA packages to land grid array (LGA) packages.

Ball grid array (BGA) packages have existed since the 1970s. Flip-chip ball grid array packages (FCBGA) developed in the 1990s allow for much higher pin count than other package types. In an FCBGA package the die is mounted upside-down (flipped) and connects to the package balls via a substrate that is similar to a printed-circuit board rather than by wires. FCBGA packages allow an array of input-output signals (called Area-I/O) to be distributed over the entire die rather than being confined to the die periphery.

Traces out of the die, through the package, and into the printed circuit board have very different electrical properties, compared to on-chip signals. They require special design techniques and need much more electric power than signals confined to the chip itself.

Stacking multiple dies in one package is called SiP, for *System In Package*, or three-dimensional integrated circuit. Combining multiple dies on a small substrate, often ceramic, is called an MCM, or Multi-Chip Module. The boundary between a big MCM and a small printed circuit board is sometimes blurry.

Operations

The following operations are performed at the stage of packaging.

Die attachment is the step during which a die is mounted and fixed to the package or support structure (header).[3] For high-powered applications, the die is usually eutectic bonded onto the package, using e.g. gold-tin or gold-silicon solder (for good heat conduction). For low-cost, low-powered applications, the die is often glued directly onto a substrate (such as a printed wiring board) using an epoxy adhesive.

- IC Bonding
  - Wire bonding
  - Thermosonic Bonding
    - Down bonding
    - Tape-automated bonding
  - Flip chip
  - Quilt packaging

  - Tab bonding
  - Film attaching
  - Spacer attaching
- IC encapsulation
  - Baking
  - Plating
  - Lasermarking
  - Trim and form
- Wafer bonding

References

[1] William J. Greig (2007). *Integrated circuit packaging, assembly and interconnections*. Springer. pp. 36–41. ISBN 0-387-28153-3.
[2] Ken Gilleo (2003). *Area array packaging processes for BGA, Flip Chip, and CSP*. McGraw-Hill Professional. p. 251. ISBN 0-07-142829-1.
[3] L. W. Turner (ed), *Electronics Engineers Reference Book*, Newnes-Butterworth, 1976, ISBN 0-408-00168-2, pages 11-34 through 11-37

External links

- wikia.com – Wikihowto on identifying chip packages (http://howto.wikia.com/wiki/Howto_identify_chip_packages)
- ivf.se – The Nordic Electronics Packaging Guideline (http://extra.ivf.se/ngl/) Investigation on the technical performance of different packaging and interconnection systems

Dry etching

Dry etching refers to the removal of material, typically a masked pattern of semiconductor material, by exposing the material to a bombardment of ions (usually a plasma of reactive gases such as fluorocarbons, oxygen, chlorine, boron trichloride; sometimes with addition of nitrogen, argon, helium and other gases) that dislodge portions of the material from the exposed surface. Unlike with many (but not all, see isotropic etching) of the wet chemical etchants used in wet etching, the dry etching process typically etches directionally or anisotropically.

Explanation

Dry etching is used in conjunction with photolithographic techniques to attack certain areas of a semiconductor surface in order to form recesses in material, such as contact holes (which are contacts to the underlying semiconductor substrate) or via holes (which are holes that are formed to provide an interconnect path between conductive layers in the layered semiconductor device) or to otherwise remove portions of semiconductor layers where predominantly vertical sides are desired. In conjunction with semiconductor manufacturing, micromachining and display production the removal of organic residues by oxygen plasmas is sometimes correctly described as a dry etch process. However, also the term plasma ashing may be used.

Dry etching is particularly useful for materials and semiconductors which are chemically resistant and could not be wet etched, such as silicon carbide or gallium nitride.

References

Dry etching is currently used in semiconductor fabrication processes due to its unique ability over wet etch to do anisotropic etching (removal of material) to create a high aspect ratio structures (e.g. deep via holes or capacitor trenches). The dry etching hardware design basically involve a vacuum chamber, special gas delivery system, RF waveform generator and an exhaust system.

Thermal oxidation

In microfabrication, **thermal oxidation** is a way to produce a thin layer of oxide (usually silicon dioxide) on the surface of a wafer. The technique forces an oxidizing agent to diffuse into the wafer at high temperature and react with it. The rate of oxide growth is often predicted by the Deal-Grove model. Thermal oxidation may be applied to different materials, but this article will only consider oxidation of silicon substrates to produce silicon dioxide.

Furnaces used for diffusion and thermal oxidation at LAAS technological facility in Toulouse, France.

The chemical reaction

Thermal oxidation of silicon is usually performed at a temperature between 800 and 1200°C, resulting in so called **High Temperature Oxide** layer (HTO). It may use either water vapor (usually UHP steam) or molecular oxygen as the oxidant; it is consequently called either *wet* or *dry* oxidation. The reaction is one of the following:

$$\mathrm{Si + 2H_2O \rightarrow SiO_2 + 2H_{2\ (g)}}$$
$$\mathrm{Si + O_2 \rightarrow SiO_2}$$

The oxidizing ambient may also contain several percent of hydrochloric acid (HCl). The chlorine removes metal ions that may occur in the oxide.

Thermal oxide incorporates silicon consumed from the substrate and oxygen supplied from the ambient. Thus, it grows both down into the wafer and up out of it. For every unit thickness of silicon consumed, 2.27 unit thicknesses of oxide will appear.[1] Conversely, if a bare silicon surface is oxidized, 44% of the oxide thickness will lie below the original surface, and 56% above it.

Deal-Grove model

According to the commonly-used Deal-Grove model, the time *t* required to grow an oxide of thickness X_o, at a constant temperature, on a bare silicon surface, is:

$$t = \frac{X_o^2}{B} + \frac{X_o}{B/A}$$

where the constants A and B encapsulate the properties of the reaction and the oxide layer, respectively.

If a wafer that already contains oxide is placed in an oxidizing ambient, this equation must be modified by adding a corrective term τ, the time that would have been required to grow the pre-existing oxide under current conditions. This term may be found using the equation for *t* above.

Solving the quadratic equation for X_o yields:

$$X_o(t) = A/2 \cdot \left[\sqrt{1 + \frac{4B}{A^2}(t+\tau)} - 1\right]$$

Oxidation technology

Most thermal oxidation is performed in furnaces, at temperatures between 800 and 1200°C. A single furnace accepts many wafers at the same time, in a specially designed quartz rack (called a "boat"). Historically, the boat entered the oxidation chamber from the side (this design is called "horizontal"), and held the wafers vertically, beside each other. However, many modern designs hold the wafers horizontally, above and below each other, and load them into the oxidation chamber from below.

Vertical furnaces stand higher than horizontal furnaces, so they may not fit into some microfabrication facilities. However, they help to prevent dust contamination. Unlike horizontal furnaces, in which falling dust can contaminate any wafer, vertical furnaces only allow it to fall on the top wafer in the boat.

Vertical furnaces also eliminate an issue that plagued horizontal furnaces: non-uniformity of grown oxide across the wafer. Horizontal furnaces typically have convection currents inside the tube which causes the bottom of the tube to be slightly colder than the top of the tube. As the wafers lie vertically in the tube the convection and the temperature gradient with it causes the top of the wafer to have a thicker oxide than the bottom of the wafer. Vertical furnaces solve this problem by having wafer sitting horizontally, and then having the gas flow in the furnace flowing from top to bottom, significantly dampening any thermal convections.

Vertical furnaces also allow the use of load locks to purge the wafers with nitrogen before oxidation to limit the growth of native oxide on the Si surface.

Oxide quality

Wet oxidation is preferred to dry oxidation for growing thick oxides, because of the higher growth rate. However, fast oxidation leaves more dangling bonds at the silicon interface, which produce quantum states for electrons and allow current to leak along the interface. (This is called a "dirty" interface.) Wet oxidation also yields a lower-density oxide, with lower dielectric strength.

The long time required to grow a thick oxide in dry oxidation makes this process impractical. Thick oxides are usually grown with a long wet oxidation bracketed by short dry ones (a *dry-wet-dry* cycle). The beginning and ending dry oxidations produce films of high-quality oxide at the outer and inner surfaces of the oxide layer, respectively.

Mobile metal ions can degrade performance of MOSFETs (sodium is of particular concern). However, chlorine can immobilize sodium by forming sodium chloride. Chlorine is often introduced by adding hydrogen chloride or trichloroethylene to the oxidizing medium. Its presence also increases the rate of oxidation.

Other notes

- Thermal oxidation can be performed on selected areas of a wafer, and blocked on others. This process, first developed at Philips,[2] is commonly referred to as the Local Oxidation of Silicon (LOCOS) process. Areas which are not to be oxidized are covered with a film of silicon nitride, which blocks diffusion of oxygen and water vapor due to its oxidation at a much slower rate.[3] The nitride is removed after oxidation is complete. This process cannot produce sharp features, because lateral (parallel to the surface) diffusion of oxidant molecules under the nitride mask causes the oxide to protrude into the masked area.
- Because impurities dissolve differently in silicon and oxide, a growing oxide will selectively take up or reject dopants. This redistribution is governed by the segregation coefficient, which determines how strongly the oxide absorbs or rejects the dopant, and the diffusivity.
- The orientation of the silicon crystal affects oxidation. A <100> wafer (see Miller indices) oxidizes more slowly than a <111> wafer, but produces an electrically cleaner oxide interface.
- Thermal oxidation of any variety produces a higher-quality oxide, with a much cleaner interface, than chemical vapor deposition of oxide resulting in **Low Temperature Oxide** layer (reaction of TEOS at about 600 °C). However, the high temperatures required to produce High Temperature Oxide (HTO) restrict its usability. For instance, in MOSFET processes, thermal oxidation is never performed after the doping for the source and drain terminals is performed, because it would disturb the placement of the dopants.

References

[1] http://www.siliconfareast.com/oxidation2.htm

[2] J. Appels, E. Kooi, M. M. Paffen, J. J. H. Schatorje, and W. H. C. G. Verkuylen, “Local oxidation of silicon and its application in semiconductor-device technology,” PHILIPS RESEARCH Reports, vol. 25, no. 2, pp. 118–132, Apr. 1970.

[3] A. Kuiper, M. Willemsen, J. M. G. Bax, and F. H. P. H. Habraken, “Oxidation behaviour of LPCVD silicon oxynitride films,” Applied Surface Science, vol. 33, no. 34, pp. 757–764, Oct. 1988.

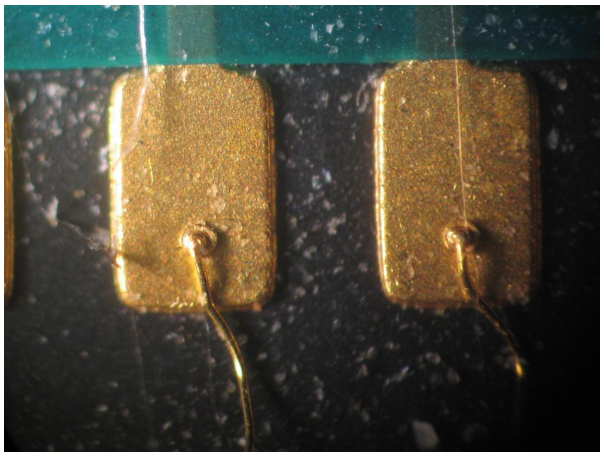
- Jaeger, Richard C. (2001). "Thermal Oxidation of Silicon". *Introduction to Microelectronic Fabrication*. Upper Saddle River: Prentice Hall. ISBN 0-201-44494-1.

External links

- Oxide growth time calculator (http://www.ee.byu.edu/cleanroom/OxideTimeCalc.phtml)
- Online calculator including deal grove and massoud oxidation models, with pressure and doping effects at: http://www.lelandstanfordjunior.com/thermaloxide.html

Wire bonding

Wire bonding is the primary method of making interconnections between an integrated circuit (IC) and a printed circuit board (PCB) during semiconductor device fabrication. Although less common, wire bonding can be used to connect an IC to other electronics or to connect from one PCB to another. Wire bonding is generally considered the most cost-effective and flexible interconnect technology, and is used to assemble the vast majority of semiconductor packages.

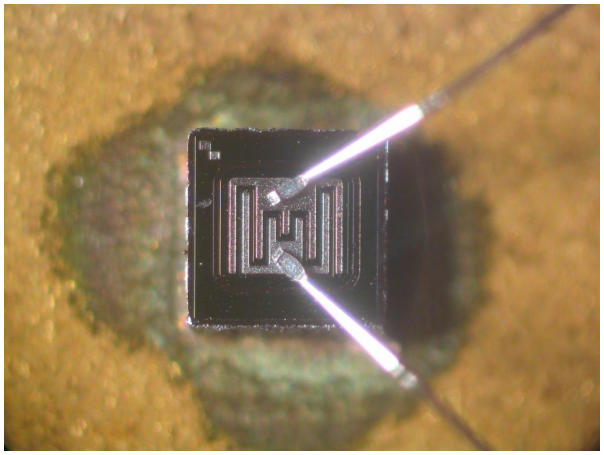


Gold wire ball-bonded to a gold contact pad

Bondwires usually consist of one of the following materials:

- Aluminum
- Copper
- Gold

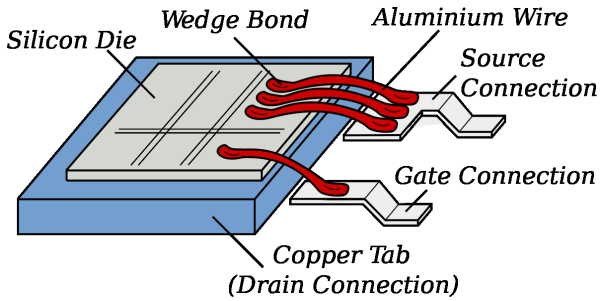
Wire diameters start at 15 µm and can be up to several hundred micrometres for high-powered applications.



Aluminium wires wedge-bonded to a KSY34 transistor die

Copper wire has become one of the preferred materials for wire bonding interconnects in many semiconductor and microelectronic applications. Copper is used for fine wire ball bonding in sizes up to 0.003 inch (75 micrometres). Copper wire has the ability of being used at smaller diameters providing the same performance as gold without the high material cost.[1]

Copper wire up to 0.010 inch (250 micrometres) can be successfully wedge bonded with the proper set-up parameters. Large diameter copper wire can and does replace aluminum wire where high current carrying capacity is needed or where there are problems with complex geometry. Annealing and process steps used by manufacturers enhance the ability to use large diameter copper wire to wedge bond to silicon without damage occurring to the die.[1]



The interconnections in a power package are made using thick (250 to 400 µm), wedge-bonded, aluminium wires.

Copper wire does pose some challenges in that it is harder than both gold and aluminum, so bonding parameters must be kept under tight control. The formation of oxides is inherent with this material, so storage and shelf life are issues that must be considered. Special packaging is required in order to protect copper wire and achieve a longer shelf life.[1]

Pure gold wire doped with controlled amounts of beryllium and other elements is normally used for ball bonding. This process brings together the two materials that are to be bonded using heat, pressure and ultrasonic energy referred to as thermosonic bonding. The most common approach in thermosonic bonding is to ball-bond to the chip,

then stitch-bond to the substrate. Very tight controls during processing enhance looping characteristics and eliminate sagging.

Junction size, bond strength and conductivity requirements typically determine the most suitable wire size for a specific wire bonding application. Typical manufacturers make gold wire in diameters from 0.0005 inch (12.5 micrometres) and larger. Production tolerance on gold wire diameter is +/-3%.[2]

Alloyed aluminum wires are generally preferred to pure aluminum wire except in high-current devices because of greater drawing ease to fine sizes and higher pull-test strengths in finished devices. Pure aluminum and 0.5% magnesium-aluminum are most commonly used in sizes larger than 0.004 inch.

All aluminum systems in semiconductor fabrication eliminate the "purple plague" (brittle gold-aluminum intermetallic compound) sometimes associated with pure gold bonding wire. Aluminum is particularly suitable for ultrasonic bonding.

In order to assure that high quality bonds can be obtained at high production speeds, special controls are used in the manufacture of 1% silicon-aluminum wire. One of the most important characteristics of high grade bonding wire of this type is homogeneity of the alloy system. Homogeneity is given special attention during the manufacturing process. Microscopic checks of the alloy structure of finished lots of 1% silicon-aluminum wire are performed routinely. Processing also is carried out under conditions which yield the ultimate in surface cleanliness and smooth finish and permits entirely snag-free de-reeling.[3]

The main classes of wire bonding:

- Ball bonding
- Wedge bonding
- Compliant bonding

Ball bonding usually is restricted to gold and copper wire and usually requires heat. Wedge bonding can use either gold or aluminum wire, with only the gold wire requiring heat.

In either type of wire bonding, the wire is attached at both ends using some combination of heat, pressure, and ultrasonic energy to make a weld.

Compliant bonding[4] transmits heat and pressure through a compliant or indentable aluminum tape and therefore is applicable in bonding gold wires and the Beam leads that have been electroformed to the silicon integrated circuit (known as the Beam leaded integrated circuit).

Composite wire: glass coated Cu wire

A new type of micro bonding wire has recently been developed (see RED Micro Wire [5]) – glass coated copper wire. This composite wire has unique characteristics which may revolutionize the bonding market. Gold wire has always been the standard of excellence for the bonding industry however, due to its increasing cost it has become necessary to search for alternatives. The high reliability of gold and relatively simple material management makes Au the industry's first choice. The mechanical advantages of Au wire have been offset by the better electrical conductivity of Cu, its fusing current (and the drastic price increases of Au), resulting in exponential growth of Cu in the wire bonding process over the last few years. A number of challenges, mainly in operation and materials management have led the semiconductor industry to search for alternative solutions to copper bonding wire. One such example is Pd coated Cu wire. Glass coated Cu wire provides a solution that overcomes the challenges of Cu wire (materials management, oxidation). Hardness/softness testing reveals parameters like that of gold bonding wire (~78HV) while the cost remains like that of copper wire. The glass coating provides electrical isolation which should enable relaxed chip design rules and ultimately – higher density i/o on less chip 'real estate'.

References

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[2] http://www.coininginc.com/gold_wire_and_ribbon.asp
[3] http://www.coininginc.com/aluminum_and_silicon_ribbon.asp
[4] A.Coucoulas, “Compliant Bonding” Proceedings 1970 IEEE 20th Electronic Components Conference, pp. 380-89, 1970. http://commons.wikimedia.org/wiki/File:CompliantBondingPublic_1-10.pdf https://www.researchgate.net/publication/225284187_Compliant_Bonding_Alexander_Coucoulas_1970_Proceeding_Electronic_Components_Conference_Awarded_Best_Paper
[5] http://www.redmicrowire.com

- Copper (Cu) Wire Bonding (http://www.amkor.com/go/packaging/copper-cu-wire-bonding)

RED Micro Wire encapsulates wire bonding in glass (http:/ / eetimes. com/ electronics-news/ 4369813/ Red-Micro-Wire-encapsulates-wire-bonding-in-glass)

Challenging the limits of bonding wire (http:/ / www. electronicsnews. com. au/ news/ challenging-the-limits-of-bonding-wire)

Thermosonic bonding

Thermosonic bonding is widely used to permanently interconnect the all-important metallized silicon integrated circuit (popularly known as the “chip”) into computers. It was first introduced by Alexander Coucoulas who is "The Father Of Thermosonic Bonding" (as referenced below).

Thermosonic Bonding can be used to form solid-state bonds well below the melting point of the mating metals such as gold wires to gold metallized pads which have been previously deposited on the peripheral surface of the silicon integrated circuit “chip” during its manufacturing stage. The bond is formed by transmitting a combination of heat, ultrasonic energy and pressure to the mating surfaces. Since relatively low bonding parameters are required to form reliable bonds when using Thermosonic Bonding, the integrity of the fragile silicon integrated circuit “chip”, is assured throughout its intended lifetime use as the "brains" of the computer.

As a result of Coucoulas introducing the Thermosonic bonding concept, its many uses have grown as confirmed by the more than 60,000 thermosonic google sites shown today.

History

Three methods of solid state wire bonding were sequentially developed to improve the permanent interconnections between the silicon integrated circuits (ICs) to the outside circuitry. In the mid 1950s, solid state wire bonds were made using heat and pressure and was referred to as Thermocompression bonding.[1] The process was generally limited to bonding pre-cleaned oxide-free gold-to-gold since the desired shearing action at the bonding interface was limited. Orson L. Anderson, a coauthor of the thermocompression bonding paper,[1] later described the importance of interfacial shear in forming reliable solid-state bonds.[2] In the early 1960s commercial ultrasonic wire bonders were introduced which used vibratory energy and pressure to form solid-state bonds without a provision to add heat.[3] The vibratory action enhanced the shearing action at the bonding interface which enhanced the reliability of forming gold-to-gold solid state bonds and also extended the range of mating metals to aluminum and copper.

Invention

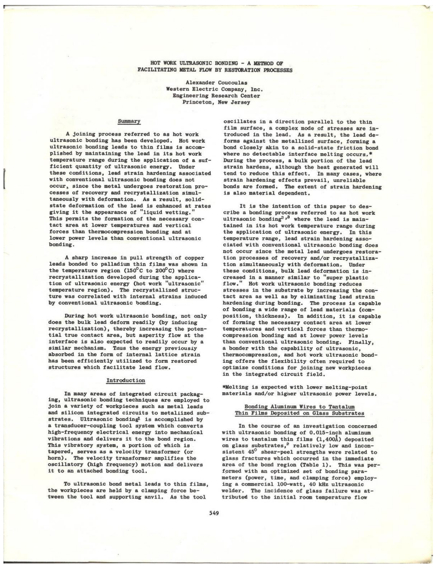
In the mid 1960s, Alexander Coucoulas[4][5] reported the first thermosonic wire bonds using a combination of heat, ultrasonic vibrations and pressure. He used a commercial ultrasonic wire bonder to investigate the attachment of aluminum wires to tantalum thin films deposited on glass substrates which closely simulated bonding to the fragile metallized silicon integrated circuit or "Chip". He observed that the ultrasonic energy and pressures levels needed to sufficiently deform the wire and form the required contact areas significantly increased the incidences of cracks in

the glass substrates. A means of heating the bond region was then added to the ultrasonic bonder. The bond region was then heated during the ultrasonic bonding cycle which virtually eliminated the glass failure mode since the required contact area was achieved with lower ultrasonic energy and pressure levels. The enhanced wire deformation during the ultrasonic bonding cycle was attributed to the transition from cold working (or strain hardening of the wire) to hot working where its softness was largely maintained due to the onset of recrystallization. Christian Hagar[6] and George Harman[7] stated that in 1970 Alexander Coucoulas,[8] reported additional work in forming thermosonic-type bonds which he initially called *hot work ultrasonic bonding*. In this case, copper wires were bonded to palladium thin films deposited on aluminum oxide substrate. As a result of these earliest reported thermosonic wire bonds, G.Harman (the world's foremost authority on wire bonding) stated: "as such, Alexander Coucoulas is the Father of Thermosonic Bonding".[7]

(Inventor's Background)

Coucoulas retired from AT&T Bell Labs as a Member Of The Technical Staff in 1996 where he pioneered research in the areas of electronic/photonic packaging and optical fibers which resulted in obtaining about 30 patents. He was twice awarded best paper at the 20th and 43rd IEEE Electronic Components Conference for “Compliant Bonding” in 1970 ”[9] and AlO Bonding in 1993 [10] both of which were his patented inventions.[11][12]

His Ionian-Greek immigrant parents were born in the biblical city of Smyrna which was the birthplace of Homer. After Coucoulas served in the US Army as a combat engineer in the Far East Command in the early 1950’s, he obtained his undergraduate and graduate degrees in Metallurgical Engineering and Material Science at New York University which was financed by the Gi Bill, a graduate scholarship and part time jobs in the New York Metropolitan area. His graduate thesis, included in a co-authored paper,[13] was under the tutorage of dr. Kurt Komarek who is the former Rector (President) and present professor emeritus of the University Of Vienna.



HOT WORK ULTRASONIC BONDING - A METHOD OF FACILITATING METAL FLOW BY RESTORATION PROCESSES

Alexander Coucoulas
Western Electric Company, Inc.
Engineering Research Center
Princeton, New Jersey

Summary

A joining process referred to as hot work ultrasonic bonding has been developed. Hot work ultrasonic bonding leads to thin films is accomplished by maintaining the lead in its hot work temperature range during the application of a sufficient quantity of ultrasonic energy. Under these conditions, lead strain hardening associated with conventional ultrasonic bonding does not occur, since the metal undergoes restoration processes of recovery and recrystallization simultaneously with deformation. As a result, solid-state deformation of the lead is enhanced at rates giving it the appearance of "liquid wetting." This permits the formation of the necessary contact area at lower temperatures and vertical forces than thermocompression bonding and at lower power levels than conventional ultrasonic bonding.

A sharp increase in pull strength of copper leads bonded to palladium thin films was shown in the temperature region (150°C to 200°C) where recrystallization developed during the application of ultrasonic energy (hot work "ultrasonic" temperature region). The recrystallized structure was correlated with internal strains induced by conventional ultrasonic bonding.

During hot work ultrasonic bonding, not only does the bulk lead deform readily (by inducing recrystallization), thereby increasing the potential true contact area, but asperity flow at the interface is also expected to readily occur by a similar mechanism. Thus the energy previously absorbed in the form of internal lattice strain has been efficiently utilized to form restored structures which facilitate lead flow.

Introduction

In many areas of integrated circuit packaging, ultrasonic bonding techniques are employed to join a variety of workpieces such as metal leads and silicon integrated circuits to metalized substrates. Ultrasonic bonding[1] is accomplished by a transducer-coupling tool system which converts high-frequency electrical energy into mechanical vibrations and delivers it to the bond region. This vibratory system, a portion of which is tapered, serves as a velocity transformer (or horn). The velocity transformer amplifies the oscillatory (high frequency) motion and delivers it to an attached bonding tool.

To ultrasonic bond metal leads to thin films, the workpieces are held by a clamping force between the tool and supporting anvil. As the tool oscillates in a direction parallel to the thin film surface, a complex mode of stresses are introduced in the lead. As a result, the lead deforms against the metallized surface, forming a bond closely akin to a solid-state friction bond where no detectable interface melting occurs.* During the process, a bulk portion of the lead strain hardens, although the heat generated will tend to reduce this effect. In many cases, where strain hardening effects prevail, unreliable bonds are formed. The extent of strain hardening is also material dependent.

It is the intention of this paper to describe a bonding process referred to as hot work ultrasonic bonding[2,3] where the lead is maintained in its hot work temperature range during the application of ultrasonic energy. In this temperature range, lead strain hardening associated with conventional ultrasonic bonding does not occur since the metal lead undergoes restoration processes of recovery and/or recrystallization simultaneously with deformation. Under these conditions, bulk lead deformation is increased in a manner similar to "super plastic flow." Hot work ultrasonic bonding reduces stresses in the substrate by increasing the contact area as well as by eliminating lead strain hardening during bonding. The process is capable of bonding a wide range of lead materials (composition, thickness). In addition, it is capable of forming the necessary contact area at lower temperatures and vertical forces than thermocompression bonding and at lower power levels than conventional ultrasonic bonding. Finally, a bonder with the capability of ultrasonic, thermocompression, and hot work ultrasonic bonding offers the flexibility often required to optimize conditions for joining new workpieces in the integrated circuit field.

*Melting is expected with lower melting-point materials and/or higher ultrasonic power levels.

Bonding Aluminum Wires to Tantalum Thin Films Deposited on Glass Substrates

In the course of an investigation concerned with ultrasonic bonding of 0.015-inch aluminum wires to tantalum thin films (1,400Å) deposited on glass substrates,[2] relatively low and inconsistent 45° shear-peel strengths were related to glass fractures which occurred in the immediate area of the bond region (Table 1). This was performed with an optimized set of bonding parameters (power, time, and clamping force) employing a commercial 100-watt, 40 kHz ultrasonic welder. The incidence of glass failure was attributed to the initial room temperature flow

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Alexander Coucoulas' publication that first introduced Thermosonic Bonding which is widely used to connect the all important silicon integrated circuit known as "The Chip" and "brains' of the computer.[8] Click to read full resolution

Summary

At present, the majority of connections to silicon integrated circuits (also known as "The Chip") are made using Thermosonic Bonding[7][8] because it employs lower bonding temperatures, forces and dwell times than thermocompression bonding,[1] as well as lower vibratory energy levels than ultrasonic bonding[3] to form the required bond area. Therefore the use of Thermosonic Bonding largely eliminates damaging the relatively fragile silicon integrated circuit (“The Chip”) during the bonding cycle. The proven reliability of Thermosonic Bonding has made it the process of choice, since such potential failure modes could be costly whether they occur during the manufacturing stage or detected later, during an operational field-failure of "a Chip" which had been permanently connected inside a computer or a myriad of other electronic devices.

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External links

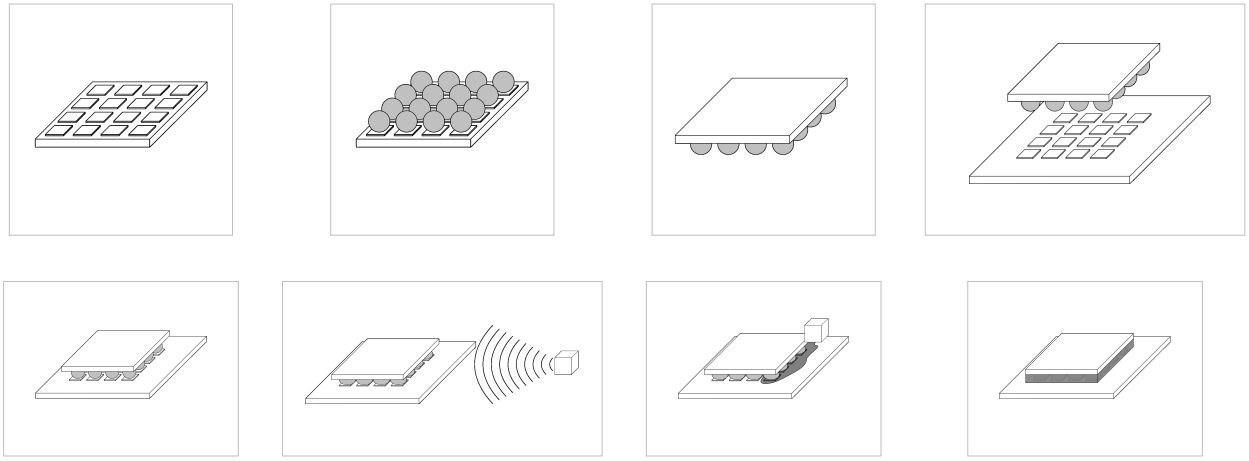
Search Thermosonic bonding at Google: https:/ / www. google. com/ #hl=en& sugexp=les%3B& gs_rn=1& gs_ri=hp& tok=qPtxoZXxG3MWOvaRpZpnBw& cp=12& gs_id=1a& xhr=t& q=thermosonic+ bonding& es_nrs=true& pf=p& tbo=d& output=search& sclient=psy-ab& oq=thermosonic+ & gs_l=& pbx=1& bav=on. 2,or. r_gc.r_pw.r_qf.&bvm=bv.41524429,d.dmQ&fp=325752036066648b&biw=1216&bih=533

Flip chip

Flip chip, also known as **controlled collapse chip connection** or its acronym, **C4**, is a method for interconnecting semiconductor devices, such as IC chips and microelectromechanical systems (MEMS), to external circuitry with solder bumps that have been deposited onto the chip pads. The solder bumps are deposited on the chip pads on the top side of the wafer during the final wafer processing step. In order to mount the chip to external circuitry (e.g., a circuit board or another chip or wafer), it is flipped over so that its top side faces down, and aligned so that its pads align with matching pads on the external circuit, and then the solder is flowed to complete the interconnect. This is in contrast to wire bonding, in which the chip is mounted upright and wires are used to interconnect the chip pads to external circuitry.

Process steps

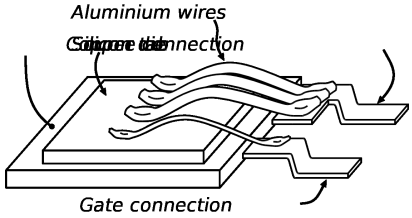
1. Integrated circuits are created on the wafer
2. Pads are metalized on the surface of the chips
3. Solder dots are deposited on each of the pads
4. Chips are cut
5. Chips are flipped and positioned so that the solder balls are facing the connectors on the external circuitry
6. Solder balls are then remelted (typically using hot air reflow)
7. Mounted chip is “underfilled” using an electrically-insulating adhesive



Comparison of mounting technologies

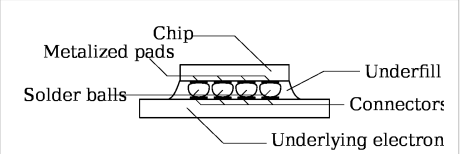
Wire bonding/Thermosonic bonding

In typical semiconductor fabrication systems chips are built up in large numbers on a single large wafer of semiconductor material, typically silicon. The individual chips are patterned with small pads of metal near their edges that serve as the connections to an eventual mechanical carrier. The chips are then cut out of the wafer and attached to their carriers, typically via wire bonding such as Thermosonic Bonding. These wires eventually lead to pins on the outside of the carriers, which are attached to the rest of the circuitry making up the electronic system.



The interconnections in a power package are made using thick aluminium wires (250 to 400 µm) wedge-bonded

Flip chip



Side-view schematic of a typical flip chip mounting

Processing a flip chip is similar to conventional IC fabrication, with a few additional steps.[1] Near the end of the manufacturing process, the attachment pads are metalized to make them more receptive to solder. This typically consists of several treatments. A small dot of solder is then deposited on each metalized pad. The chips are then cut out of the wafer as normal.

To attach the flip chip into a circuit, the chip is inverted to bring the solder dots down onto connectors on the underlying electronics or circuit board. The solder is then re-melted to produce an electrical connection, typically using an ultrasonic or alternatively reflow solder process. This also leaves a small space between the chip's circuitry and the underlying mounting. In most cases an electrically-insulating adhesive is then "underfilled" to provide a stronger mechanical connection, provide a heat bridge, and to ensure the solder joints are not stressed due to differential heating of the chip and the rest of the system.

Recently, high-speed mounting methods evolved through a cooperation between Reel Service Ltd. and Siemens AG in the development of a high speed mounting tape known as 'MicroTape.'[2]. By adding a tape-and-reel process into the assembly methodology, placement at high speed is possible, achieving a 99.90% pick rate and a placement rate of 21,000 cph (components per hour), using standard PCB assembly equipment.

Advantages

The resulting completed flip chip assembly is much smaller than a traditional carrier-based system; the chip sits directly on the circuit board, and is much smaller than the carrier both in area and height. The short wires greatly reduce inductance, allowing higher-speed signals, and also conduct heat better.

Disadvantages

Flip chips have several disadvantages. The lack of a carrier means they are not suitable for easy replacement, or manual installation. They also require very flat surfaces to mount to, which is not always easy to arrange, or sometimes difficult to maintain as the boards heat and cool. Also, the short connections are very stiff, so the thermal expansion of the chip must be matched to the supporting board or the connections can crack.[3] The underfill material acts as an intermediate between the difference in CTE of the chip and board.

History

The process was originally introduced commercially by IBM in the 1960s for individual transistors and diodes packaged for use in their mainframe systems.[4] DEC followed IBM's lead, but was unable to achieve the quality they demanded, and eventually gave up on the concept. It was pursued once again in the mid-90s for the Alpha product line, but then abandoned due to the fragmentation of the company and subsequent sale to Compaq. In the 1970s it was taken up by Delco Electronics, and has since become very common in automotive applications.

Alternatives

Since the flip chip's introduction a number of alternatives to the solder bumps have been introduced, including gold balls or molded studs, electrically conductive polymer and the "plated bump" process that *removes* an insulating plating by chemical means. Flip chips have recently gained popularity among manufacturers of cell phones, pagers and other small electronics where the size savings are valuable.

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Further reading

- Wikihowto: Guide to IC packages (http://en.howto.wikia.com/wiki/Guide_to_IC_packages)

Wafer bonding

Wafer bonding is a packaging technology on wafer-level for the fabrication of microelectromechanical systems (MEMS), nanoelectromechanical systems (NEMS), microelectronics and optoelectronics, ensuring a mechanically stable and hermetically sealed encapsulation. The wafers' diameter range from 100 mm to 200 mm (4 inch to 8 inch) for MEMS/NEMS and up to 300 mm (12 inch) for the production of microelectronic devices.

Overview

In microelectromechanical systems (MEMS) and nanoelectromechanical systems (NEMS), the package is an important part of the device. It enhances a proper function and protects the sensitive internal structures from environmental influences such as temperature, moisture, high pressure and oxidizing species. So, the long-term stability and reliability of the functional elements directly depend on the encapsulation process as well as a significant fraction on the overall device costs.[1] In conclusion, the package has to fulfill the following requirements:[2]

- protection against environmental influences
- heat dissipation
- integration of elements with different technologies
- compatibility to the surrounding periphery
- maintenance of energy and information flow

Techniques

The commonly used and developed bonding methods are as follows:

- Direct bonding
- Plasma activated bonding
- Anodic bonding
- Eutectic bonding
- Glass frit bonding
- Adhesive bonding
- Thermocompression bonding
- Reactive bonding

Requirements

The bonding of wafers requires specific environmental conditions which can generally be defined as follows:[3]

1. substrate surface
   - flatness
   - smoothness
   - cleanliness
2. bonding environment
   - bond temperature
   - ambient pressure
   - applied force
3. materials
   - substrate materials
   - intermediate layer materials

The actual bond is an interaction of all those conditions and requirements. Hence, the applied technology needs to be chosen in respect to the present substrate and defined specification like max. bearable temperature, mechanical pressure or desired gaseous atmosphere.

Evaluation

The bonded wafers are characterized in order to evaluate a technology's yield, bonding strength and level of hermeticity either for fabricated devices or for the purpose of process development. Therefore, several different approaches for the bond characterization have emerged. On the one hand non-destructive optical methods to find cracks or interfacial voids are used beside destructive techniques for the bond strength evaluation, like tensile or shear testing. On the other hand the unique properties of carefully chosen gases or the pressure depending vibration behavior of micro resonators are exploited for hermeticity testing.

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External links

- Wafer bonding at Fraunhofer ENAS (http://www.enas.fraunhofer.de/EN/abteilungen/mdi/forschung/advanced-technologies/Waferbonden/index.jsp)
- Handbook of Wafer Bonding, Wiley-VCH, edited by Peter Ramm, James Lu, Maaike Taklo (http://www.wiley-vch.de/publish/dt/books/forthcomingTitles/NT00/3-527-32646-4/?sID=p2qlnooj68su7htl8qrrc2qjt3)

Plating

Plating is a surface covering in which a metal is deposited on a conductive surface. Plating has been done for hundreds of years, but it is also critical for modern technology. Plating is used to decorate objects, for corrosion inhibition, to improve solderability, to harden, to improve wearability, to reduce friction, to improve paint adhesion, to alter conductivity, for radiation shielding, and for other purposes. Jewelery typically uses plating to give a silver or gold finish. Thin-film deposition has plated objects as small as an atom, therefore plating finds uses in nanotechnology.

There are several plating methods, and many variations. In one method, a solid surface is covered with a metal sheet, and then heat and pressure are applied to fuse them (a version of this is Sheffield plate). Other plating techniques include vapor deposition under vacuum and sputter deposition. Recently, plating often refers to using liquids. Metallizing refers to coating metal on non-metallic objects.

Electroplating

In electroplating, an ionic metal is supplied with electrons to form a non-ionic coating on a substrate. A common system involves a chemical solution with the ionic form of the metal, an anode (positively charged) which may consist of the metal being plated (a soluble anode) or an insoluble anode (usually carbon, platinum, titanium, lead, or steel), and finally, a cathode (negatively charged) where electrons are supplied to produce a film of non-ionic metal.

Electroless plating

Electroless plating, also known as chemical or auto-catalytic plating, is a non-galvanic plating method that involves several simultaneous reactions in an aqueous solution, which occur without the use of external electrical power. The reaction is accomplished when hydrogen is released by a reducing agent, normally sodium hypophosphite (Note: the hydrogen leaves as a hydride ion), and oxidized, thus producing a negative charge on the surface of the part. The most common electroless plating method is electroless nickel plating, although silver, gold and copper layers can also be applied in this manner, as in the technique of Angel gilding.

Specific cases

Gold plating

Gold plating is a method of depositing a thin layer of gold on the surface of glass or metal, most often copper or silver.

Gold plating is often used in electronics, to provide a corrosion-resistant electrically conductive layer on copper, typically in electrical connectors and printed circuit boards. With direct gold-on-copper plating, the copper atoms have the tendency to diffuse through the gold layer, causing tarnishing of its surface and formation of an oxide/sulfide layer. Therefore, a layer of a suitable barrier metal, usually nickel, has to be deposited on the copper substrate, forming a copper-nickel-gold sandwich.

Metals and glass may also be coated with gold for ornamental purposes, using a number of different processes usually referred to as *gilding*.

Silver plating

For applications in electronics, silver is sometimes used for plating copper, as its electrical resistance is lower (see Resistivity of various materials); more so at higher frequencies due to the skin effect. Variable capacitors are considered of the highest quality when they have silver-plated plates. Similarly, silver-plated, or even solid silver cables, are prized in audiophile applications; however some experts consider that in practice the plating is often poorly implemented, making the result inferior to similarly priced copper cables.[1]

A silver-plated alto saxophone

Care should be used for parts exposed to high humidity environments. When the silver layer is porous or contains cracks, the underlying copper undergoes rapid galvanic corrosion, flaking off the plating and exposing the copper itself; a process known as red plague.

Historically, silver plate was used to provide a cheaper version of items that might otherwise be made of silver, including cutlery and candlesticks. The earliest kind was Old Sheffield Plate, but in the 19th century new methods of production (including electroplating) were introduced: see Sheffield Plate.

Another method that can be used to apply a thin layer of silver to several objects, such as glass, is to place Tollens' reagent in a glass, add Glucose/Dextrose, and shake the bottle to promote the reaction.

$$AgNO_3 + KOH \rightarrow AgOH + KNO_3$$

$$AgOH + 2\ NH_3 \rightarrow [Ag(NH_3)_2]^+ + [OH]^-$$ (Note: see Tollens' reagent)

$$[Ag(NH_3)_2]^+ + [OH]^- + \text{aldehyde (usually glucose/dextrose)} \rightarrow Ag + 2\ NH_3 + H_2O$$

Rhodium plating

Rhodium plating is occasionally used on white gold, silver or copper and its alloys. A barrier layer of nickel is usually deposited on silver first, though in this case it is not to prevent migration of silver through rhodium, but to prevent contamination of the rhodium bath with silver and copper, which slightly dissolve in the sulfuric acid usually present in the bath composition.[2]

Chrome plating

Chrome plating is a finishing treatment utilizing the electrolytic deposition of chromium. The most common form of chrome plating is the thin, decorative *bright chrome*, which is typically a 10-µm layer over an underlying nickel plate. When plating on iron or steel, an underlying plating of copper allows the nickel to adhere. The pores (tiny holes) in the nickel and chromium layers also promote corrosion resistance. Bright chrome imparts a mirror-like finish to items such as metal furniture frames and automotive trim. Thicker deposits, up to 1000 µm, are called *hard chrome* and are used in industrial equipment to reduce friction and wear.

The traditional solution used for industrial hard chrome plating is made up of about 250 g/L of CrO_3 and about 2.5 g/L of SO_4^{-}. In solution, the chrome exists as chromic acid, known as hexavalent chromium. A high current is used, in part to stabilize a thin layer of chromium(+2) at the surface of the plated work. Acid chrome has poor throwing power, fine details or holes are further away and receive less current resulting in poor plating.

Zinc plating

Zinc coatings prevent oxidation of the protected metal by forming a barrier and by acting as a sacrificial anode if this barrier is damaged. Zinc oxide is a fine white dust that (in contrast to iron oxide) does not cause a breakdown of the substrate's surface integrity as it is formed. Indeed the zinc oxide, if undisturbed, can act as a barrier to further oxidation, in a way similar to the protection afforded to aluminum and stainless steels by their oxide layers. The majority of hardware parts are zinc plated, rather than cadmium plated.[3]

Tin plating

The tin-plating process is used extensively to protect both ferrous and nonferrous surfaces. Tin is a useful metal for the food processing industry since it is non-toxic, ductile and corrosion resistant. The excellent ductility of tin allows a tin coated base metal sheet to be formed into a variety of shapes without damage to the surface tin layer. It provides sacrificial protection for copper, nickel and other non-ferrous metals, but not for steel.

Tin is also widely used in the electronics industry because of its ability to protect the base metal from oxidation thus preserving its solderability. In electronic applications, 3% to 7% lead may be added to improve solderability and to prevent the growth of metallic "whiskers" in compression stressed deposits, which would otherwise cause electrical shorting. However, RoHS (Restriction of Hazardous Substances) regulations enacted beginning in 2006 require that no lead be added intentionally and that the maximum percentage not exceed 1%. Some exemptions have been issued to RoHS requirements in critical electronics applications due to failures which are known to have occurred as a result of tin whisker formation.

Alloy plating

In some cases, it is desirable to co-deposit two or more metals resulting in an electroplated alloy deposit. Depending on the alloy system, an electroplated alloy may be solid solution strengthened or precipitation hardened by heat treatment to improve the plating's physical and chemical properties. Nickel-Cobalt is a common electroplated alloy.

Composite plating

Metal matrix composite plating can be manufactured when a substrate is plated in a bath containing a suspension of ceramic particles. Careful selection of the size and composition of the particles can fine-tune the deposit for wear resistance, high temperature performance, or mechanical strength. Tungsten carbide, silicon carbide, chromium carbide, and aluminum oxide (alumina) are commonly used in composite electroplating.

Cadmium plating

Cadmium plating is under scrutiny because of the environmental toxicity of the cadmium metal. However, cadmium plating is still widely used in some applications such as aerospace fasteners and it remains in military and aviation specs however it is being phased out due to its toxicity and corrosive properties.[4]

Cadmium plating (or "cad plating") offers a long list of technical advantages such as excellent corrosion resistance even at relatively low thickness and in salt atmospheres, softness and malleability, freedom from sticky and/or bulky corrosion products, galvanic compatibility with aluminum, freedom from stick-slip thus allowing reliable torquing of plated threads, can be dyed to many colors and clear, has good lubricity and solderability, and works well either as a final finish or as a paint base.[3][5]

If environmental concerns matter, in most aspects cadmium plating can be directly replaced with gold plating as it shares most of the material properties, but gold is more expensive and cannot serve as a paint base.

Nickel plating

The chemical reaction for nickel plating is:

At cathode: $Ni \rightarrow Ni^{2+} + 2e^{-}$

At anode: $H_2PO_2 + H_2O \rightarrow H_2PO_3 + 2\ H^{+}$

Compared to cadmium plating, nickel plating offers a shinier and harder finish, but lower corrosion resistance, lubricity, and malleability, resulting in a tendency to crack or flake if the piece is further processed.[3]

Electroless nickel plating

Electroless nickel plating, also known as *enickel* and *NiP*, offers many advantages: uniform layer thickness over most complicated surfaces, direct plating of ferrous metals (steel), superior wear and corrosion resistance to electroplated nickel or chrome. Much of the chrome plating done in aerospace industry can be replaced with electroless nickel plating, again environmental costs, costs of hexavalent chromium waste disposal and notorious tendency of uneven current distribution favor electroless nickel plating.[6]

Electroless nickel plating is self-catalyzing process, the resultant nickel layer is NiP compound, with 7–11% phosphorus content. Properties of the resultant layer hardness and wear resistance are greatly altered with bath composition and deposition temperature, which should be regulated with 1 °C precision, typically at 91 °C.

During bath circulation, any particles in it will become also nickel plated, this effect is used to advantage in processes which deposit plating with particles like silicon carbide (SiC) or polytetrafluoroethylene (PTFE). While superior compared to many other plating processes, it is expensive because the process is complex. Moreover, the process is lengthy even for thin layers. When only corrosion resistance or surface treatment is of concern, very strict bath composition and temperature control is not required and the process is used for plating many tons in one bath at

once.

Electroless nickel plating layers are known to provide extreme surface adhesion when plated properly. Electroless nickel plating is non-magnetic and amorphous. Electroless nickel plating layers are not easily solderable, nor do they seize with other metals or another electroless nickel plated workpiece under pressure. This effect benefits electroless nickel plated screws made out of malleable materials like titanium. Electrical resistance is higher compared to pure metal plating.

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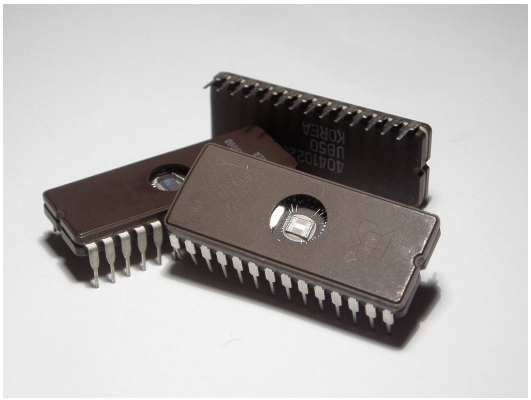
- New nano-ceramic coating technology brings zinc plating totally free of chromate and heavy metal ions (http://nanomatetech.com/Download/Eco-friendly-coating-FastenerInt'l-2009-10.pdf)

Integrated circuit

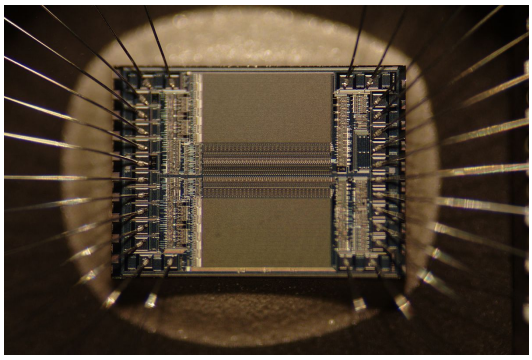
An **integrated circuit** or **monolithic integrated circuit** (also referred to as an **IC**, a **chip**, or a **microchip**) is a set of electronic circuits on one small plate ("chip") of semiconductor material, normally silicon. This can be made much smaller than a discrete circuit made from independent components.



Wide angle shot of the memory microchip shown in detail below. The microchips have a transparent window, showing the integrated circuit inside. The window allows the memory contents of the chip to be erased, by exposure to strong ultraviolet light in an eraser device.

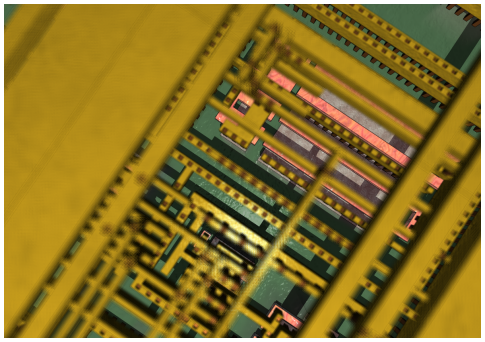
Integrated circuits are used in virtually all electronic equipment today and have revolutionized the world of electronics. Computers, mobile phones, and other digital home appliances are now inextricable parts of the structure of modern societies, made possible by the low cost of producing integrated circuits.

ICs can be made very compact, having up to several billion transistors and other electronic components in an area the size of a fingernail. The width of each conducting line in a circuit (the line width) can be made smaller and smaller as the technology advances, in 2008 it dropped below 100 nanometers and in 2013 it is expected to be in the teens of nanometers.[1]



Integrated circuit from an EPROM memory microchip showing the memory blocks, the supporting circuitry and the fine silver wires which connect the integrated circuit die to the legs of the packaging.

Introduction



Synthetic detail of an integrated circuit through four layers of planarized copper interconnect, down to the polysilicon (pink), wells (greyish), and substrate (green)

ICs were made possible by experimental discoveries showing that semiconductor devices could perform the functions of vacuum tubes and by mid-20th-century technology advancements in semiconductor device fabrication. The integration of large numbers of tiny transistors into a small chip was an enormous improvement over the manual assembly of circuits using discrete electronic components. The integrated circuit's mass production capability, reliability, and building-block approach to circuit design ensured the rapid adoption of standardized Integrated Circuits in place of designs using discrete transistors.

There are two main advantages of ICs over discrete circuits: cost and performance. Cost is low because the chips, with all their components, are printed as a unit by photolithography rather than being constructed one transistor at a time. Furthermore, much less material is used to construct a packaged IC die than to construct a discrete circuit. Performance is high because the components switch quickly and consume little power (compared to their discrete counterparts) as a result of the small size and close proximity of the components. As of 2012, typical chip areas range from a few square millimeters to around 450 mm^2, with up to 9 million transistors per mm^2.

Terminology

Integrated circuit originally referred to a miniaturized electronic circuit consisting of semiconductor devices, as well as passive components bonded to a substrate or circuit board.[2] This configuration is now commonly referred to as a hybrid integrated circuit. *Integrated circuit* has since come to refer to the single-piece circuit construction originally known as a *monolithic integrated circuit*.[3]

Invention

Early developments of the integrated circuit go back to 1949, when the German engineer Werner Jacobi (de) (Siemens AG)[4] filed a patent for an integrated-circuit-like semiconductor amplifying device[5] showing five transistors on a common substrate in a 3-stage amplifier arrangement. Jacobi disclosed small and cheap hearing aids as typical industrial applications of his patent. An immediate commercial use of his patent has not been reported.

The idea of the integrated circuit was conceived by a radar scientist working for the Royal Radar Establishment of the British Ministry of Defence, Geoffrey W.A. Dummer (1909–2002). Dummer presented the idea to the public at the Symposium on Progress in Quality Electronic Components in Washington, D.C. on 7 May 1952.[6] He gave many symposia publicly to propagate his ideas, and unsuccessfully attempted to build such a circuit in 1956.

A precursor idea to the IC was to create small ceramic squares (wafers), each one containing a single miniaturized component. Components could then be integrated and wired into a bidimensional or tridimensional compact grid. This idea, which looked very promising in 1957, was proposed to the US Army by Jack Kilby, and led to the short-lived Micromodule Program (similar to 1951's Project Tinkertoy).[7] However, as the project was gaining momentum, Kilby came up with a new, revolutionary design: the IC.

Robert Noyce credited Kurt Lehovec of Sprague Electric for the *principle of p-n junction isolation* caused by the action of a biased p-n junction (the diode) as a key concept behind the IC.[8]

Newly employed by Texas Instruments, Kilby recorded his initial ideas concerning the integrated circuit in July 1958, successfully demonstrating the first working integrated example on 12 September 1958.[9] In his patent application of 6 February 1959, Kilby described his new device as “a body of semiconductor material ... wherein all the components of the electronic circuit are completely integrated.”[10] The first customer for the new invention was the US Air Force.[11]

Kilby won the 2000 Nobel Prize in Physics for his part of the invention of the integrated circuit.[12] Kilby's work was named an IEEE Milestone in 2009.[13]

Noyce also came up with his own idea of an integrated circuit half a year later than Kilby. His chip solved many practical problems that Kilby's had not. Produced at Fairchild Semiconductor, it was made of silicon, whereas Kilby's chip was made of germanium.

Fairchild Semiconductor was also home of the first silicon gate IC technology with self-aligned gates, which stands as the basis of all modern CMOS computer chips. The technology was developed by Italian physicist Federico Faggin in 1968, who later joined Intel in order to develop the very first Central Processing Unit (CPU) on one chip (Intel 4004), for which he received the National Medal of Technology and Innovation in 2010.

Generations

In the early days of integrated circuits, only a few transistors could be placed on a chip, as the scale used was large because of the contemporary technology, and manufacturing yields were low by today's standards. As the degree of integration was small, the design process was relatively simple. Over time, millions, and today billions,[14] of transistors could be placed on one chip, and a good design required thorough planning. This gave rise to new design methods.

SSI, MSI and LSI

The first integrated circuits contained only a few transistors. Called "**small-scale integration**" (**SSI**), digital circuits containing transistors numbering in the tens provided a few logic gates for example, while early linear ICs such as the Plessey SL201 or the Philips TAA320 had as few as two transistors. The term Large Scale Integration was first used by IBM scientist Rolf Landauer when describing the theoretical concept, from there came the terms for SSI, MSI, VLSI, and ULSI.

SSI circuits were crucial to early aerospace projects, and aerospace projects helped inspire development of the technology. Both the Minuteman missile and Apollo program needed lightweight digital computers for their inertial guidance systems; the Apollo guidance computer led and motivated the integrated-circuit technology,[15] while the Minuteman missile forced it into mass-production. The Minuteman missile program and various other Navy programs accounted for the total $4 million integrated circuit market in 1962, and by 1968, U.S. Government space and defense spending still accounted for 37% of the $312 million total production. The demand by the U.S. Government supported the nascent integrated circuit market until costs fell enough to allow firms to penetrate the industrial and eventually the consumer markets. The average price per integrated circuit dropped from $50.00 in 1962 to $2.33 in 1968.[16] Integrated circuits began to appear in consumer products by the turn of the decade, a typical application being FM inter-carrier sound processing in television receivers.

The next step in the development of integrated circuits, taken in the late 1960s, introduced devices which contained hundreds of transistors on each chip, called "**medium-scale integration**" (**MSI**).

They were attractive economically because while they cost little more to produce than SSI devices, they allowed more complex systems to be produced using smaller circuit boards, less assembly work (because of fewer separate components), and a number of other advantages.

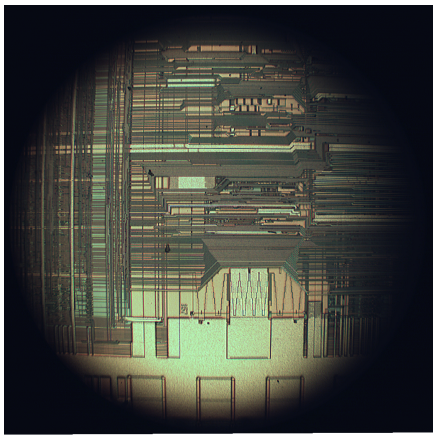
Further development, driven by the same economic factors, led to "**large-scale integration**" (**LSI**) in the mid 1970s, with tens of thousands of transistors per chip.

Integrated circuits such as 1K-bit RAMs, calculator chips, and the first microprocessors, that began to be manufactured in moderate quantities in the early 1970s, had under 4000 transistors. True LSI circuits, approaching 10,000 transistors, began to be produced around 1974, for computer main memories and second-generation microprocessors.

VLSI

The final step in the development process, starting in the 1980s and continuing through the present, was "very large-scale integration" (VLSI). The development started with hundreds of thousands of transistors in the early 1980s, and continues beyond several billion transistors as of 2009.

Multiple developments were required to achieve this increased density. Manufacturers moved to smaller design rules and cleaner fabrication facilities, so that they could make chips with more transistors and maintain adequate yield. The path of process improvements was summarized by the International Technology Roadmap for Semiconductors (ITRS). Design tools improved enough to make it practical to finish these designs in a reasonable time. The more energy efficient CMOS replaced NMOS and PMOS, avoiding a prohibitive increase in power consumption.



Upper interconnect layers on an Intel 80486DX2 microprocessor die

In 1986 the first one megabit RAM chips were introduced, which contained more than one million transistors. Microprocessor chips passed the million transistor mark in 1989 and the billion transistor mark in 2005.[17] The trend continues largely unabated, with chips introduced in 2007 containing tens of billions of memory transistors.[18]

ULSI, WSI, SOC and 3D-IC

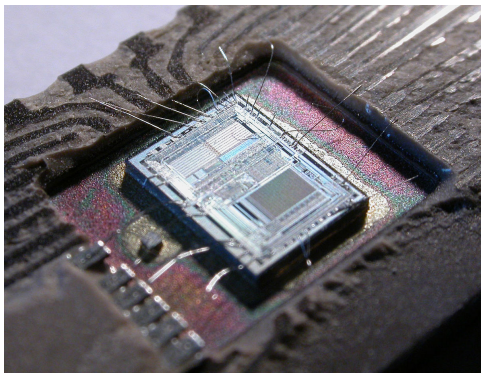
To reflect further growth of the complexity, the term *ULSI* that stands for "ultra-large-scale integration" was proposed for chips of complexity of more than 1 million transistors.

Wafer-scale integration (WSI) is a system of building very-large integrated circuits that uses an entire silicon wafer to produce a single "super-chip". Through a combination of large size and reduced packaging, WSI could lead to dramatically reduced costs for some systems, notably massively parallel supercomputers. The name is taken from the term Very-Large-Scale Integration, the current state of the art when WSI was being developed.

A system-on-a-chip (SoC or SOC) is an integrated circuit in which all the components needed for a computer or other system are included on a single chip. The design of such a device can be complex and costly, and building disparate components on a single piece of silicon may compromise the efficiency of some elements. However, these drawbacks are offset by lower manufacturing and assembly costs and by a greatly reduced power budget: because signals among the components are kept on-die, much less power is required (see Packaging).

A three-dimensional integrated circuit (3D-IC) has two or more layers of active electronic components that are integrated both vertically and horizontally into a single circuit. Communication between layers uses on-die signaling, so power consumption is much lower than in equivalent separate circuits. Judicious use of short vertical wires can substantially reduce overall wire length for faster operation.

Advances in integrated circuits



The die from an Intel 8742, an 8-bit microcontroller that includes a CPU running at 12 MHz, 128 bytes of RAM, 2048 bytes of EPROM, and I/O in the same chip

Among the most advanced integrated circuits are the microprocessors or "**cores**", which control everything from computers and cellular phones to digital microwave ovens. Digital memory chips and ASICs are examples of other families of integrated circuits that are important to the modern information society. While the cost of designing and developing a complex integrated circuit is quite high, when spread across typically millions of production units the individual IC cost is minimized. The performance of ICs is high because the small size allows short traces which in turn allows low power logic (such as CMOS) to be used at fast switching speeds.

ICs have consistently migrated to smaller feature sizes over the years, allowing more circuitry to be packed on each chip. This increased capacity per unit area can be used to decrease cost and/or increase functionality—see Moore's law which, in its modern interpretation, states that the number of transistors in an integrated circuit doubles every two years. In general, as the feature size shrinks, almost everything improves—the cost per unit and the switching power consumption go down, and the speed goes up. However, ICs with nanometer-scale devices are not without their problems, principal among which is leakage current (see subthreshold leakage for a discussion of this), although these problems are not insurmountable and will likely be solved or at least ameliorated by the introduction of high-k dielectrics. Since these speed and power consumption gains are apparent to the end user, there is fierce competition among the manufacturers to use finer geometries. This process, and the expected progress over the next few years, is well described by the International Technology Roadmap for Semiconductors (ITRS).

In current research projects, integrated circuits are also developed for sensoric applications in medical implants or other bioelectronic devices. Particular sealing strategies have to be taken in such biogenic environments to avoid corrosion or biodegradation of the exposed semiconductor materials.[19] As one of the few materials well established in CMOS technology, titanium nitride (TiN) turned out as exceptionally stable and well suited for electrode applications in medical implants.[20][21]

Classification

A CMOS 4000 IC in a DIP

Integrated circuits can be classified into analog, digital and mixed signal (both analog and digital on the same chip).

Digital integrated circuits can contain anything from one to millions of logic gates, flip-flops, multiplexers, and other circuits in a few square millimeters. The small size of these circuits allows high speed, low power dissipation, and reduced manufacturing cost compared with board-level integration. These digital ICs, typically microprocessors, DSPs, and micro controllers, work using binary mathematics to process "one" and "zero" signals.

Analog ICs, such as sensors, power management circuits, and operational amplifiers, work by processing continuous signals. They perform functions like amplification, active filtering, demodulation, and mixing. Analog ICs ease the burden on circuit designers by having expertly designed analog circuits available instead of designing a difficult analog circuit from scratch.

ICs can also combine analog and digital circuits on a single chip to create functions such as A/D converters and D/A converters. Such mixed-signal circuits offer smaller size and lower cost, but must carefully account for signal interference.

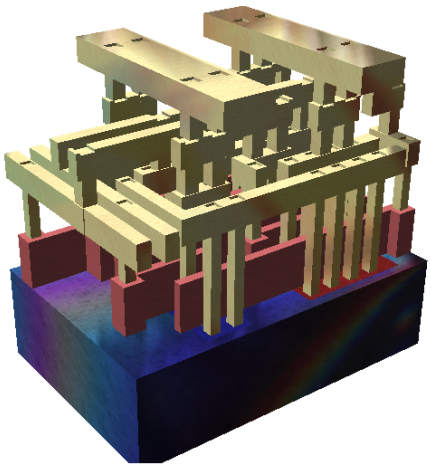
Modern electronic component distributors often further sub-categorize the huge variety of integrated circuits now available:

- Digital ICs are further sub-categorized as logic ICs, memory chips, interface ICs (level shifters, serializer/deserializer, etc.), Power Management ICs, and programmable devices.
- Analog ICs are further sub-categorized as linear ICs and RF ICs.
- mixed-signal integrated circuits are further sub-categorized as data acquisition ICs (including A/D converters, D/A converter, digital potentiometers) and clock/timing ICs.

Manufacturing

Fabrication

The semiconductors of the periodic table of the chemical elements were identified as the most likely materials for a *solid-state vacuum tube*. Starting with copper oxide, proceeding to germanium, then silicon, the materials were systematically studied in the 1940s and 1950s. Today, silicon monocrystals are the main substrate used for ICs although some III-V compounds of the periodic table such as gallium arsenide are used for specialized applications like LEDs, lasers, solar cells and the highest-speed integrated circuits. It took decades to perfect methods of creating crystals without defects in the crystalline structure of the semiconducting material.



Rendering of a small standard cell with three metal layers (dielectric has been removed). The sand-colored structures are metal interconnect, with the vertical pillars being contacts, typically plugs of tungsten. The reddish structures are polysilicon gates, and the solid at the bottom is the crystalline silicon bulk.

Semiconductor ICs are fabricated in a layer process which includes these key process steps:

- Imaging
- Deposition
- Etching

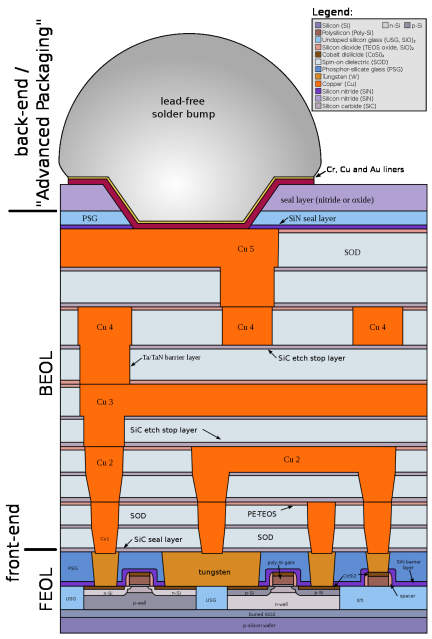
The main process steps are supplemented by doping and cleaning.

Mono-crystal silicon wafers (or for special applications, silicon on sapphire or gallium arsenide wafers) are used as the *substrate*. Photolithography is used to mark different areas of the substrate to be doped or to have polysilicon, insulators or metal (typically aluminium) tracks deposited on them.

- Integrated circuits are composed of many overlapping layers, each defined by photolithography, and normally shown in different colors. Some layers mark where various dopants are diffused into the substrate (called diffusion layers), some define where additional ions are implanted (implant layers), some define the conductors (polysilicon or metal layers), and some define the connections between the conducting layers (via or contact layers). All components are constructed from a specific combination of these layers.

- In a self-aligned CMOS process, a transistor is formed wherever the gate layer (polysilicon or metal) crosses a diffusion layer.
- Capacitive structures, in form very much like the parallel conducting plates of a traditional electrical capacitor, are formed according to the area of the "plates", with insulating material between the plates. Capacitors of a wide range of sizes are common on ICs.
- Meandering stripes of varying lengths are sometimes used to form on-chip resistors, though most logic circuits do not need any resistors. The ratio of the length of the resistive structure to its width, combined with its sheet resistivity, determines the resistance.
- More rarely, inductive structures can be built as tiny on-chip coils, or simulated by gyrators.

Since a CMOS device only draws current on the *transition* between logic states, CMOS devices consume much less current than bipolar devices.



Schematic structure of a CMOS chip, as built in the early 2000s. The graphic shows LDD-MISFET's on an SOI substrate with five metallization layers and solder bump for flip-chip bonding. It also shows the section for FEOL (front-end of line), BEOL (back-end of line) and first parts of back-end process.

A random access memory is the most regular type of integrated circuit; the highest density devices are thus memories; but even a microprocessor will have memory on the chip. (See the regular array structure at the bottom of the first image.) Although the structures are intricate – with widths which have been shrinking for decades – the layers remain much thinner than the device widths. The layers of material are fabricated much like a photographic process, although light waves in the visible spectrum cannot be used to "expose" a layer of material, as they would be too large for the features. Thus photons of higher frequencies (typically ultraviolet) are used to create the patterns for each layer. Because each feature is so small, electron microscopes are essential tools for a process engineer who might be debugging a fabrication process.

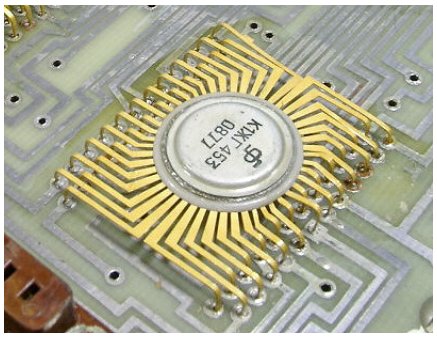
Each device is tested before packaging using automated test equipment (ATE), in a process known as wafer testing, or wafer probing. The wafer is then cut into rectangular blocks, each of which is called a *die*. Each good die (plural *dice*, *dies*, or *die*) is then connected into a package using aluminium (or gold) bond wires which are thermosonic bonded[22] to *pads*, usually found around the edge of the die. . Thermosonic bonding was first introduced by A. Coucoulas which provided a reliable means of forming these vital electrical connections to the outside world. After packaging, the devices go through final testing on the same or similar ATE used during wafer probing. Industrial CT scanning can also be used. Test cost can account for over 25% of the cost of fabrication on lower cost products, but can be negligible on low yielding, larger, and/or higher cost devices.

As of 2005, a fabrication facility (commonly known as a *semiconductor fab*) costs over US$1 billion to construct,[23] because much of the operation is automated. Today, the most advanced processes employ the following techniques:

- The wafers are up to 300 mm in diameter (wider than a common dinner plate).
- Use of 32 nanometer or smaller chip manufacturing process. Intel, IBM, NEC, and AMD are using ~32 nanometers for their CPU chips. IBM and AMD introduced immersion lithography for their 45 nm processes[24]
- Copper interconnects where copper wiring replaces aluminium for interconnects.
- Low-K dielectric insulators.
- Silicon on insulator (SOI)
- Strained silicon in a process used by IBM known as strained silicon directly on insulator (SSDOI)
- Multigate devices such as tri-gate transistors being manufactured by Intel from 2011 in their 22 nm process.

Packaging

The earliest integrated circuits were packaged in ceramic flat packs, which continued to be used by the military for their reliability and small size for many years. Commercial circuit packaging quickly moved to the dual in-line package (DIP), first in ceramic and later in plastic. In the 1980s pin counts of VLSI circuits exceeded the practical limit for DIP packaging, leading to pin grid array (PGA) and leadless chip carrier (LCC) packages. Surface mount packaging appeared in the early 1980s and became popular in the late 1980s, using finer lead pitch with leads formed as either gull-wing or J-lead, as exemplified by small-outline integrated circuit – a carrier which occupies an area about 30–50% less than an equivalent DIP, with a typical thickness that is 70% less. This package has "gull wing" leads protruding from the two long sides and a lead spacing of 0.050 inches.



A Soviet MSI nMOS chip made in 1977, part of a four-chip calculator set designed in 1970[25]

In the late 1990s, plastic quad flat pack (PQFP) and thin small-outline package (TSOP) packages became the most common for high pin count devices, though PGA packages are still often used for high-end microprocessors. Intel and AMD are currently transitioning from PGA packages on high-end microprocessors to land grid array (LGA) packages.

Ball grid array (BGA) packages have existed since the 1970s. Flip-chip Ball Grid Array packages, which allow for much higher pin count than other package types, were developed in the 1990s. In an FCBGA package the die is mounted upside-down (flipped) and connects to the package balls via a package substrate that is similar to a printed-circuit board rather than by wires. FCBGA packages allow an array of input-output signals (called Area-I/O) to be distributed over the entire die rather than being confined to the die periphery.

Traces out of the die, through the package, and into the printed circuit board have very different electrical properties, compared to on-chip signals. They require special design techniques and need much more electric power than signals confined to the chip itself.

When multiple dies are put in one package, it is called SiP, for *System In Package*. When multiple dies are combined on a small substrate, often ceramic, it's called an MCM, or Multi-Chip Module. The boundary between a big MCM and a small printed circuit board is sometimes fuzzy.

Chip labeling and manufacture date

Most integrated circuits large enough to include identifying information include four common sections: the manufacturer's name or logo, the part number, a part production batch number and/or serial number, and a four-digit code that identifies when the chip was manufactured. Extremely small surface mount technology parts often bear only a number used in a manufacturer's lookup table to find the chip characteristics.

The manufacturing date is commonly represented as a two-digit year followed by a two-digit week code, such that a part bearing the code 8341 was manufactured in week 41 of 1983, or approximately in October 1983.

Legal protection of semiconductor chip layouts

Like most of the other forms of intellectual property, IC layout designs are creations of the human mind. They are usually the result of an enormous investment, both in terms of the time of highly qualified experts, and financially. There is a continuing need for the creation of new layout-designs which reduce the dimensions of existing integrated circuits and simultaneously increase their functions. The smaller an integrated circuit, the less the material needed for its manufacture, and the smaller the space needed to accommodate it. Integrated circuits are utilized in a large range of products, including articles of everyday use, such as watches, television sets, appliances, automobiles, etc.,

as well as sophisticated data processing equipment.

The possibility of copying by photographing each layer of an integrated circuit and preparing photomasks for its production on the basis of the photographs obtained is the main reason for the introduction of legislation for the protection of layout-designs.

A diplomatic conference was held at Washington, D.C., in 1989, which adopted a Treaty on Intellectual Property in Respect of Integrated Circuits (IPIC Treaty).

The Treaty on Intellectual Property in respect of Integrated Circuits, also called Washington Treaty or IPIC Treaty (signed at Washington on 26 May 1989) is currently not in force, but was partially integrated into the TRIPS agreement.

National laws protecting IC layout designs have been adopted in a number of countries.

Other developments

In the 1980s, programmable logic devices were developed. These devices contain circuits whose logical function and connectivity can be programmed by the user, rather than being fixed by the integrated circuit manufacturer. This allows a single chip to be programmed to implement different LSI-type functions such as logic gates, adders and registers. Current devices called field-programmable gate arrays can now implement tens of thousands of LSI circuits in parallel and operate up to 1.5 GHz (Achronix holding the speed record).

The techniques perfected by the integrated circuits industry over the last three decades have been used to create very small mechanical devices driven by electricity using a technology known as microelectromechanical systems. These devices are used in a variety of commercial and military applications. Example commercial applications include DLP projectors, inkjet printers, and accelerometers used to deploy automobile airbags.

In the past, radios could not be fabricated in the same low-cost processes as microprocessors. But since 1998, a large number of radio chips have been developed using CMOS processes. Examples include Intel's DECT cordless phone, or Atheros's 802.11 card.

Future developments seem to follow the multi-core multi-microprocessor paradigm, already used by the Intel and AMD dual-core processors. Rapport Inc. and IBM started shipping the KC256 in 2006, a 256-core microprocessor. Intel, as recently as February–August 2011, unveiled a prototype, "not for commercial sale" chip that bears 80 cores. Each core is capable of handling its own task independently of the others. This is in response to the heat-versus-speed limit that is about to be reached using existing transistor technology (see: thermal design power). This design provides a new challenge to chip programming. Parallel programming languages such as the open-source X10 programming language are designed to assist with this task.[26]

Since the early 2000s, the integration of optical functionality into silicon chips has been actively pursued in both academic research and in industry resulting in the successful commercialization of silicon based integrated optical transceivers combining optical devices (modulators, detectors, routing) with CMOS based electronics.[27]

Silicon labelling and graffiti

To allow identification during production most silicon chips will have a serial number in one corner. It is also common to add the manufacturer's logo. Ever since ICs were created, some chip designers have used the silicon surface area for surreptitious, non-functional images or words. These are sometimes referred to as Chip Art, *Silicon Art*, *Silicon Graffiti* or *Silicon Doodling*.

ICs and IC families

- The 555 timer IC
- The 741 operational amplifier
- 7400 series TTL logic building blocks
- 4000 series, the CMOS counterpart to the 7400 series (see also: 74HC00 series)
- Intel 4004, the world's first microprocessor, which led to the famous 8080 CPU and then the IBM PC's 8088, 80286, 486 etc.
- The MOS Technology 6502 and Zilog Z80 microprocessors, used in many home computers of the early 1980s
- The Motorola 6800 series of computer-related chips, leading to the 68000 and 88000 series (used in some Apple computers and in the 1980s Commodore Amiga series).

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Silicon graffiti

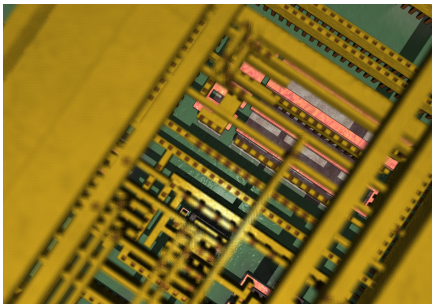
- The Chipworks silicon art gallery (http://www.chipworks.com/silicon_art_gallery.aspx)

Integrated circuit die photographs

- IC Die Photography (http://diephotos.blogspot.com/) – A gallery of IC die photographs

Microfabrication

Microfabrication is the term that describes processes of fabrication of miniature structures, of micrometre sizes and smaller. Historically the earliest microfabrication processes were used for integrated circuit fabrication, also known as "semiconductor manufacturing" or "semiconductor device fabrication". In the last two decades microelectromechanical systems (MEMS), microsystems (European usage), micromachines (Japanese terminology) and their subfields, microfluidics/lab-on-a-chip, optical MEMS (also called MOEMS), RF MEMS, PowerMEMS, BioMEMS and their extension into nanoscale (for example NEMS, for nano electro mechanical systems) have re-used, adapted or extended microfabrication methods. Flat-panel displays and solar cells are also using similar techniques.



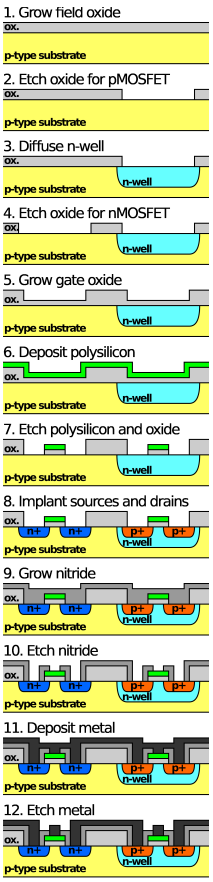
Synthetic detail of a micromanufactured integrated circuit through four layers of planarized copper interconnect, down to the polysilicon (pink), wells (greyish) and substrate (green)

Miniaturization of various devices presents challenges in many areas of science and engineering: physics, chemistry, material science, computer science, ultra-precision engineering, fabrication processes, and equipment design. It is also giving rise to various kinds of interdisciplinary research.[1] The major concepts and principles of microfabrication are microlithography, doping, thin films, etching, bonding, and polishing.

Fields of Use

Microfabricated devices include:

- Fabrication of integrated circuits (“microchips”) (see semiconductor manufacturing)
- Microelectromechanical systems (MEMS), MOEMS,
- microfluidic devices (ink jet print heads)
- solar cells
- Flat Panel Displays (see AMLCD and Thin Film Transistor)
- Sensors (micro-sensors) (biosensors, nanosensors)
- PowerMEMSs, fuel cells, energy harvesters/scavengers



Simplified illustration of the process of fabrication of a CMOS inverter on p-type substrate in semiconductor microfabrication. Each etch step is detailed in the following image. Note: Gate, source and drain contacts are not normally in the same plane in real devices, and the diagrams are not to scale.

Origins

Microfabrication technologies originate from the microelectronics industry, and the devices are usually made on silicon wafers even though glass, plastics and many other substrate are in use. Micromachining, semiconductor processing, microelectronic fabrication, semiconductor fabrication, MEMS fabrication and integrated circuit technology are terms used instead of microfabrication, but microfabrication is the broad general term.

Traditional machining techniques such as *electro-discharge machining*, *spark erosion machining*, and *laser drilling* have been scaled from the millimeter size range to micrometer range, but they do not share the main idea of microelectronics-originated microfabrication: replication and parallel fabrication of hundreds or millions of identical structures. This parallelism is present in various imprint, casting and moulding techniques which have successfully been applied in the microregime. For example, injection moulding of DVDs involves fabrication of submicrometer-sized spots on the disc.

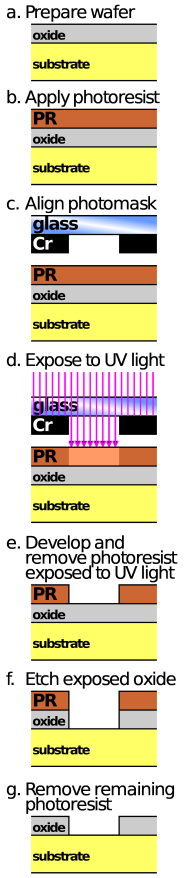
Microfabrication processes

Microfabrication is actually a collection of technologies which are utilized in making microdevices. Some of them have very old origins, not connected to manufacturing, like lithography or etching. Polishing was borrowed from optics manufacturing, and many of the vacuum techniques come from 19th century physics research. Electroplating is also a 19th century technique adapted to produce micrometre scale structures, as are various stamping and embossing techniques.

To fabricate a microdevice, many processes must be performed, one after the other, many times repeatedly. These processes typically include depositing a film, patterning the film with the desired micro features, and removing (or etching) portions of the film. For example, in memory chip fabrication there are some 30 lithography steps, 10 oxidation steps, 20 etching steps, 10 doping steps, and many others are performed. The complexity of microfabrication processes can be described by their *mask count*. This is the number of different pattern layers that constitute the final device. Modern microprocessors are made with 30 masks while a few masks suffice for a microfluidic device or a laser diode. Microfabrication resembles multiple exposure photography, with many patterns aligned to each other to create the final structure.

Substrates

Microfabricated devices are not generally freestanding devices but are usually formed over or in a thicker support substrate. For electronic applications, semiconducting substrates such as silicon wafers can be used. For optical devices or flat panel displays, transparent substrates such as glass or quartz are common. The substrate enables easy handling of the micro device through the many fabrication steps. Often many individual devices are made together on one substrate and then singulated into separated devices toward the end of fabrication.



Detail of an etch step.

Deposition or Growth

Microfabricated devices are typically constructed using one or more thin films (see Thin film deposition). The purpose of these thin films depends on the type of device. Electronic devices may have thin films which are conductors (metals), insulators (dielectrics) or semiconductors. Optical devices may have films which are reflective, transparent, light guiding or scattering. Films may also have a chemical or mechanical purpose as well as for MEMS applications. Examples of deposition techniques include:

- Thermal oxidation
- chemical vapor deposition (CVD)
  - APCVD
  - LPCVD
  - PECVD
- Physical vapor deposition(PVD)
  - sputtering
  - evaporative deposition
  - Electron beam PVD
- epitaxy

Patterning

It is often desirable to pattern a film into distinct features or to form openings (or vias) in some of the layers. These features are on the micrometer or nanometer scale and the patterning technology is what defines microfabrication. The patterning technique typically uses a 'mask' to define portions of the film which will be removed. Examples of patterning techniques include:

- Photolithography
- Shadow Masking

Etching

Etching is the removal of some portion of the thin film or substrate. The substrate is exposed to an etching (such as an acid or plasma) which chemically or physically attacks the film until it is removed. Etching techniques include:

- Dry etching (Plasma etching) such as Reactive-ion etching (RIE) or Deep reactive-ion etching(DRIE)
- Wet etching or Chemical Etching

Other

A wide variety of other processes for cleaning, planarizing, or modifying the chemical properties of the microfabricated devices can also be performed. Some examples include:

- Doping by either thermal diffusion or ion implantation
- Chemical-mechanical planarization (CMP)
- Wafer cleaning, also known as "surface preparation" (see below)
- Wire bonding

Micro cutting / microfabrication

Micro cutting/milling is an alternative to lithographic techniques, by downscaling macro processes such as cutting and forming, to tool sizes under 100 μm in diameter.

Cleanliness in wafer fabrication

Microfabrication is carried out in cleanrooms, where air has been filtered of particle contamination and temperature, humidity, vibrations and electrical disturbances are under stringent control. Smoke, dust, bacteria and cells are micrometers in size, and their presence will destroy the functionality of a microfabricated device.

Cleanrooms provide passive cleanliness but the wafers are also actively cleaned before every critical step. RCA-1 clean in ammonia-peroxide solution removes organic contamination and particles; RCA-2 cleaning in hydrogen chloride-peroxide mixture removes metallic impurities. Sulfuric acid-peroxide mixture (a.k.a. Piranha) removes organics. Hydrogen fluoride removes native oxide from silicon surface. These are all wet cleaning steps in solutions. Dry cleaning methods include oxygen and argon plasma treatments to remove unwanted surface layers, or hydrogen bake at elevated temperature to remove native oxide before epitaxy. Pre-gate cleaning is the most critical cleaning step in CMOS fabrication: it ensures that the ca. 2 nm thick oxide of a MOS transistor can be grown in an orderly fashion. Oxidation, and all high temperature steps are very sensitive to contamination, and cleaning steps must precede high temperature steps.

Surface preparation is just a different viewpoint, all the steps are the same as described above: it is about leaving the wafer surface in a controlled and well known state before you start processing. Wafers are contaminated by previous process steps (e.g. metals bombarded from chamber walls by energetic ions during ion implantation), or they may have gathered polymers from wafer boxes, and this might be different depending on wait time.

Wafer cleaning and surface preparation work a little bit like the machines in a bowling alley: first they remove all unwanted bits and pieces, and then they reconstruct the desired pattern so that the game can go on.

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External links

- Videos and animations on microfabrication techniques and related applications (http://www.memsuniverse.com/?p=1156).
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