Pipelined Architecture (2A)

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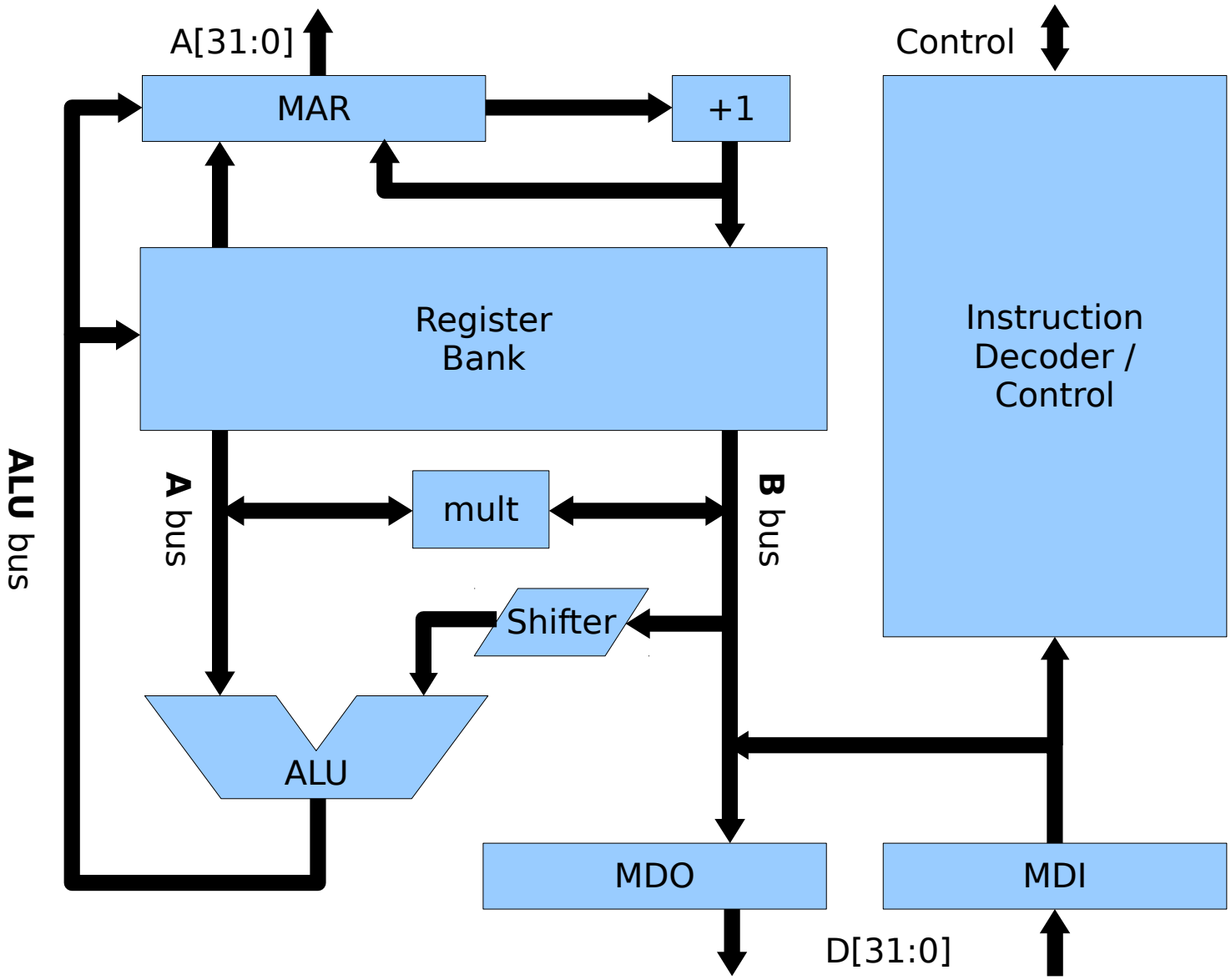
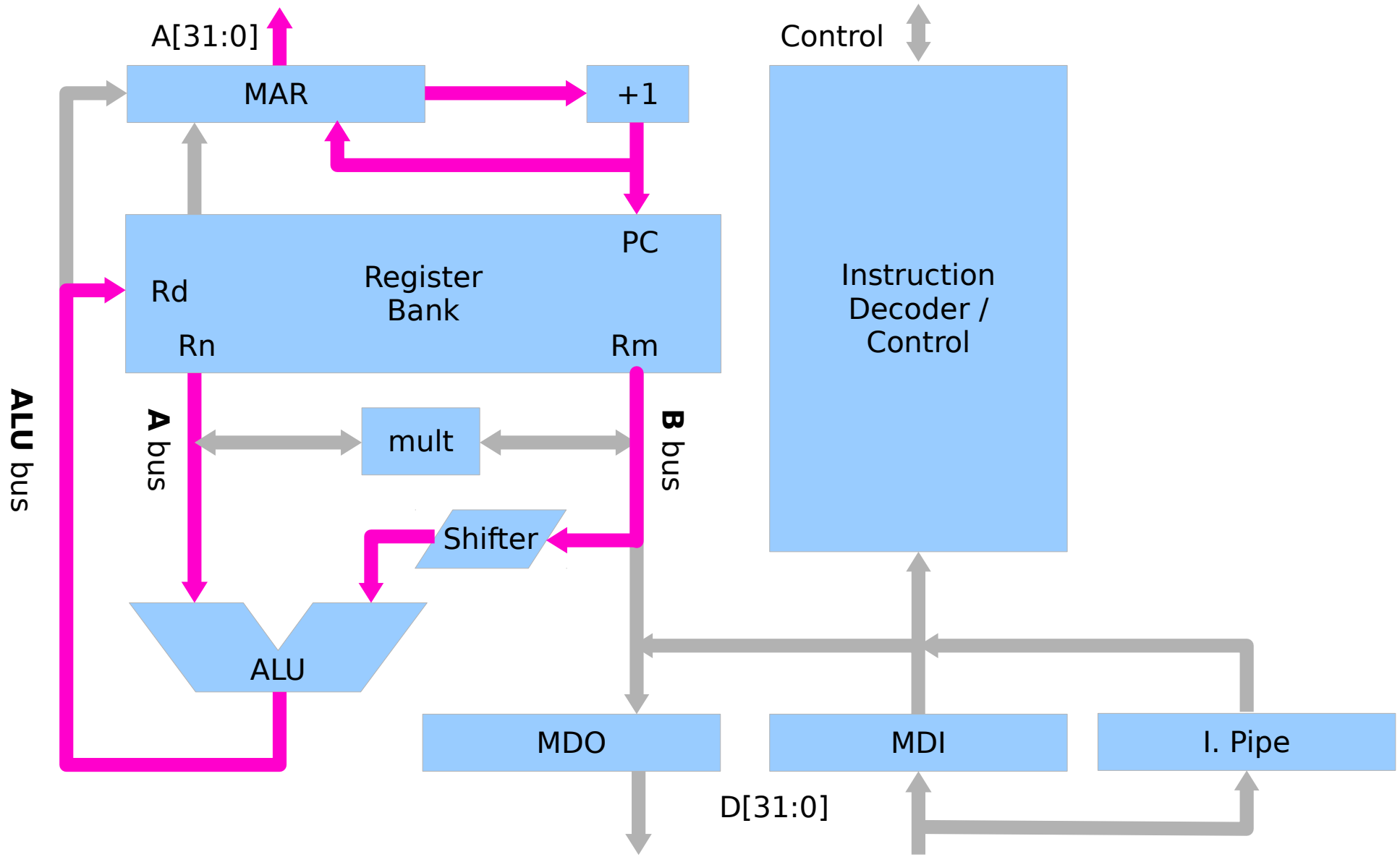
Based on

ARM System-on-Chip Architecture, 2nd ed, Steve Furber

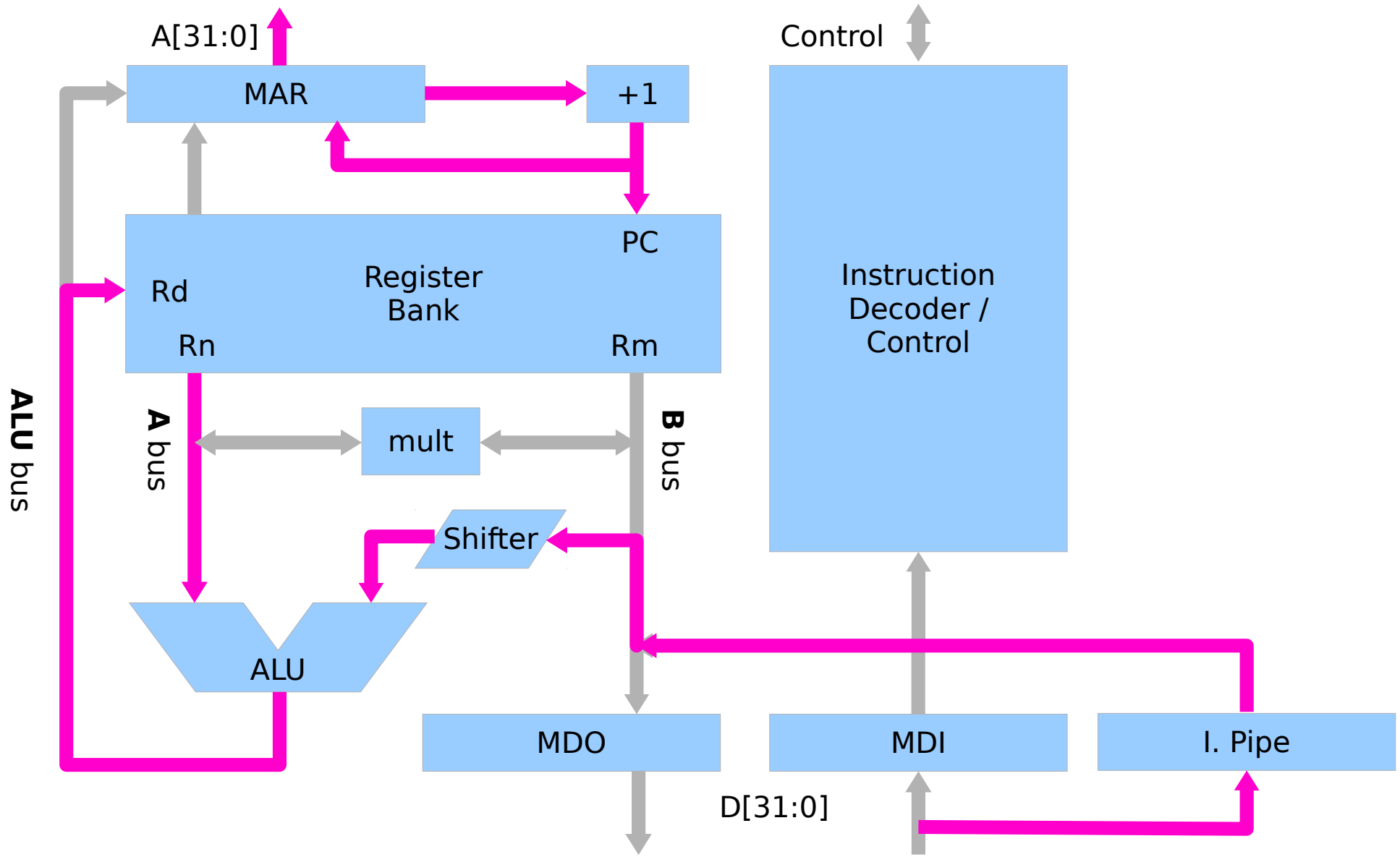
3-stage Pipeline



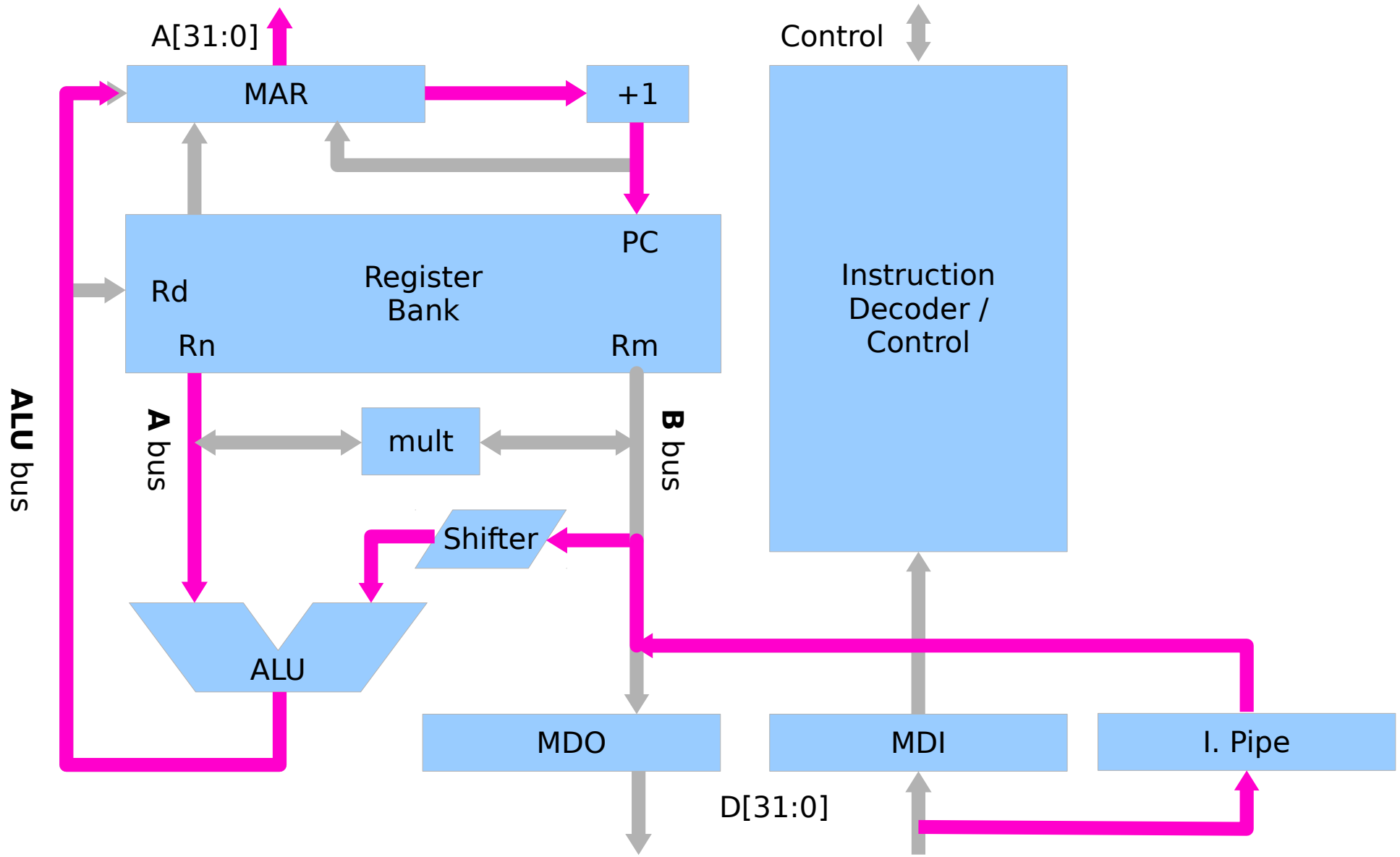
Register-Register Operations



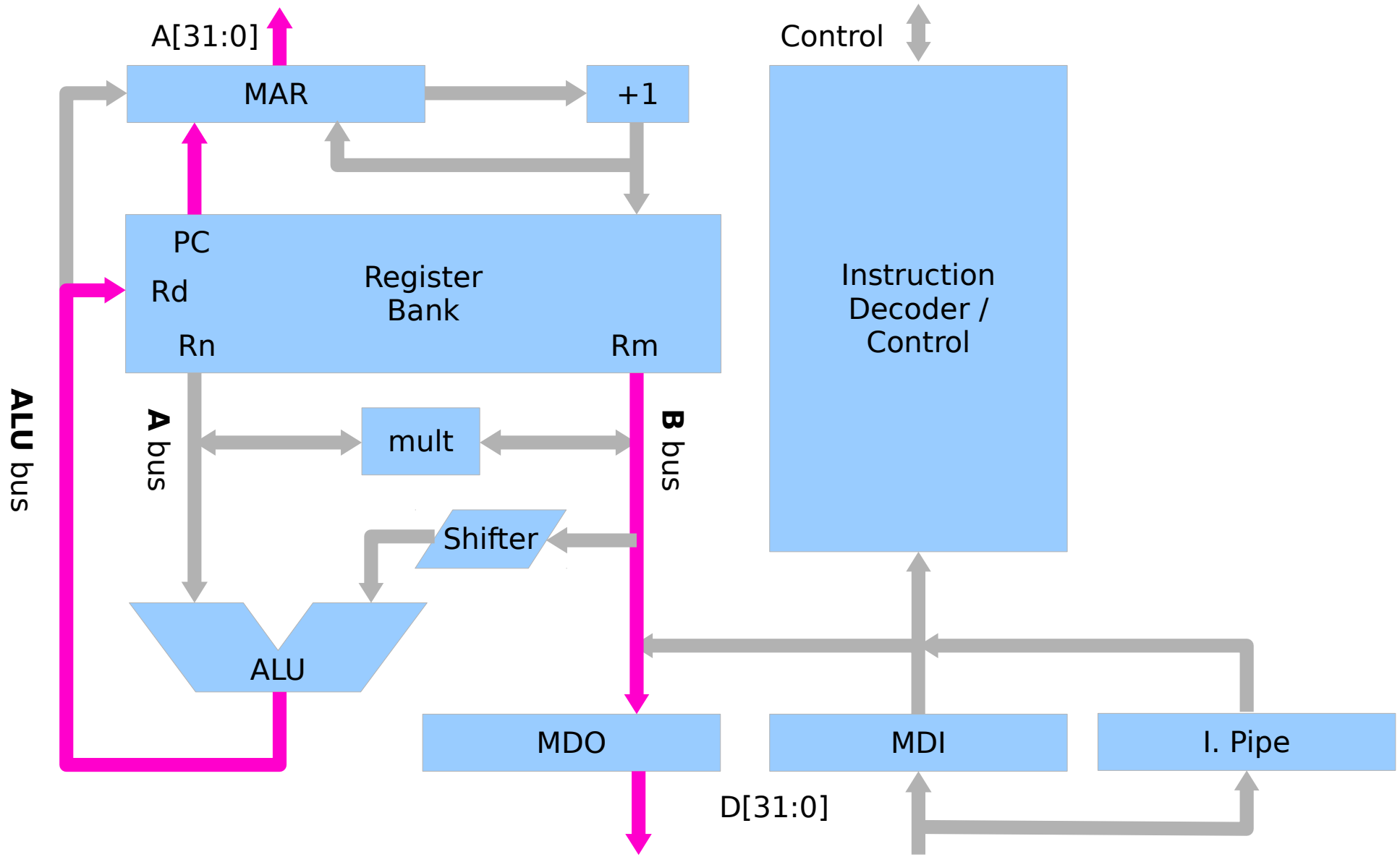
Register-Immediate Operations



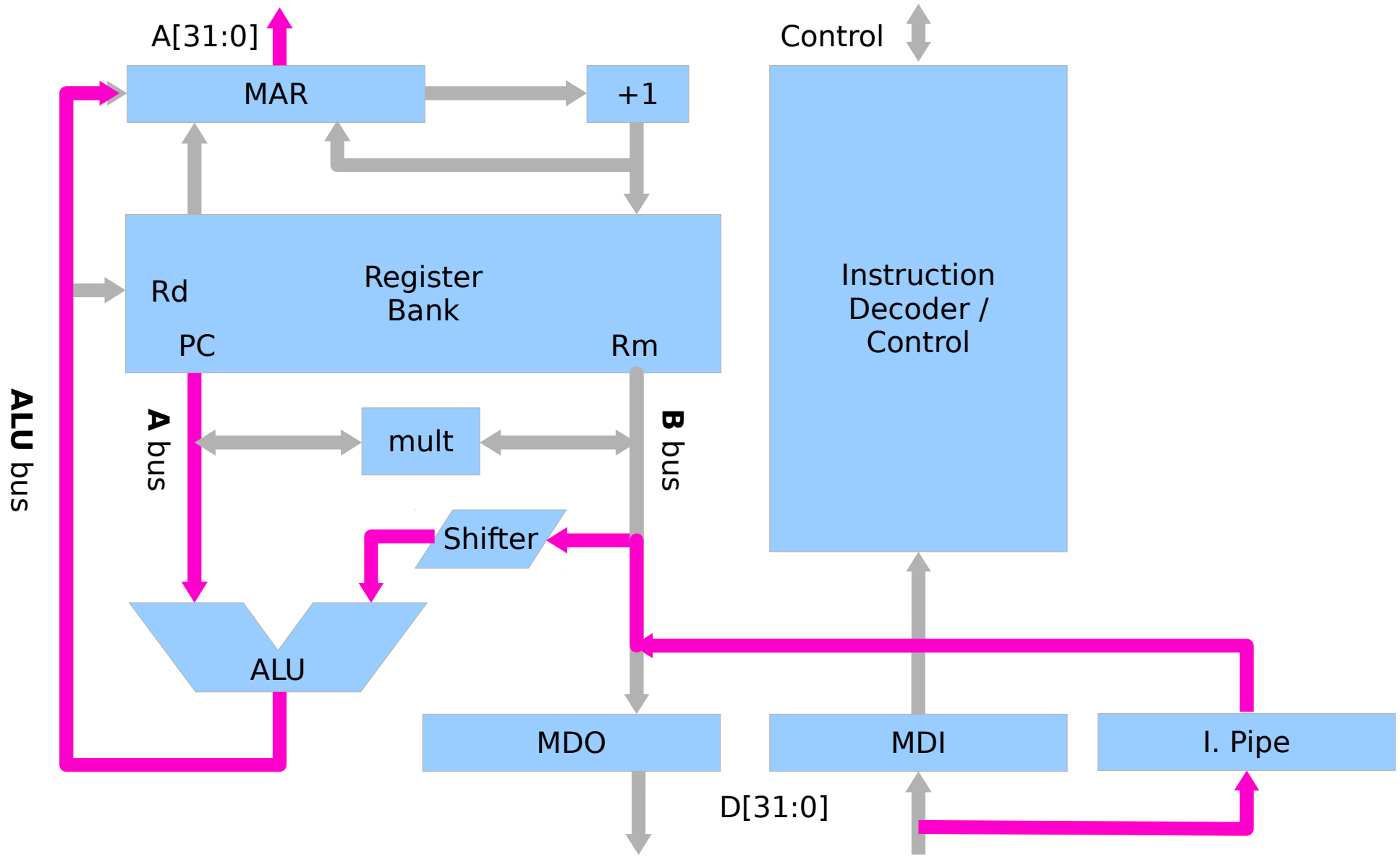
STR - 1st Cycle



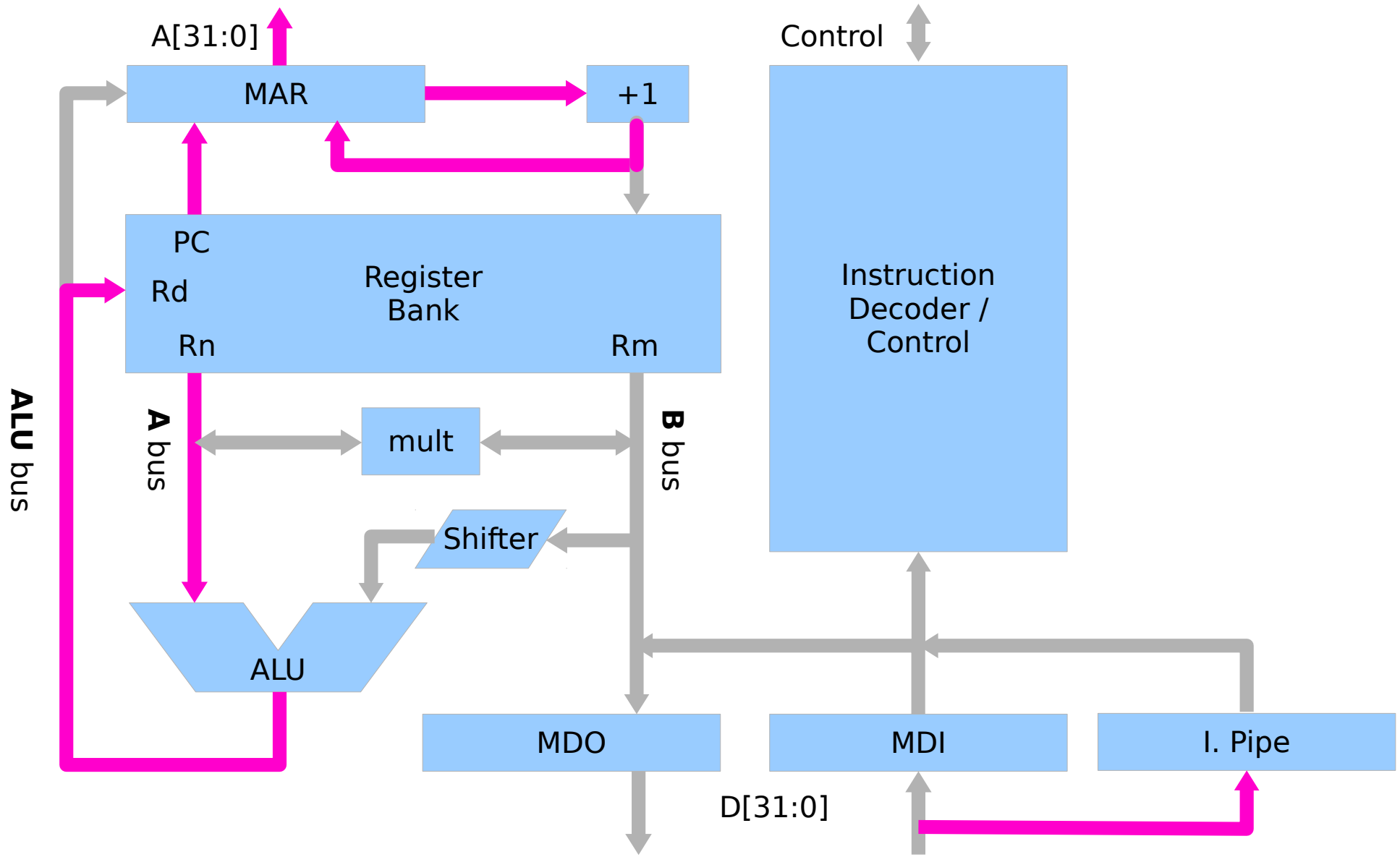
STR - 2nd Cycle



B - 1st Cycle


A[31:0]
Control
MAR
+1
Rd
Register
Bank
PC
Rm
Instruction
Decoder /
Control
ALU bus
A bus
mult
B bus
Shifter
ALU
MDO
MDI
I. Pipe
D[31:0]

B - 2nd Cycle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B bus
Shifter
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MDI
I. Pipe
D[31:0]

ARM Instruction Set

The load-store architecture

3-address data processing instructions

(2 source registers + 1 destination register)

Conditionally executes every instruction

Multiple data transfer instruction

Single cycle execution of shift and ALU operations

Open instruction set for coprocessors

A very dense 16-bit compressed instruction set (Thumb)

3-stage

fetch

- the instruction is fetched from memory
- it is placed in the instruction pipeline

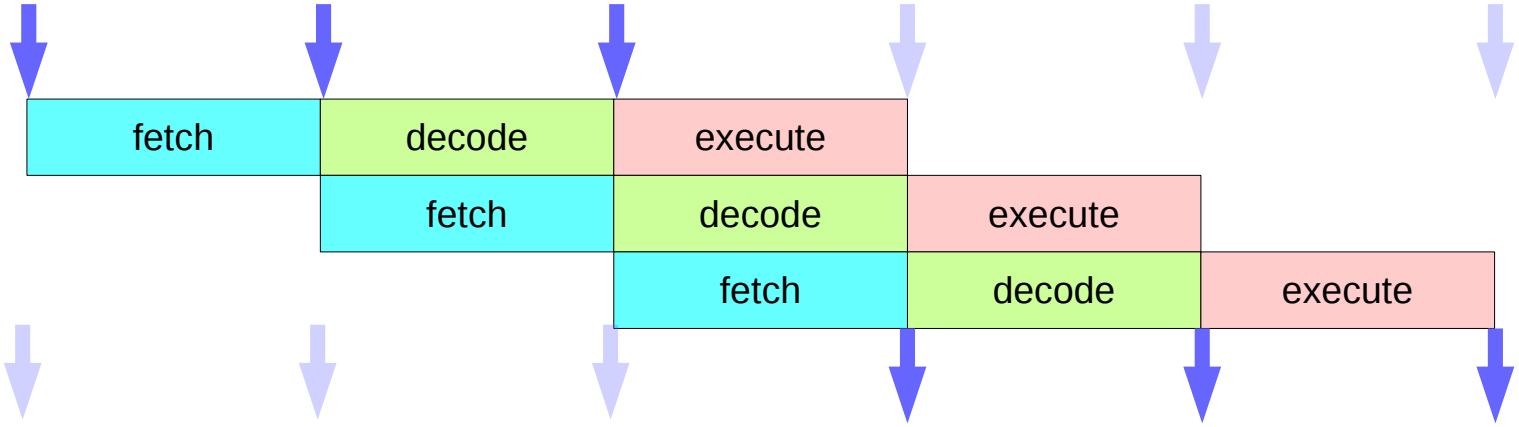
decode

- the instruction is decoded
- next cycle control signal is prepared
- the decode logic but not the datapath is dedicated

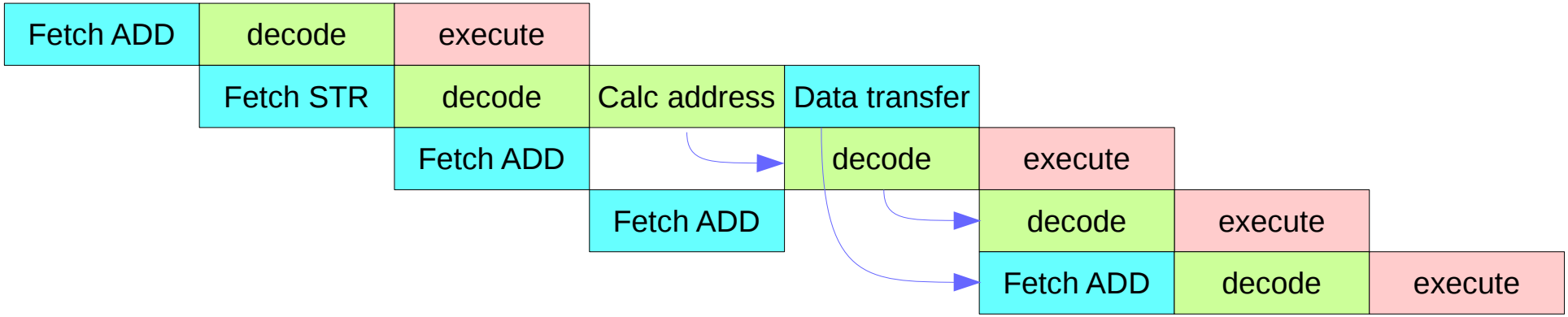
execute

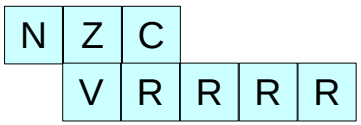
- the datapath is dedicated
  - reading the register bank
  - shifting an operand
  - performing ALU operations
  - writing back the result into the register bank

3 stage pipeline – single cycle



3-stage pipeline – multi-cycle





ARM Exception Handling

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
N	Z	C	V	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

References

[1] ftp://ftp.geoinfo.tuwien.ac.at/navratil/HaskellTutorial.pdf
[2] https://www.umiacs.umd.edu/~hal/docs/daume02yaht.pdf