

Carry Skip Adder (5A)

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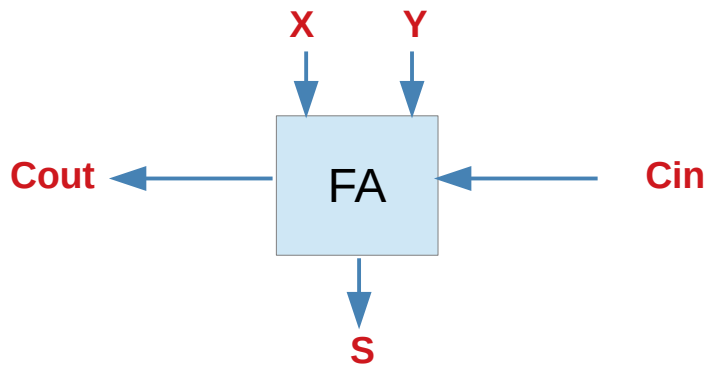
https://en.wikipedia.org/wiki/AND_gate
https://en.wikipedia.org/wiki/OR_gate
https://en.wikipedia.org/wiki/XOR_gate
https://en.wikipedia.org/wiki/NAND_gate

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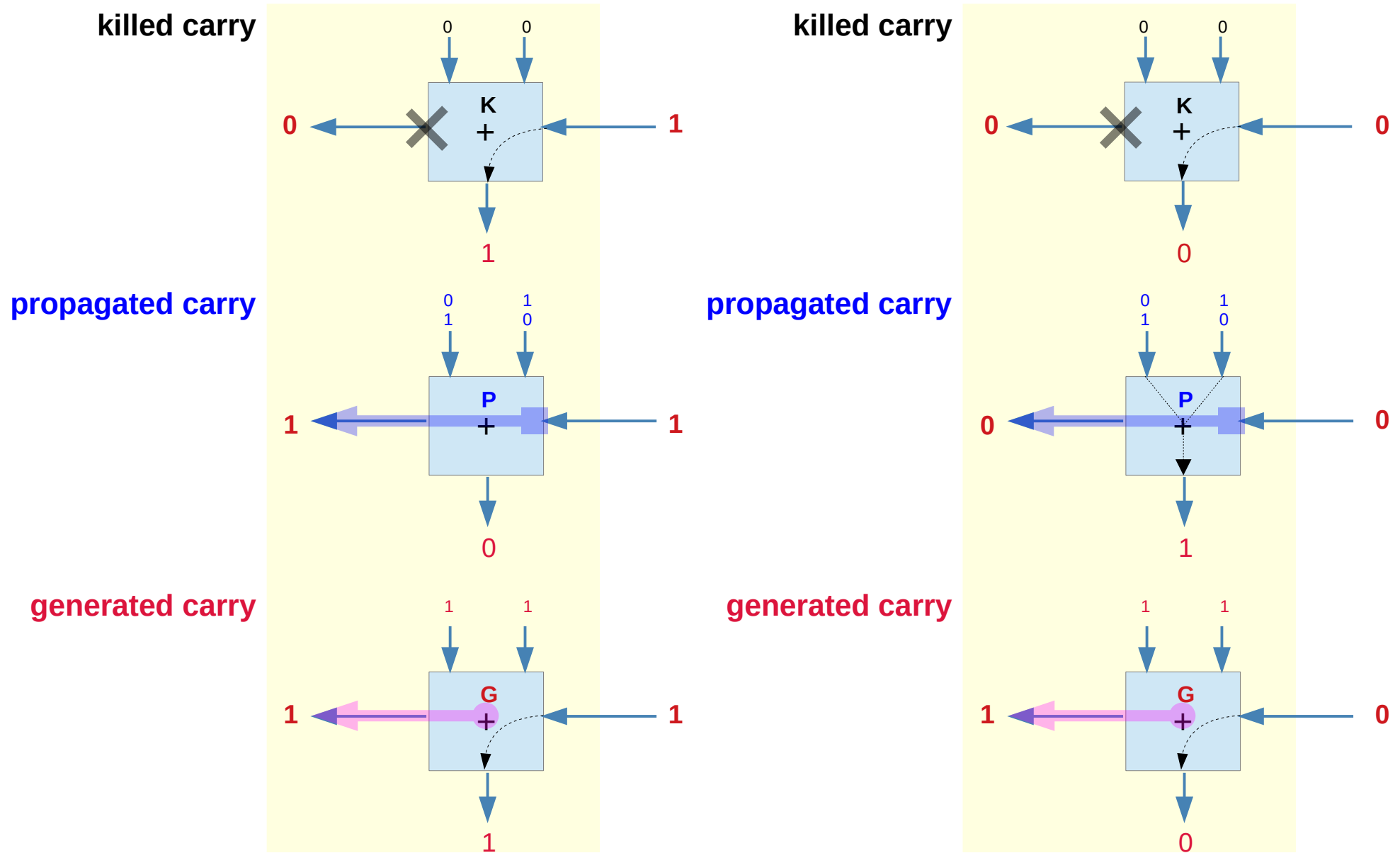
Carry Kill, Propagate, Generate conditions (1)

X	Y		
0	0	K	Kill ($=\bar{P}\bar{G}$)
0	1	P	Propagate
1	0	P	Propagate
1	1	G	Generate



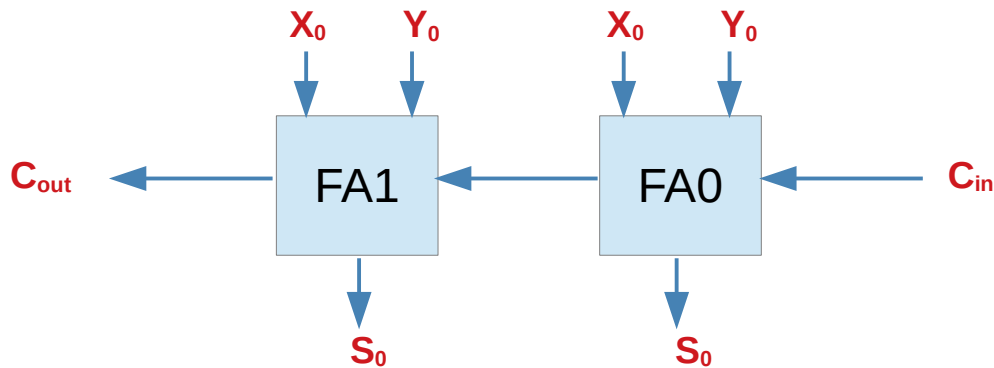
<https://electronics.stackexchange.com/questions/21251/critical-path-for-carry-skip-adder>

Carry Kill, Propagate, Generate conditions (2)



K, P, and G conditions in a 2-bit adder (1)

X	Y		
0	0	K	Kill ($=\bar{P}G$)
0	1	P	Propagate
1	0	P	Propagate
1	1	G	Generate



Unless the two FA's are in **propagate** mode, the transition of C_{in} does not affect the transition of C_{out}

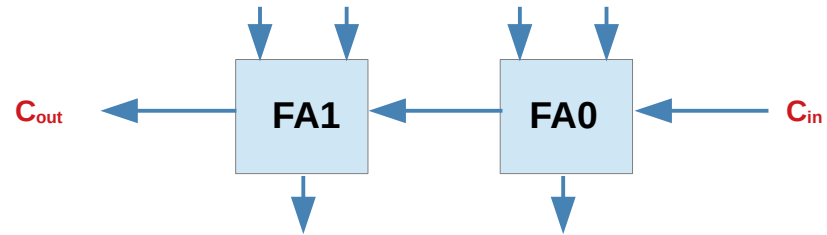
Critical path – all FA's in **propagate** mode

Broken paths for any FA in other mode
- kill mode, **generate** mode

<https://electronics.stackexchange.com/questions/21251/critical-path-for-carry-skip-adder>

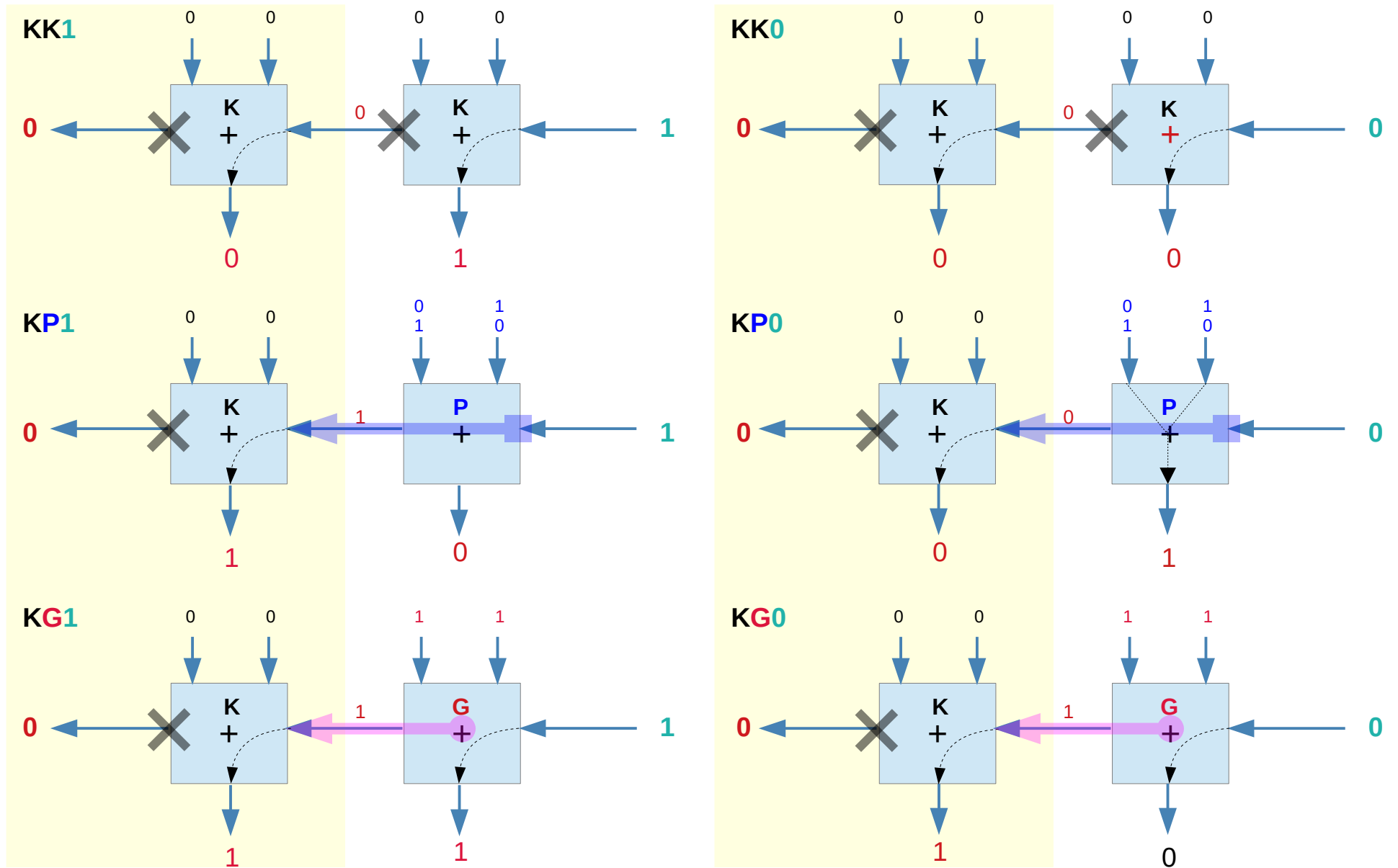
K, P, and G conditions in a 2-bit adder (2)

X	Y		
0	0	K	Kill ($=\bar{P}G$)
0	1	P	Propagate
1	0	P	Propagate
1	1	G	Generate

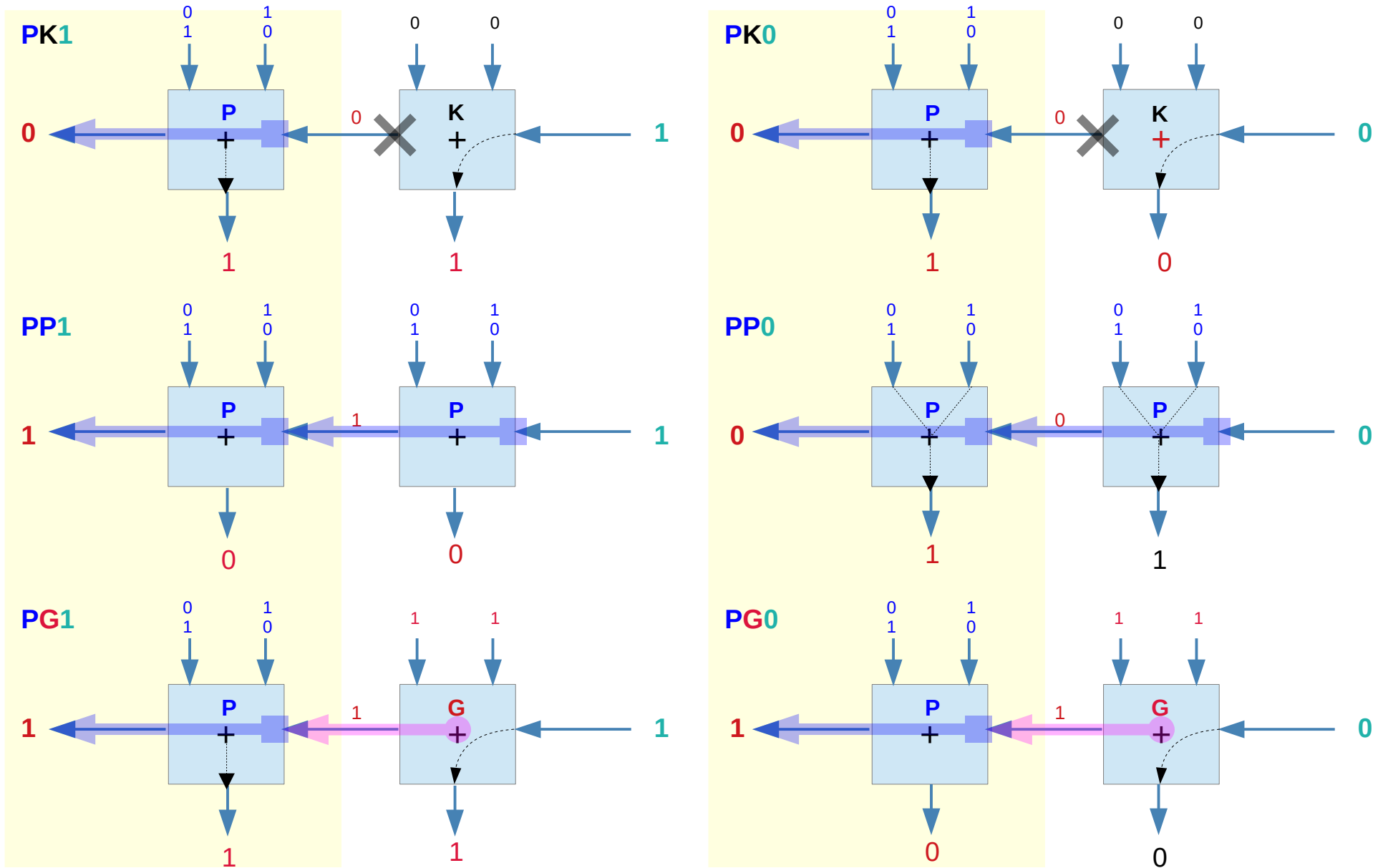


K	K	0
K	K	1
K	P	0
K	P	1
K	G	0
K	G	1
P	K	0
P	K	1
P	P	0
P	P	1
P	G	0
P	G	1
G	K	0
G	K	1
G	P	0
G	P	1
G	G	0
G	G	1

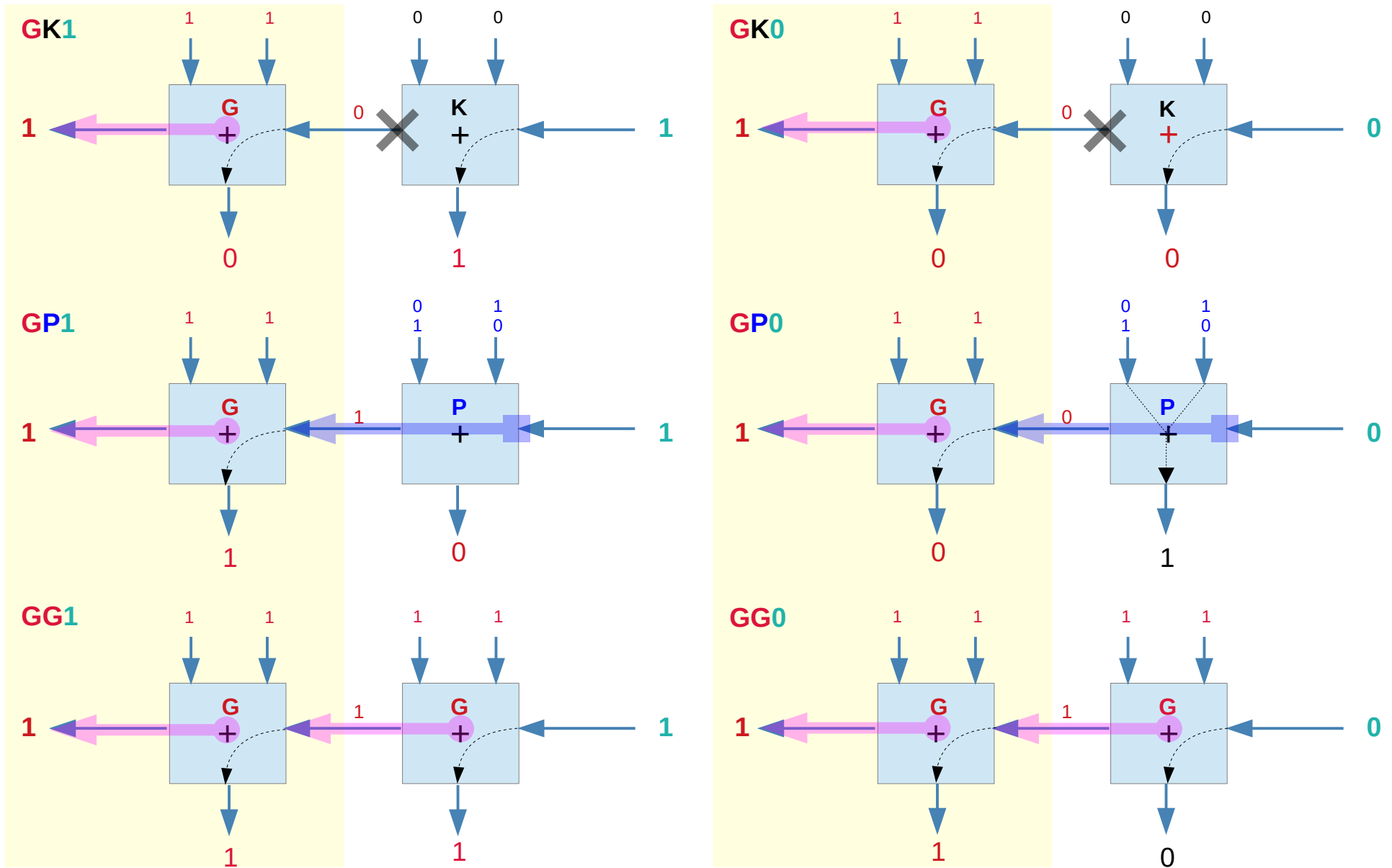
1. Cases when **FA1** is in the **K** mode



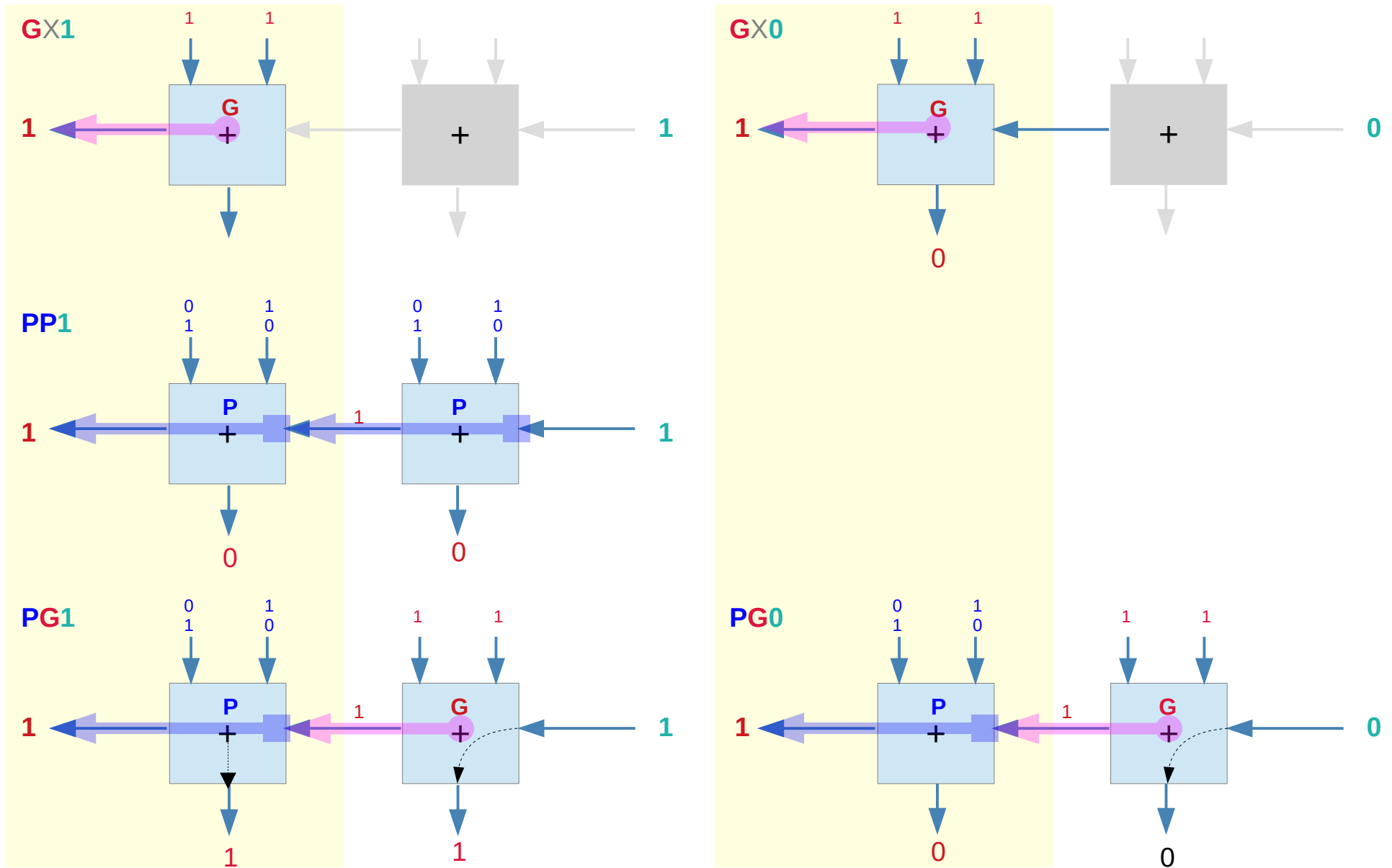
2. Cases when **FA1** is in the **P** mode



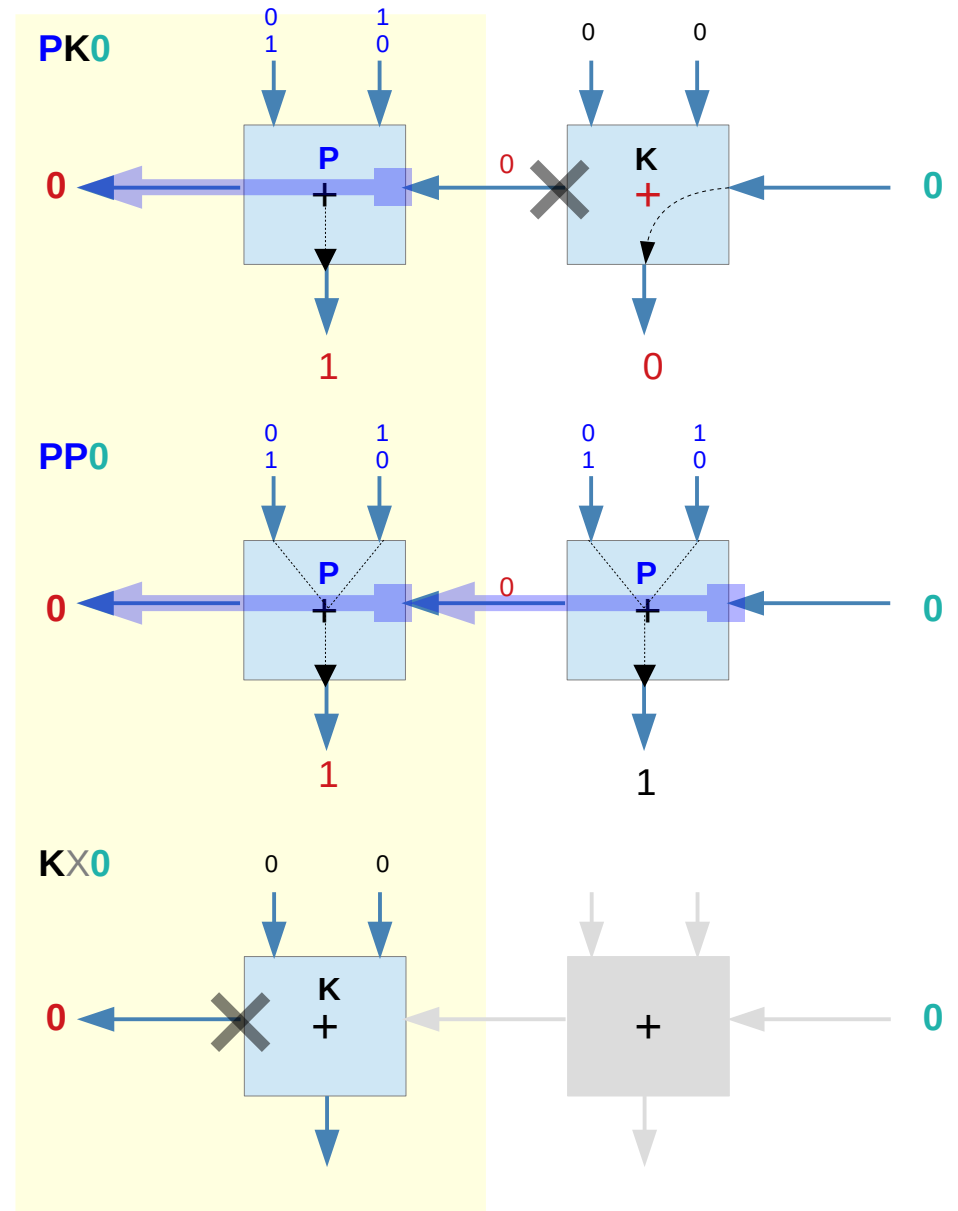
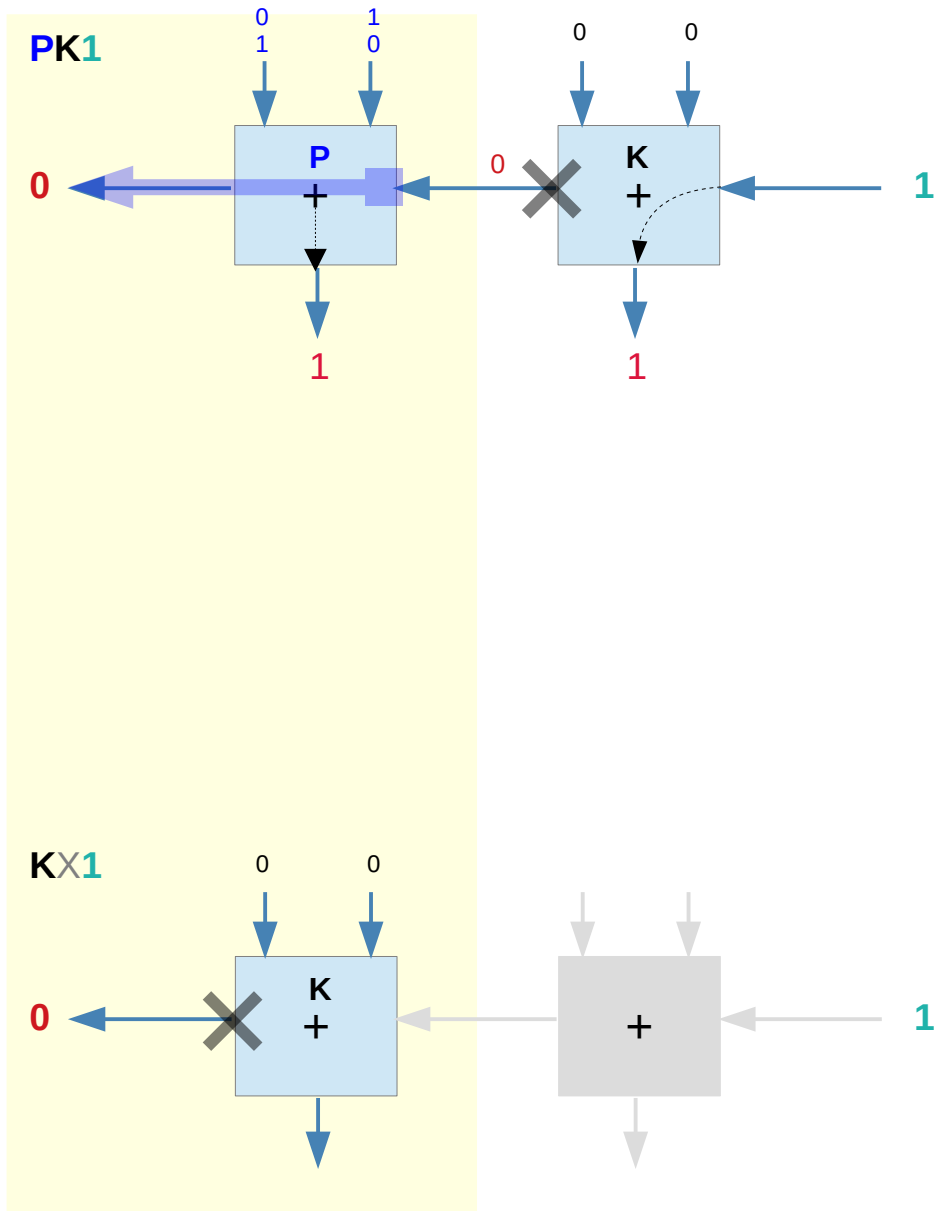
3. Cases when **FA1** is in the **G** mode



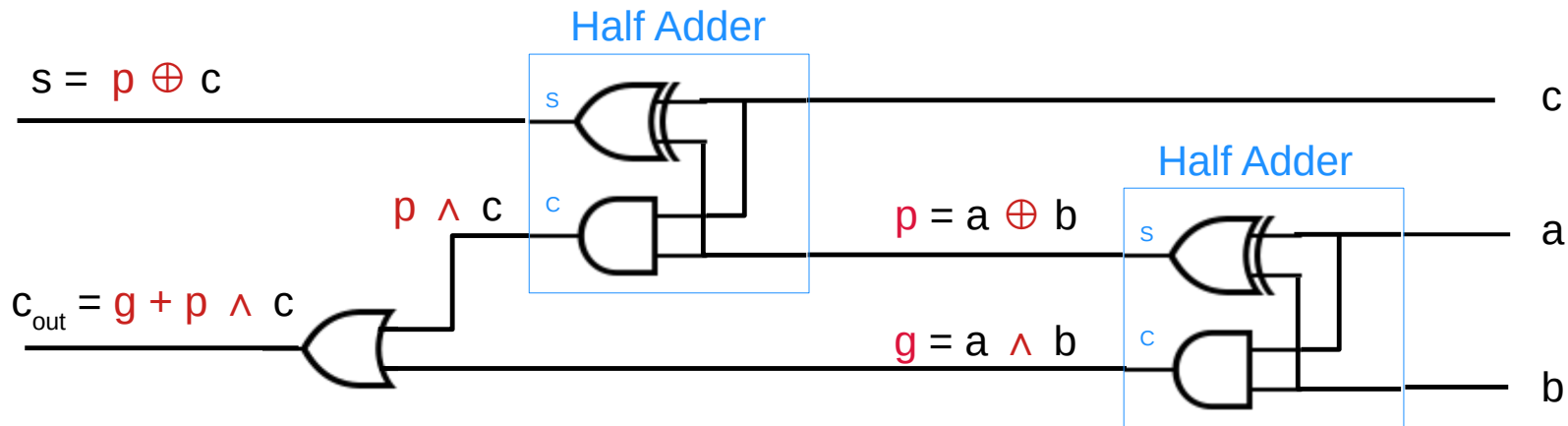
Cases for $C_{out} = 1$



Cases for $C_{out} = 0$

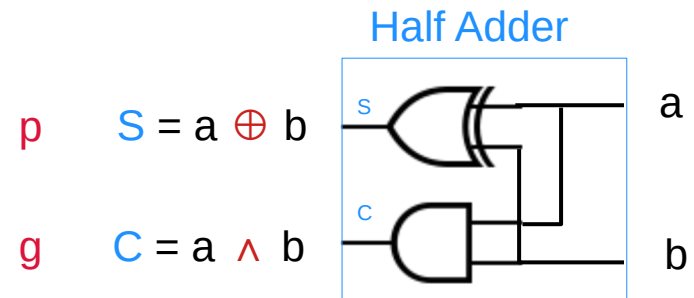


FA with P & G



Half Adder
 $S = a \oplus b$
 $C = a \wedge b$

a	b	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0



Full adder with additional generate and propagate signals.

https://en.wikipedia.org/wiki/Carry-skip_adder

Ripple Carry Adder

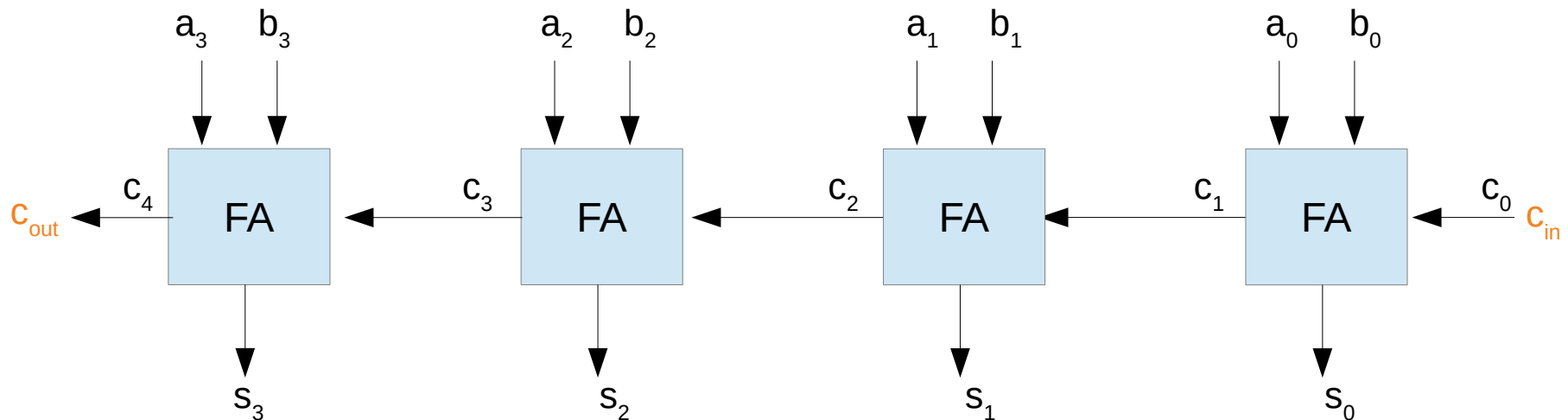
$$p_i = a_i \oplus b_i$$

$$g_i = a_i \wedge b_i$$

$$\begin{aligned} c_1 &= g_0 + p_0 \wedge c_0 \\ c_2 &= g_1 + p_1 \wedge c_1 \\ c_3 &= g_2 + p_2 \wedge c_2 \\ c_4 &= g_3 + p_3 \wedge c_3 \end{aligned}$$

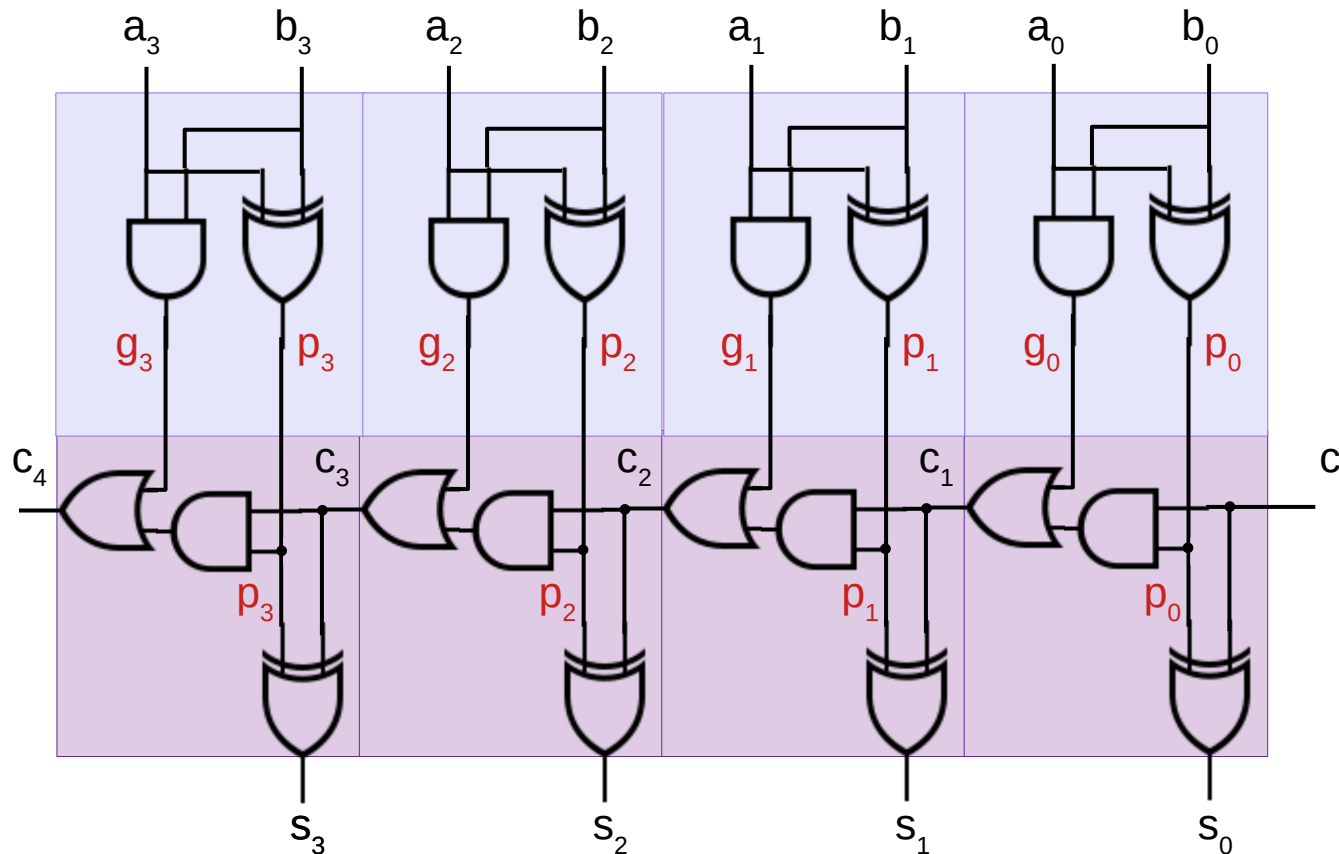
generated carry

propagated carry



https://en.wikipedia.org/wiki/Carry-skip_adder

4-bit Full Adder with P and G



Half Adder

$$p_i = a_i \oplus b_i$$

$$g_i = a_i \wedge b_i$$

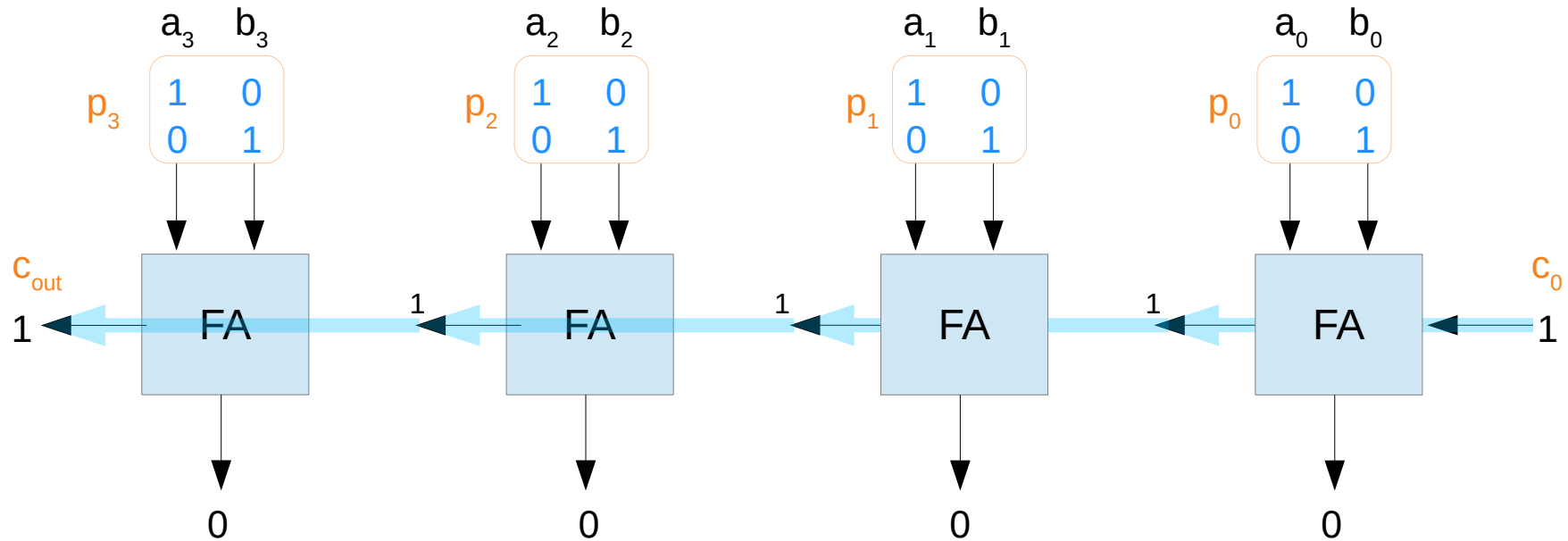
Half Adder

$$c_{i+1} = g_i + p_i \wedge c_i$$

$$s_i = p_i \oplus c_i$$

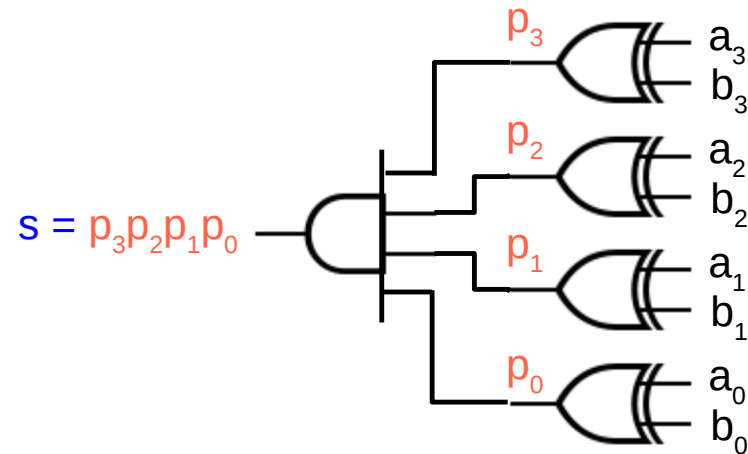
<https://upload.wikimedia.org/wikiversity/en/1/18/RCA.Note.H.1.20151215.pdf>

C_0 propagation condition



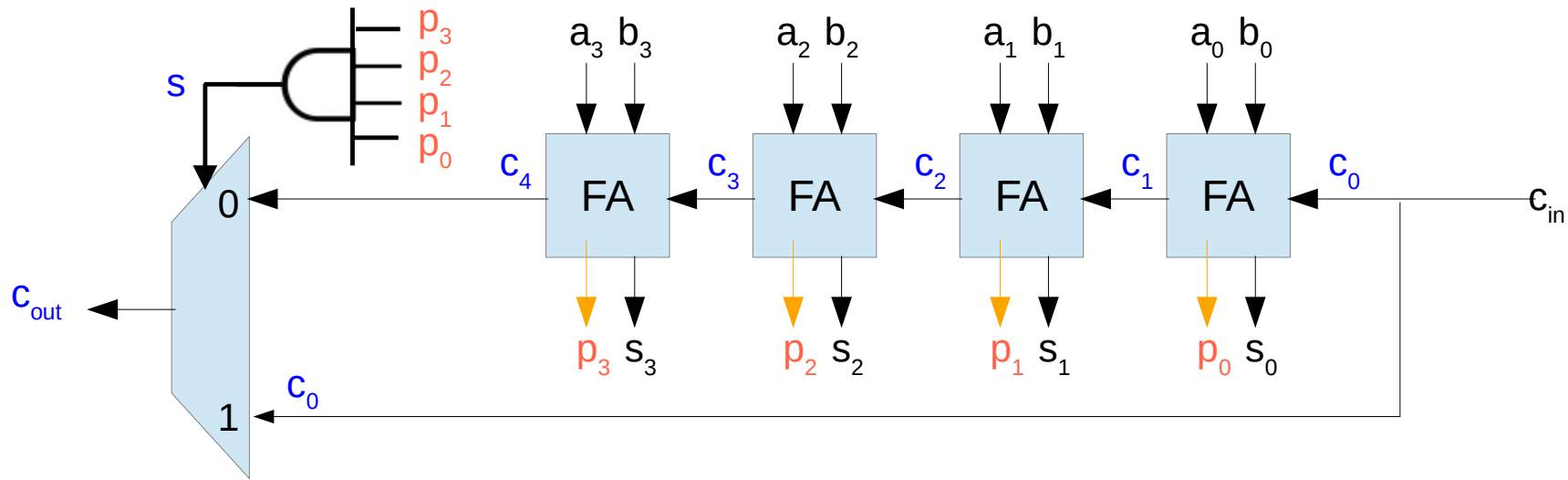
c_0 can be propagated to c_{out} only when $s = 1$

$$\begin{aligned}
 s &= p_3 \wedge p_2 \wedge p_1 \wedge p_0 = p_{[3:0]} \\
 &= (a_3 \oplus b_3) \\
 &\quad \wedge (a_2 \oplus b_2) \\
 &\quad \wedge (a_1 \oplus b_1) \\
 &\quad \wedge (a_0 \oplus b_0)
 \end{aligned}$$



https://en.wikipedia.org/wiki/Carry-skip_adder

Carry Skip Adder



The n-bit Carry Skip Adder consists of

a n-bit **carry-ripple-chain**,
a n-input **AND-gate** and
one **multiplexer**.

a multiplexer switches
either the last carry-bit c_n or the carry-in c_0
to the carry-out signal c_{out}

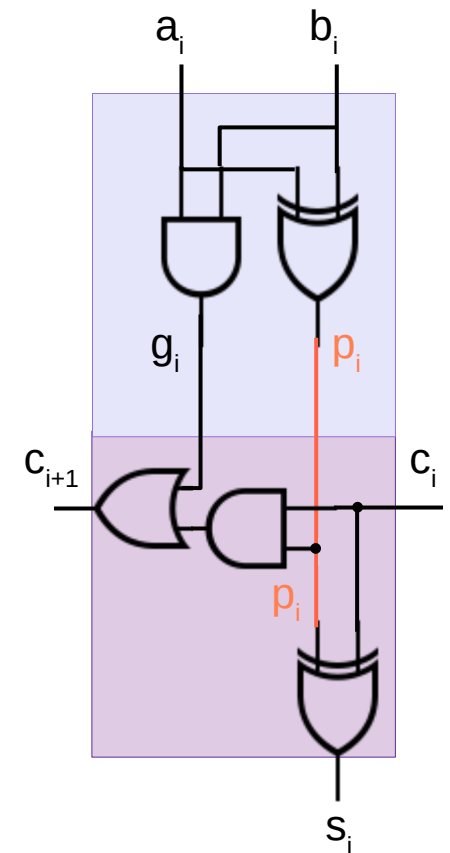
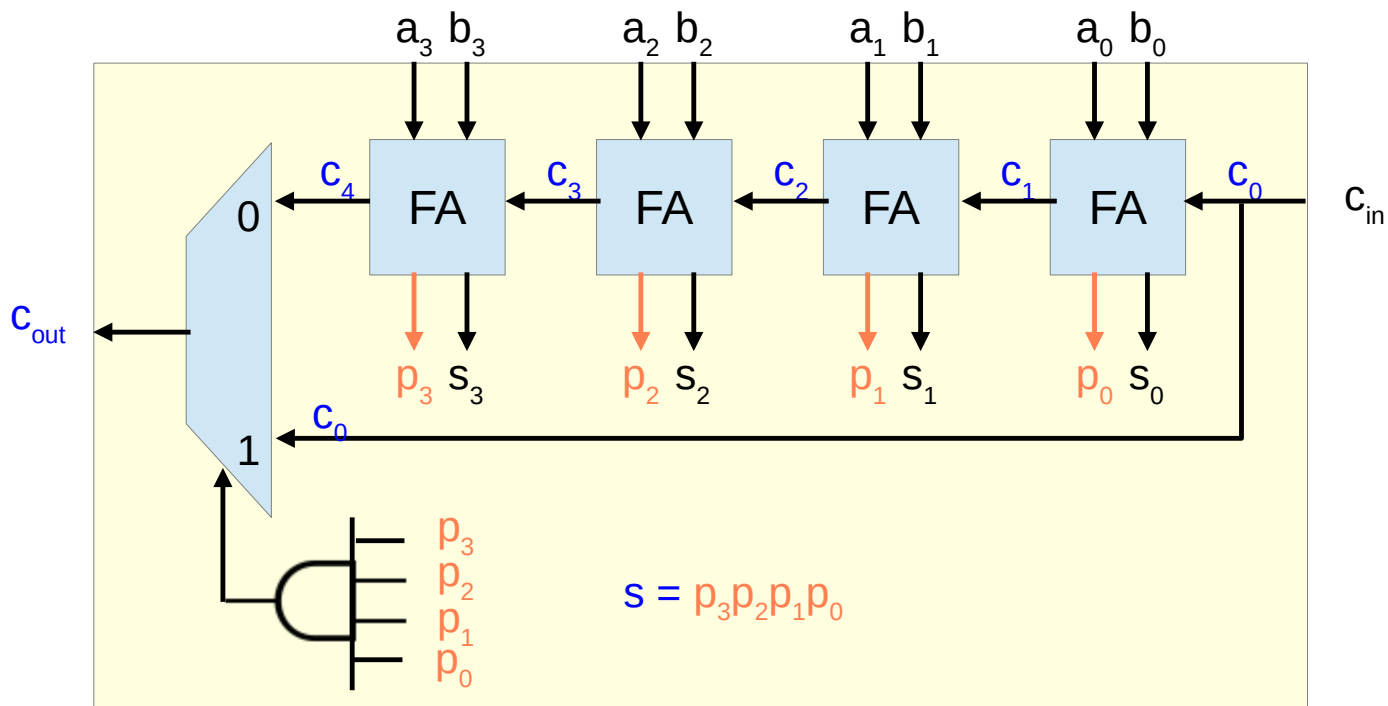
$$s = p_3 \wedge p_2 \wedge p_1 \wedge p_0 = p_{[3:0]}$$

when $s = 1$, $c_{out} \leftarrow c_0$

otherwise, internally generated carries
can be propagated to $c_{out} \leftarrow c_4$

https://en.wikipedia.org/wiki/Carry-skip_adder

Carry Skip Adder



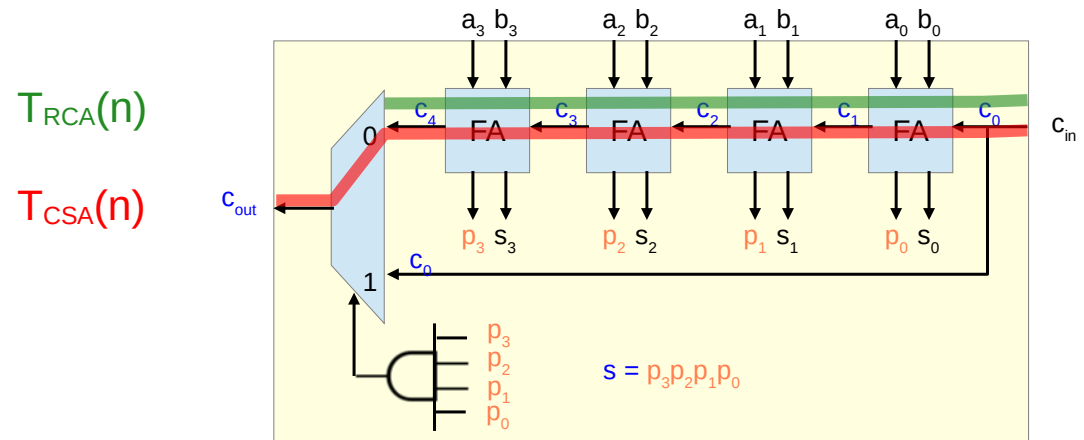
https://en.wikipedia.org/wiki/Carry-skip_adder

Carry Skip Adder

The **critical path** of a Carry Skip Adder begins at the first full adder, passes through all adders and ends at the sum bit s_{n-1}

Since a single *n-bit* Carry Skip Adder has no real speed benefit compared to a *n-bit* Ripple Carry Adder

$$T_{CSA}(n) = T_{RCA}(n)$$



https://en.wikipedia.org/wiki/Carry-skip_adder

Carry Skip Adder

the skip logic consists of a **k-input** AND gate and one MUX

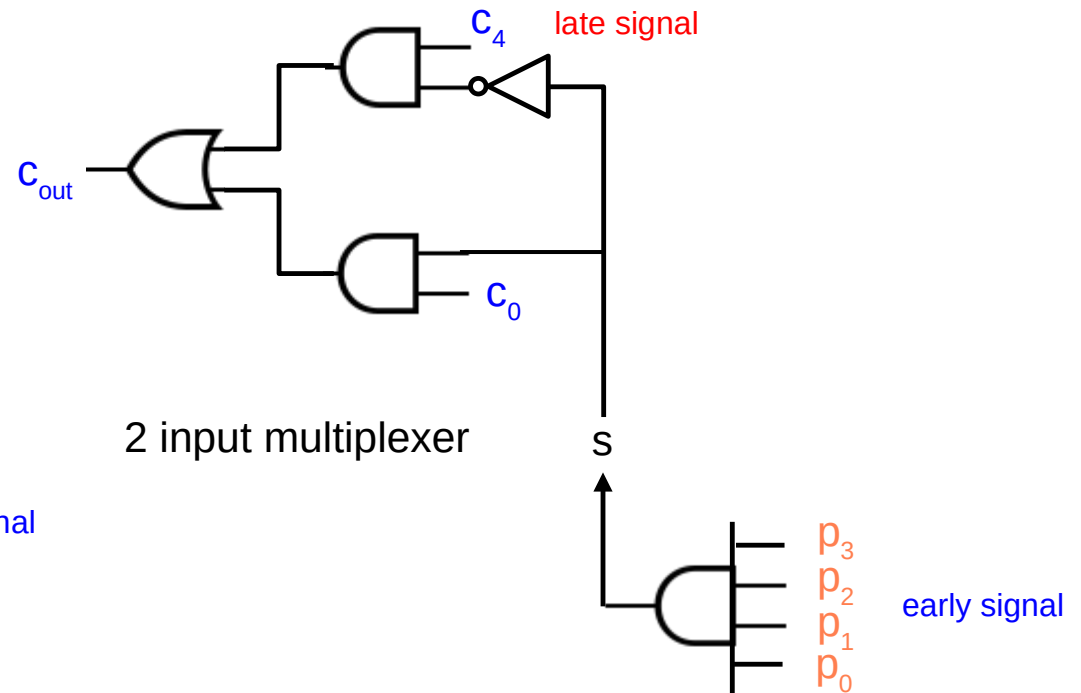
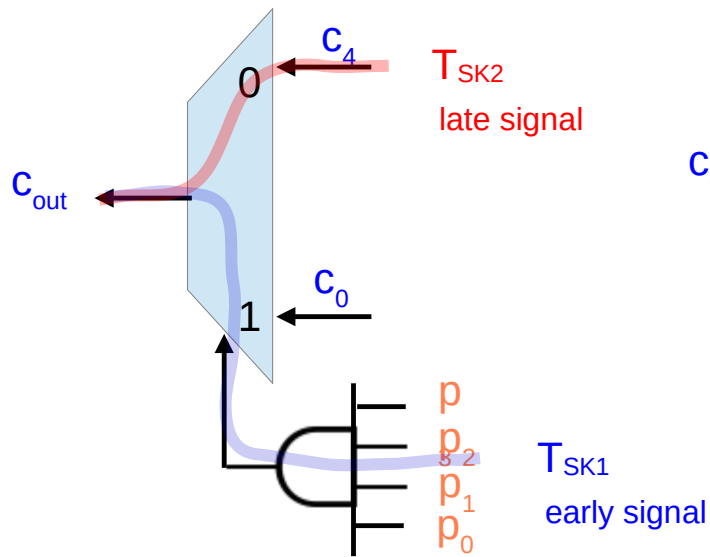
$$T_{SK1} = T_{AND}(k) + T_{MUX}$$

$$T_{SK2} = T_{MUX}$$

delay path through the AND gate

delay path from the ripple carry

... the critical path



https://en.wikipedia.org/wiki/Carry-skip_adder

Carry Skip Adder

As the **propagate** signals are computed in parallel and are early available,

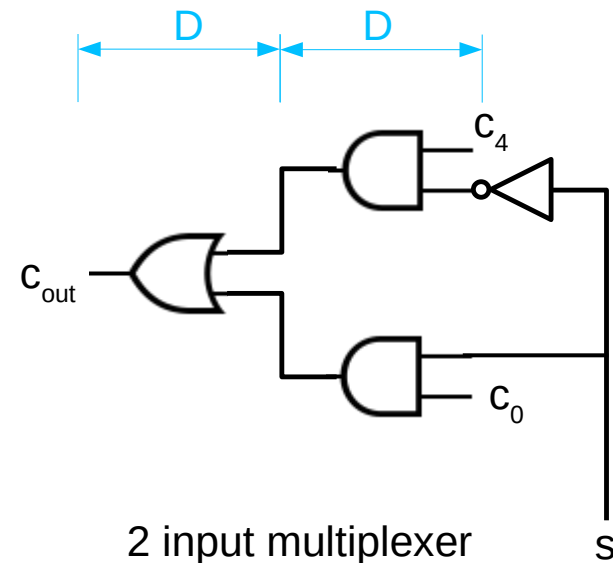
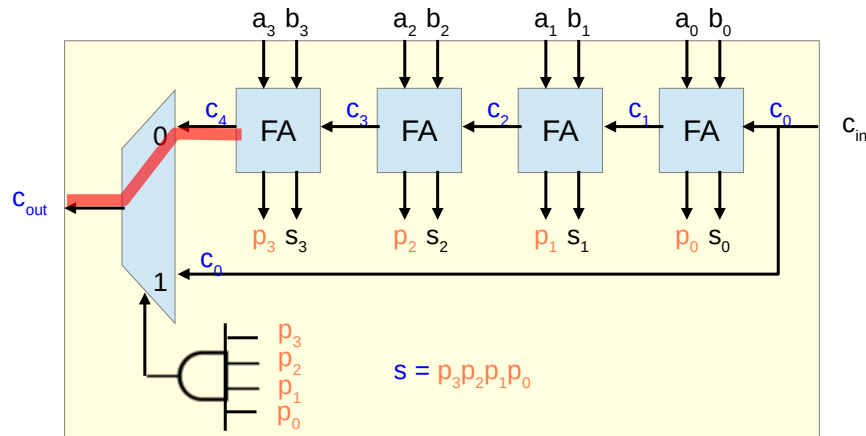
$$p_i = a_i \oplus b_i$$

The critical path in a Carry Skip Adder consists of ripple carry path and mux path for ripple carry (T_{SK2})

the **critical path** for the skip logic in a Carry Skip Adder consists of the delay imposed by the multiplexer (conditional skip)

T_{CSK} skip logic delay in the critical path

$$T_{CSK} = T_{SK2} = T_{MUX} = 2D$$



https://en.wikipedia.org/wiki/Carry-skip_adder

Block Carry Skip Adder

Block carry skip adders are composed of a number of carry skip adders

There are two types of block carry skip adders

The two operands $A = (a_{n-1}, a_{n-2}, \dots, a_1, a_0)$ and $B = (b_{n-1}, b_{n-2}, \dots, b_1, b_0)$ are split in k blocks of $(m_k, m_{k-1}, \dots, m_2, m_1)$ bits

- Why are **block** carry skip adders used
- Should the **block size** be constant or variable?
- Fixed **block size** vs. variable **block size**

Oklobdzija: High-Speed VLSI arithmetic units : adders and multipliers

Fixed-size Block Carry Skip Adder

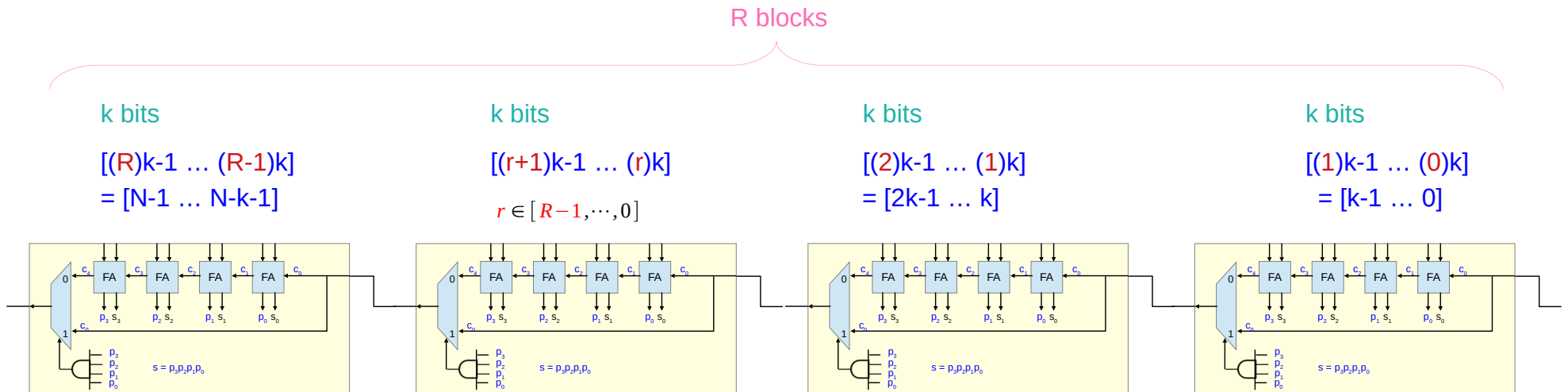
Carry Skip Adders are chained to reduce the overall critical path,
(Block Carry Skip Adders)

Fixed size block Carry Skip Adders (FCSA) split the n bits of the input bits
into blocks of k bits each, resulting in $R = n / k$ blocks.

Fixed-size block CSA
(FCSA)

number of blocks \downarrow
bits per block block size \downarrow

$$n = R \cdot k$$



Carry Skip Adder

the critical path

the longest carry path must be

- generate in the first block
- terminated in the last block
- propagated in the blocks between the first and the last

X	Y		
0	0	K	Kill ($=\overline{PG}$)
0	1	P	Propagate
1	0	P	Propagate
1	1	G	Generate

Fixed-size block CSA
(FCSA)

R groups

k bits

$$n = R \cdot k$$

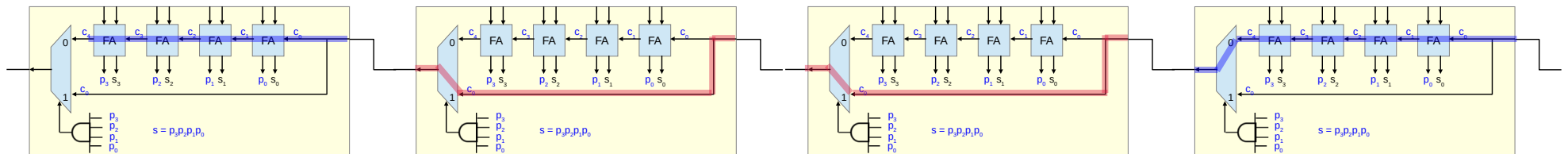
the last block

carry terminated in
the last FA

(R-2) blocks

the first block

carry generated in
the first FA



https://en.wikipedia.org/wiki/Carry-skip_adder

Carry Skip Adder

The critical path consists of

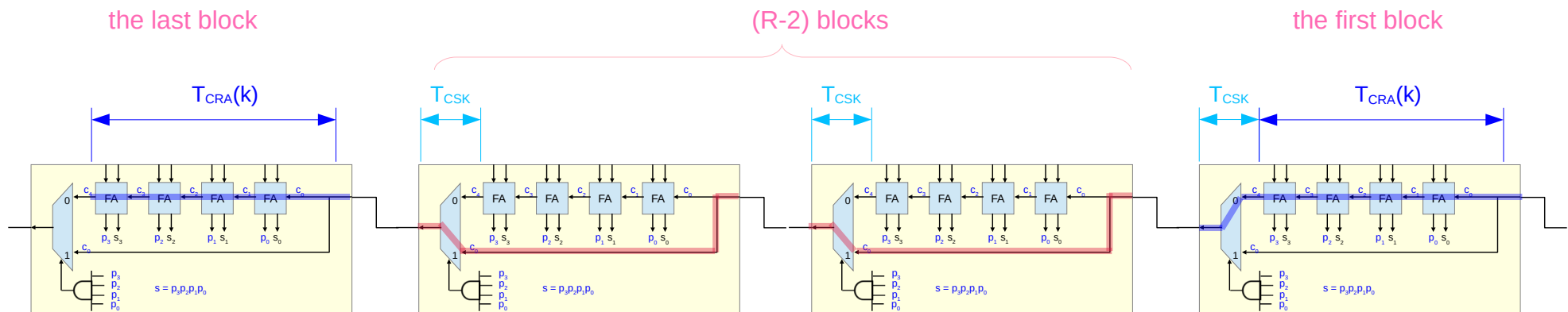
- the ripple path and the skip element of the first block
 $T_{CRA(k)} + T_{CSK}$
 $T_{CRA[0:cout]}(k)$
- the skip paths that are enclosed between the first and the last block
 $(R-2)T_{CSK}$
- finally the ripple path of the last block
 $T_{CRA(k)}$

Fixed-size block CSA
(FCSA)

R groups

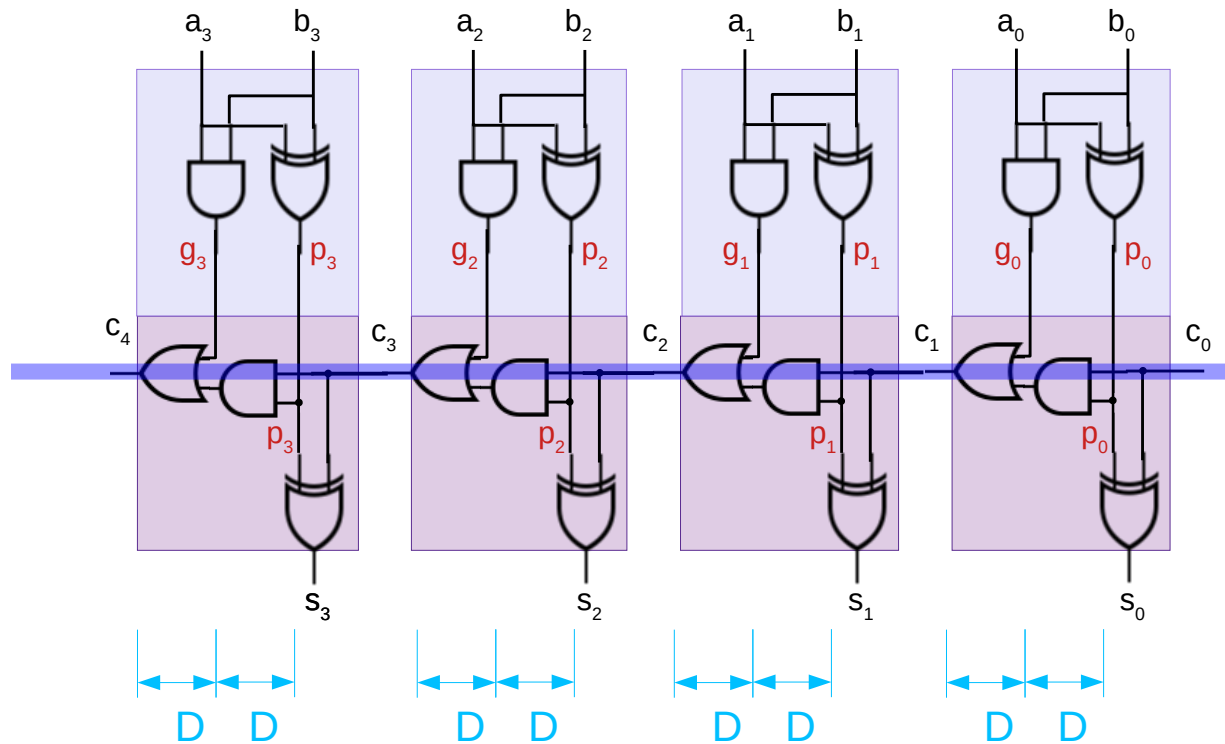
k bits

$$n = R \cdot k$$



https://en.wikipedia.org/wiki/Carry-skip_adder

4-bit Full Adder with P and G



k bits

$$T_{CRA}(k) = 2D \cdot k$$

<https://upload.wikimedia.org/wikiversity/en/1/18/RCA.Note.H.1.20151215.pdf>

Critical Path Delay

Fixed-size block CSA (FCSA)

The critical path consists of

- the ripple path and the skip element of the first block $T_{CRA}(k) + T_{CSK}$
- the skip paths that are enclosed between the first and the last block $(R-2)T_{CSK}$
- finally the ripple path of the last block $T_{CRA}(k)$

$$\begin{aligned}T_{FCSA}(n) &= T_{CRA}(k) + T_{CSK} + (R-2)T_{CSK} + T_{CRA}(k) \\ &= k2D + 2D + (R-2)2D + k2D \\ &= k2D + 2D + (R-1)2D - 2D + k2D \\ &= k2D + (R-1)2D + k2D \\ &= 2k2D + (R-1)2D \\ &= (2k+R)2D \\ &= (2k+n/k)2D\end{aligned}$$

$$\begin{aligned}&= k2D + 3D + (R-1)2D + (k+2)2D \\ &= 3D + k2D + R2D - 2D + k2D + 4D \\ &= (2k+R)2D + 5D\end{aligned}$$

R groups

k bits

$$n = R \cdot k$$

Optimal block size k

$$\begin{aligned}T_{\text{FCSA}}(n) &= T_{\text{CRA}}(k) + T_{\text{CSK}} + (R-2)T_{\text{CSK}} + T_{\text{CRA}}(k) \\ &= (2k+R)2D \\ &= (2k+n/k)2D\end{aligned}$$

The optimal block size k for a given adder width n

$$dT_{\text{FCSA}}(n) / dk = 0 \qquad \frac{dT_{\text{FCSA}}(n)}{dk} = 0$$

$$(2-n(1/k^2)) = 0$$

$$2 = n/k^2$$

$$k^2 = n / 2$$

$$k = \text{sqrt}(n/2)$$

$$5.6 = \text{sqrt}(64/2) \qquad n = 64\text{bits} \rightarrow k = 6$$

$$4 = \text{sqrt}(32/2) \qquad n = 32\text{bits} \rightarrow k = 4$$

https://en.wikipedia.org/wiki/Carry-skip_adder

Fixed-size block CSA
(FCSA)

R groups

k bits

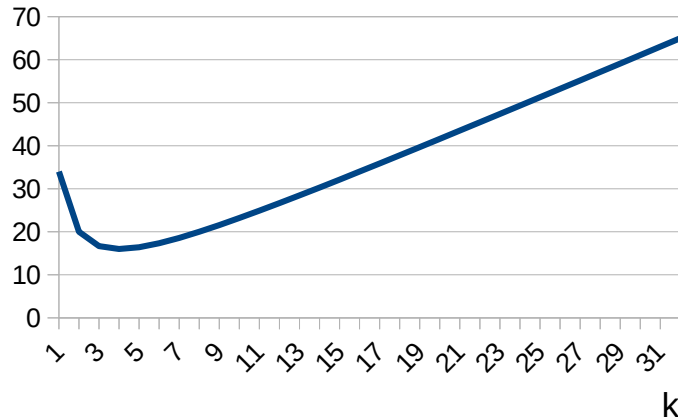
$$n = R \cdot k$$

Examples of Optimal Block Sizes

$$T_{FCSA,opt}(n) = \left(2k + \frac{n}{k}\right)2D$$

$$T_{FCSA}(32) = (2k + 32/k)2D$$

(2k+32/k)



$$4 = \text{sqrt}(32/2) \quad k_{opt} = \sqrt{\frac{n}{2}}$$

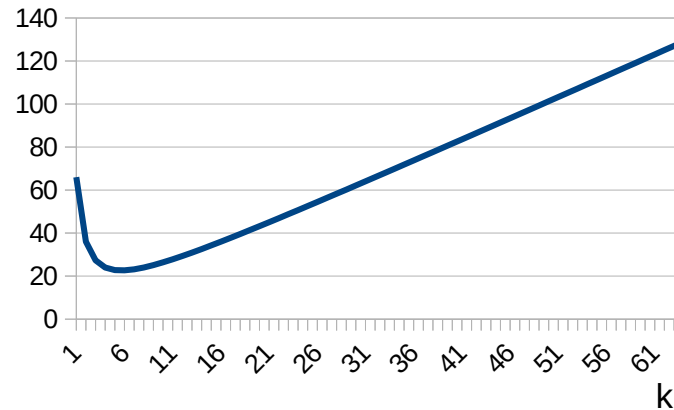
n = 32bits
→ k = 4

https://en.wikipedia.org/wiki/Carry-skip_adder

$$T_{FCSA,opt}(n) = \left(2k + \frac{n}{k}\right)2D$$

$$T_{FCSA}(64) = (2k + 64/k)2D$$

(2k+64/k)



$$5.6 = \text{sqrt}(64/2) \quad k_{opt} = \sqrt{\frac{n}{2}}$$

n = 64bits
→ k = 6

Fixed-size block CSA
(FCSA)

R groups

k bits

$$n = R \cdot k$$

Asymptotic Analysis

$$T_{\text{FCSA}}(n) = (2k+n/k)2D$$

The optimal block size k for a given adder width n

$$k = \sqrt{n/2}$$

$$\begin{aligned} T_{\text{FCSA, opt}}(n) &= (2\sqrt{n/2} + n/\sqrt{n/2})2D \\ &= (\sqrt{2n} + \sqrt{n^2 / n / 2}) 2D \\ &= (\sqrt{2n} + \sqrt{2n})2D \\ &= (2\sqrt{2n})2D \end{aligned}$$

$$\begin{aligned} T_{\text{FCSA, opt}}(n) &= \left(2\sqrt{n/2} + \frac{n}{\sqrt{n/2}}\right) 2D \\ &= (2\sqrt{2n}) 2D \quad \text{when } k_{\text{opt}} = \sqrt{\frac{n}{2}} \end{aligned}$$

https://en.wikipedia.org/wiki/Carry-skip_adder

Fixed-size block CSA
(FCSA)

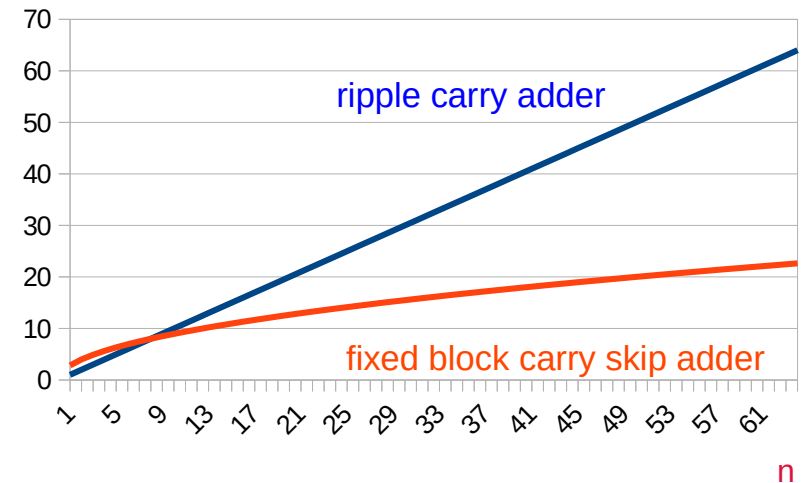
R groups

k bits

$$n = R \cdot k$$

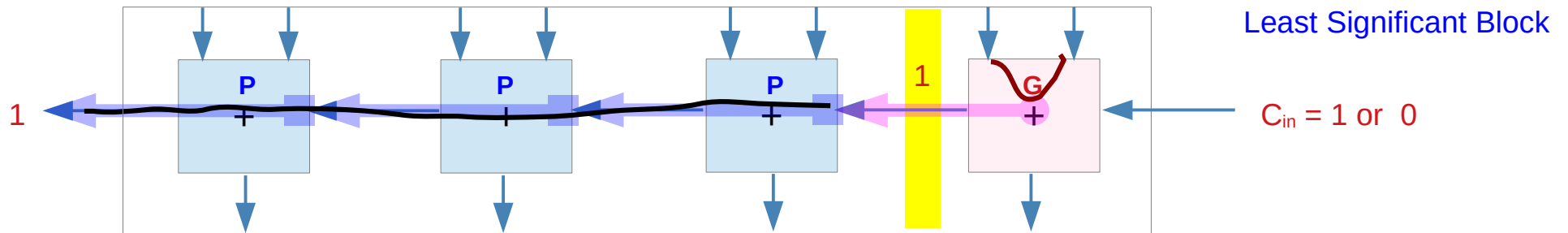
$$T_{\text{CRA}}(n) = 2D \cdot n$$

$$T_{\text{FCSA, opt}}(n) = 2D \cdot (2\sqrt{2n})$$

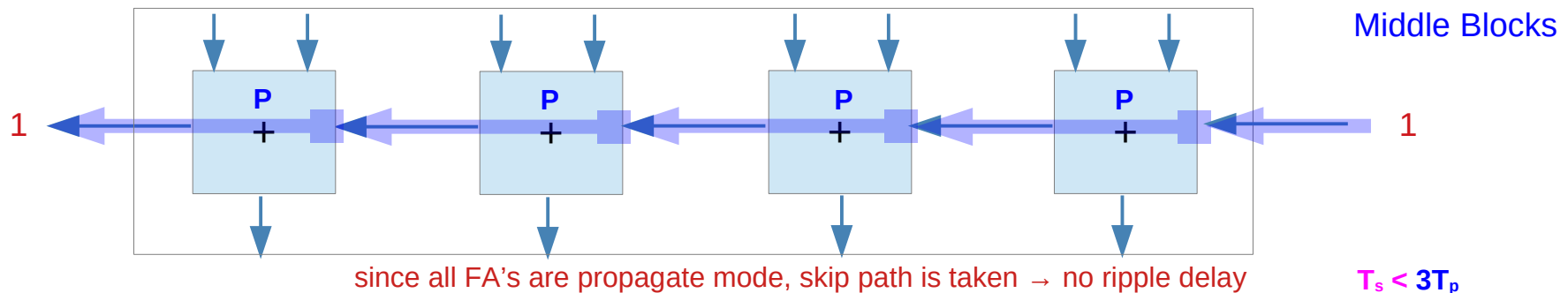


Critical Carry Path (1)

For longest carry path, if any block generates a carry, that carry will propagate through the remaining 3 FA's of the block



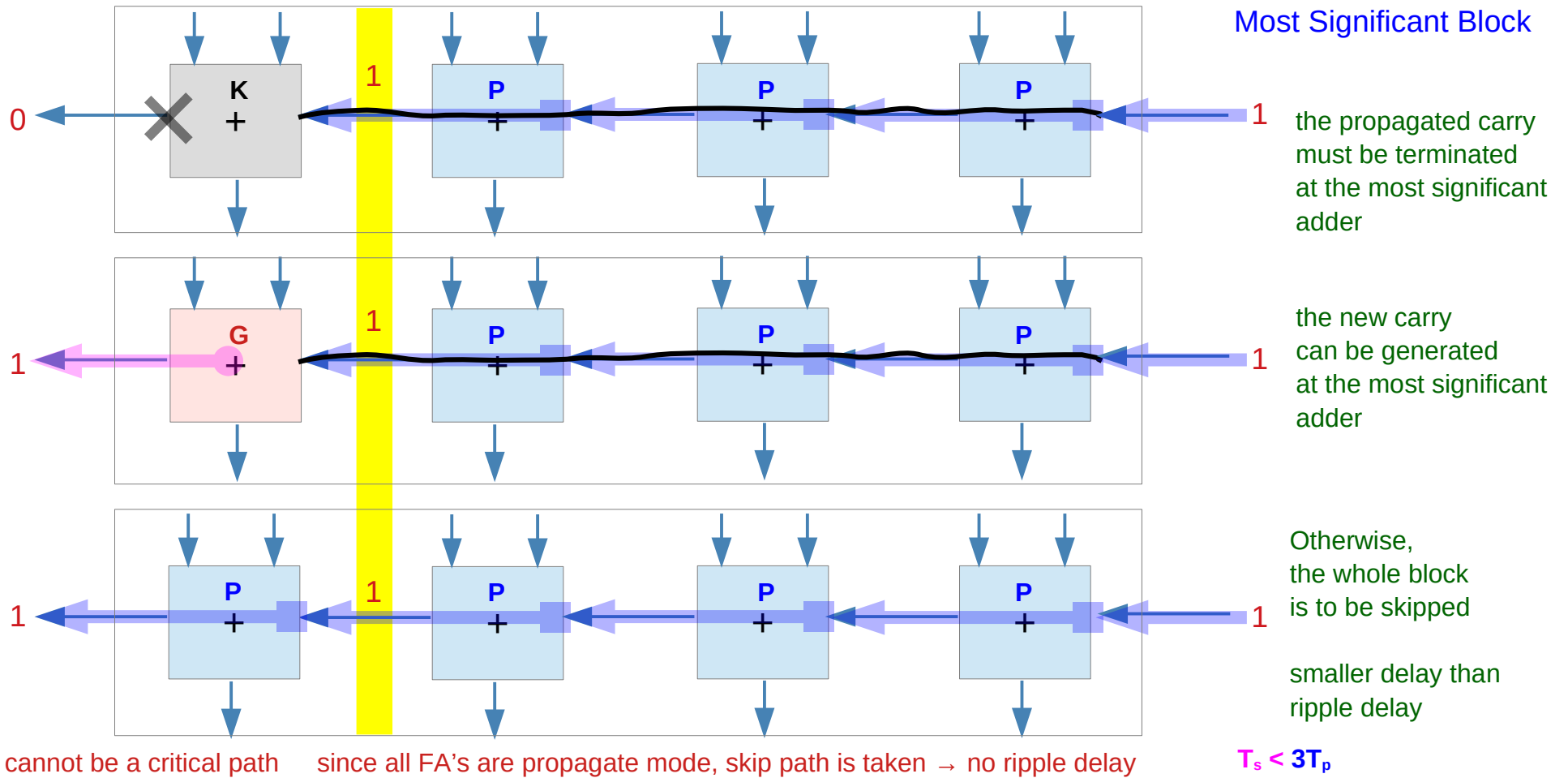
and then through the carry skip gates to the final block,



More Fast Adders, Ivor Page, University of Texas at Dallas

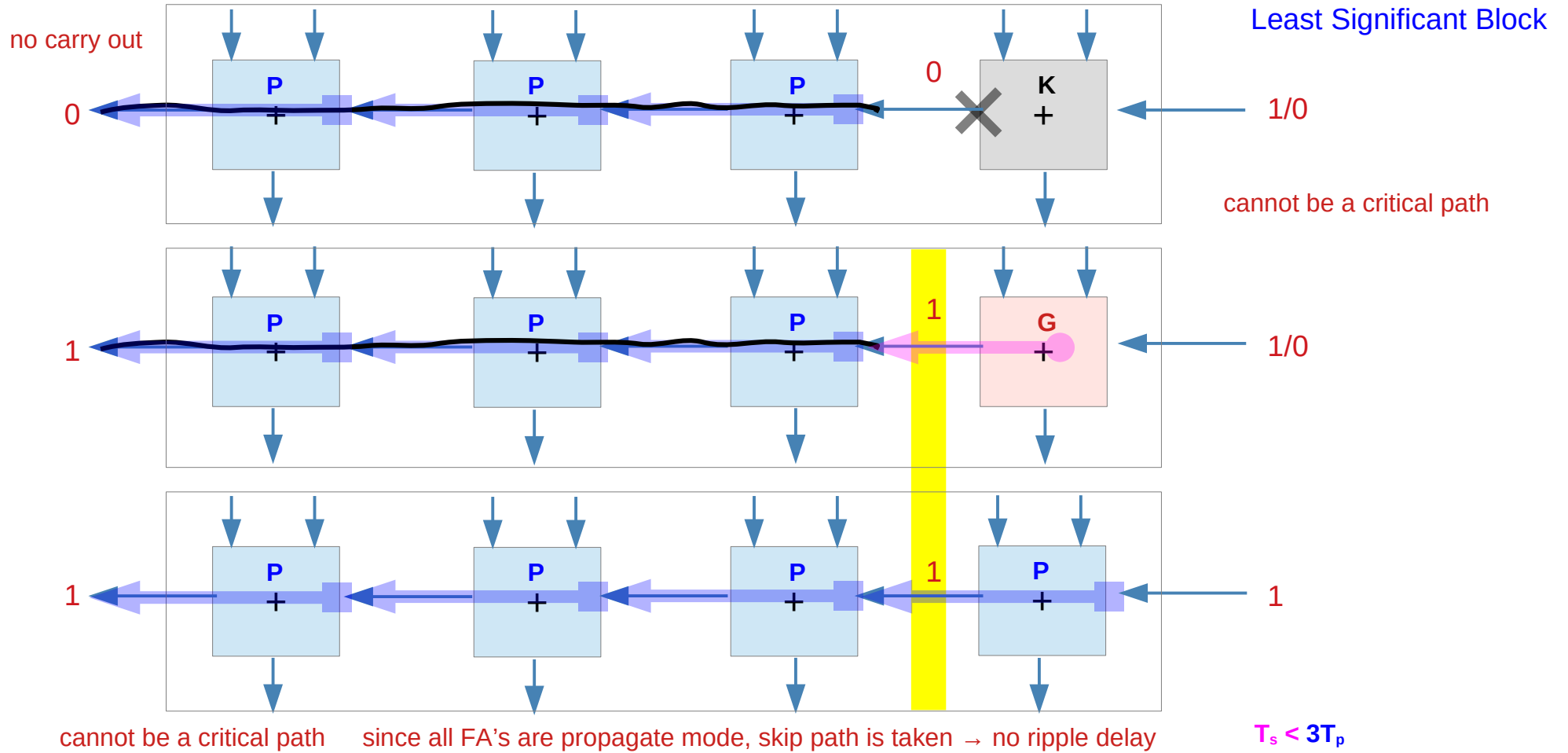
Critical Carry Path (2)

At the final block, it may have to propagate through 3 FA's to reach the most significant adder



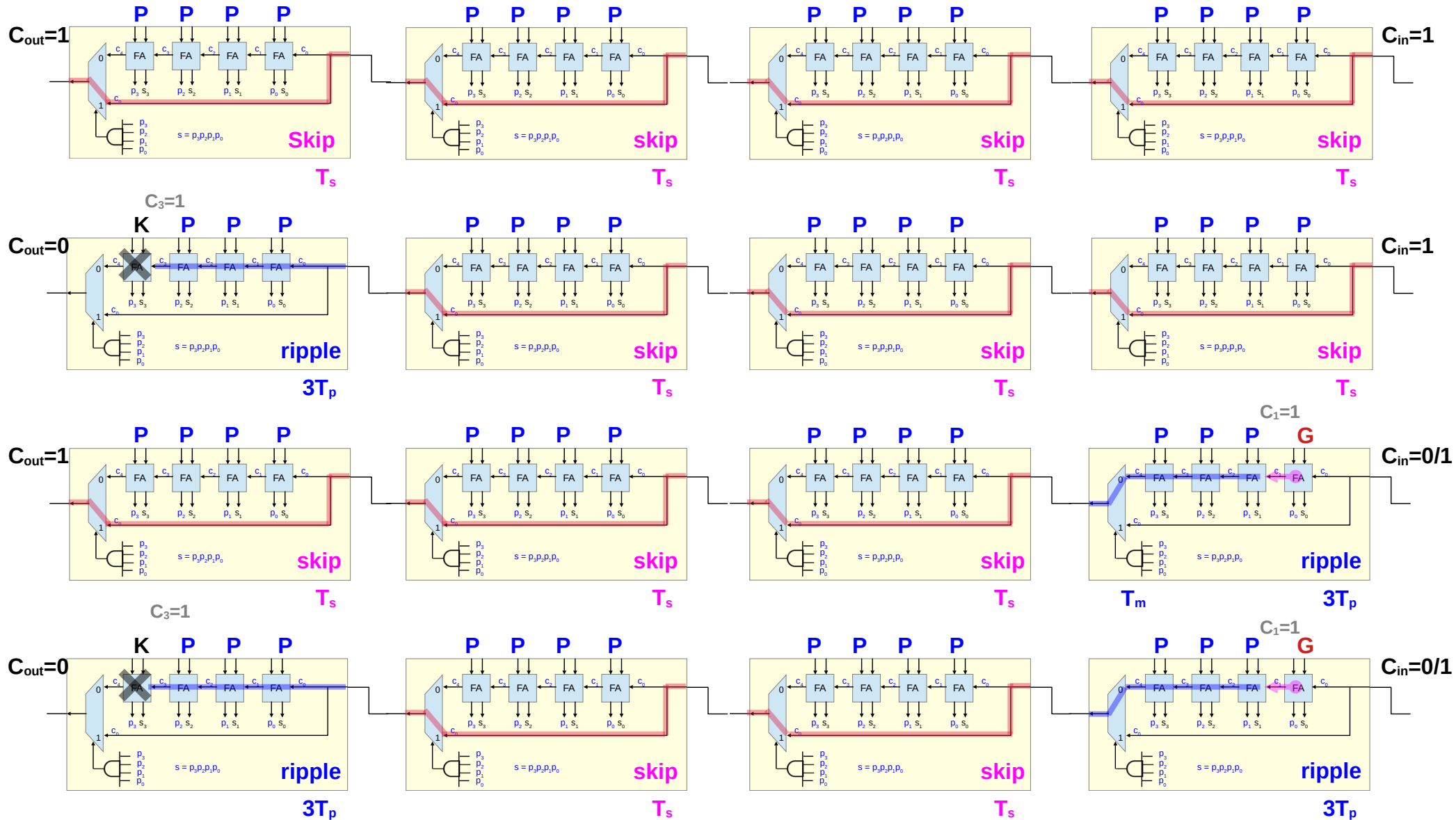
More Fast Adders, Ivor Page, University of Texas at Dallas

Critical Carry Path (3)



More Fast Adders, Ivor Page, University of Texas at Dallas

Critical Carry Path (4)



Carry Skip Adder

Fixed-size block CSA (FCSA)

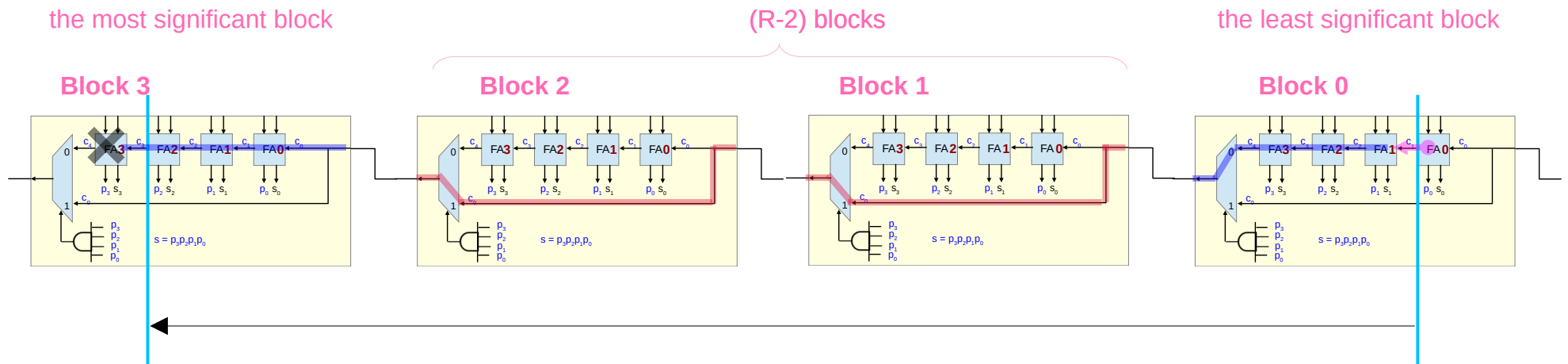
The longest delay path from c_1 to c_{n-1}

begins with a carry generated in FA0 in the least significant block 0, propagates through FA3 in block 0, then through the skip element (MUX can be replaced with OR gate), then through carry skip units of (R-2) blocks, and then through fa0, fa1, fa2 in the most significant block (R-1), to the c_{n-1} signal

R groups

k bits

$$n = R \cdot k$$



More Fast Adders, Ivor Page, University of Texas at Dallas

Carry Skip Adder

The longest delay path from c_1 to c_{n-1}

$$(k-1)T_p + D + (n/k-2)T_s + (k-1)T_p$$

T_p is the time to propagate a carry through one stage of the full adder (from c_i to c_{i+1})

T_s is the delay through one carry-skip stage

Fixed-size block CSA (FCSA)

R groups

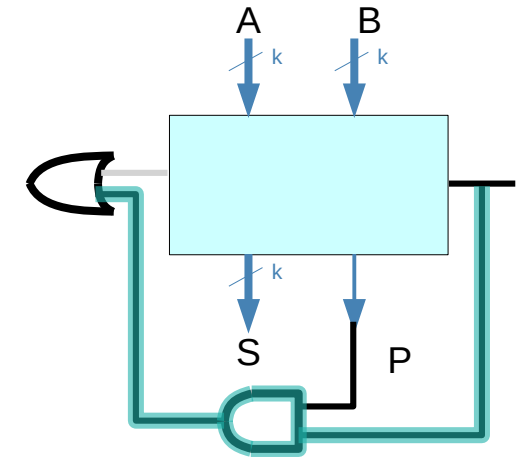
k bits

$$n = R \cdot k$$

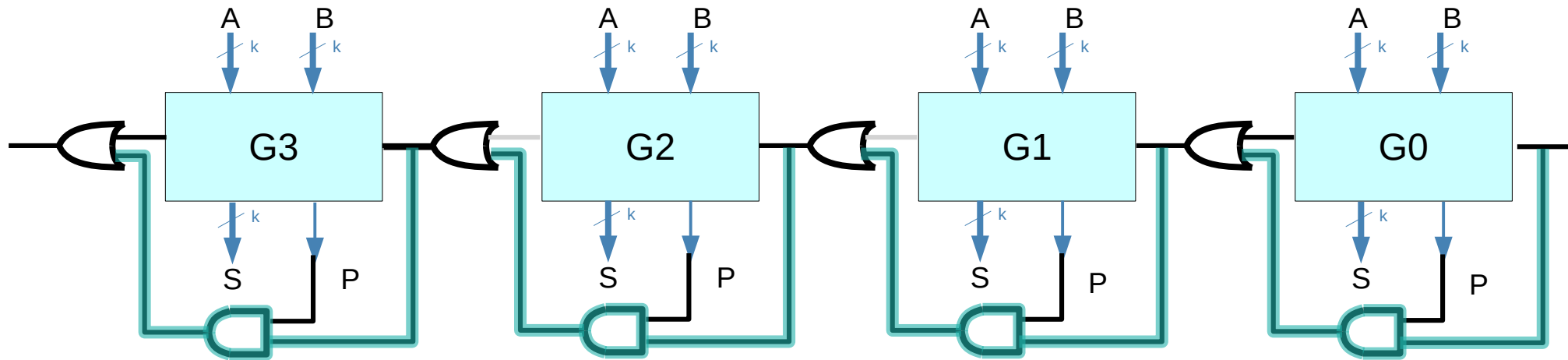
More Fast Adders, Ivor Page, University of Texas at Dallas

Carry Skip Adder

A carry signal entering a certain block can be propagated past the block without waiting for the signal to propagate through the 4 individual stages of the block



If all $n/4$ blocks propagate, a carry entering the least significant stage will pass to the most significant carry-out in time $n/4$ times the delay through the carry-skip unit

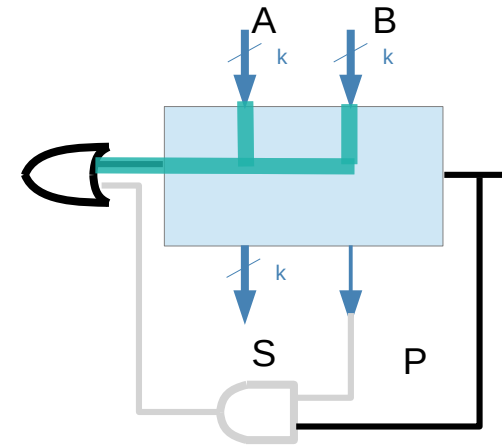
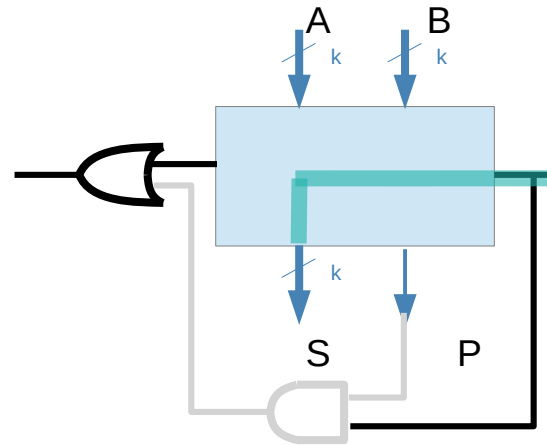


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Carry Skip Adder

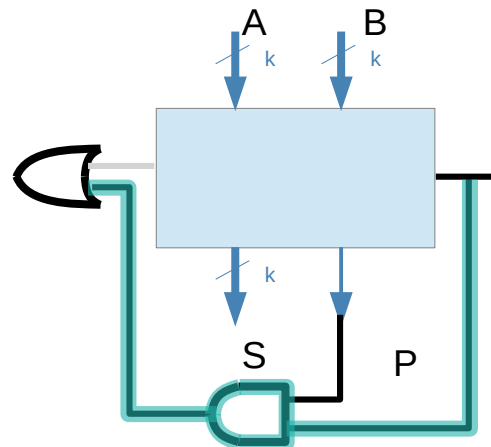
Ripple through $k-1$ bits

$$(k - 1) \Delta_{rca}$$



Skip carry

$$\Delta_{SKIP}$$



Oklobdzija: High-Speed VLSI arithmetic units : adders and multipliers

Carry Skip Adder

The maximal delay Δ of a Carry Skip Adder is encountered when **carry** is generated in the **least-significant bit** position,

- rippling through $k-1$ bit positions,
- skipping over $R-2 = N/k-2$ groups in the middle,
- rippling to the $k-1$ bits of most significant group and
- being assimilated in the N -th bit position to produce the sum S_N :

$$\begin{aligned}\Delta_{\text{CSA}} &= (k - 1) \Delta_{\text{rca}} + (R - 2) \Delta_{\text{SKIP}} + (k - 1) \Delta_{\text{rca}} \\ &= 2 (k - 1) \Delta_{\text{rca}} + (R - 2) \Delta_{\text{SKIP}} \\ &= 2 (k - 1) \Delta_{\text{rca}} + (N/k - 2) \Delta_{\text{SKIP}}\end{aligned}$$

Oklobdzija: High-Speed VLSI arithmetic units : adders and multipliers

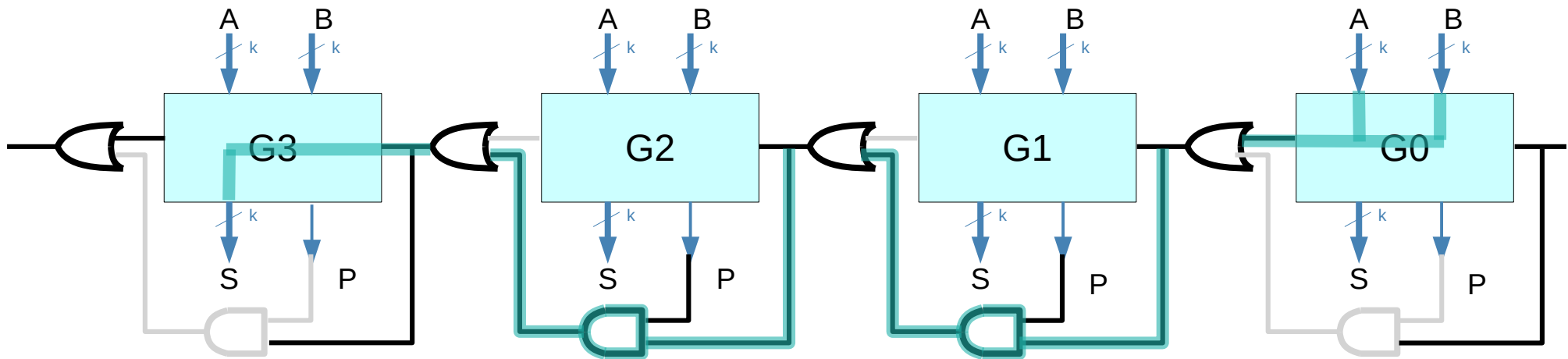
Carry Skip Adder

$$\begin{aligned}\Delta_{CSA} &= (k - 1) \Delta_{rca} + (R - 2) \Delta_{SKIP} + (k - 1) \Delta_{rca} \\ &= 2(k - 1) \Delta_{rca} + (R - 2) \Delta_{SKIP} \\ &= 2(k - 1) \Delta_{rca} + (N/k - 2) \Delta_{SKIP}\end{aligned}$$

Carry Skip Adder is faster than RCA at the expense of a few relatively simple modifications.

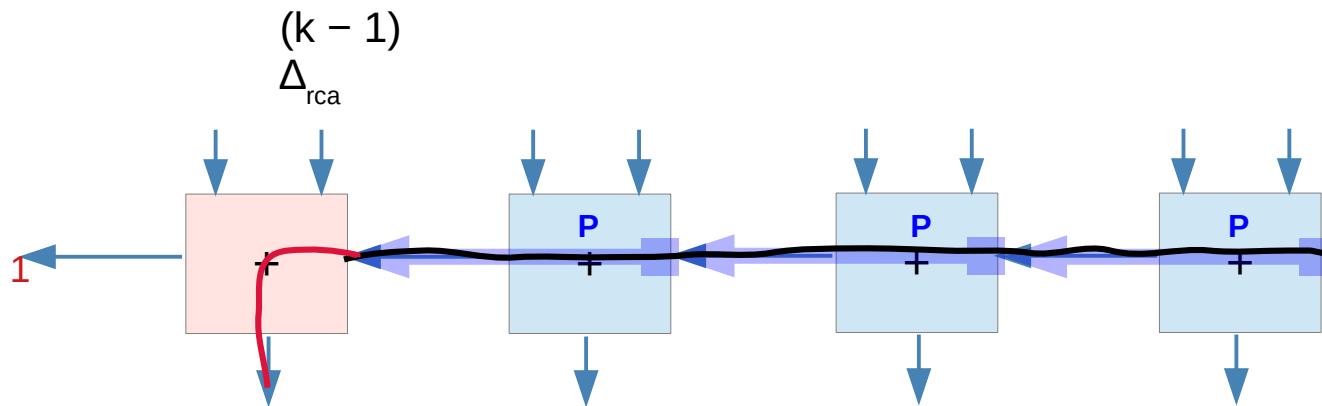
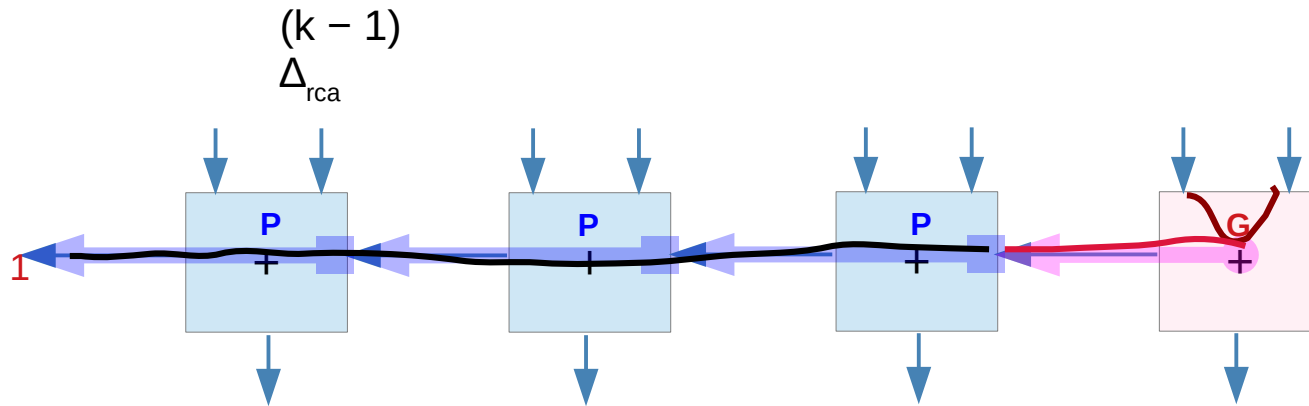
The delay is still linearly dependent on the size of the adder N , however this linear dependence is reduced by a factor of $1/k$

$$N = R \cdot k$$



Oklobdzija: High-Speed VLSI arithmetic units : adders and multipliers

Design C (9) – When Cout1 = 1



High Performance Carry Chains for FPGAs, S. Hauck, M. M. Hosler, T. W. Fry

Carry Skip Adder

If an arbitrary block generated a carry by itself,
The carry will always propagate to the next block
However, if the second block generates a carry itself,
Or kill the carry, then that is the end of the critical path

If the second block propagates the carry, then we see
The advantage of the CSA architecture

<https://electronics.stackexchange.com/questions/21251/critical-path-for-carry-skip-adder>

<https://electronics.stackexchange.com/questions/21251/critical-path-for-carry-skip-adder>

Variable size Block Carry Skip Adder

The performance can be improved, ie.
all carries propagated quickly
by varying the **block sizes**

Accordingly the **initial blocks** of the adder are
made smaller so as to quickly detect **carry generates**
that must be propagated the furthers,
the **middle blocks** are made larger
because they are not the problem case,
and then the **most significant blocks** are again
made smaller so that the late arriving carry inputs
can be processed quickly

<https://electronics.stackexchange.com/questions/21251/critical-path-for-carry-skip-adder>

References

- [1] en.wikipedia.org
- [2] Parhami, “Computer Arithmetic Algorithms and Hardware Designs”