

Pipelined Architecture (2A)

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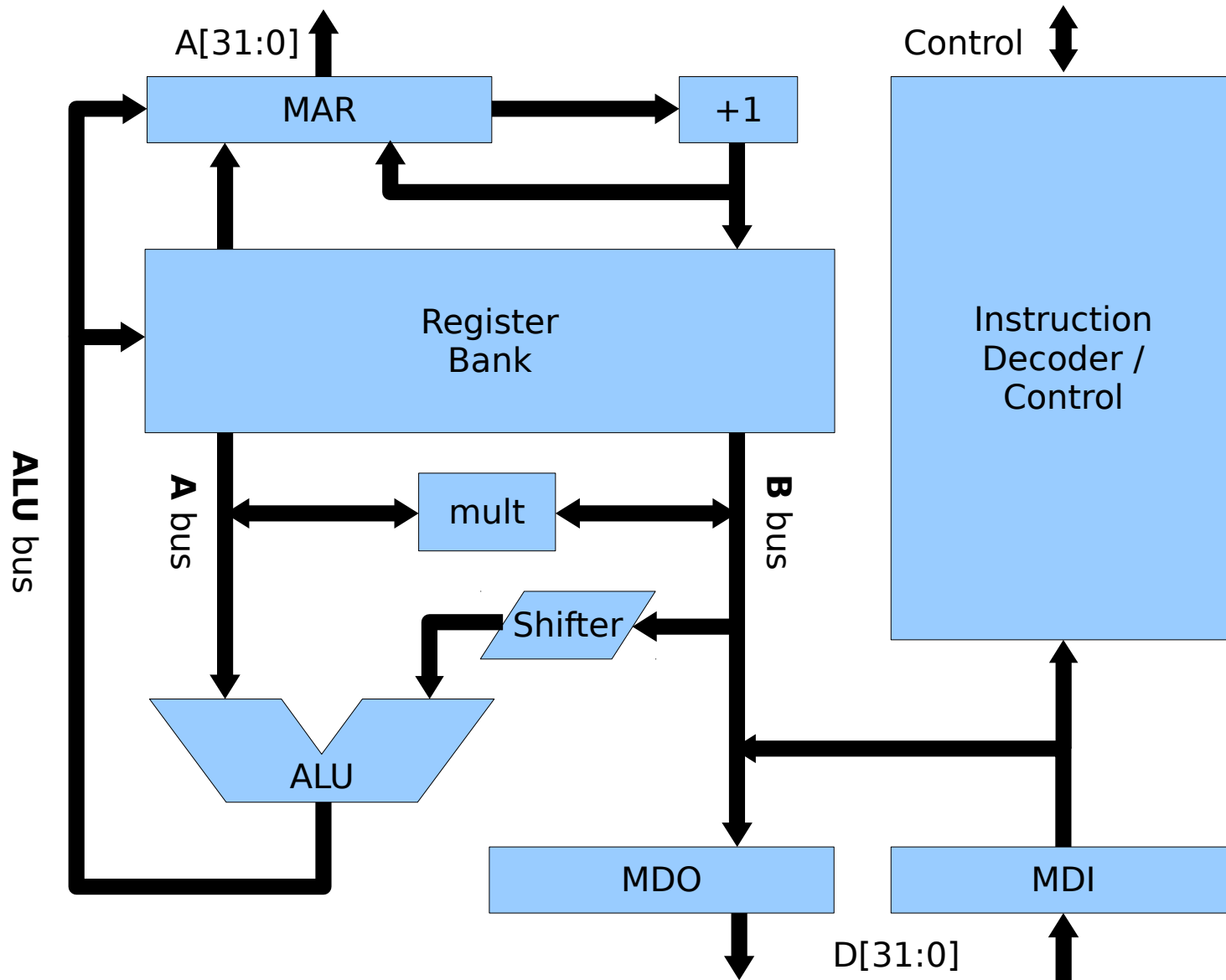
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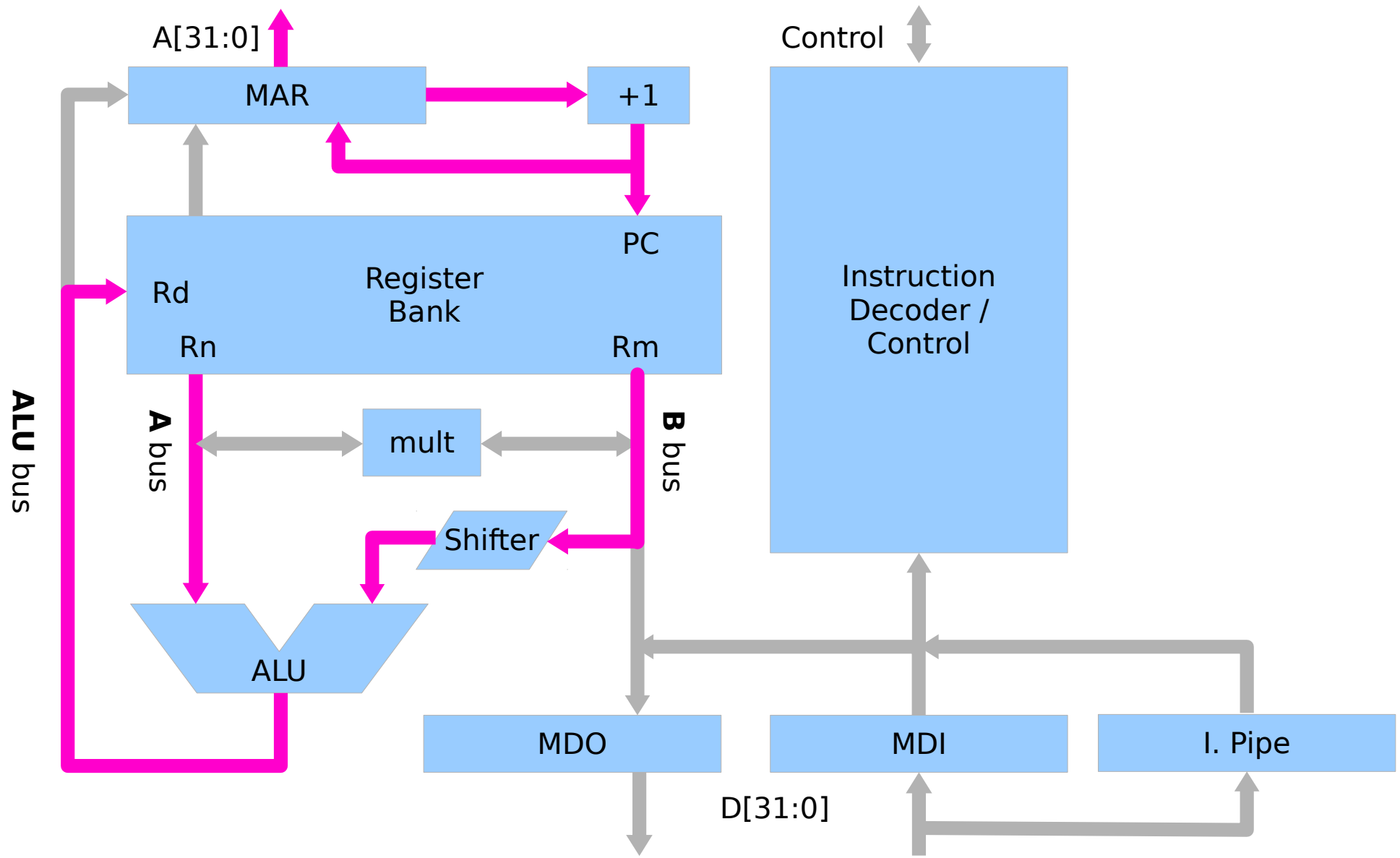
Based on

ARM System-on-Chip Architecture, 2nd ed, Steve Furber

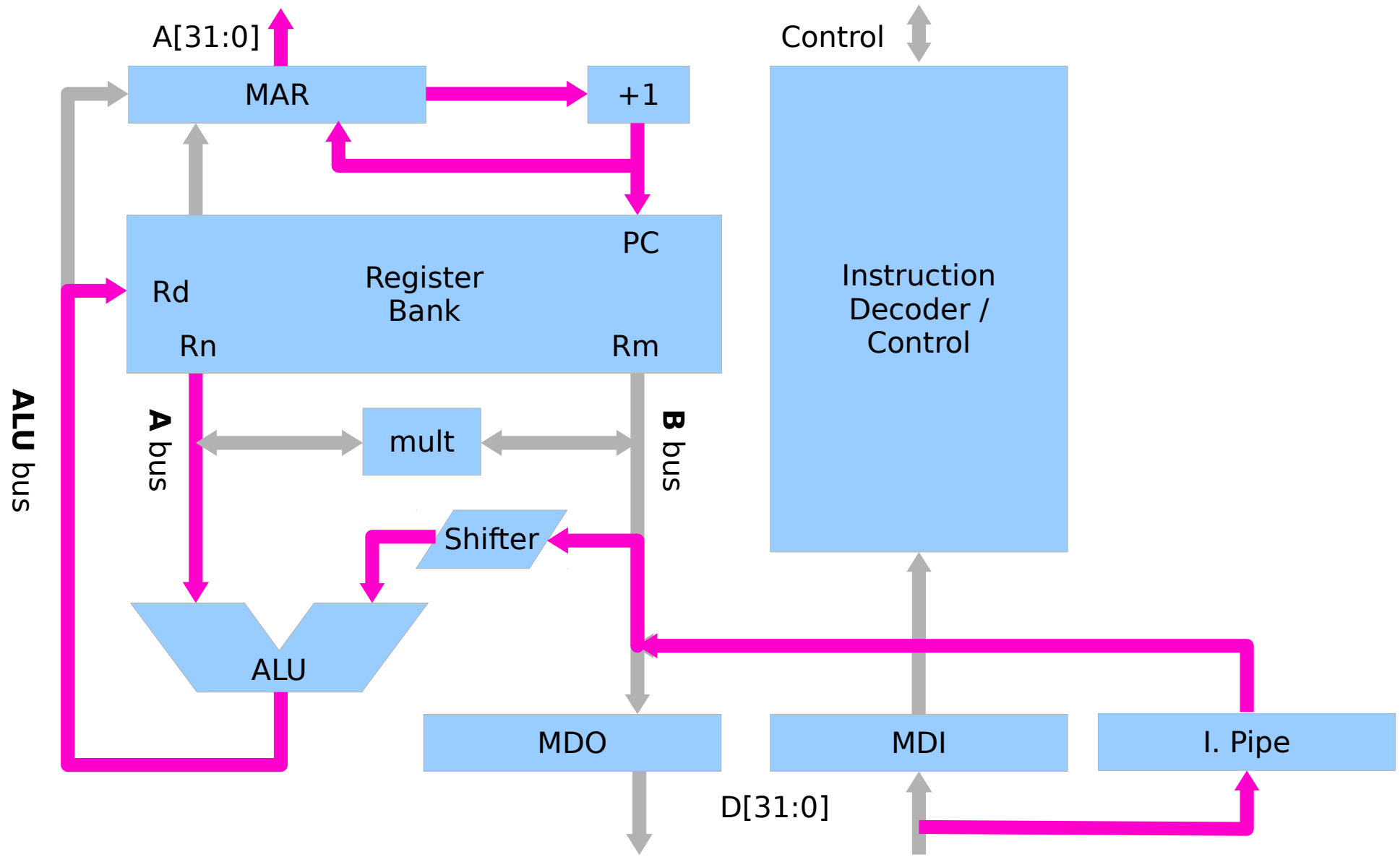
3-stage Pipeline



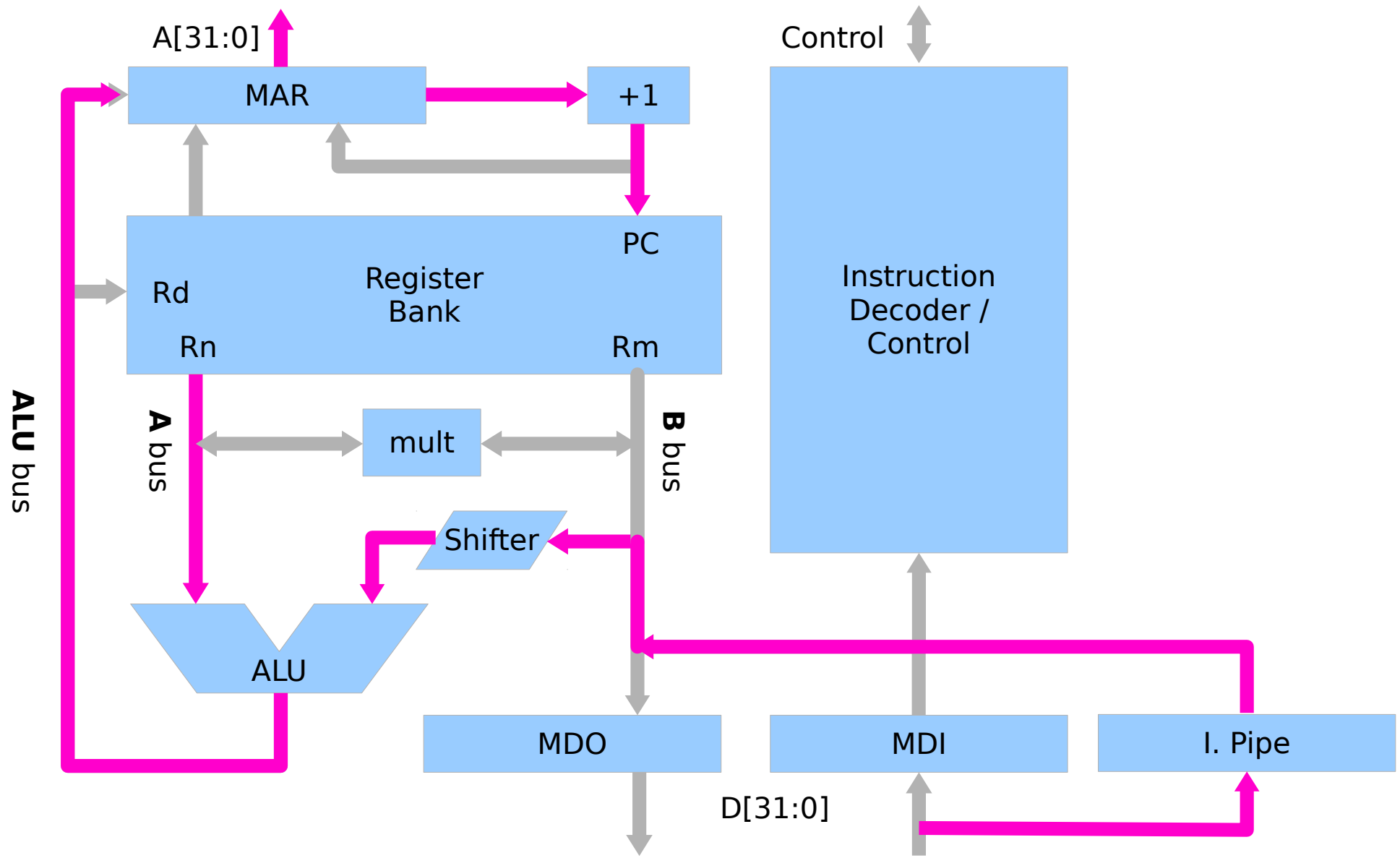
Register-Register Operations



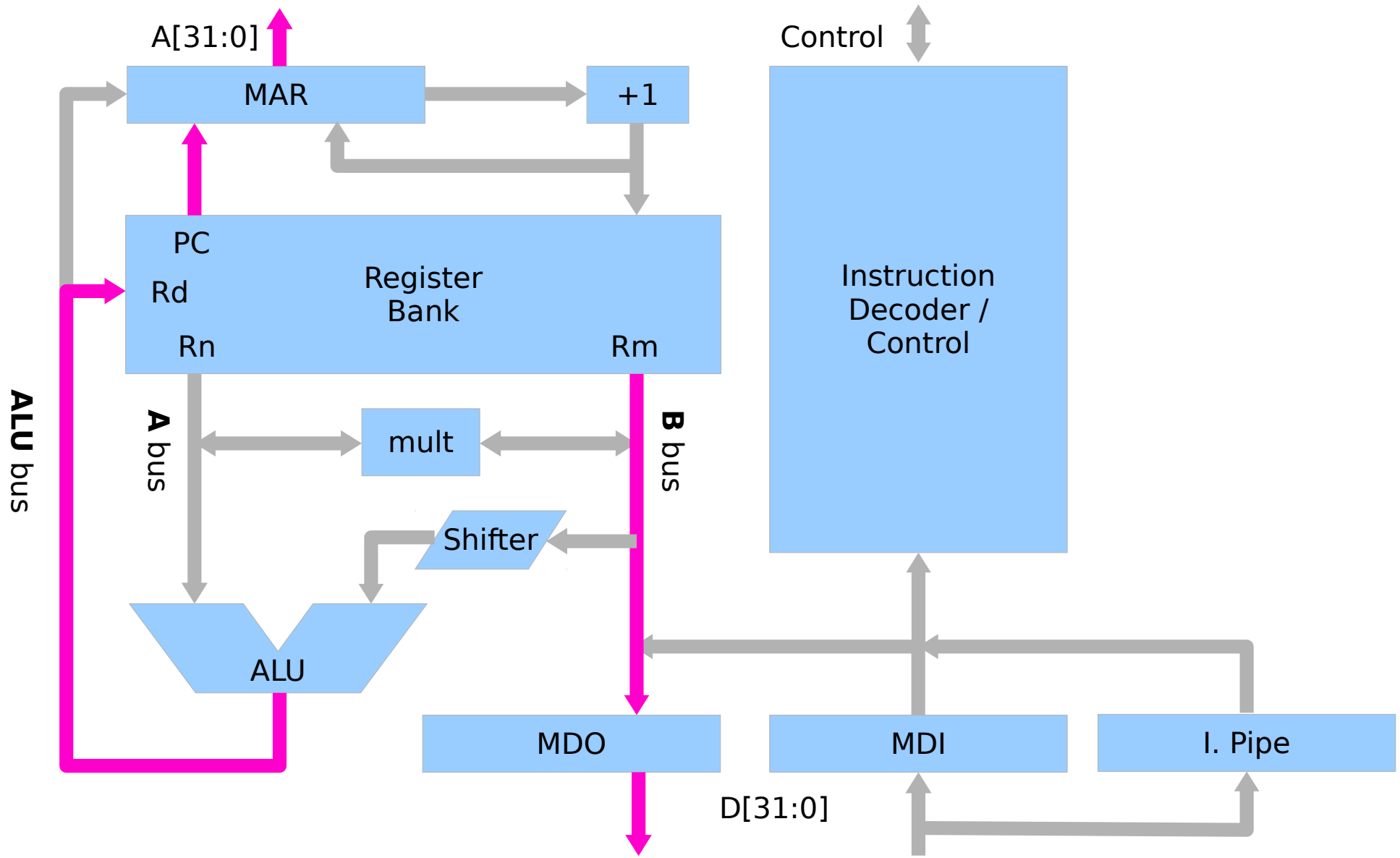
Register-Immediate Operations



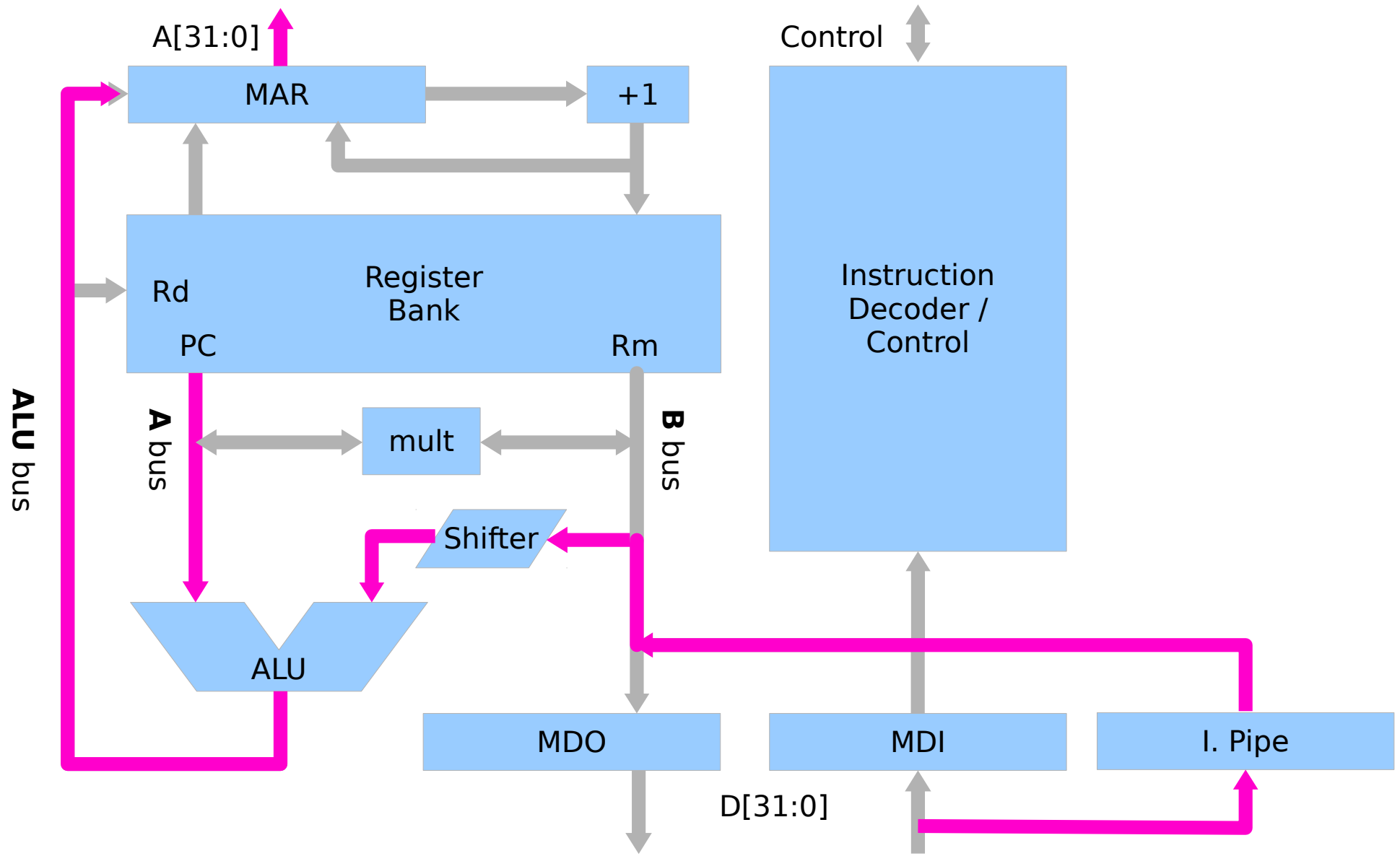
STR - 1st Cycle



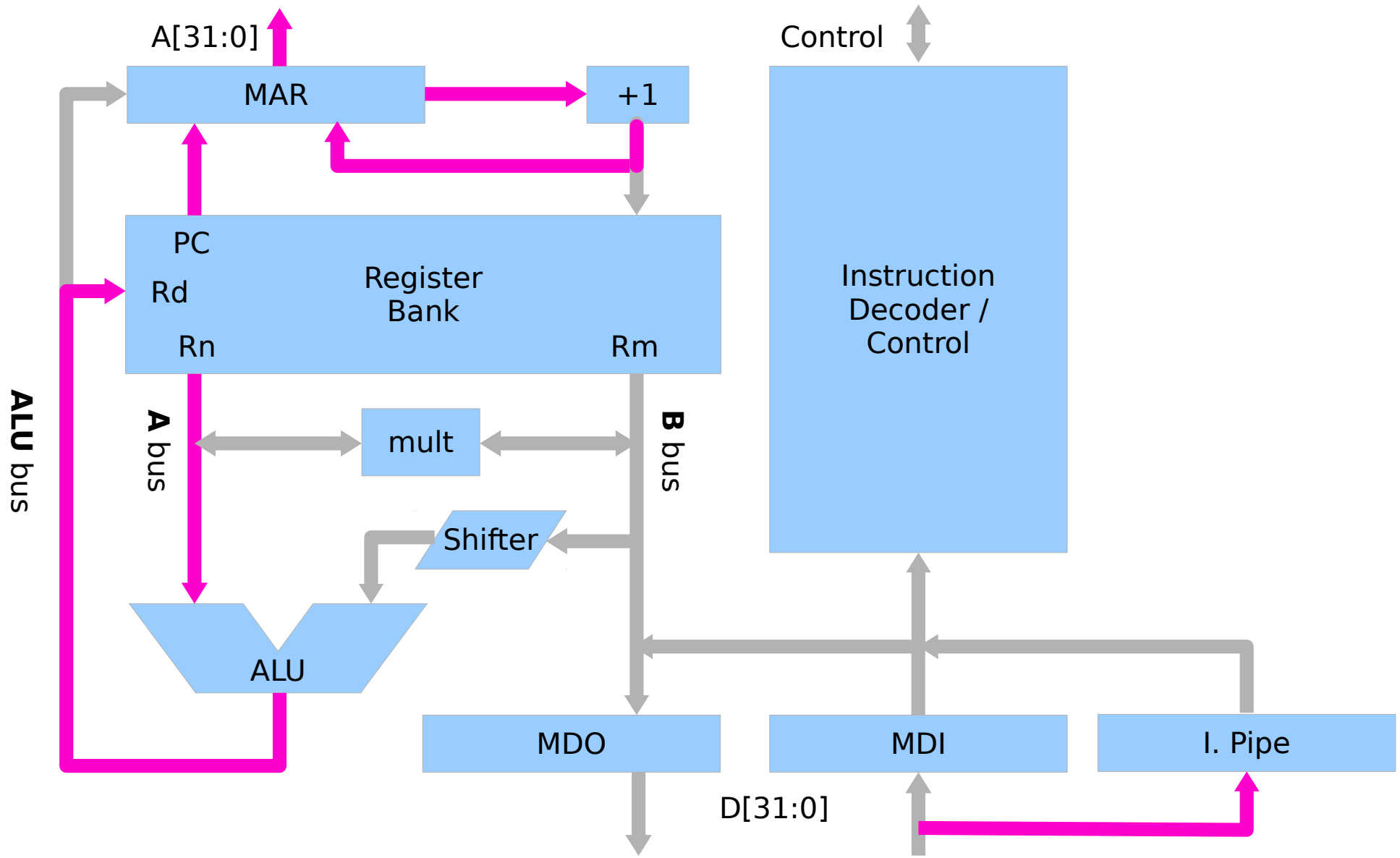
STR - 2nd Cycle



B - 1st Cycle



B - 2nd Cycle



ARM Instruction Set

The load-store architecture

3-address data processing instructions

(2 source registers + 1 destination register)

Conditionally executes every instruction

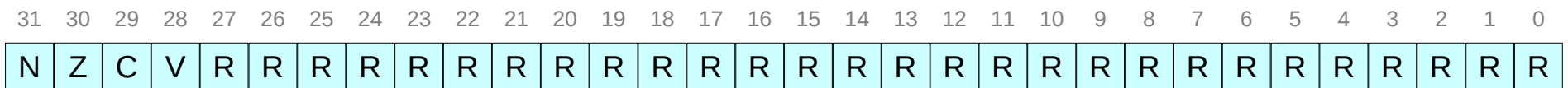
Multiple data transfer instruction

Single cycle execution of shift and ALU operations

Open instruction set for coprocessors

A very dense 16-bit compressed instruction set (Thumb)

ARM Exception Handling



References

- [1] <ftp://ftp.geoinfo.tuwien.ac.at/navratil/HaskellTutorial.pdf>
- [2] <https://www.umiacs.umd.edu/~hal/docs/daume02yaht.pdf>