Flip Flop Timing

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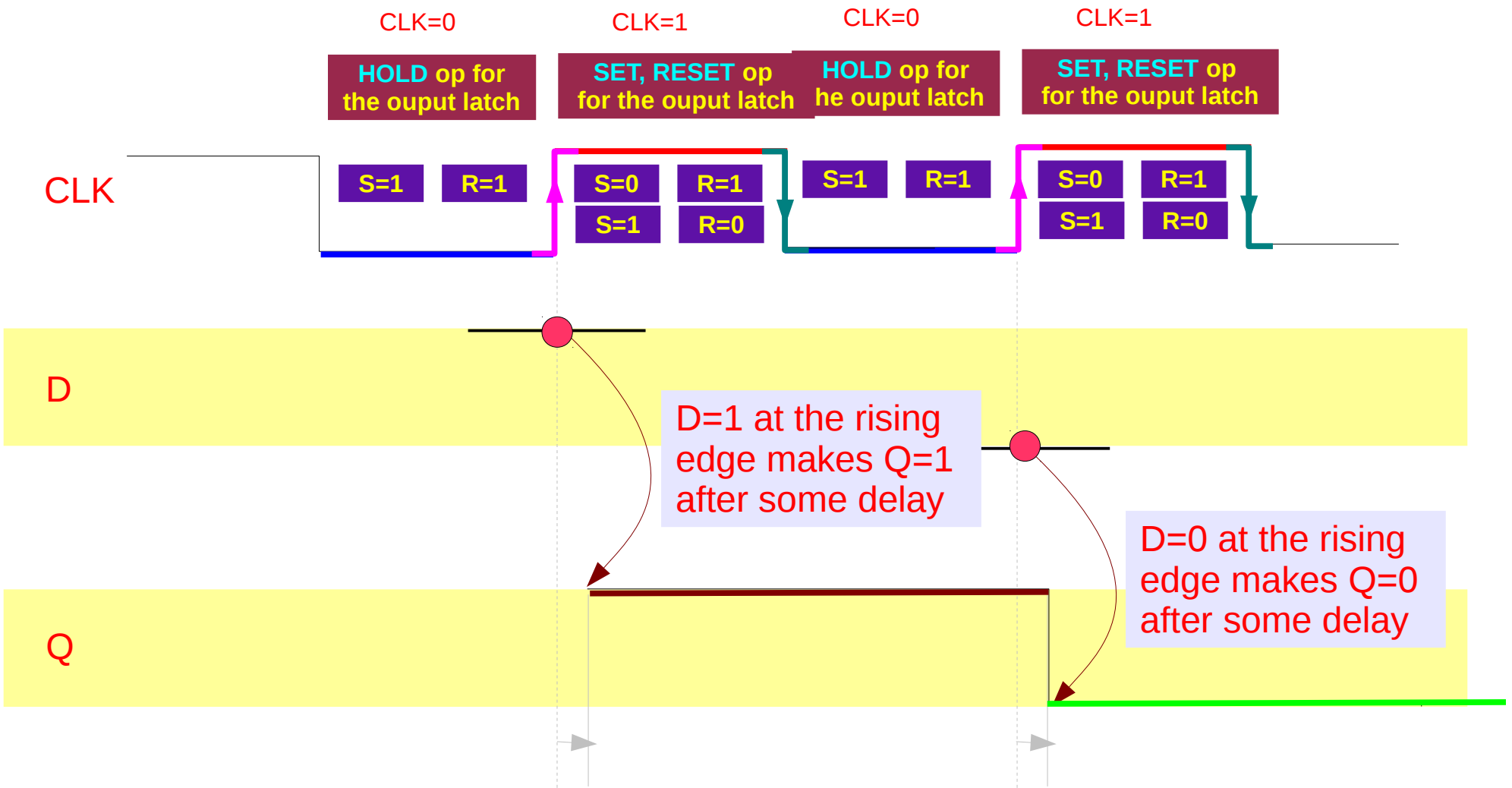
Please send corrections (or suggestions) to youngwlim@hotmail.com.

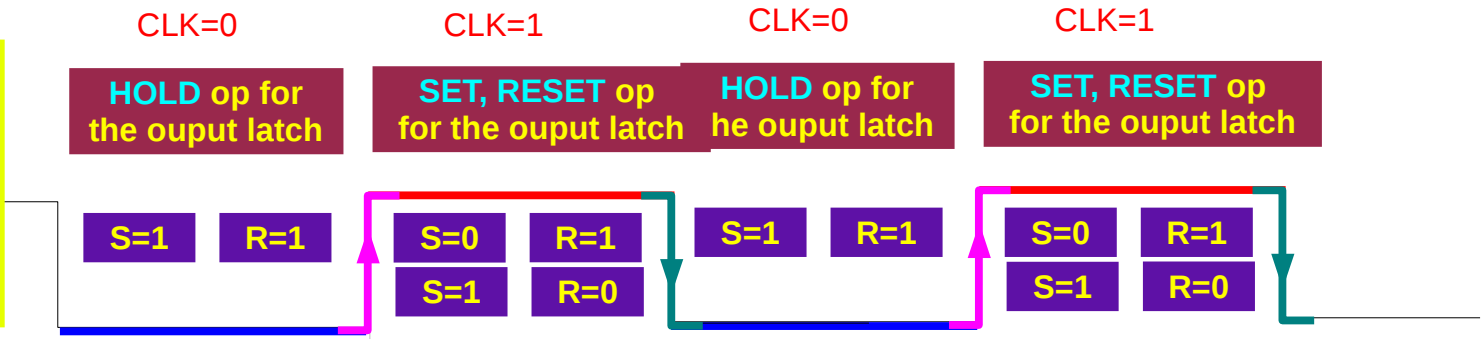
This document was produced by using OpenOffice and Octave.

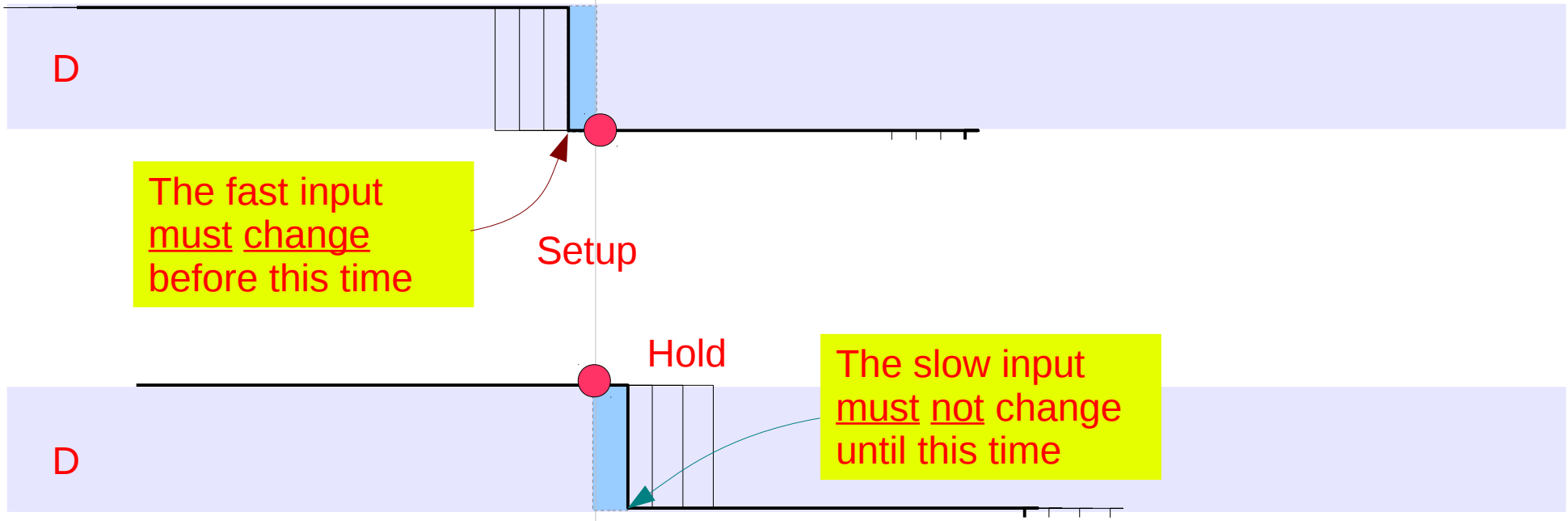
Input Data Sampling



Setup and Hold Time

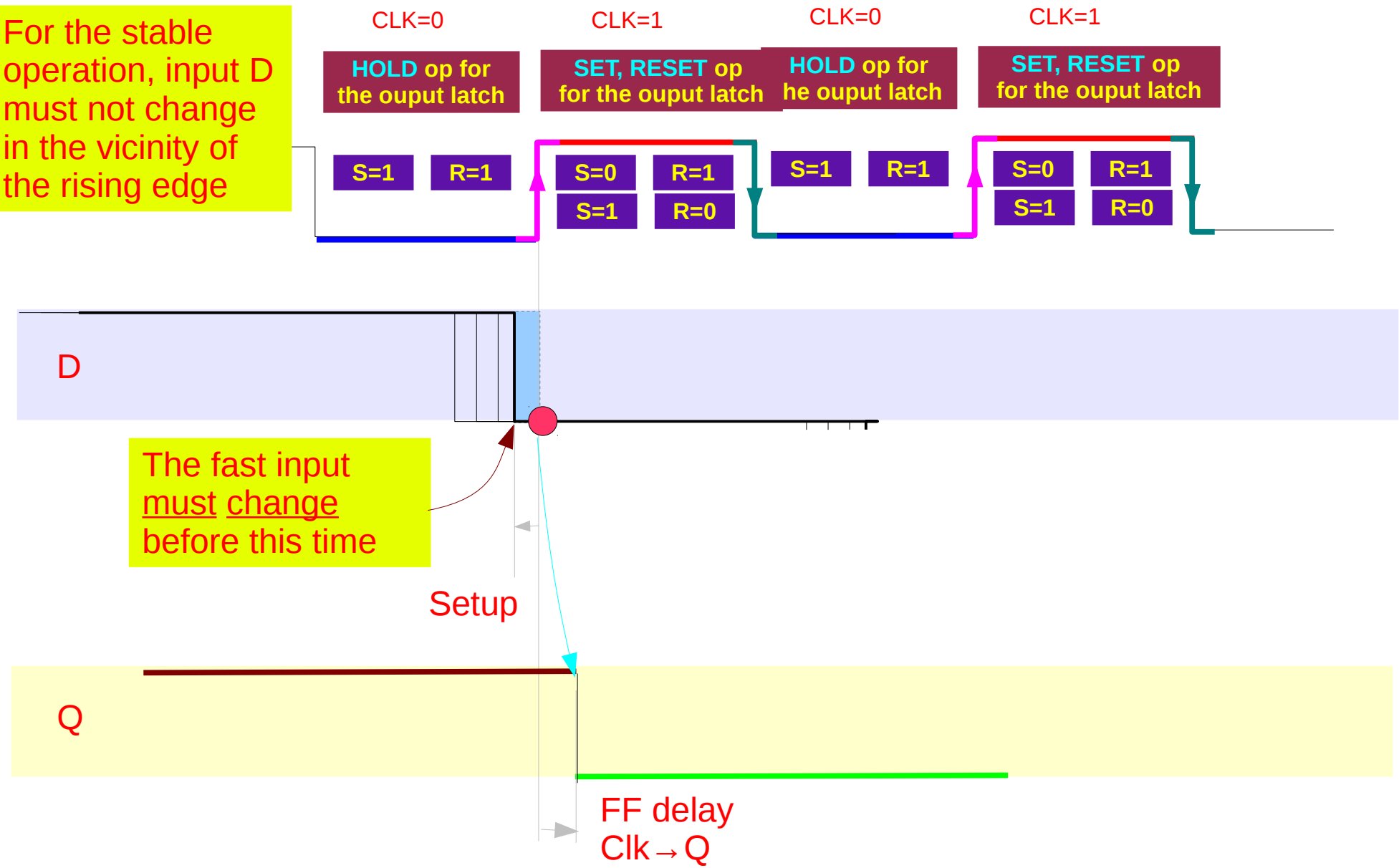
For the stable operation, input D must not change in the vicinity of the rising edge





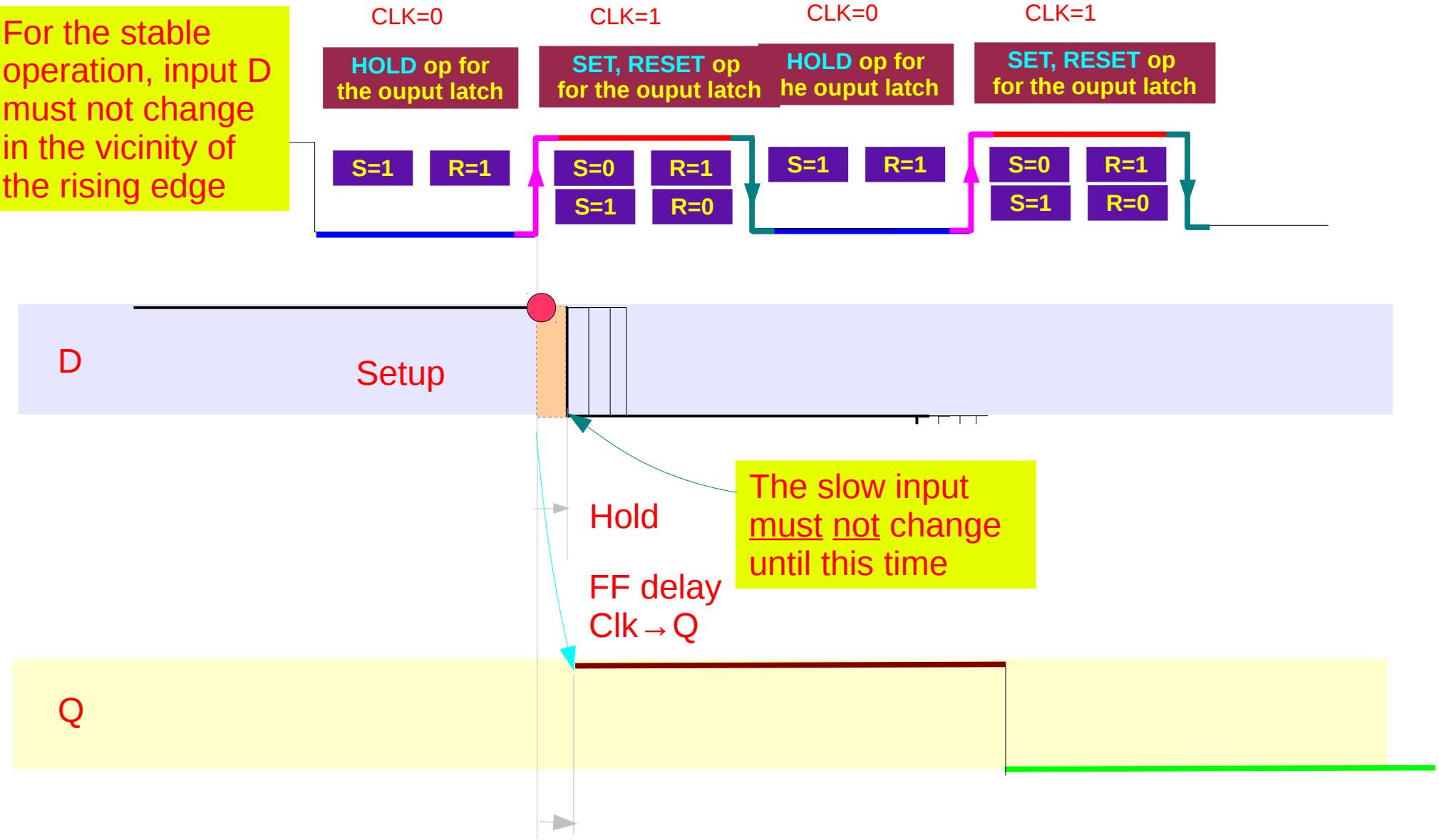
Setup Time

For the stable operation, input D must not change in the vicinity of the rising edge



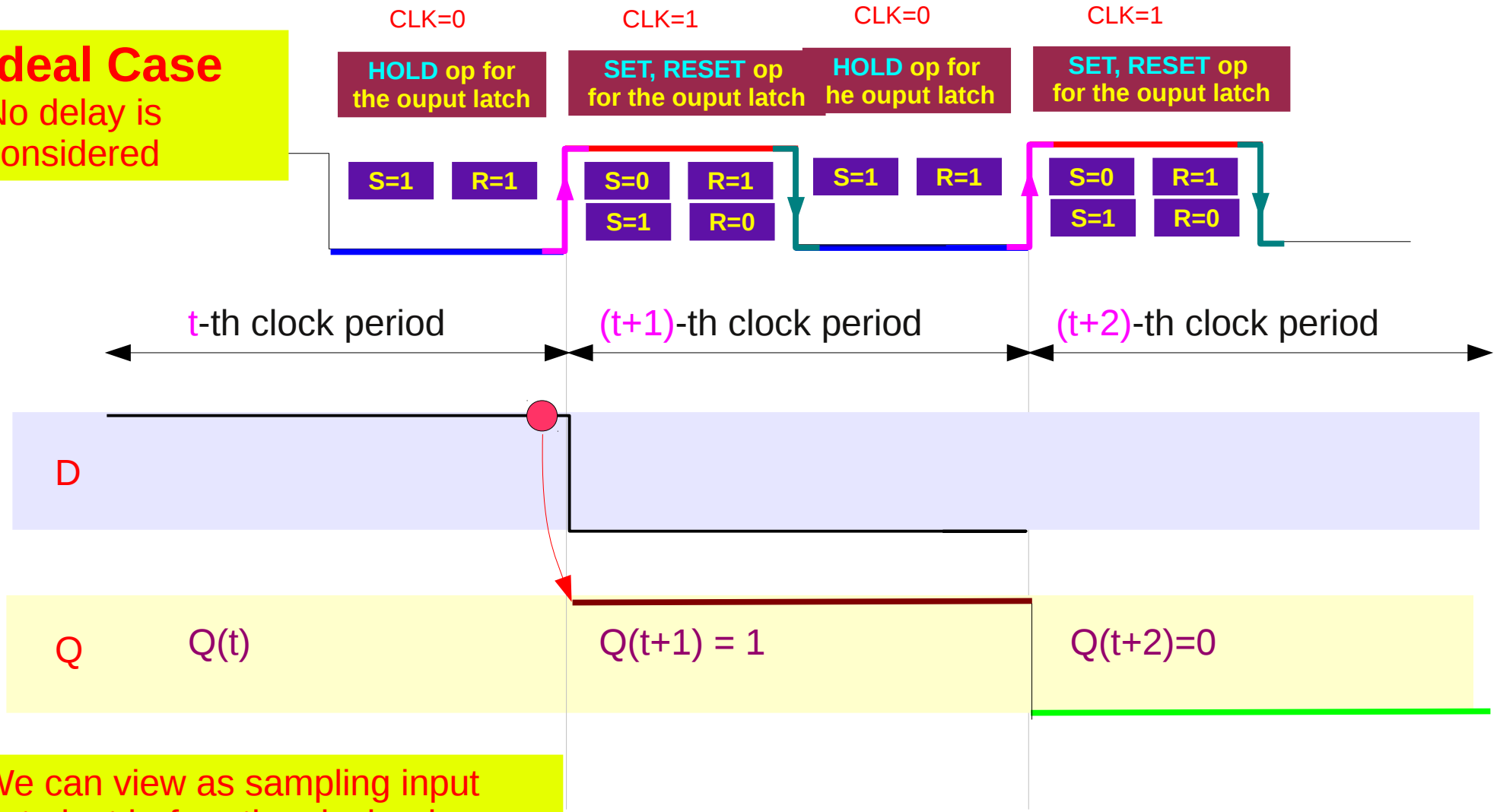
Hold Time

For the stable operation, input D must not change in the vicinity of the rising edge



Ideal Waveform (No delay)

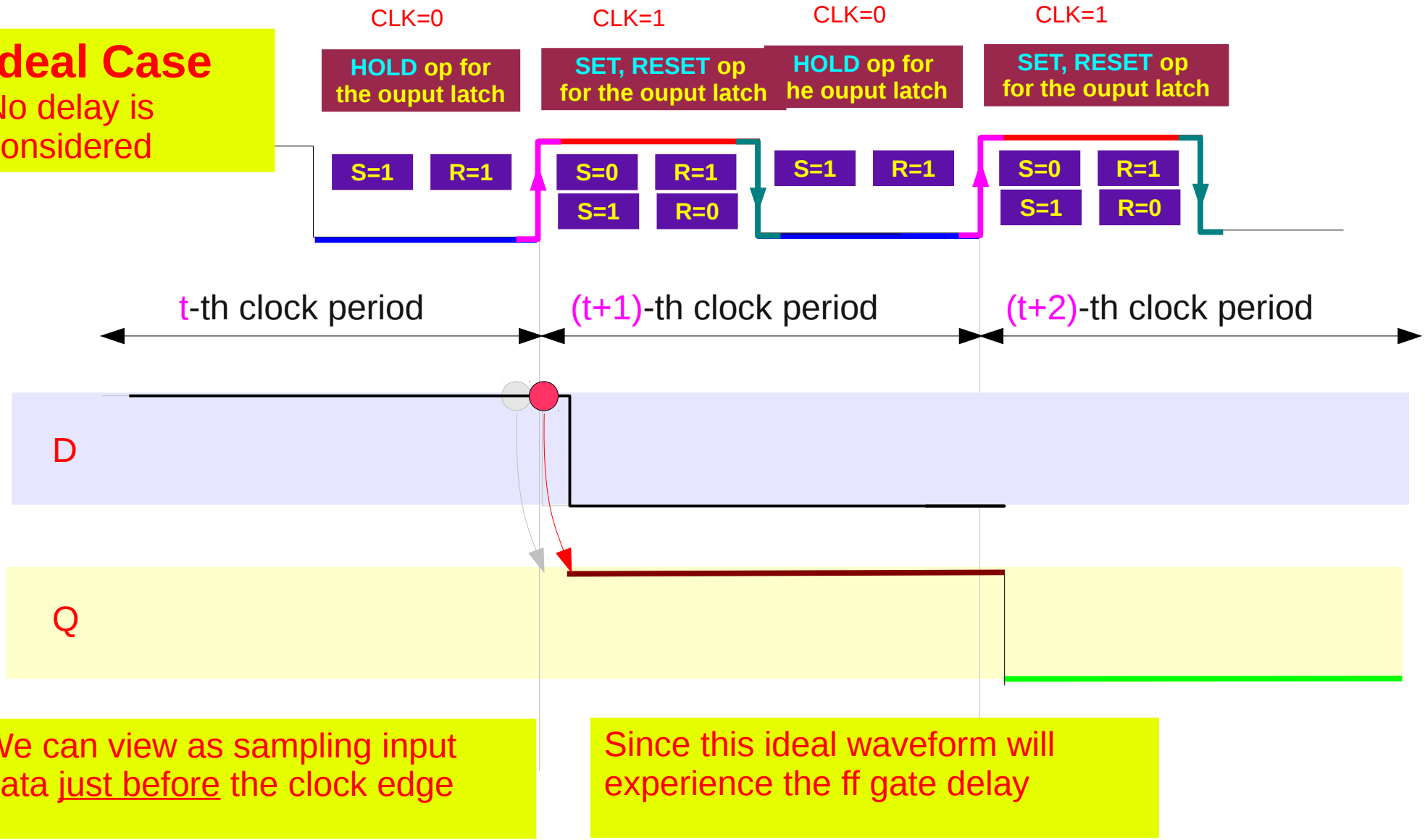
Ideal Case
No delay is considered



We can view as sampling input data just before the clock edge

Ideal Waveform (After delay)

Ideal Case
No delay is considered



We can view as sampling input data just before the clock edge

Since this ideal waveform will experience the ff gate delay