

Logic Families Static-1 (H.1)

20151215

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References

Some Figures from the following sites

[1] <http://pages.hmc.edu/harris/cmosvlsi/4e/index.html>

Weste & Harris Book Site

[2] en.wikipedia.org

[3] Digital Integrated Circuits : A Design Perspective,

Jan M. Rabaey,

(<http://bwrcs.eecs.berkeley.edu/Classes/lcBook/>)

[4] Digital Electronics and Design with VHDL

Pedroni

Other MOS Architectures

Static MOS

Pseudo-nMOS Logic

Transmission-gate Logic

BiCMOS Logic

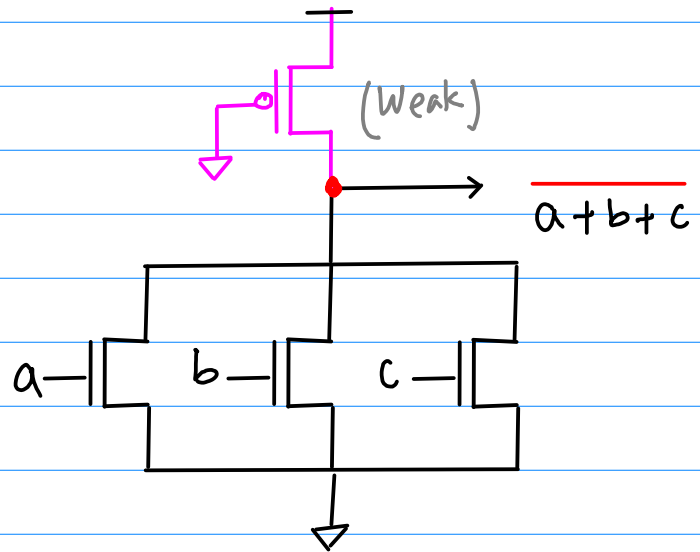
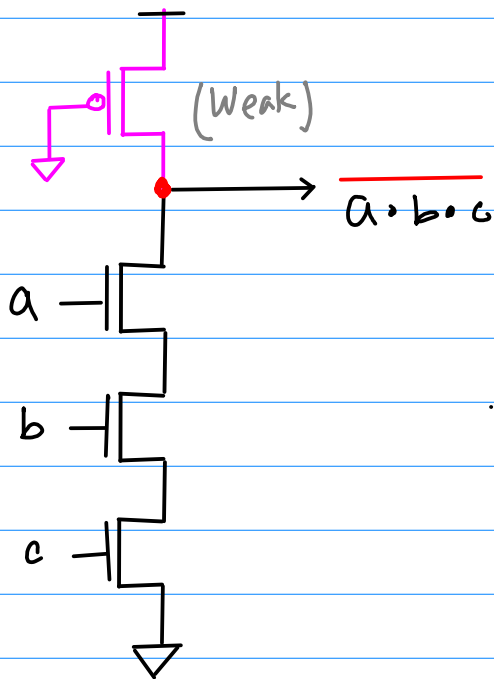
Dynamic MOS

Dynamic Logic

Domino Logic

C2MOS Logic

Pseudo-nMOS Logic

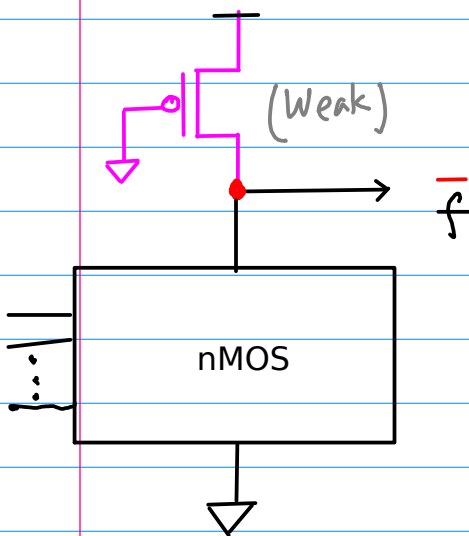


simply replace all pMOS with just one pMOS that is always ON

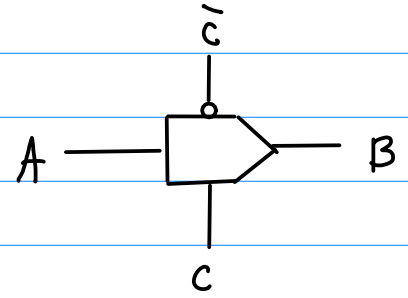
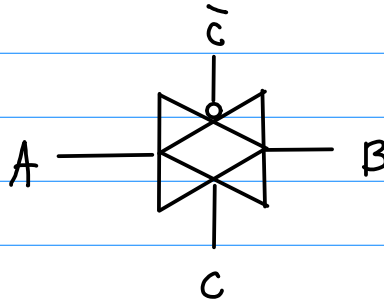
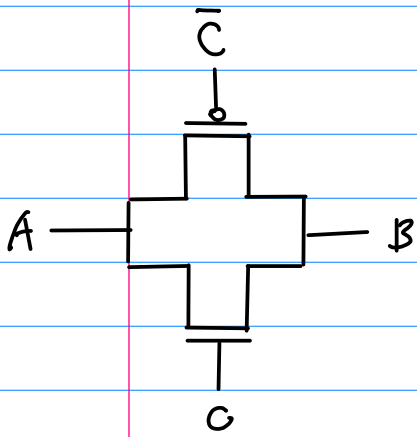
Pull-Up transistor
weak (small W/L, large R)
always nMOS wins (Off-On)

Reduced circuit size
Large fan-in possible
(no piled transistor)

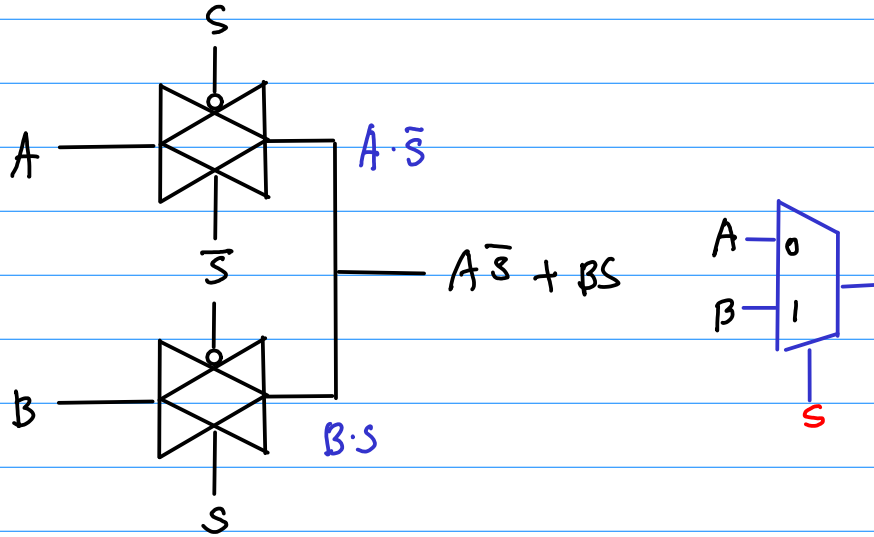
static power consumption
Slow rising time (large R)
Slow falling time (competing nMOS & pMOS)
Weak 0



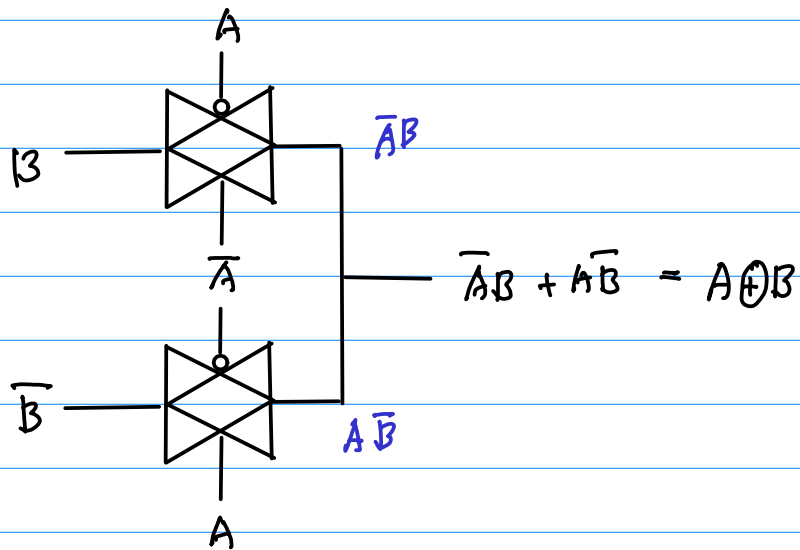
Transmission Gate Logic

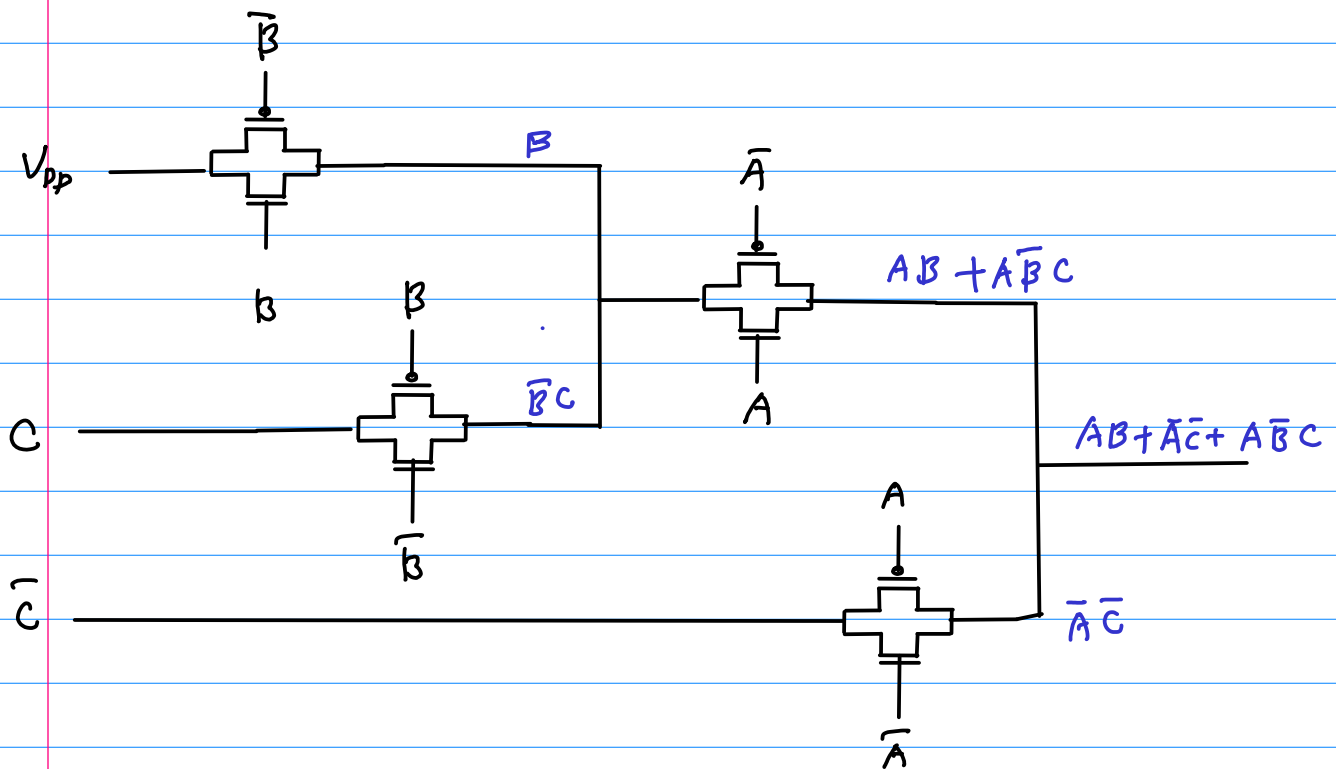
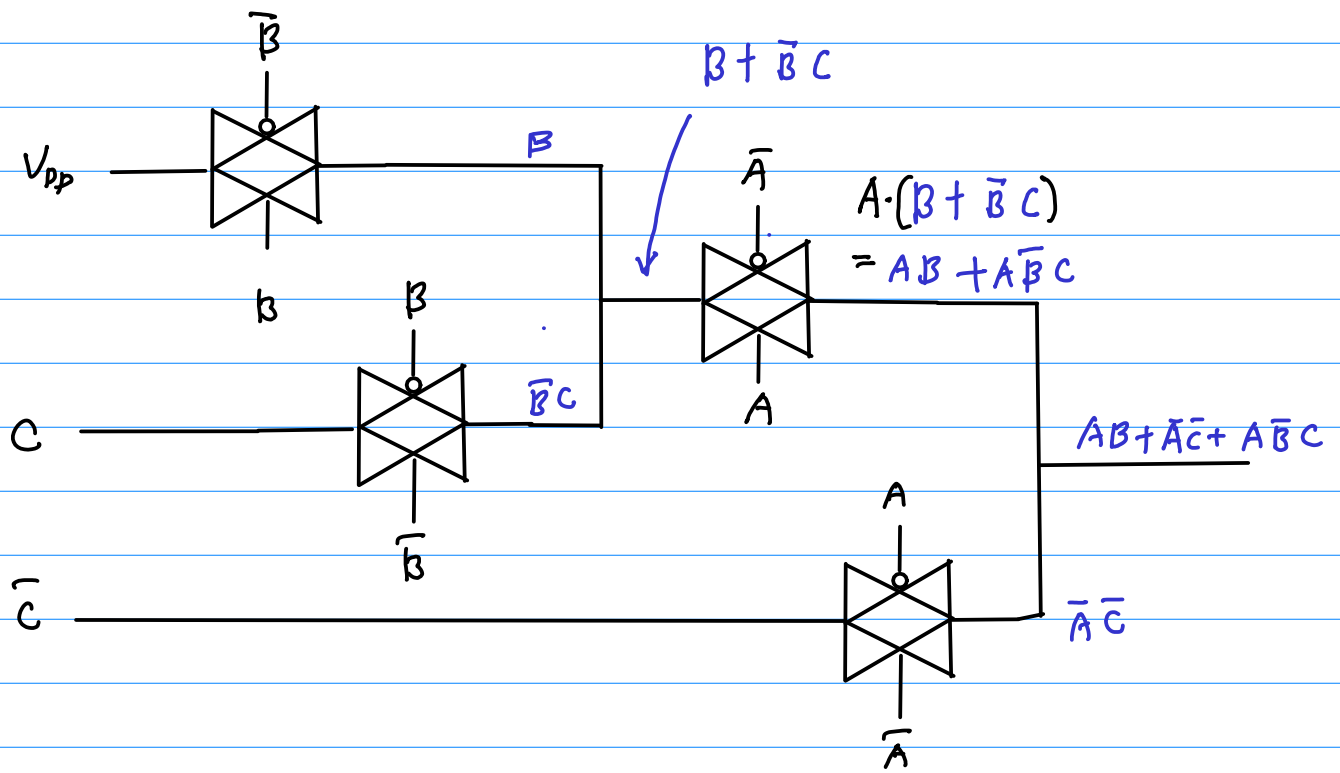


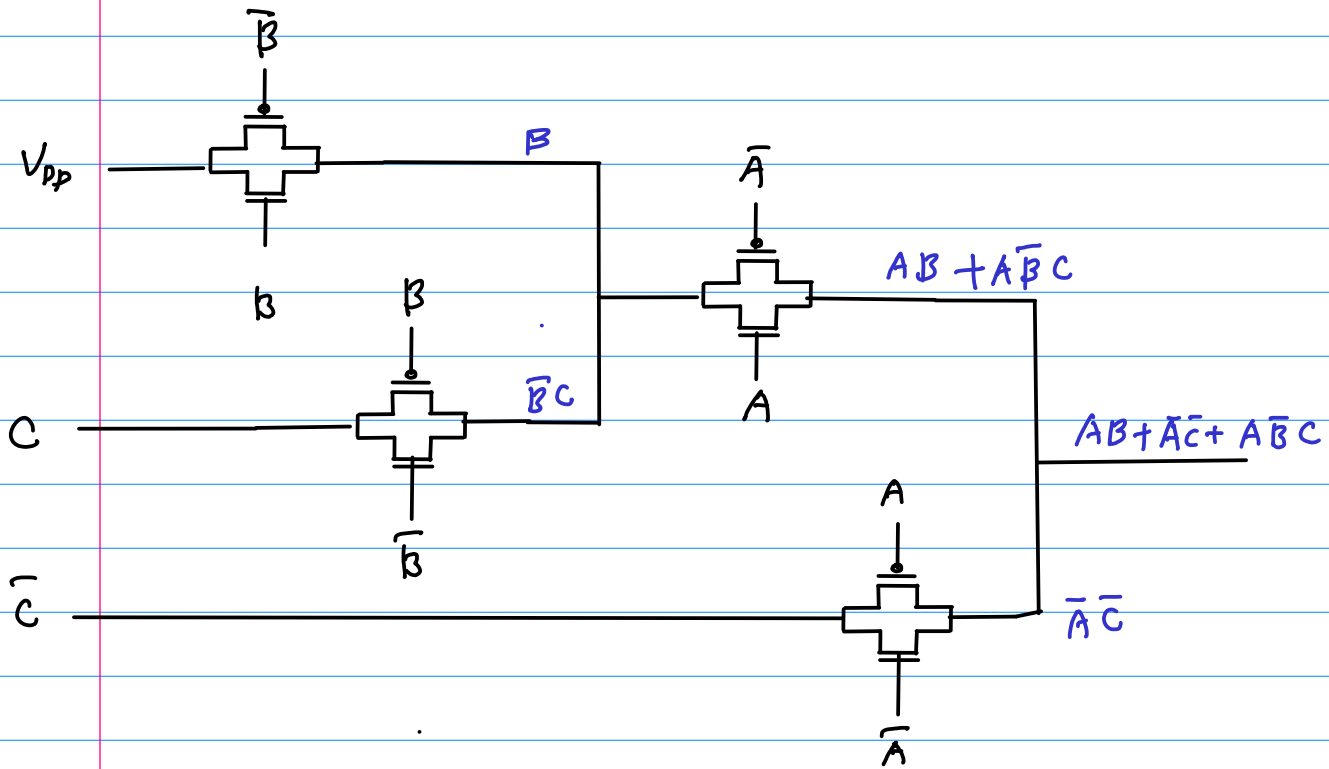
Mux



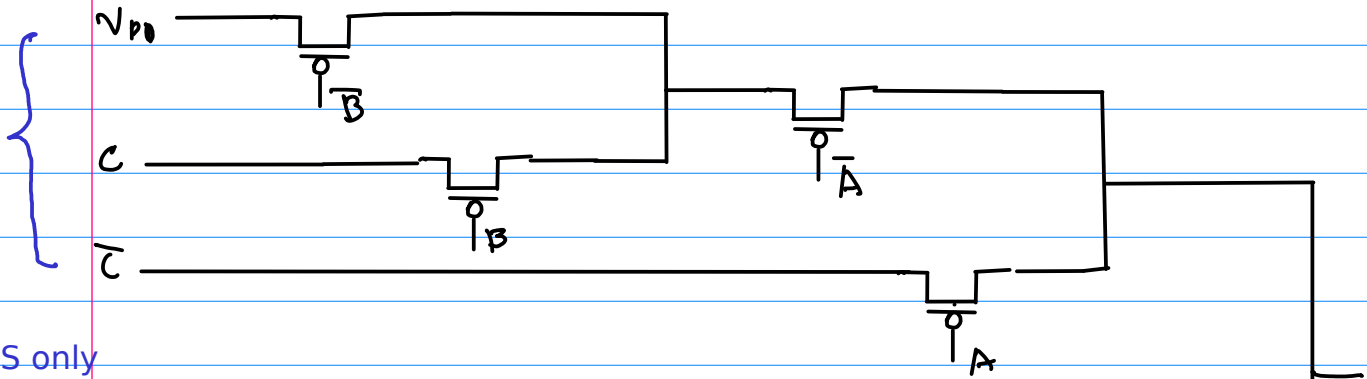
XOR



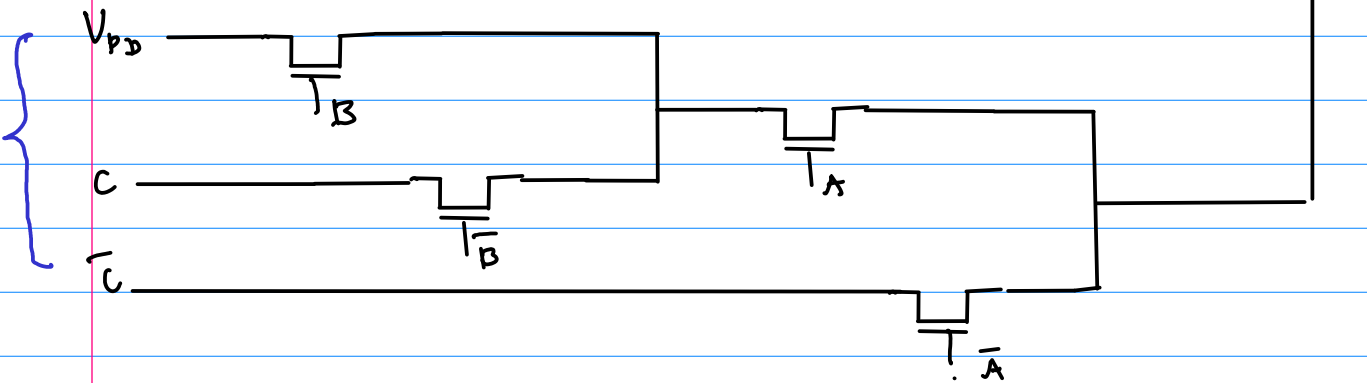




pMOS only

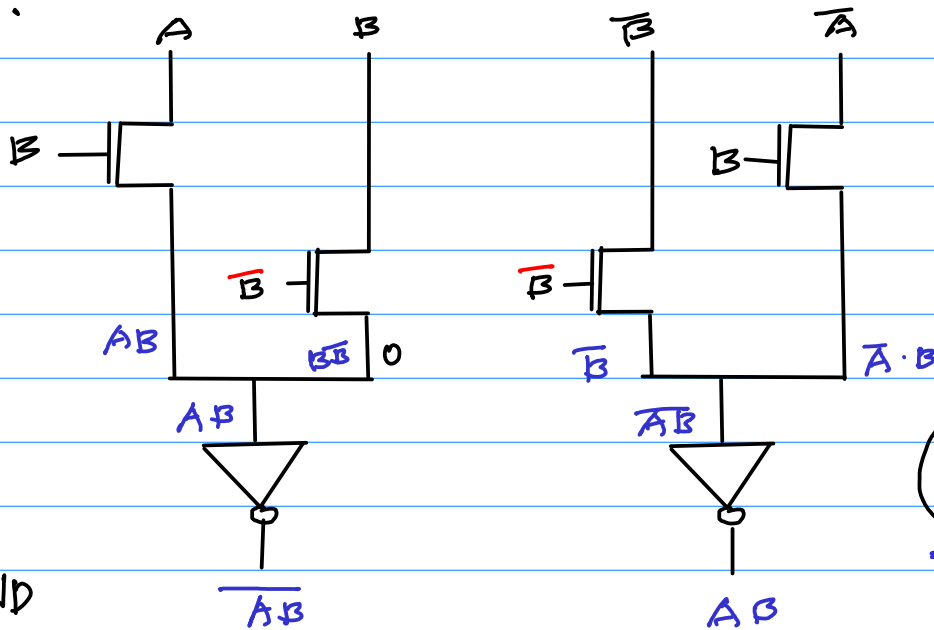


nMOS only



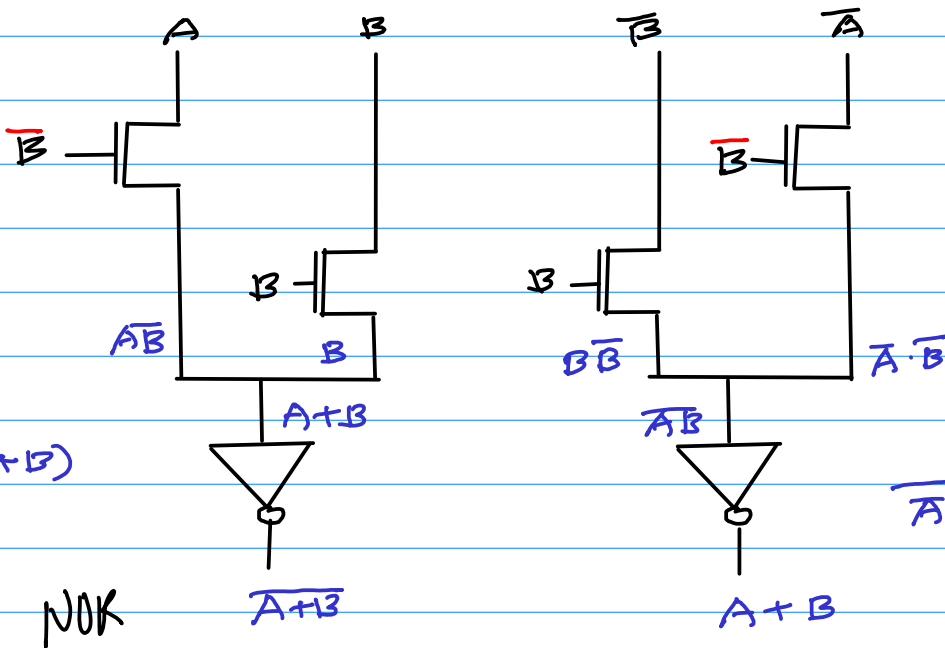
CPL

Complimentary Pass-Transistor Logic



NAND

$$\begin{aligned}
 & \overline{B + \overline{A \cdot B}} \\
 &= \overline{B + A} \cdot \overline{B + B} \\
 &= \overline{A + B} \\
 &= \overline{A \cdot B}
 \end{aligned}$$

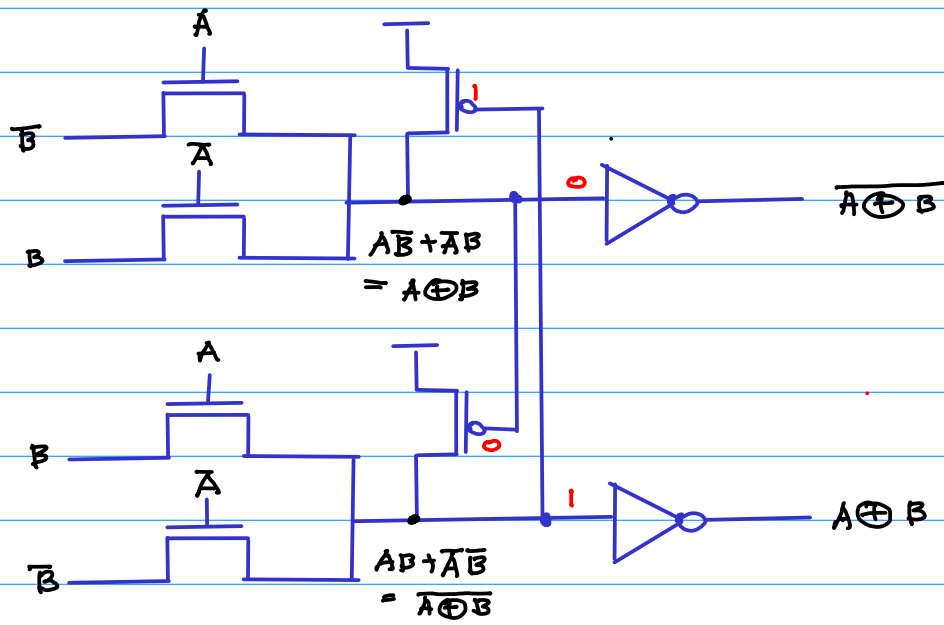


$$\begin{aligned}
 & \overline{A \cdot \overline{B} + B} \\
 &= \overline{(A + B) \cdot (B + B)} \\
 &= \overline{A + B}
 \end{aligned}$$

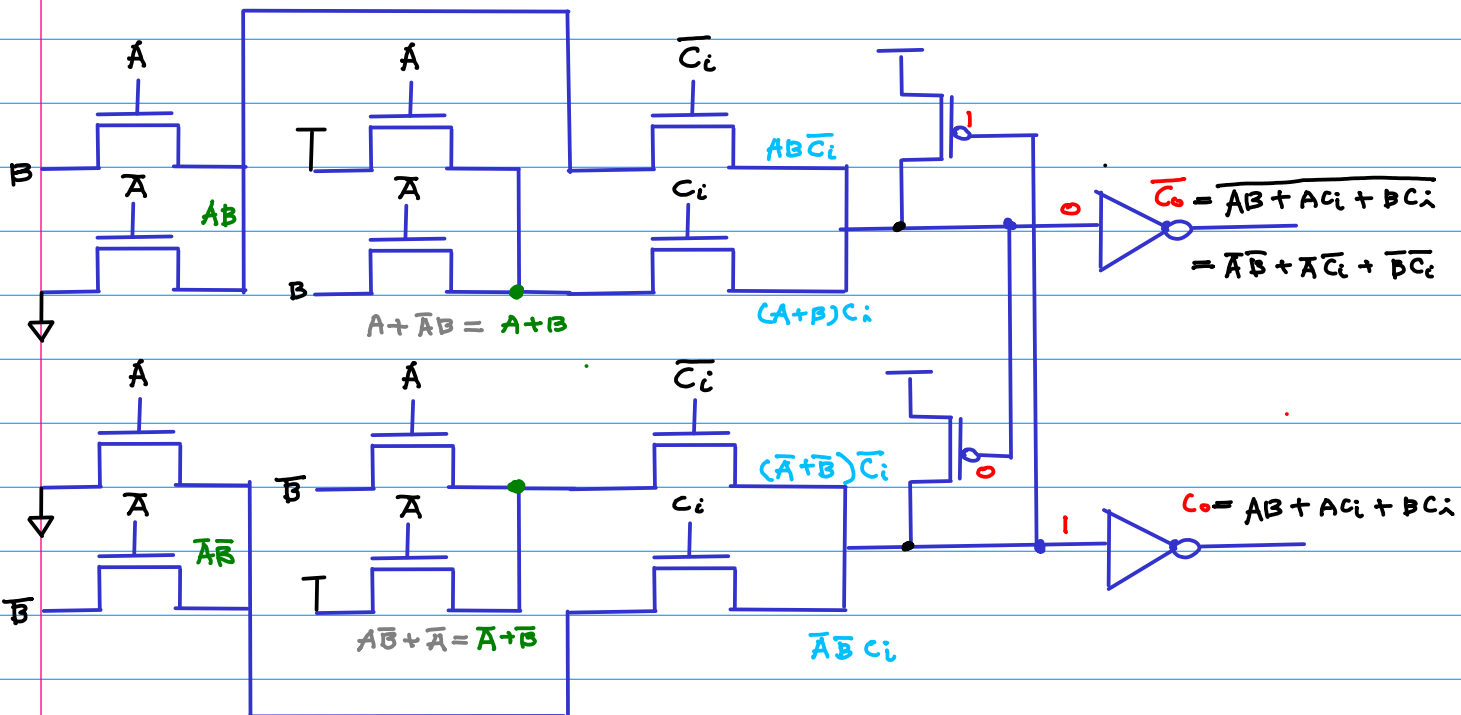
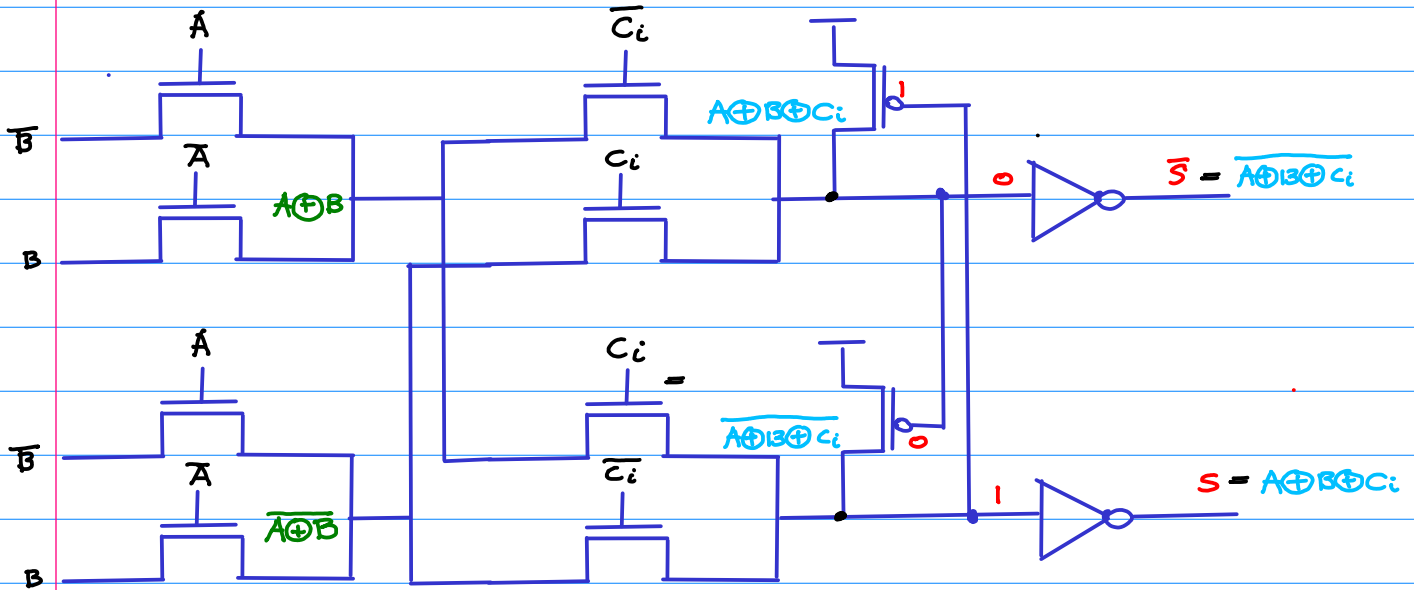
NOR

$$\overline{\overline{A \cdot B}} = A + B$$

CPL XOR



CPL FA



$C_i \backslash AB$	00	01	11	10
0			1	
1		1	1	1

$C_i \backslash AB$	00	01	11	10
0	1	1		1
1	1			

