ROM based FPGAs (3A)

Please send corrections (or suggestions) to youngwlim@hotmail.com.

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Young Won Lim
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Based on

The VLSI Handbook, edited by Wai-Kai Chen, CRC

ROM based connection

Use of anti-fuse

Once anti-fuse becomes conductive,
it cannot be non-conductive again

Typical applications use 85% of the logic gates
But only 2~3% of antifuses are used for connection
If fuses instead of antifuses are used,
then 97~98% of fuses would be used for disconnection

ROM based connection

Actel

Row-based structure

Logic block (called as a logic module)
three mux'es to form a 4:1 mux
one OR gate to select the final mux
Some of inputs and outputs can be complemented
8 inputs
1 output
Can realize many different logic gates
With some inputs inverted

ROM based connection

4 basic logic gates:
NAND, AND, NOR, OR gates with 2, 3, or 4 inputs

EXCLUSIVE-OR, EXCLUSIVE-NOR gates
AND-EXCLUSIVE-OR gates
AND-OR gates
OR-AND gates
A variety of D latches

ROM based connection

Vertical Control
Vertical Track Segment
Cross antifuse
Vertical Pass Transistor

Logic Module
Connection to an input of the output of Logic Block

Horizontal Control
Horizontal Track Segment
Horizontal antifuse
Horizontal Pass Transistor

References

[1] ftp://ftp.geoinfo.tuwien.ac.at/navratil/HaskellTutorial.pdf
[2] https://www.umiacs.umd.edu/~hal/docs/daume02yaht.pdf