

Carry Lookahead Adder (1A)

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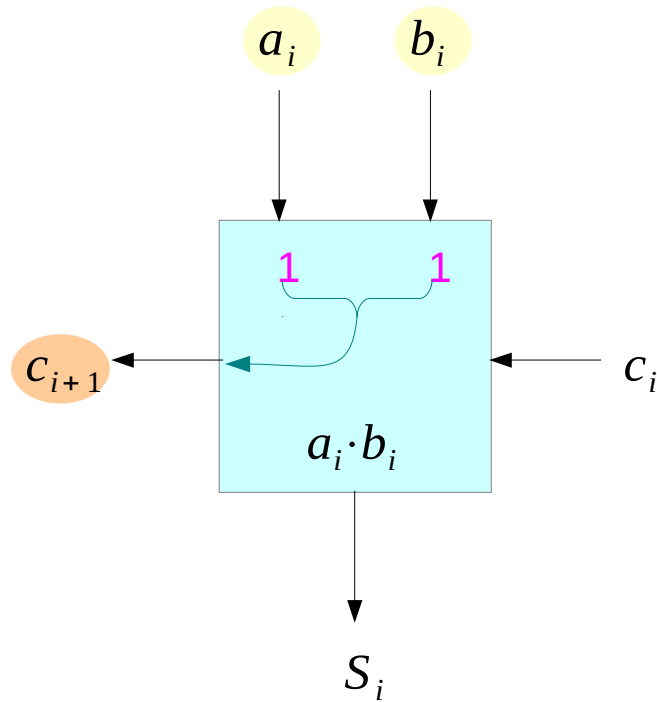
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G and P

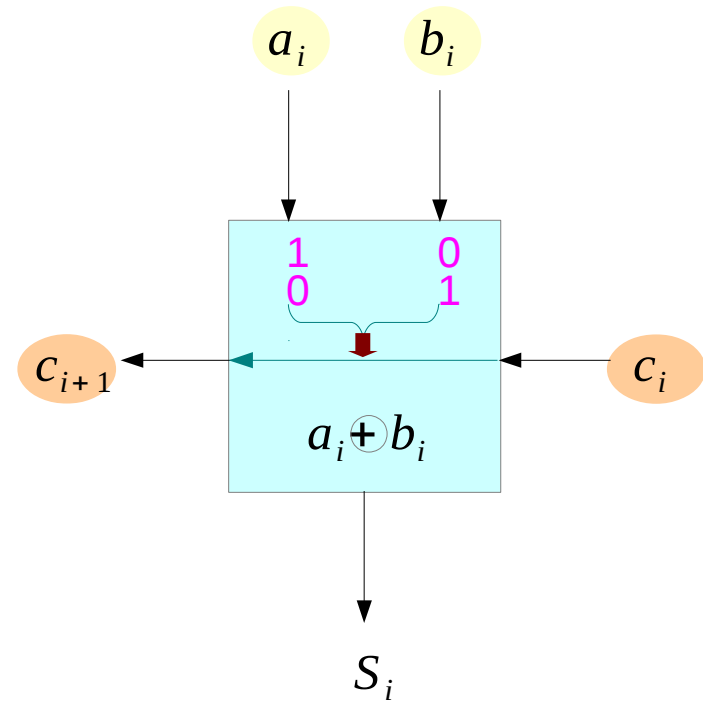
Generate $G_i = a_i \cdot b_i$

Propagate $P_i = a_i \oplus b_i$

$$c_{out} = G_i + P_i c_i$$



Generate c_{i+1}



Propagate c_i

Carry Equations

$$c_{i+1} = G_i + P_i c_i$$

$$c_1 = G_0 + P_0 c_0$$

$$c_2 = G_1 + P_1 c_1$$

$$c_3 = G_2 + P_2 c_2$$

$$c_4 = G_3 + P_3 c_3$$

$$c_1 = G_0 + P_0 c_0$$

$$c_2 = G_1 + P_1 [G_0 + P_0 c_0]$$

$$c_3 = G_2 + P_2 [G_1 + P_1 [G_0 + P_0 c_0]]$$

$$c_4 = G_3 + P_3 [G_2 + P_2 [G_1 + P_1 [G_0 + P_0 c_0]]]$$

$$G_0 + P_0 c_0 = c_1$$

$$G_1 + P_1 G_0 + P_1 P_0 c_0 = c_2$$

$$G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 c_0 = c_3$$

$$G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 c_0 = c_4$$

Carry Equations into Gates (1)

$$c_{i+1} = G_i + P_i c_i$$

$$c_1 = G_0 + P_0 c_0$$

$$c_2 = G_1 + P_1 c_1$$

$$c_3 = G_2 + P_2 c_2$$

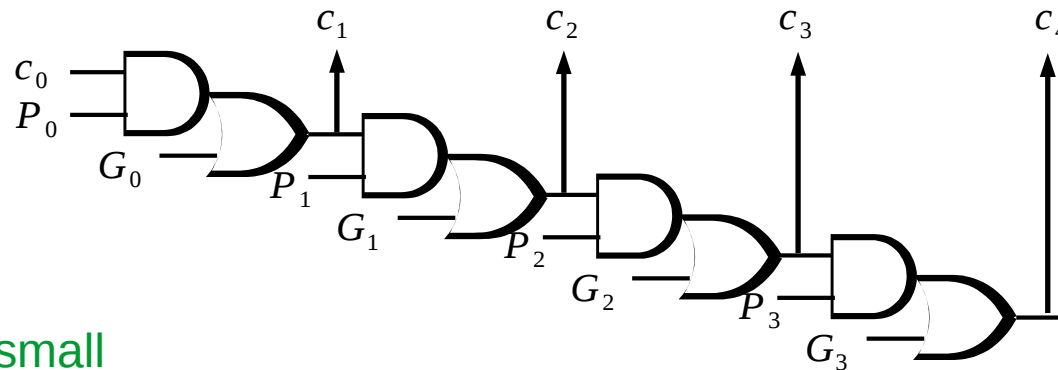
$$c_4 = G_3 + P_3 c_3$$

$$c_1 = G_0 + P_0 c_0$$

$$c_2 = G_1 + P_1 [G_0 + P_0 c_0]$$

$$c_3 = G_2 + P_2 [G_1 + P_1 [G_0 + P_0 c_0]]$$

$$c_4 = G_3 + P_3 [G_2 + P_2 [G_1 + P_1 [G_0 + P_0 c_0]]]$$



Fan-in number: small
Stage number: large

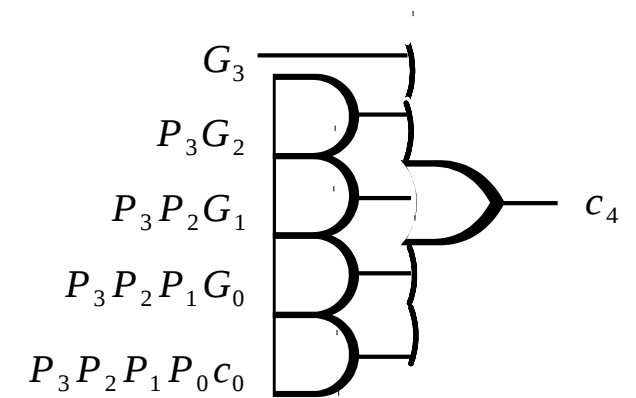
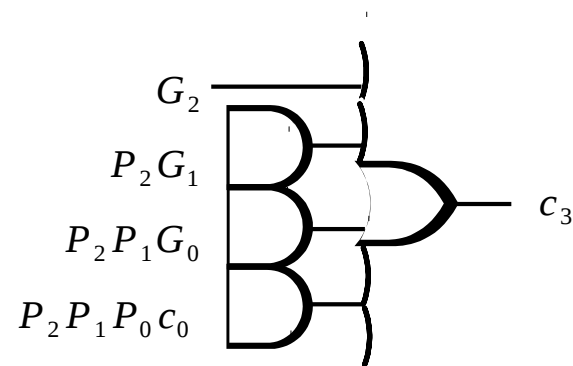
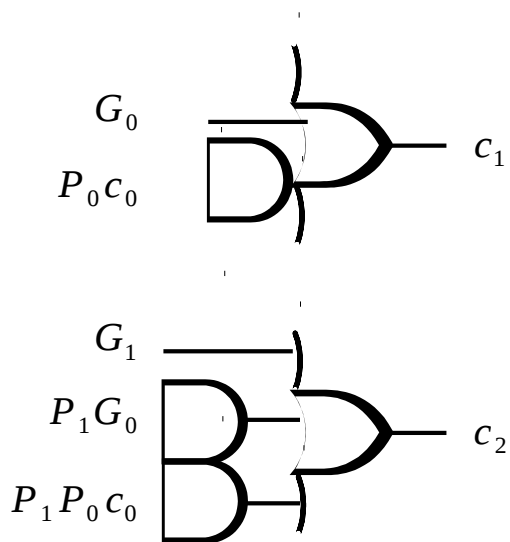
Carry Equations into Gates (2)

$$G_0 + P_0 c_0 = c_1$$

$$G_1 + P_1 G_0 + P_1 P_0 c_0 = c_2$$

$$G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 c_0 = c_3$$

$$G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 c_0 = c_4$$



Fan-in number: large
Stage number: small

Full Carry Lookahead

AND2, OR2

$$G_0 + P_0 c_0 = c_1$$

AND3, OR3

$$G_1 + P_1 G_0 + P_1 P_0 c_0 = c_2$$

AND4, OR4

$$G_2 + P_2 G_1 + P_2 P_1 G_0 + P_2 P_1 P_0 c_0 = c_3$$

AND5, OR5

$$G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 c_0 = c_4$$

AND32, OR32

$$= c_{32}$$

Large number of fan-in : Impractical

- High Radix Addition (2^g)
- Multi-level Lookahead

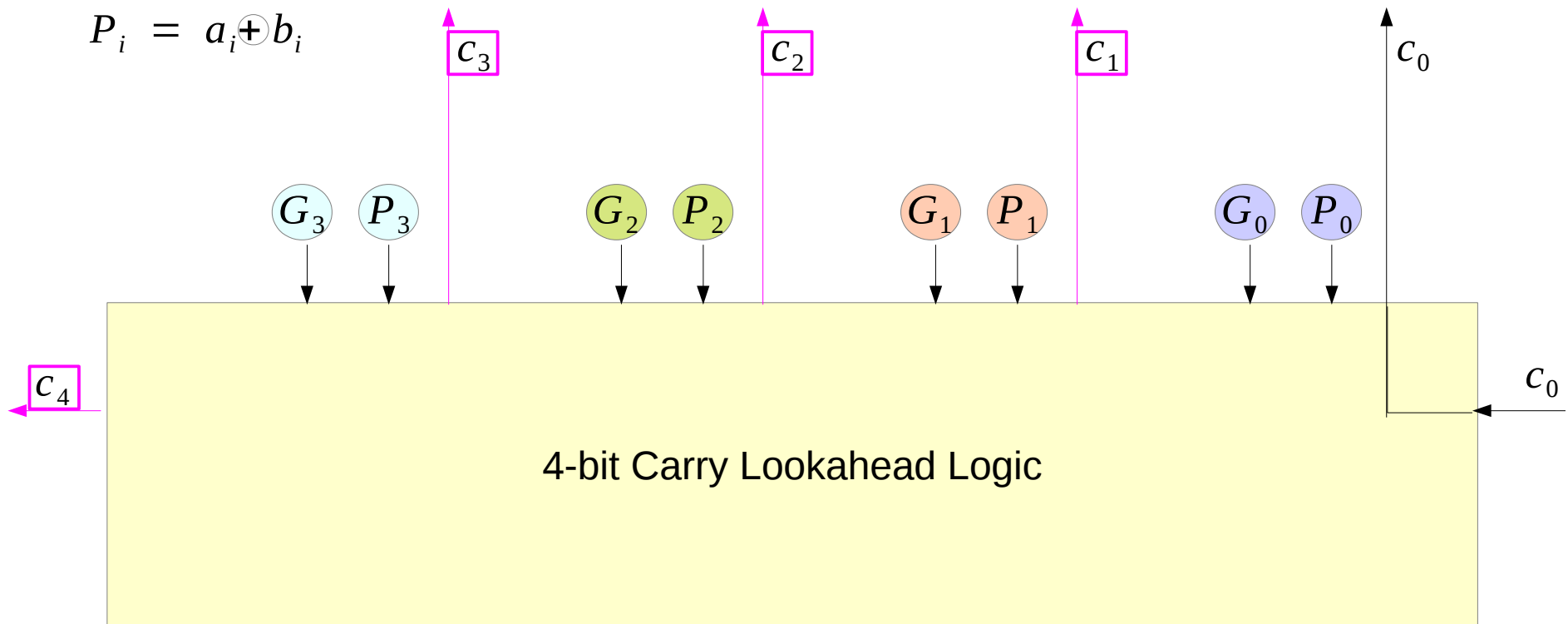
4-bit Carry Lookahead Logic – interface

All G_i 's P_i 's are computed
simultaneously from a_i and b_i

each c_i 's takes 2 gate delays

$$G_i = a_i \cdot b_i$$

$$P_i = a_i \oplus b_i$$



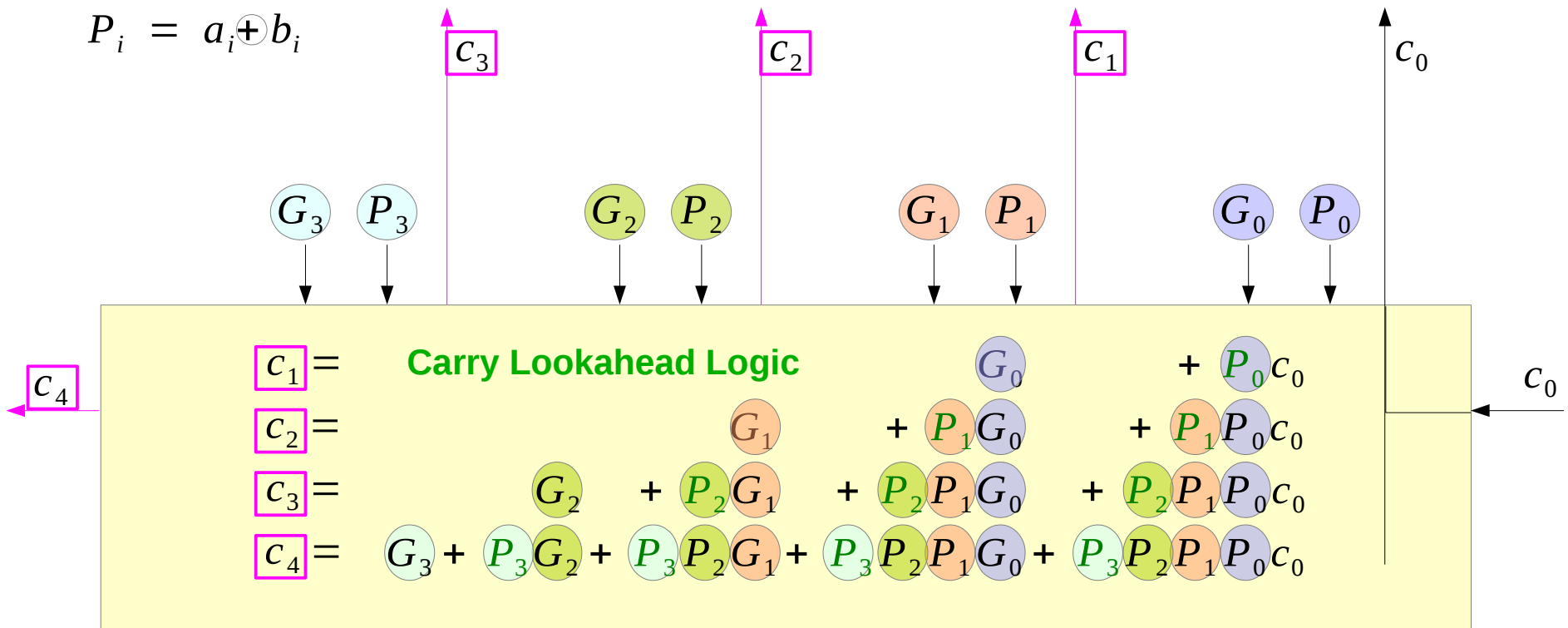
4-bit Carry Lookahead Logic – boolean equations

All G_i 's P_i 's are computed simultaneously from a_i and b_i

each c_i 's takes 2 gate delays

$$G_i = a_i \cdot b_i$$

$$P_i = a_i \oplus b_i$$



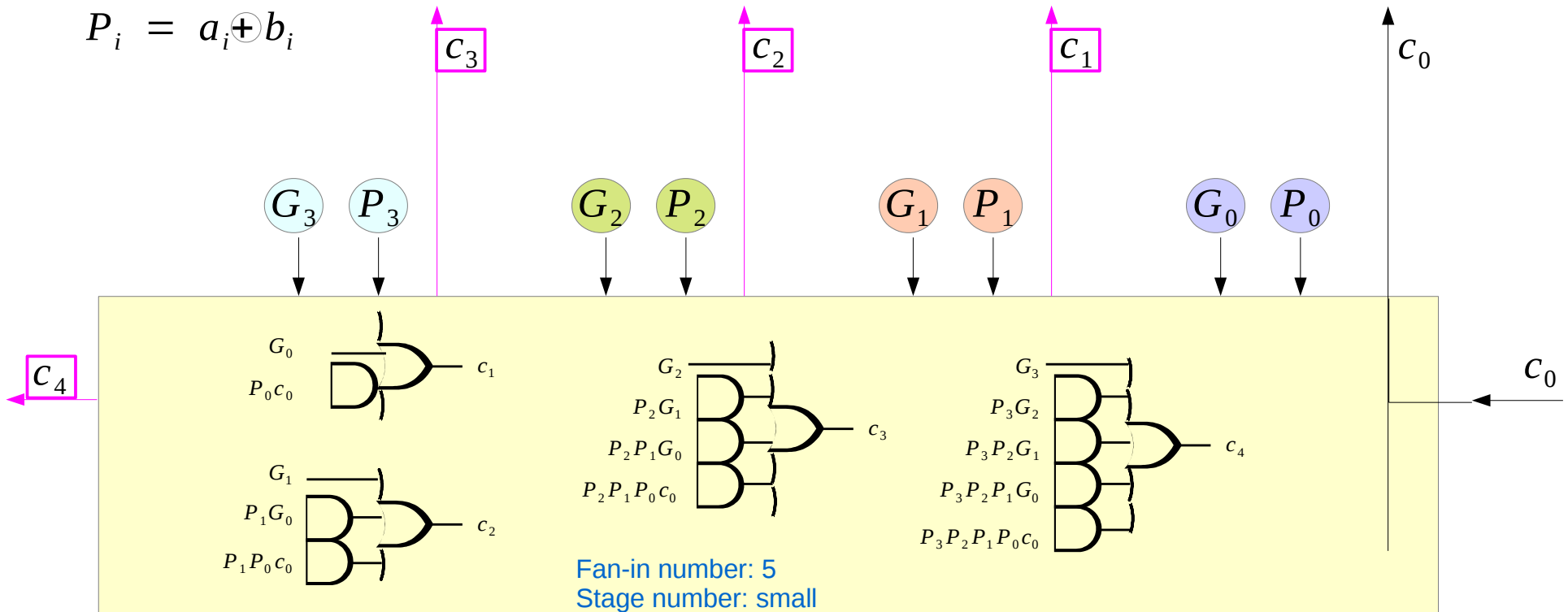
4-bit Carry Lookahead Logic – POS

All G_i 's P_i 's are computed simultaneously from a_i and b_i

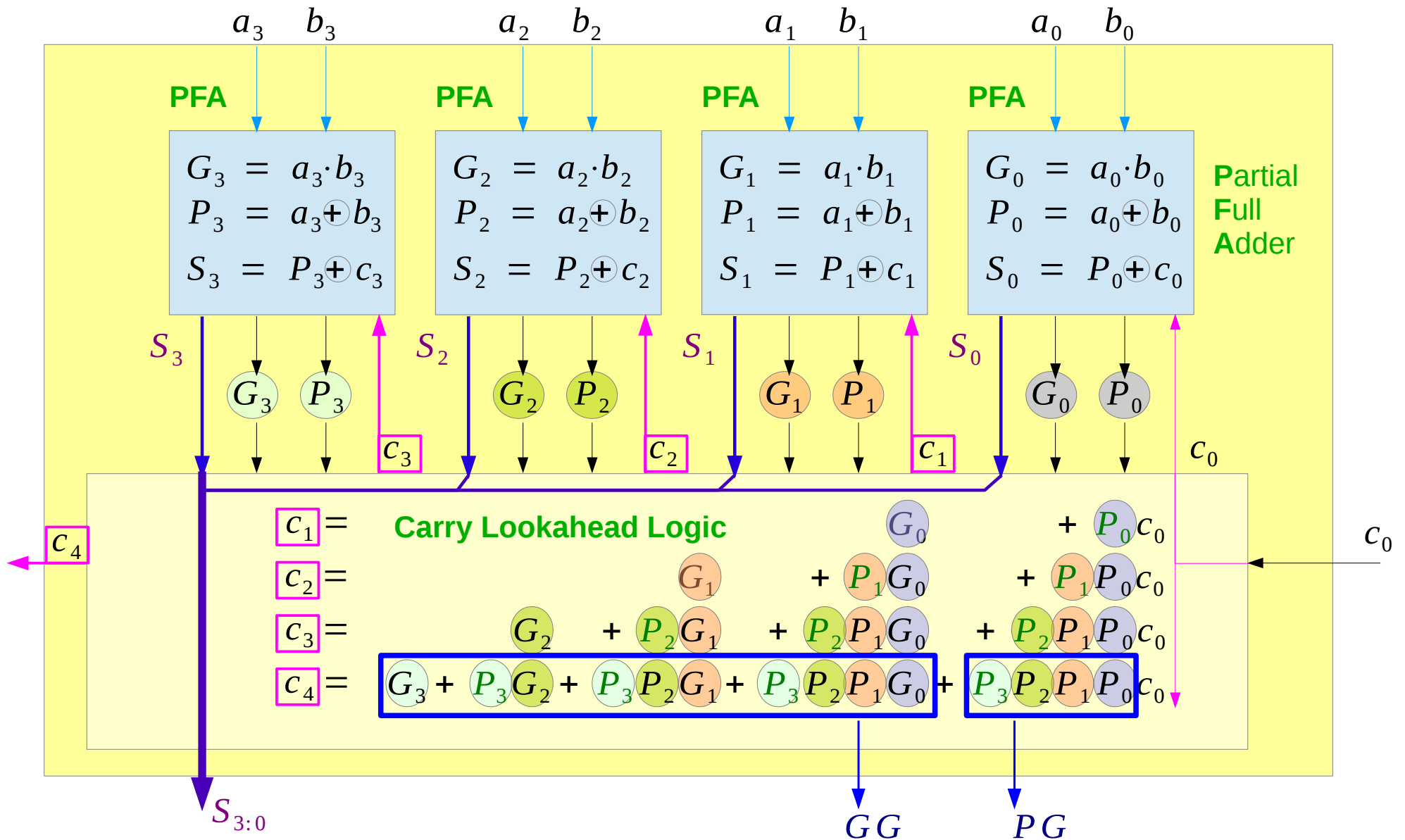
each c_i 's takes 2 gate delays

$$G_i = a_i \cdot b_i$$

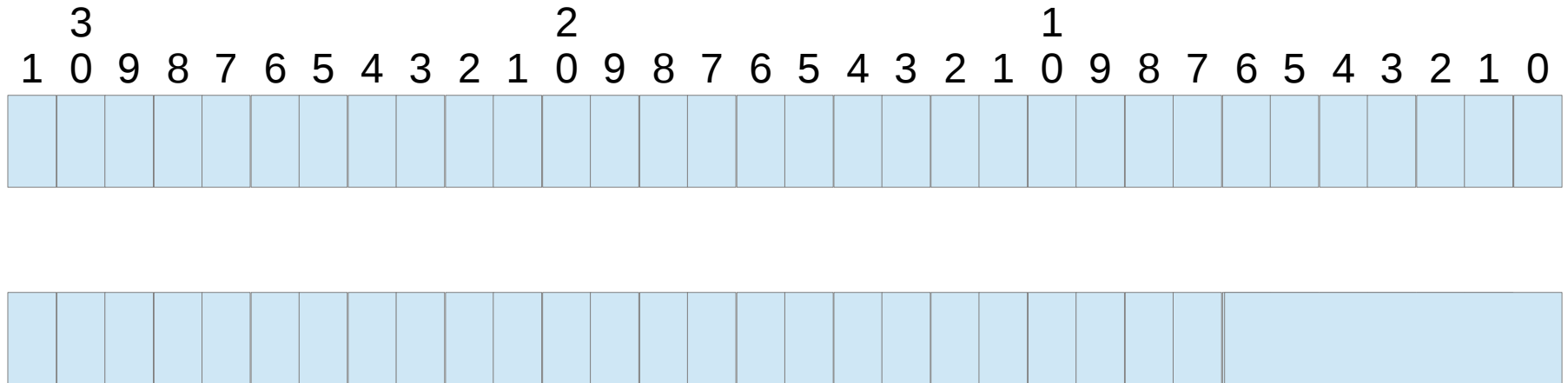
$$P_i = a_i \oplus b_i$$



4-bit CLA

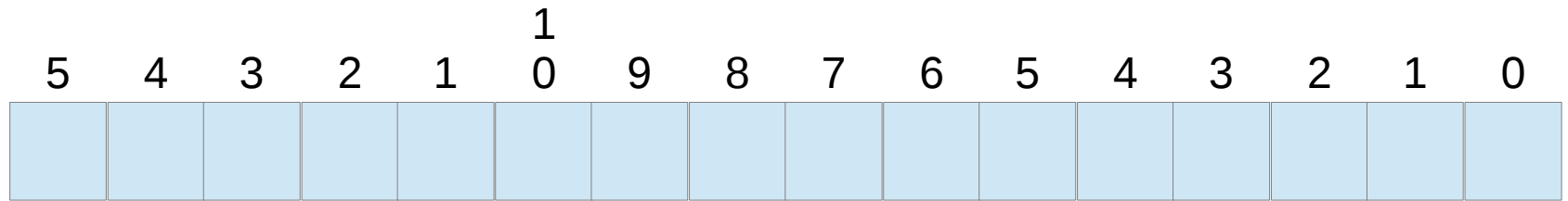


Multi-level Carry Lookahead

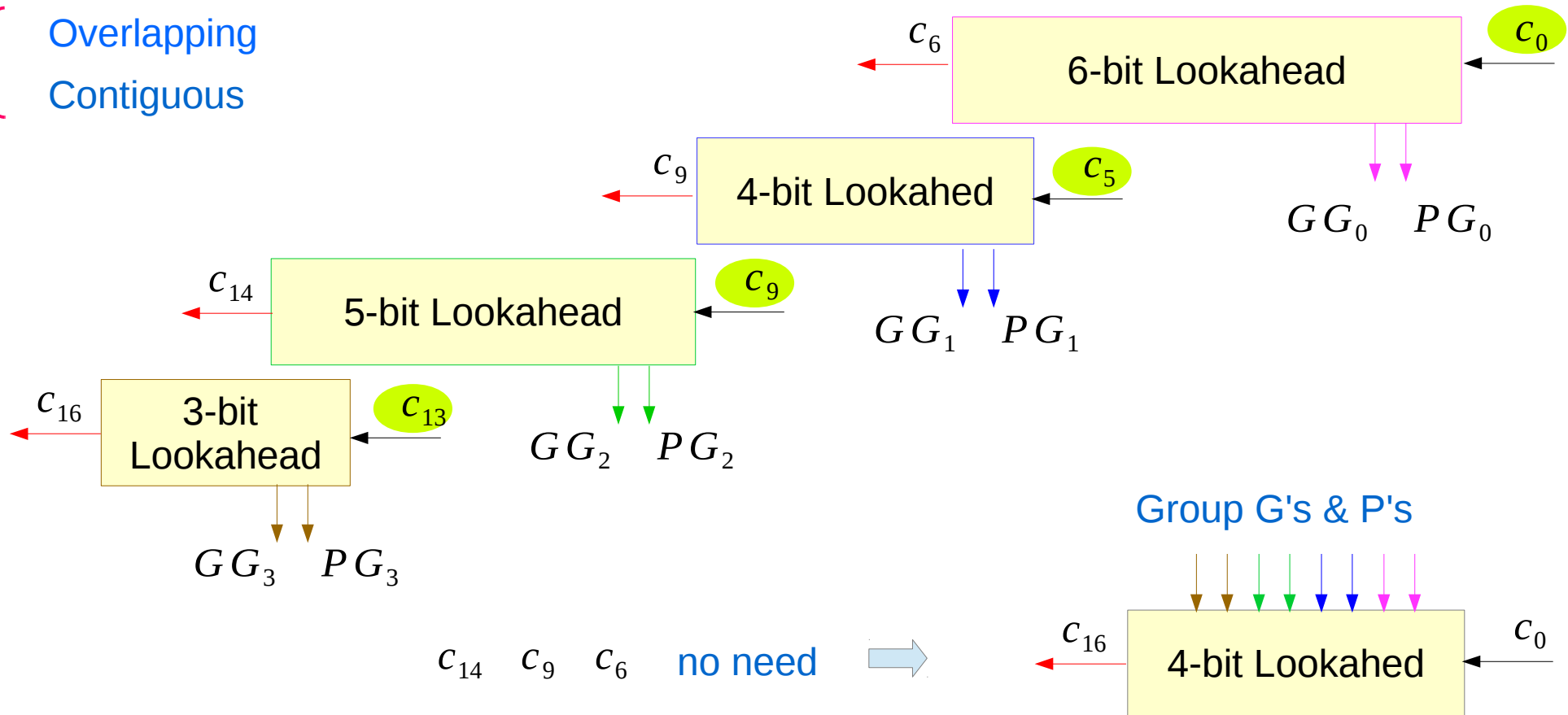


{ High Radix Addition (2^g)
Multi-level Lookahead

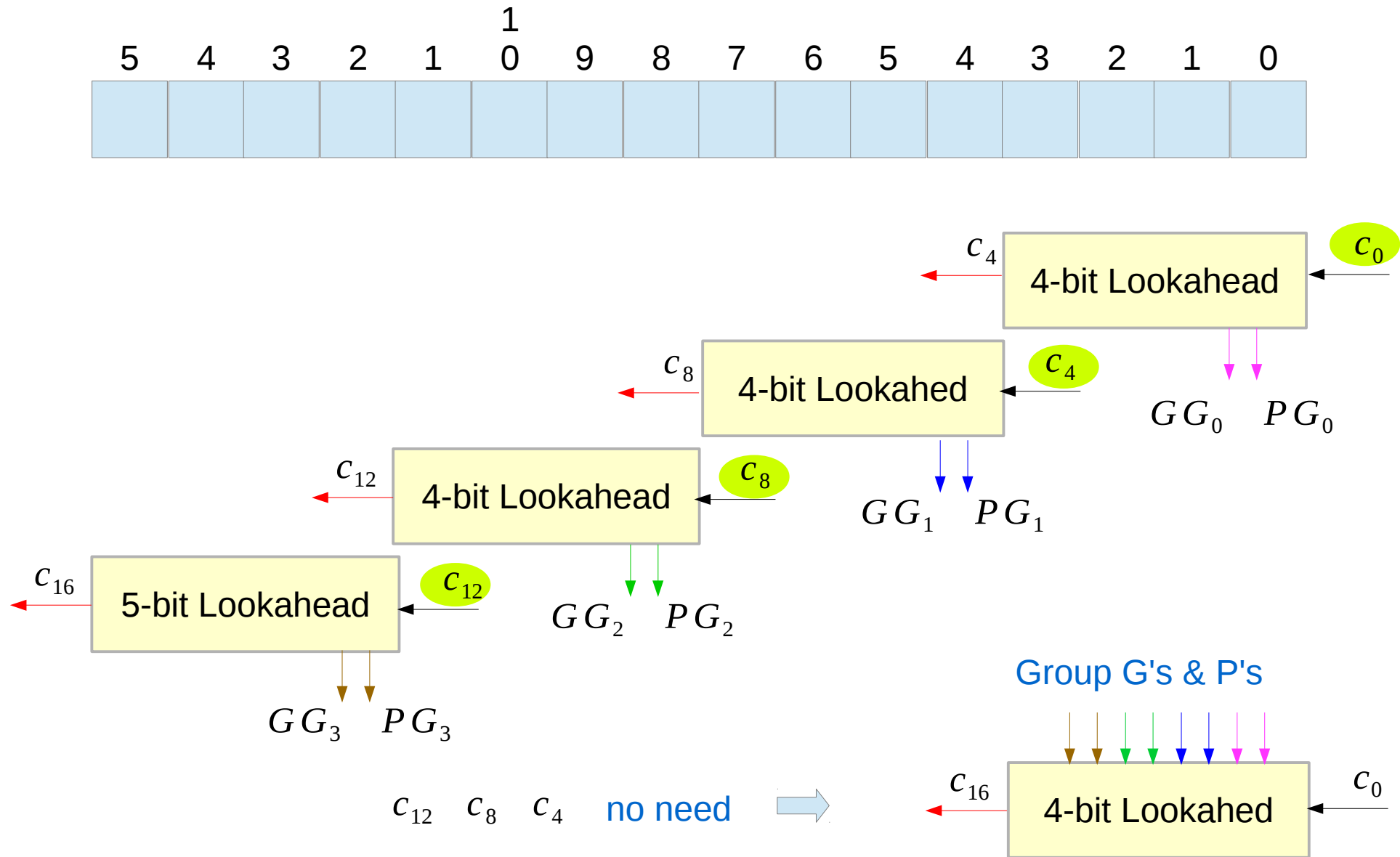
Multi-level Carry Lookahead



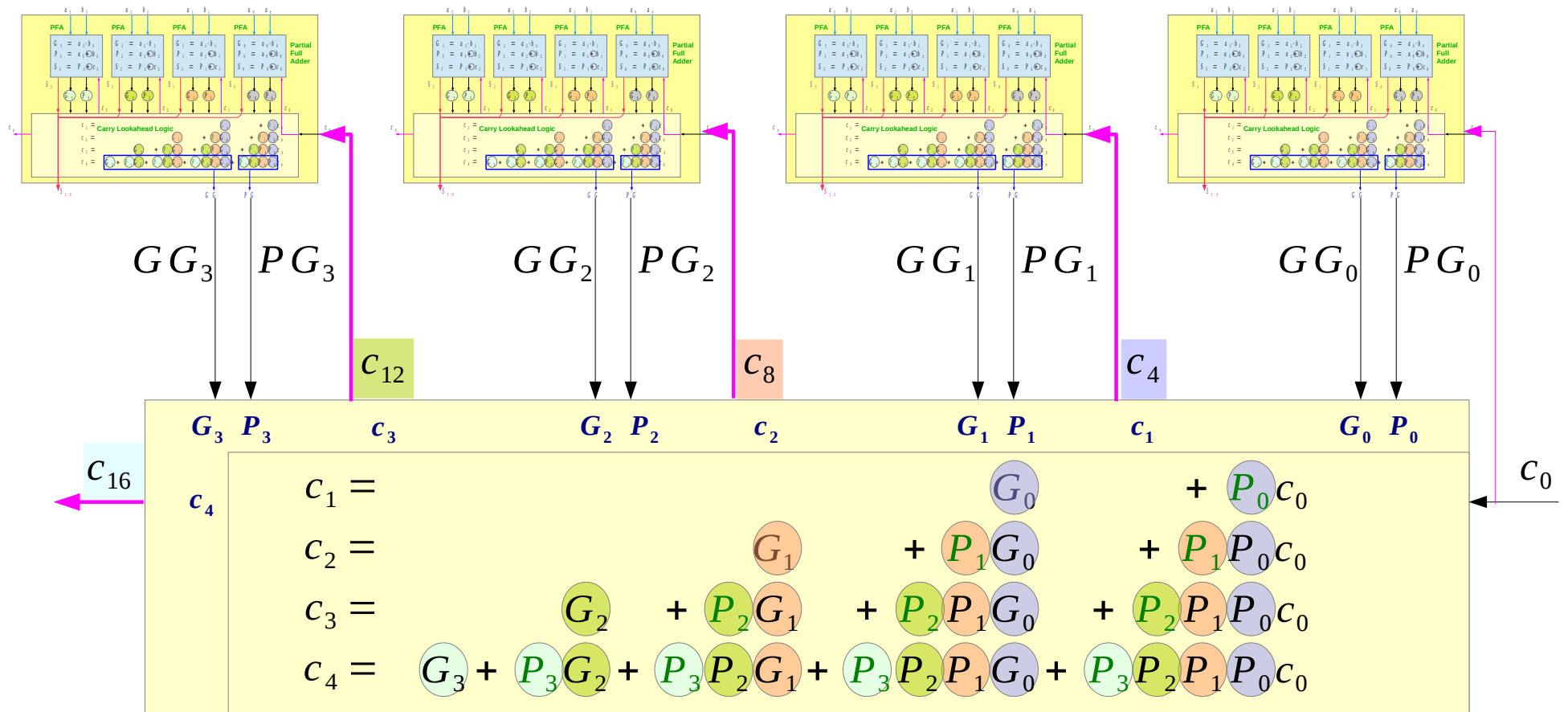
Overlapping
Contiguous



Contiguous Multi-level Carry Lookahead



Group Carry Lookahead Logic



GG and PG (1)

$$c_1 = G_0 + P_0 c_0$$

$$c_2 = G_1 + P_1 [G_0 + P_0 c_0]$$

$$c_3 = G_2 + P_2 [G_1 + P_1 [G_0 + P_0 c_0]]$$

$$c_4 = G_3 + P_3 [G_2 + P_2 [G_1 + P_1 [G_0 + P_0 c_0]]]$$

$$c_4 = G_3 + P_3 G_2 + P_3 P_2 G_1 + P_3 P_2 P_1 G_0 + P_3 P_2 P_1 P_0 c_0 = GG_0 + PG_0 c_0$$

$$c_5 = G_4 + P_4 [c_4]$$

$$c_6 = G_5 + P_5 [G_4 + P_4 [c_4]]$$

$$c_7 = G_6 + P_6 [G_5 + P_5 [G_4 + P_4 [c_4]]]$$

$$c_8 = G_7 + P_7 [G_6 + P_6 [G_5 + P_5 [G_4 + P_4 [c_4]]]]$$

$$c_8 = G_7 + P_7 G_6 + P_7 P_6 G_5 + P_7 P_6 P_5 G_4 + P_7 P_6 P_5 P_4 c_4 = GG_1 + PG_1 c_4$$

GG and PG (2)

$$c_9 = G_8 + P_8 [c_8]$$

$$c_{10} = G_9 + P_9 [G_8 + P_8 [c_8]]$$

$$c_{11} = G_{10} + P_{10} [G_9 + P_9 [G_8 + P_8 [c_8]]]$$

$$c_{12} = G_{11} + P_{11} [G_{10} + P_{10} [G_9 + P_9 [G_8 + P_8 [c_8]]]]$$

$$c_{12} = G_{11} + P_{11} G_{10} + P_{11} P_{10} G_9 + P_{11} P_{10} P_9 G_8 + P_{11} P_{10} P_9 P_8 c_8 = GG_2 + PG_2 c_8$$

$$c_{13} = G_{12} + P_{12} [c_{12}]$$

$$c_{14} = G_{13} + P_{13} [G_{12} + P_{12} [c_{12}]]$$

$$c_{15} = G_{15} + P_{15} [G_{13} + P_{13} [G_{12} + P_{12} [c_{12}]]]$$

$$c_{16} = G_{16} + P_{16} [G_{15} + P_{15} [G_{13} + P_{13} [G_{12} + P_{12} [c_{12}]]]]$$

$$c_{16} = G_{16} + P_{16} G_{15} + P_{16} P_{15} G_{14} + P_{16} P_{15} P_{14} G_{13} + P_{16} P_{15} P_{14} P_{13} c_{12} = GG_3 + PG_3 c_{12}$$

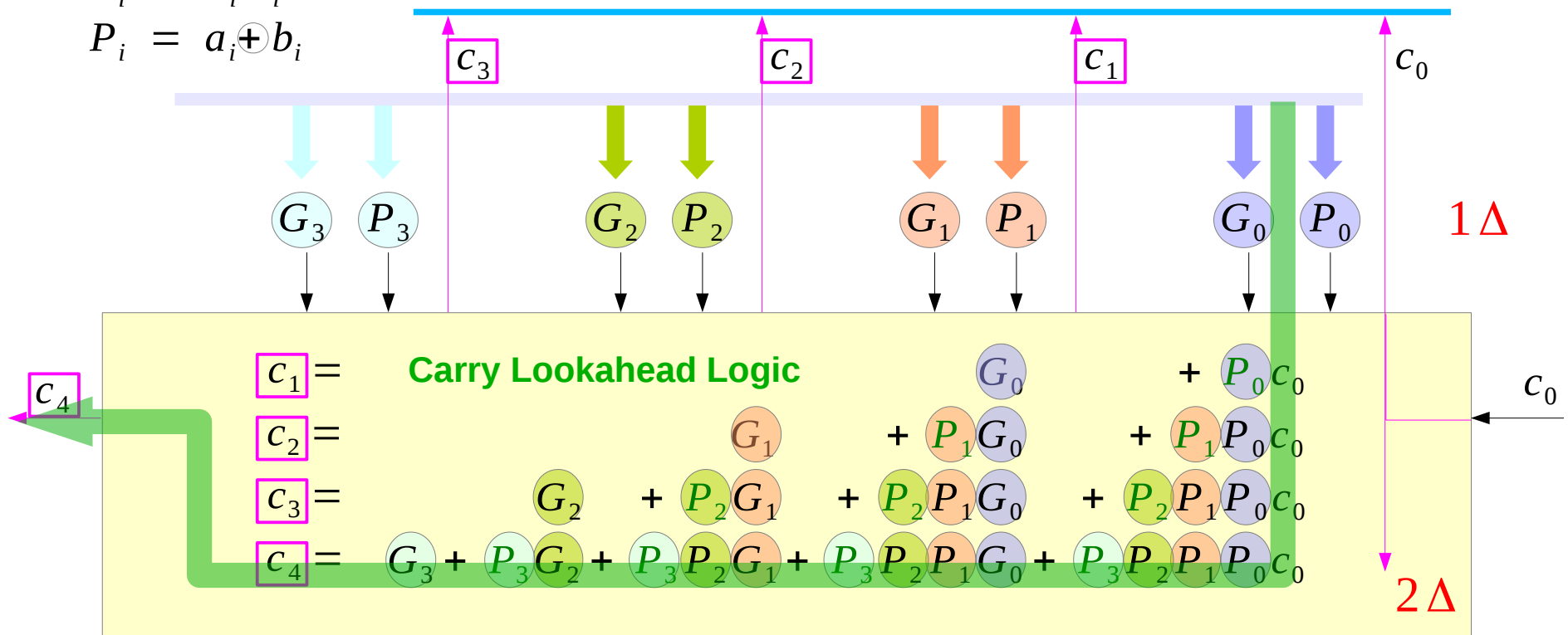
Critical Path in the Carry Lookahead Logic

All G_i 's P_i 's are computed simultaneously from a_i and b_i

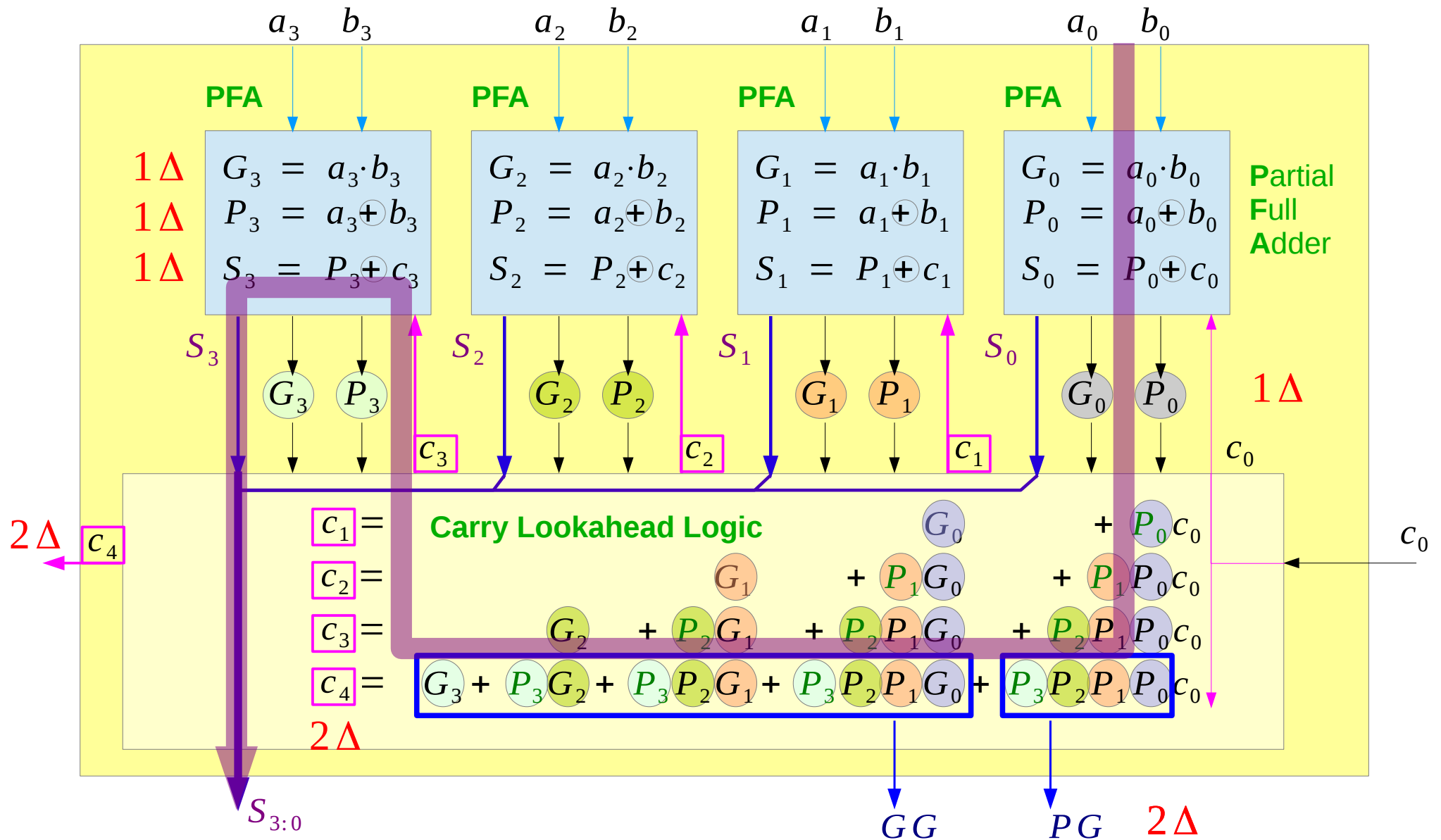
each c_i 's takes 2 gate delays

$$G_i = a_i \cdot b_i$$

$$P_i = a_i \oplus b_i$$



Critical Path in the 4-bit CLA



Critical Path in the Group Carry Lookahead Logic

