

# Gate Area

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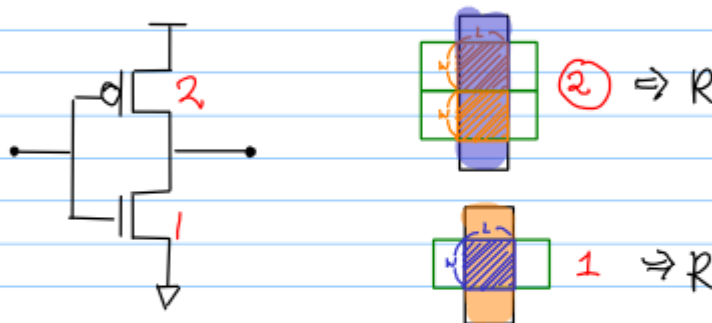
# A Unit Inverter

X1 reference gate

a symmetric inverter

$$\beta_n = \beta_p$$

$$R_n = R_p$$

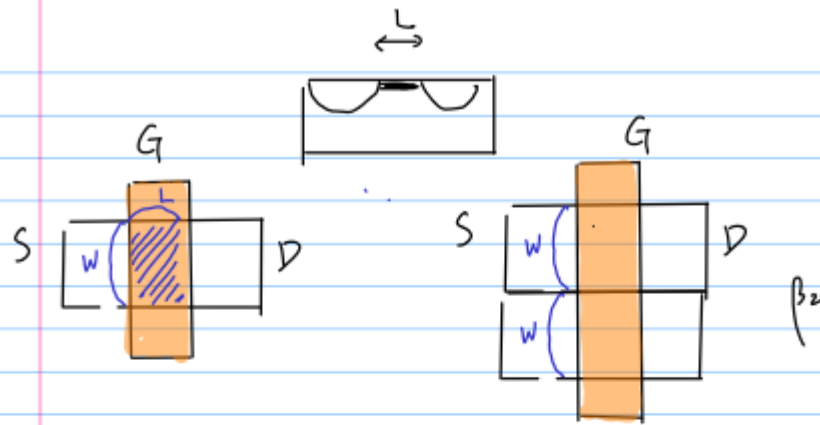


a relative aspect ratio  $r$ ,  $r$

$$\Rightarrow \left(\frac{W}{L}\right)_p = r \left(\frac{W}{L}\right)_n \quad r = 2 \sim 3$$

for a fixed  $L$ ,  $W_p = r W_n$   
↑  
consider a scale factor

# Aspect Ratio Related



$\beta_1$   
small  
conductance

<

$\beta_2$   
large  
conductance

$R_1$   
large  
resistance

>

$R_2$   
small  
resistance

$(\frac{w}{L})$

small  
size

<

$2(\frac{w}{L})$

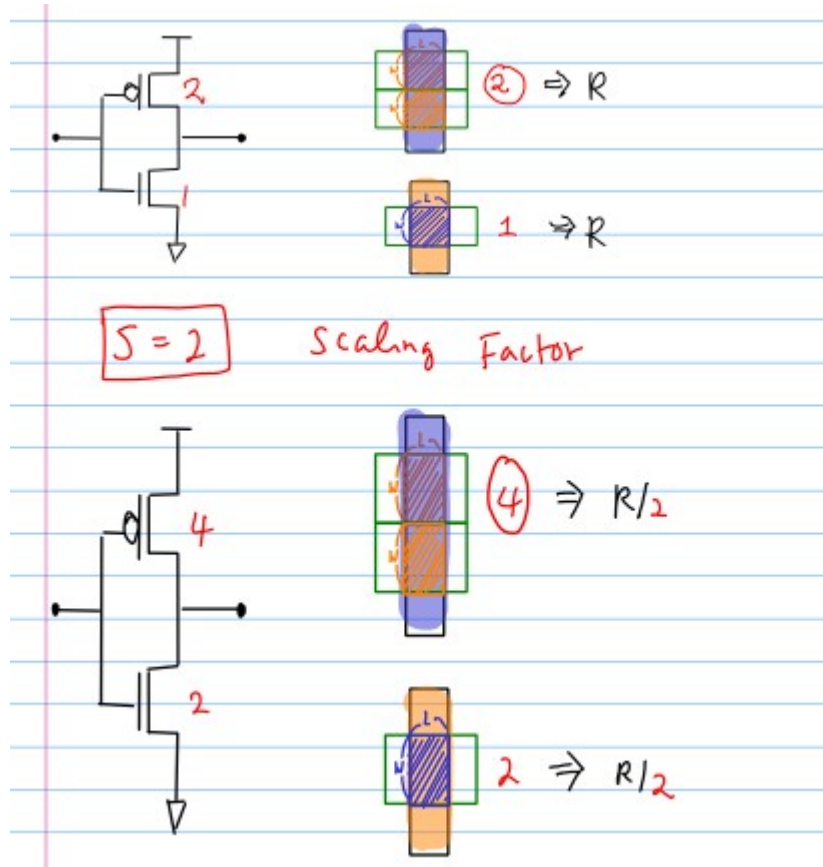
large  
size

$I_{ds1}$   
small  
driving strength

<

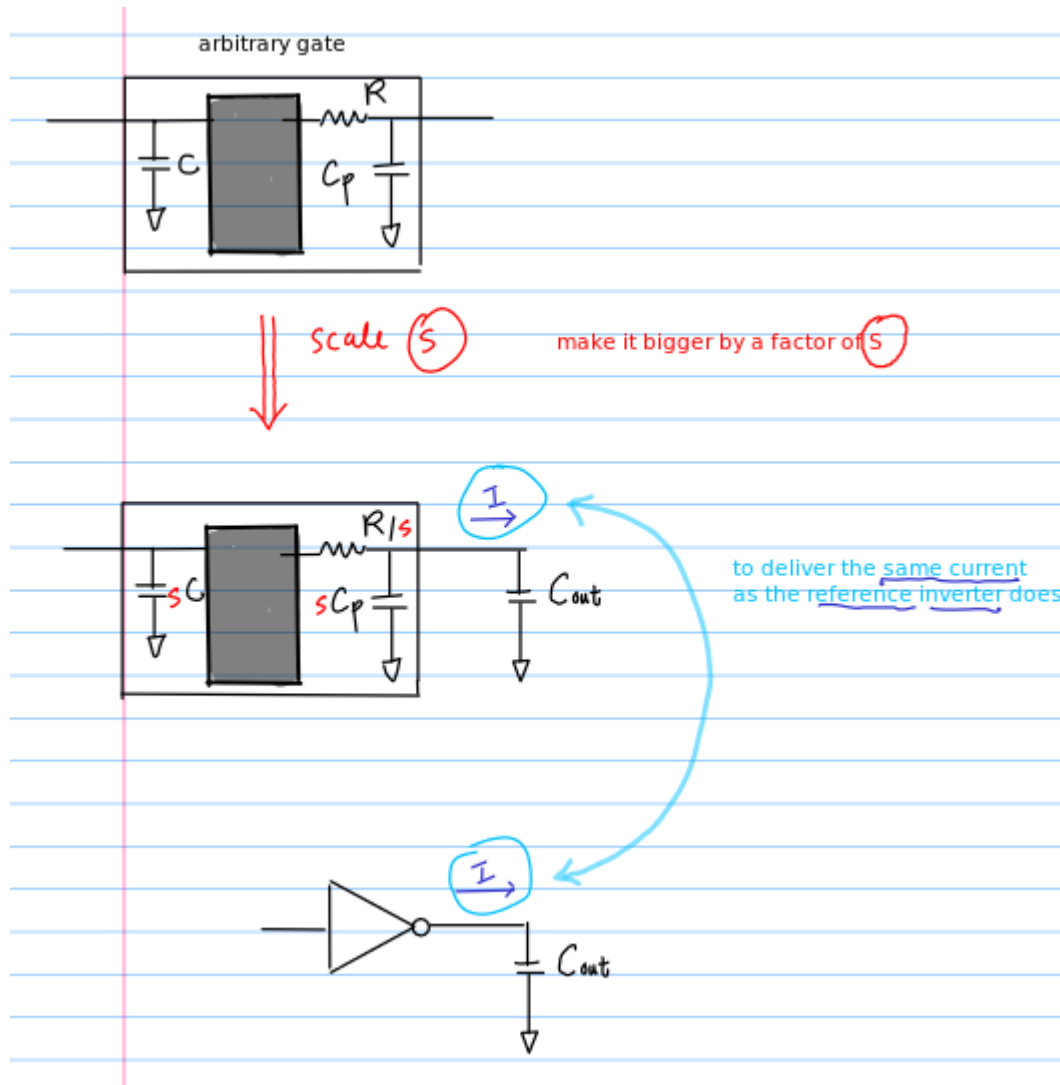
$I_{ds2}$   
large  
driving strength

# Scaling Factor



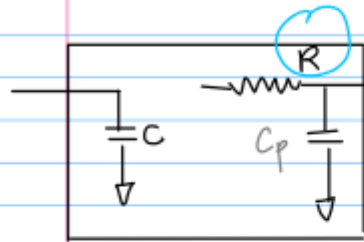
After scaling by $S$		
	$R$	$\rightarrow \frac{R}{S}$
gate	$C$	$\rightarrow S^2 C$
parasitic	$C_p$	$\rightarrow S C_p$

# Scaling for the same output I

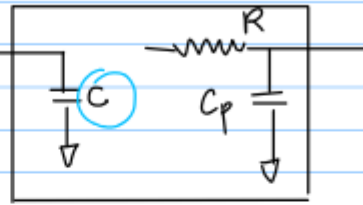


# Time Constant

arbitrary gate



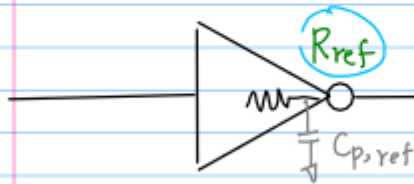
arbitrary gate



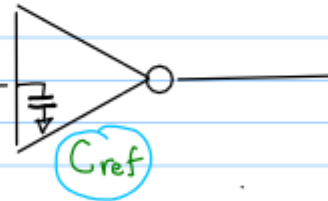
$$\tau = RC$$

time constant  
before scaling by S

ref inverter



ref inverter



$$C_{p,ref} \ll C_{ref}$$

ideal inverter :  
no parasitic delay

$$\tau_{ref} = R_{ref} C_{ref}$$

$$g \cdot h = \left( \frac{RC}{R_{ref} C_{ref}} \right) \left( \frac{C_{out}}{C_{in}} \right)$$

$$= \left( \frac{\tau}{\tau_{ref}} \right) \left( \frac{C_{out}}{C_{in}} \right)$$

# Logical Effort

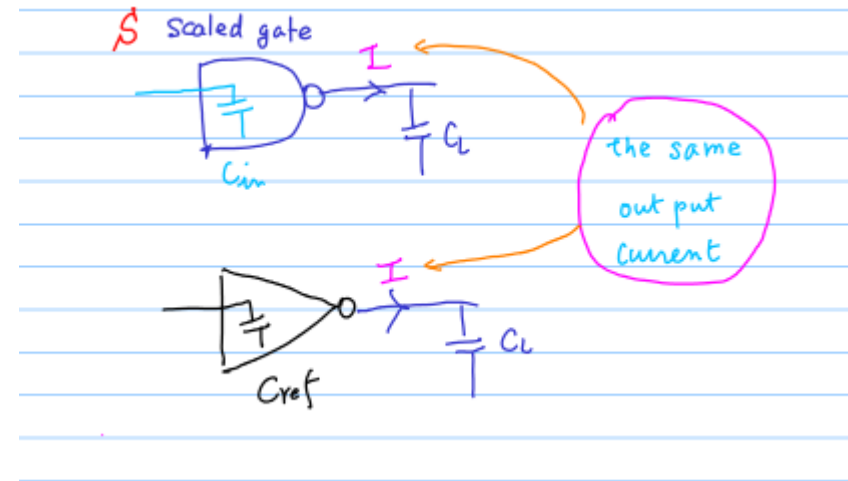
Logical effort  $g$  of a gate

the ratio of  
the input capacitance of the gate to  
the input capacitance of an inverter  
that can give the same output current

$$g = \frac{C_{in}}{C_{ref}}$$

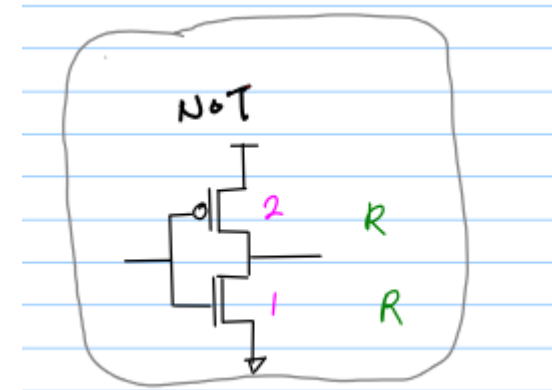
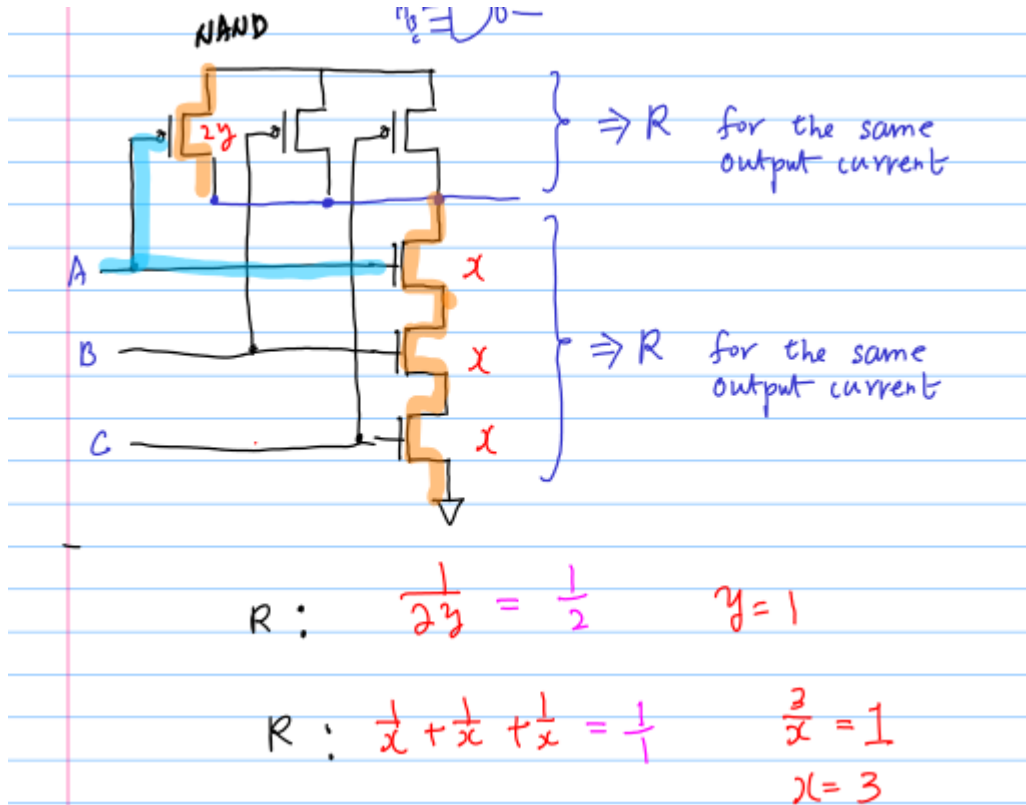
$C_{in}$  after scaling

in order to make its output current  
the same as reference gate's output current





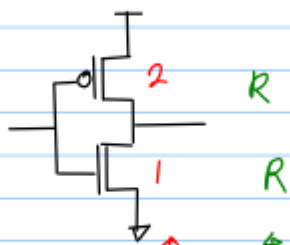
# Example



# Example

$$r = 2 \sim 3$$

NOT

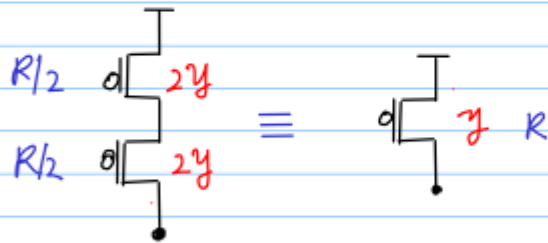
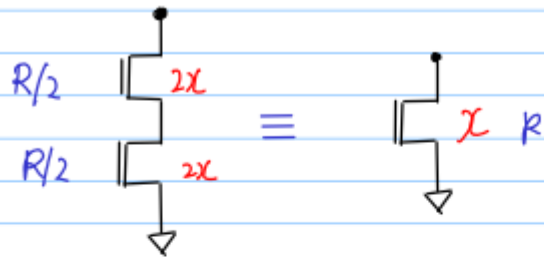


$$C_{in} = 3 = C_{ref}$$
$$g = \frac{3}{3} = 1$$

scaling  
info  
 $(\frac{W}{L})$

resistance

# Summary



$$y = 2x$$

# Parasitic Delay

parasitic delay (p)

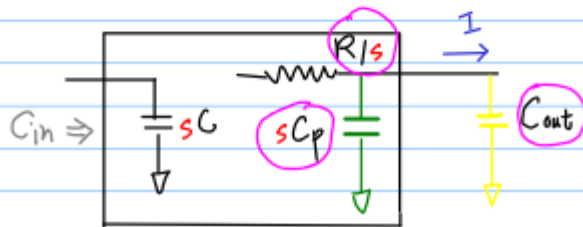
- delay due to internal parasitic capacitance

$sC_p$

- excluding external load cap

$C_{out}$

- count only diffusion capacitance of the output

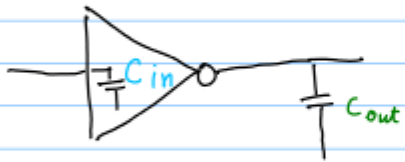


# Electrical Effort

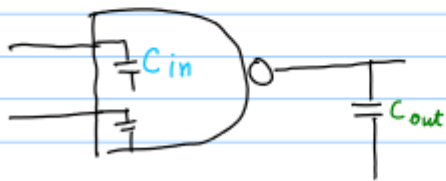
Electrical Effort : the capacitance ratio

$$h = \frac{C_{out}}{C_{in}}$$

the ratio of the drive strength to drive  $C_{out}$   
to the drive strength to drive its own capacitance  $C_{in}$



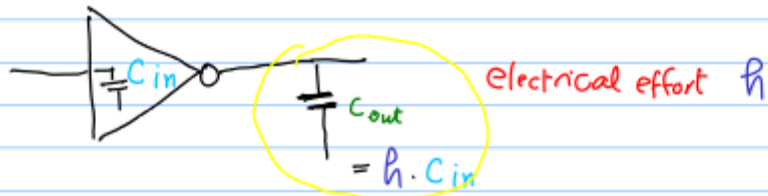
an inverter  
is driving  $C_{out}$



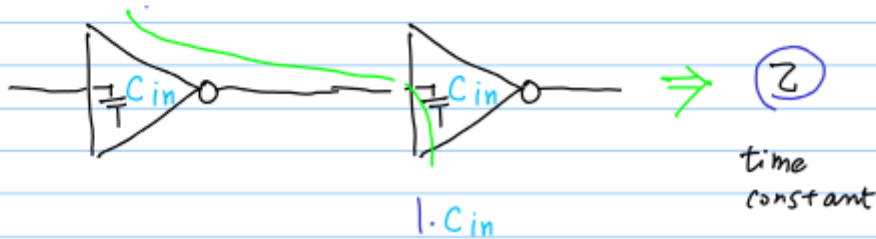
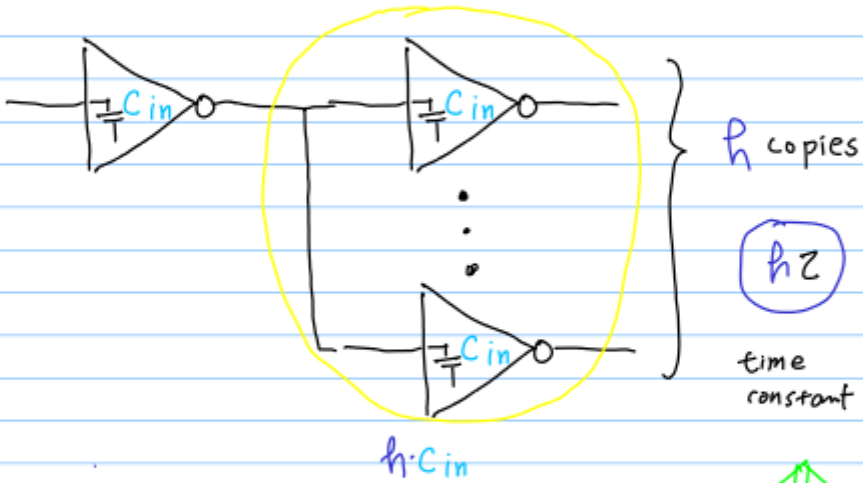
a NAND  
is driving  $C_{out}$

$C_{out}$  is  $h$  times larger than  $C_{in}$

# Electrical Effort



$h$  copies of the same gate



## References

- [1] <http://en.wikipedia.org/>
- [2] <http://www.allaboutcircuits.com/>
- [3] W. Wolf, "Modern VLSI Design : Systems on Silicon"
- [4] N. Weste, D. Harris, "CMOS VLSI Design: A Circuits and Systems Perspective"
- [5] J. P. Uyemura, "Introduction to VLSI Circuits and Systems"
- [6] [https://en.wikiversity.org/wiki/The\\_necessities\\_in\\_SOC\\_Design](https://en.wikiversity.org/wiki/The_necessities_in_SOC_Design)
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