CMOS Delay-4 (H.4)
Inverter Chain

20160927

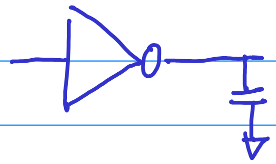
References

Some Figures from the following sites

[1] http://pages.hmc.edu/harris/cmosvlsi/4e/index.html
Weste & Harris Book Site

[2] en.wikipedia.org

Inverter Delay



$\boxed{g = 1}$ $\boxed{p = 1}$

Normalized Delay

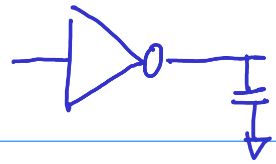
$$d = (p + g \cdot h) = (p + h)$$

$$= \frac{d_{abs}}{\tau_{ref}}$$

Absolute Delay

$$d_{abs} = \tau_{ref}(p + h)$$

Inverter Delay



$\boxed{g = 1}$

Absolute Delay

$$d_{abs} = \tau \cdot (p + h)$$

Normalized Delay

$$d = \frac{d_{abs}}{\tau} = (p + h)$$

τ reference time constant

h : Electrical Effort $\left(\frac{C_{out}}{C_{in}}\right) \longleftarrow C_{out}$

p : Parasitic Delay $\left(\frac{C_{p,ref}}{C_{ref}}\right) \longleftarrow C_{p,ref}$

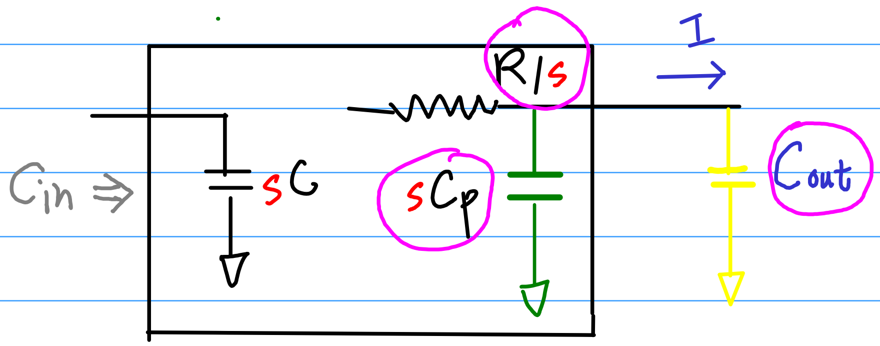
parasitic delay (p)

- delay due to internal parasitic capacitance sC_p
- excluding external load cap C_{out}
- count only diffusion capacitance of the output
- delay without output load

$$p = \frac{C_{p,ref}}{C_{ref}}$$

$C_{p,ref}$: $C_{dp} + C_{dn}$ drain parasitic cap

C_{ref}: C_{in} of the ref inverter (Symmetric Inverter)



$R \Rightarrow R_{ref}$

$$(R/s)(sC_p) = RC_p$$

$$p = \left(\frac{C_{p,ref}}{C_{ref}}\right) = \left(\frac{\text{internal diffusion cap}}{\text{gate cap of ref inv}}\right)$$

$$= \frac{\tau_{par}}{\tau_{ref}} = \left(\frac{R_{ref}\cdot C_{p,ref}}{R_{ref}\cdot C_{ref}}\right)$$

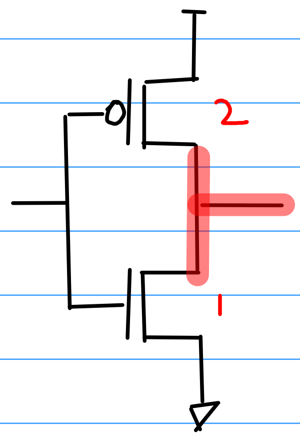
Cin of a reference inverter
(symmetric inverter)

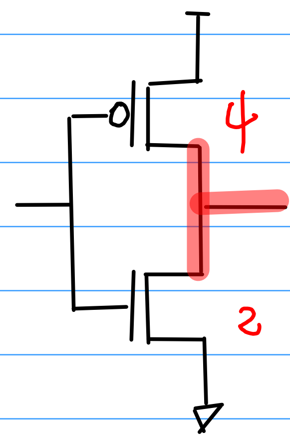
$$p = \frac{\tau_{par}}{\tau_{ref}} = \left(\frac{R_{ref} \cdot C_{p,ref}}{R_{ref} \cdot C_{ref}}\right)$$

C_{in} of a reference inverter

(Symmetric inverter)

$$p = \frac{1}{3}\left(\Sigma \text{ Output scaling factors}\right)$$



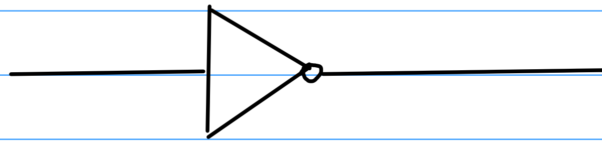


$$p = \frac{3}{3} = 1$$

$$p = \frac{6}{3} = 2.$$

reference inverter

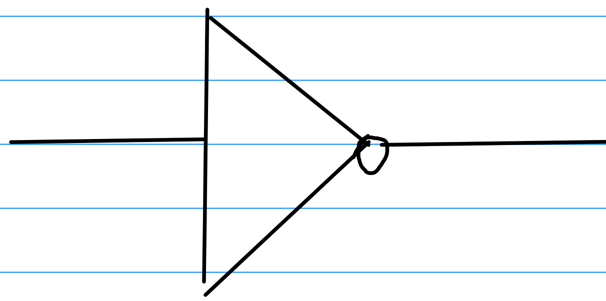
$\boxed{g = 1}$



$\boxed{p = 1}$

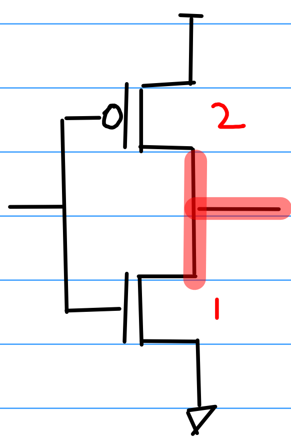
scaled inverters

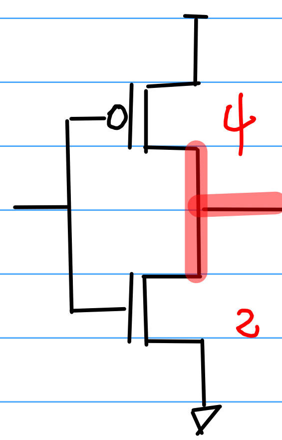
$\boxed{g = 1}$



$\cancel{\boxed{p = 1}}$

not always





$p = \frac{3}{3} = 1$

$p = \frac{6}{3} = 2.$

For the ref inverter

$$d_{abs} = Z_{ref}(h+1)$$

$$d = \frac{d_{abs}}{Z_{ref}} = (h+1)$$

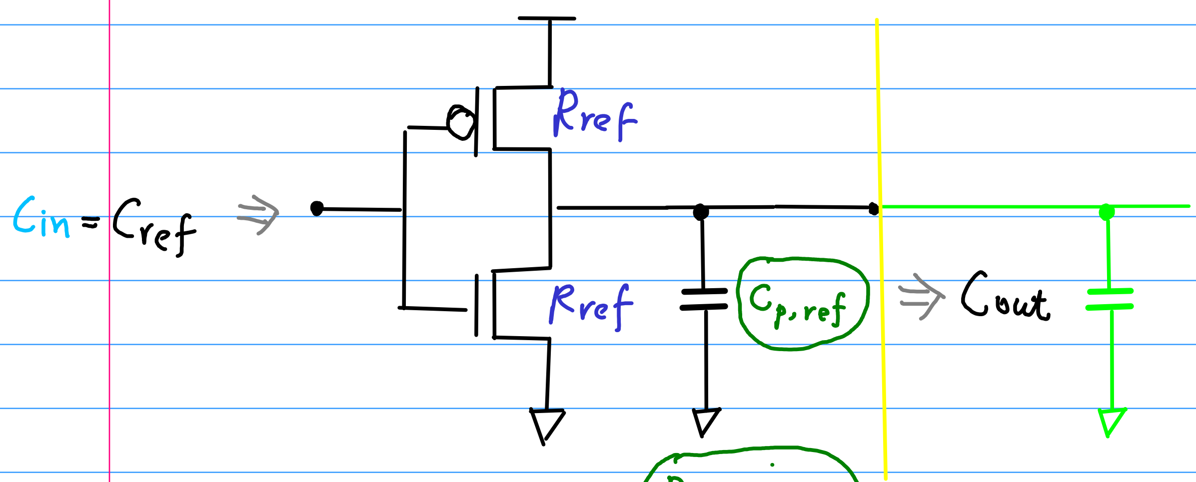
absolute delay

$$d_{abs} = k \cdot \underbrace{R_{ref}}_{R} \cdot (\underbrace{C_{p,ref} + C_{out}}_{C})$$

$R \cdot C$

$k = \ln(9) = 2.2$

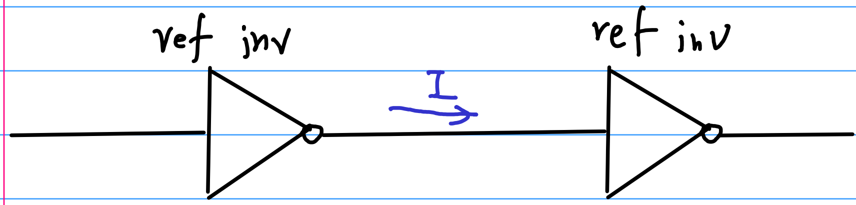
Symmetric Inverter

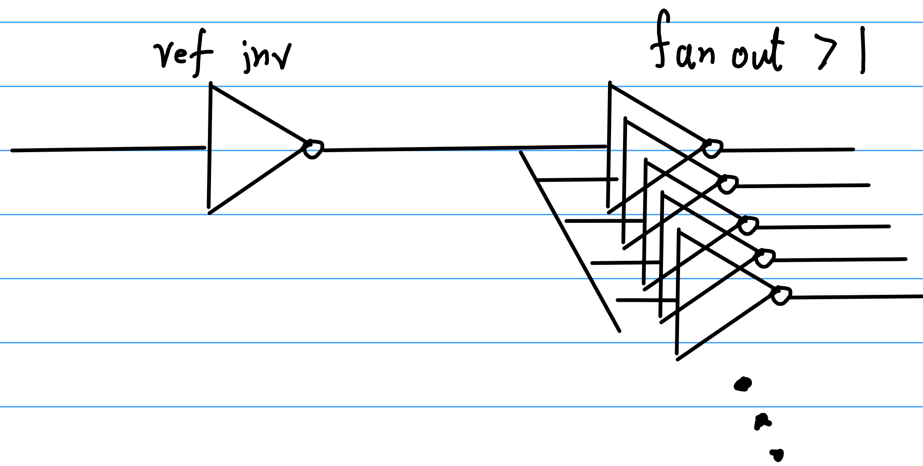


Parasitic Capacitance internal

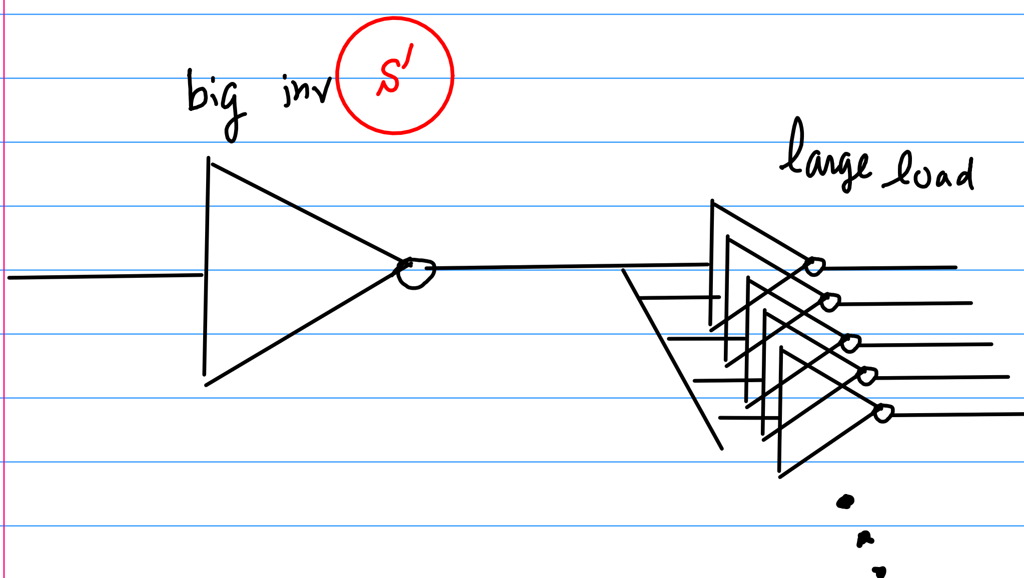
junction capacitance

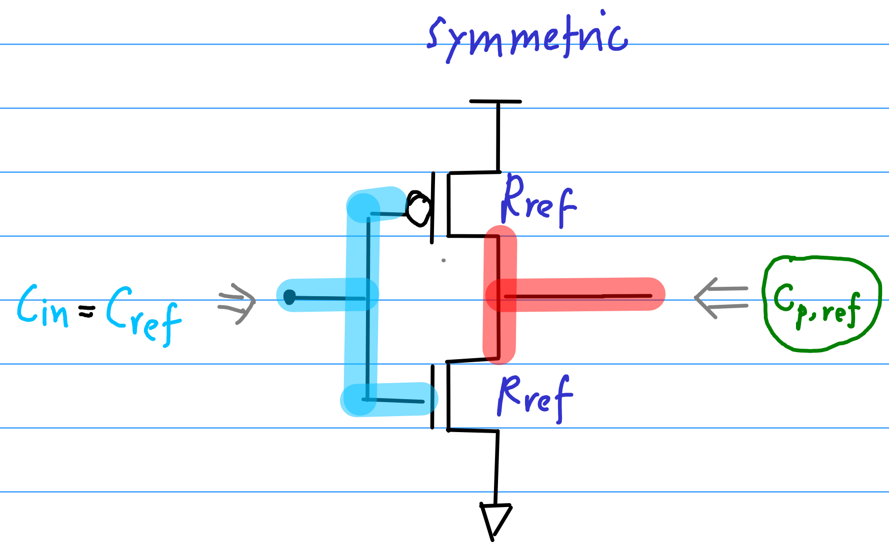
$C_{dp} + C_{dn}$





to get the same current, need bigger inverter



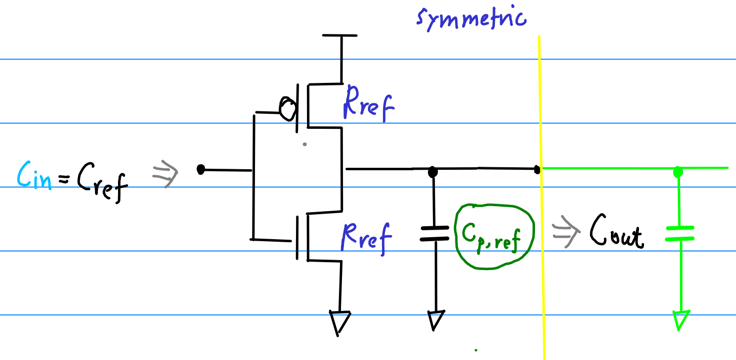


$$\boxed{\tau_{par} = k R_{ref} C_{p,ref}}$$ parasitic time const.

$$\boxed{\tau = k R_{ref} C_{ref}}$$ reference time const.

Scaling Factor $S > 1$

$$\boxed{\begin{aligned} R &= \frac{R_{ref}}{S} \\ C_p &= S \cdot C_{p,ref} \\ C_{in} &= S\, C_{ref} \end{aligned}}$$



$$d_{abs} = k\, R_{ref} \cdot (C_{p,ref} + C_{out})$$

after scaling $\Longrightarrow k \dfrac{R_{ref}}{S} (S \cdot C_{p,ref} + C_{out})$

$$= k R_{ref} C_{p,ref} + k \frac{R_{ref}}{S} C_{out}$$

$\boxed{C_{in} = C_{ref}}$

$$= k R_{ref} C_{p,ref} + k \frac{R_{ref}}{S} \left(\frac{C_{out}}{C_{ref}}\right) C_{ref}$$

$$= k R_{ref} C_{p,ref} + k R_{ref} \left(\frac{C_{out}}{C_{in}}\right) C_{ref}$$

$$= k R_{ref} C_{ref} \left(\frac{C_{p,ref}}{C_{ref}}\right) + k R_{ref} C_{ref} \left(\frac{C_{out}}{C_{in}}\right)$$

$$d_{abs} = k R_{ref} C_{ref} \left(\frac{C_{p,ref}}{C_{ref}}\right) + k R_{ref} C_{ref} \left(\frac{C_{out}}{C_{in}}\right)$$

$$= k R_{ref} C_{ref} \left[\frac{(k R_{ref})(C_{p,ref})}{(k R_{ref})(C_{ref})} + \left(\frac{C_{out}}{C_{in}}\right) \right]$$

$$= \tau \left[\left(\frac{\tau_{par}}{\tau}\right) + \left(\frac{C_{out}}{C_{in}}\right) \right]$$

$$= \tau \left[p + h \right]$$

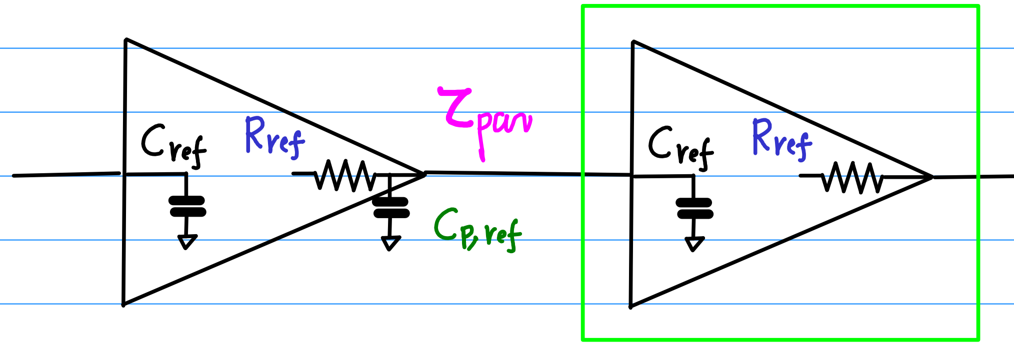
$$= \tau \cdot d$$

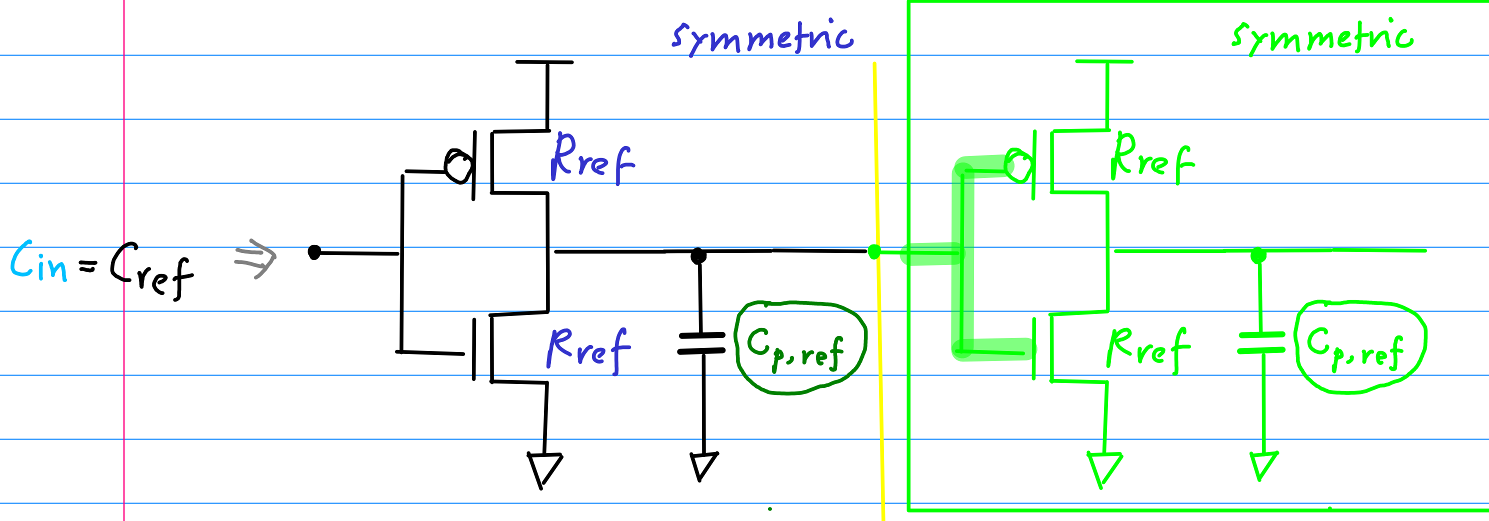
$\boxed{\tau_{par} = k R_{ref} C_{p,ref}}$ parasitic time const.

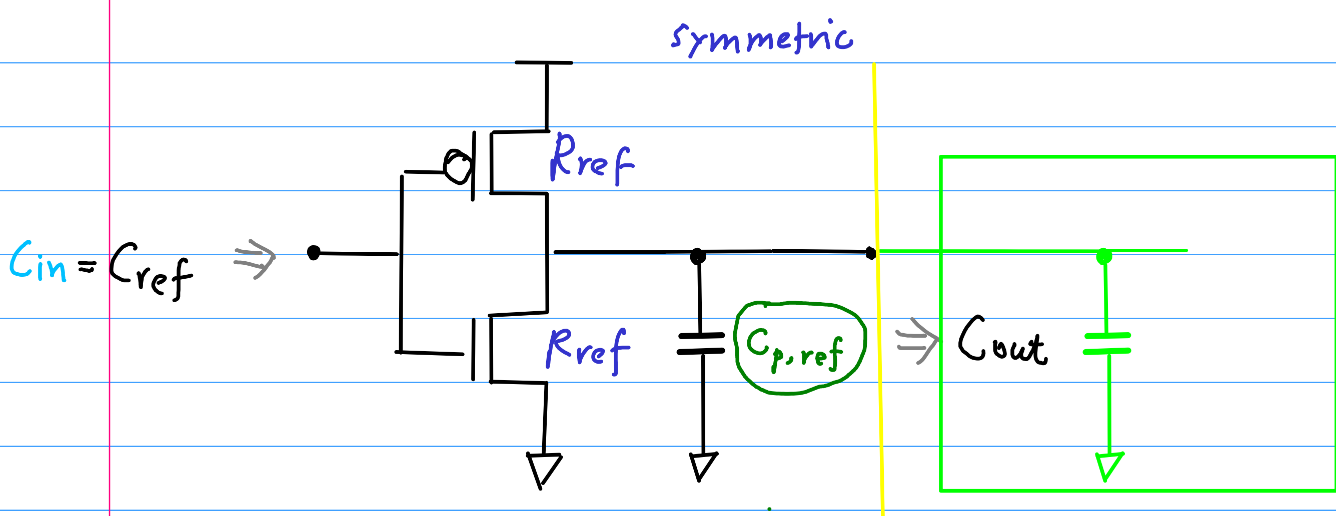
$\boxed{\tau = k R_{ref} C_{ref}}$ reference time const.

$$\tau_{par} = \tau \cdot p$$

$$d_{abs} = \tau \cdot d$$

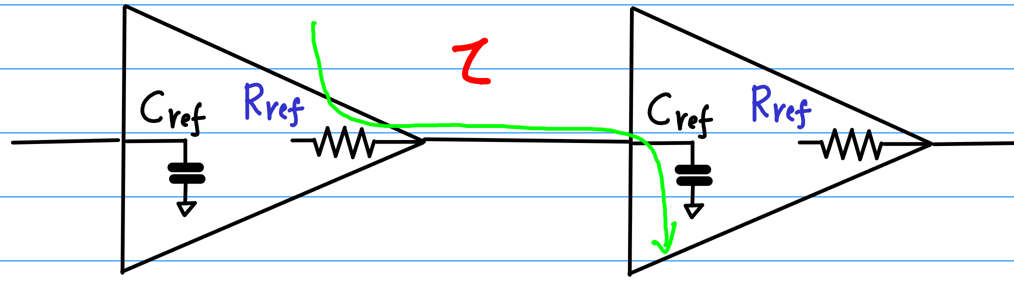

Cref
Rref
τpar
Cp,ref
Cref
Rref


symmetric
symmetric
Cin = Cref ⇒
Rref
Rref
Cp,ref
Rref
Rref
Cp,ref


symmetric
Cin = Cref ⇒
Rref
Rref
Cp,ref
⇒
Cout

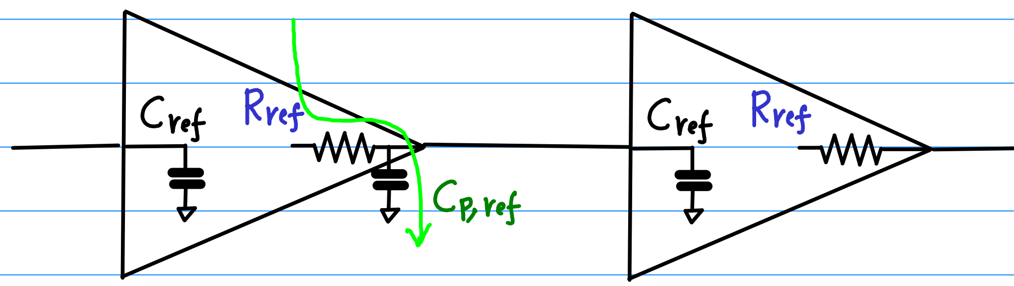
$$\boxed{\tau = k R_{ref} C_{ref}}$$

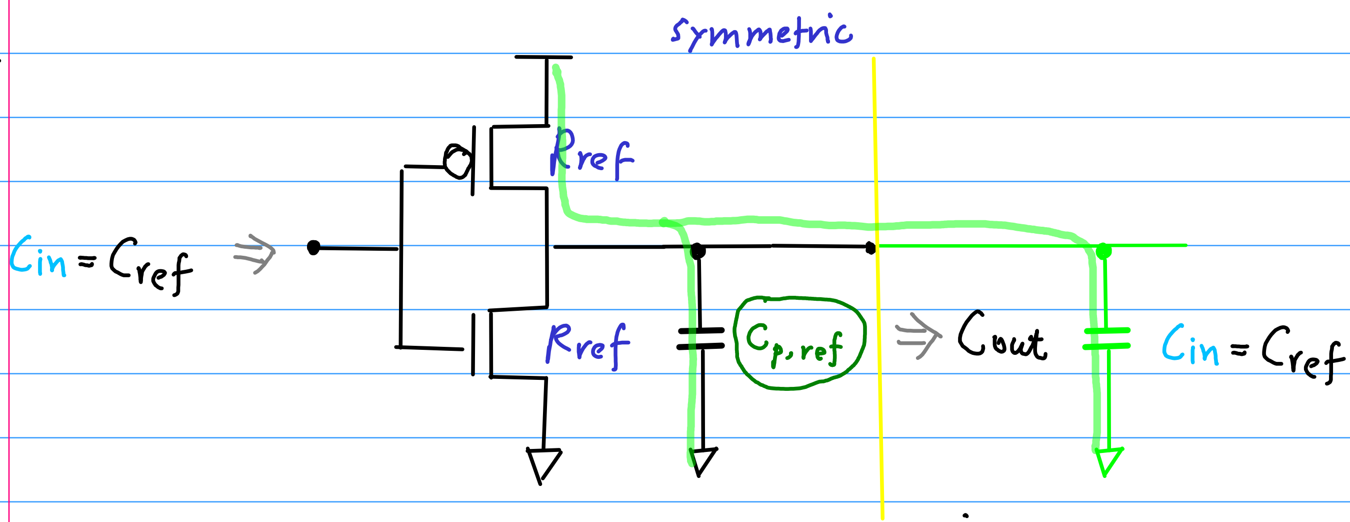
reference time const.



$$\boxed{\tau_{par} = k R_{ref} C_{p,ref}}$$

parasitic time const.





τ: reference time const. $\boxed{\tau = k R_{ref} C_{ref}}$

τ_{par}: parasitic time const. $\boxed{\tau_{par} = k R_{ref} C_{p,ref}}$

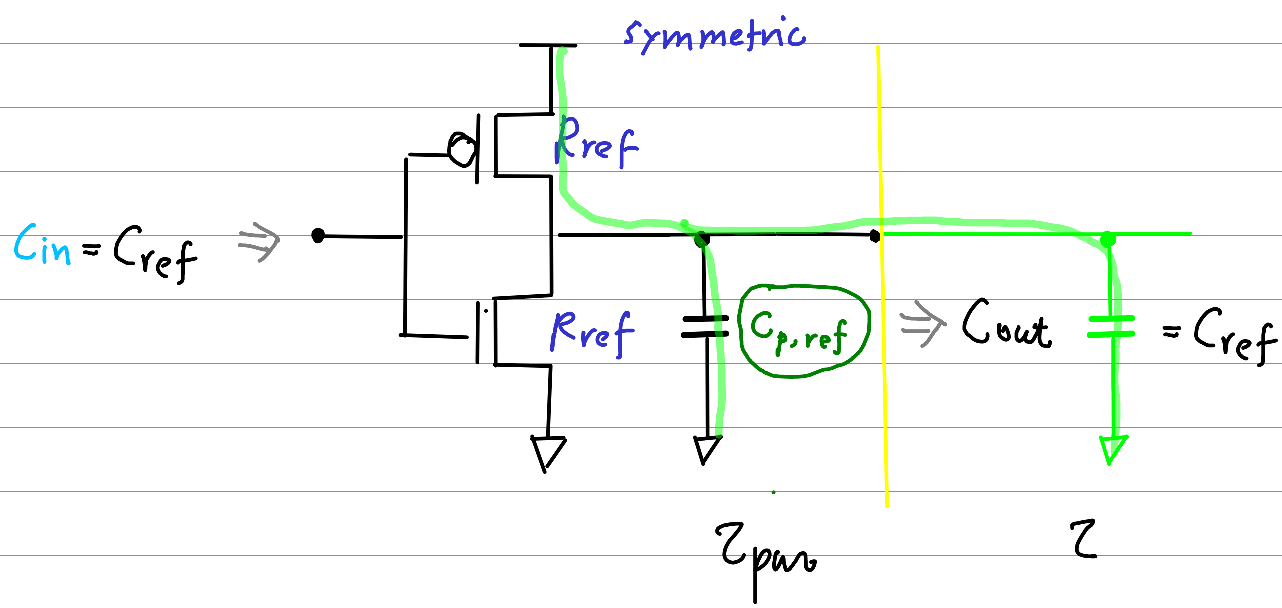
Parasitic Capacitance internal	junction capacitance $C_{dp} + C_{dn}$

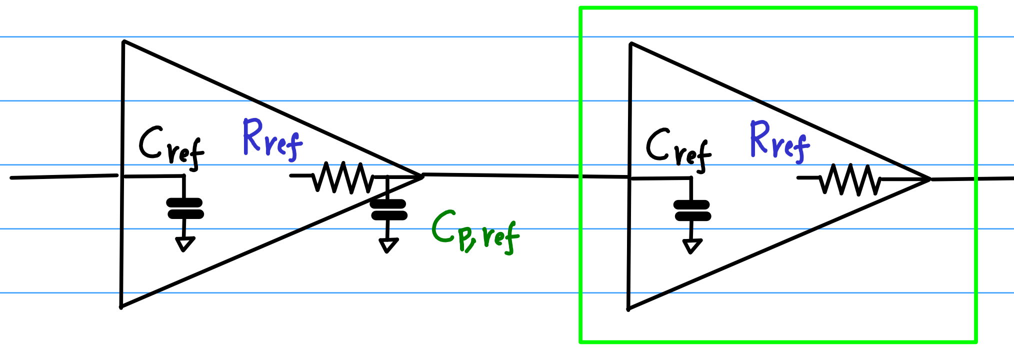
Electrical Effort

$$h = \frac{C_{out}}{C_{in}}$$

Parasitic Delay

$$p = \frac{\tau_{par}}{\tau} = \left(\frac{k R_{ref} \; C_{p,ref}}{k R_{ref} \; C_{ref}}\right) = \left(\frac{C_{p,ref}}{C_{ref}}\right)$$

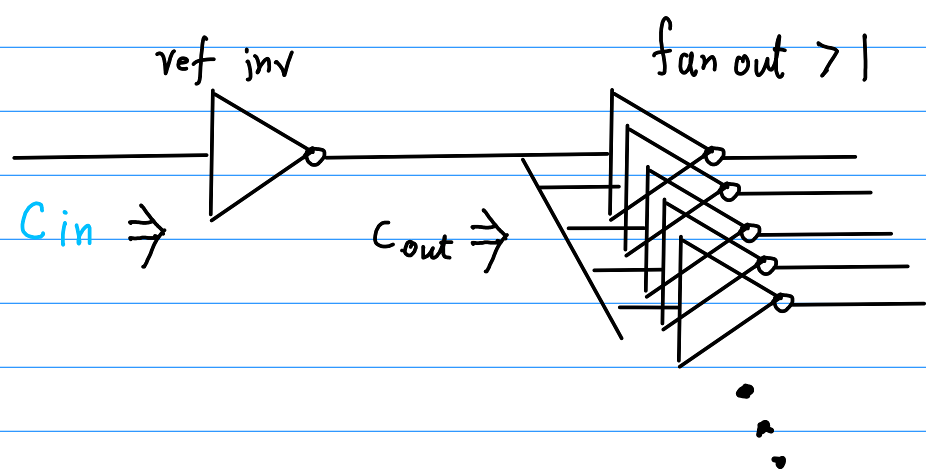




$$p = \frac{\tau_{par}}{\tau} = \left(\frac{\cancel{k}\, R_{ref}\, C_{p,ref}}{\cancel{k}\, R_{ref}\, C_{ref}}\right) = \left(\frac{C_{p,ref}}{C_{ref}}\right)$$

fixed for an inverter

$$h = \frac{C_{out}}{C_{in}}$$



β : Device Transconductance Parameter
k : Process Transconductance Parameter
μ : Electron / Hole Mobility

pMOS $\quad \beta_p = k'_p \left(\frac{W}{L}\right)_p \qquad k'_p = \mu_p C_{ox} \qquad C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

nMOS $\quad \beta_n = k'_n \left(\frac{W}{L}\right)_n \qquad k'_n = \mu_n C_{ox} \qquad C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

Saturation Current

$$I_{dp} = \frac{\beta_p}{2} \left(V_{Gsn} - |V_{Tp}|\right)^2 \qquad V_{Tp} < 0$$

$$I_{dn} = \frac{\beta_n}{2} \left(V_{Gsn} - V_{Tn}\right)^2 \qquad V_{Tn} > 0$$

$$\frac{\beta_n}{\beta_p} = \frac{k'_n \left(\frac{W}{L}\right)_n}{k'_p \left(\frac{W}{L}\right)_p}$$

$$\frac{k'_n}{k'_p} = 2 \sim 3$$

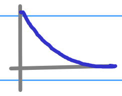
$$\frac{k'_n}{k'_p} = \frac{\mu_n}{\mu_p} = r$$

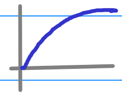
$$\left(\frac{W}{L}\right)_p = r\left(\frac{W}{L}\right)_n$$

$$r = \frac{\mu_n}{\mu_p} = \frac{k'_n}{k'_p} > 1$$

$$R_n = R_p = R = \frac{1}{\beta(V_{DD} - V_T)}$$

$$\begin{cases} V_{out}(t) = V_{DD}\left(1 - e^{-t/\tau}\right) \\ V_{out}(t) = V_{DD}\, e^{-t/\tau} \end{cases}$$





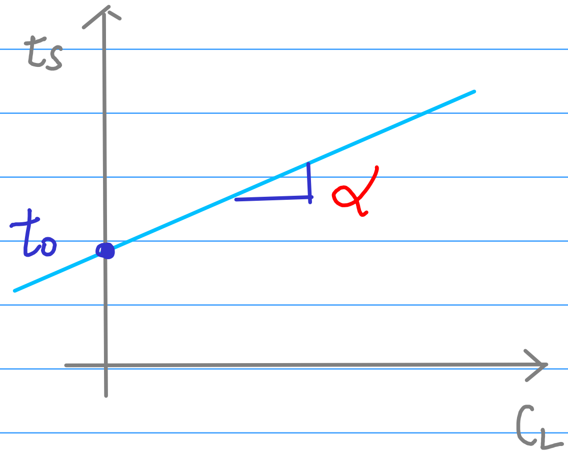
$$\tau = R\, C_{out} = R\left(C_{par} + C_L\right)$$

Generic Switching Delay

$$t_s = t_0 + \alpha C_L \Rightarrow t_s = t_r = t_f$$

Generic Switching Delay

$$t_s = t_0 + \alpha C_L$$



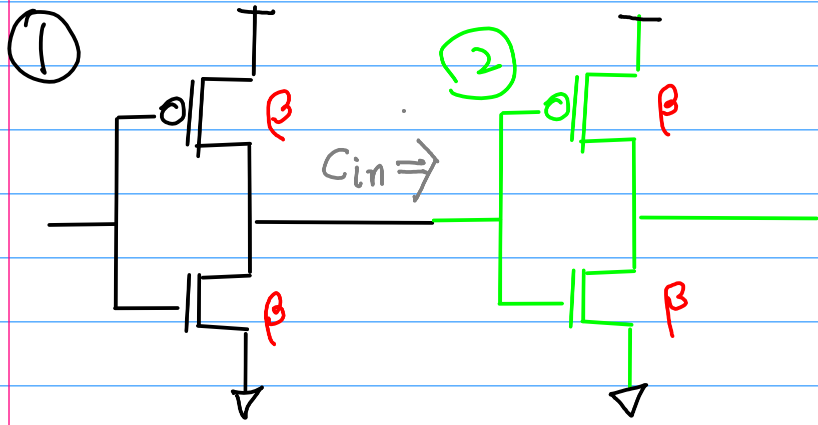
t_0 : zero delay

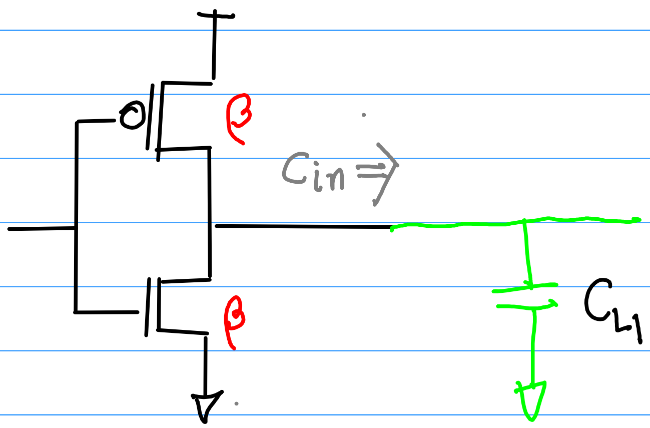
α : slope

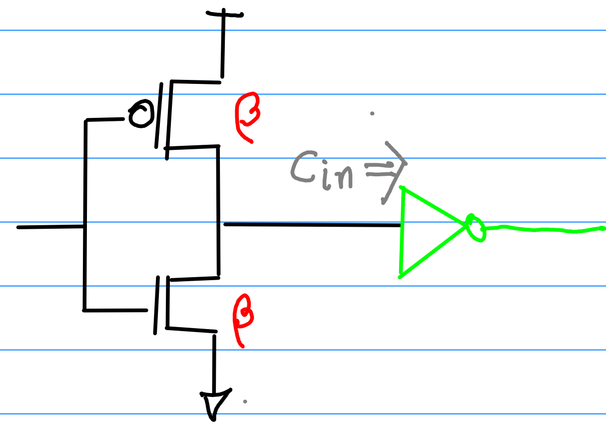
$$t \approx R\,C$$

$$\alpha \propto \frac{1}{\beta(V_{DD} - V_T)}$$

C_L







reference case $\boxed{C_{in} = C_{L1}}$

Generic Switching Delay of 1

$$t_{s1} = t_0 + \alpha C_{L1}$$

$$= t_0 + \alpha C_{in}$$

$$C_{in} = C_{Gn} + C_{Gp}$$

$$= C_{ox} (A_{Gn} + A_{Gp})$$ A: gate area

the channel length L assumed

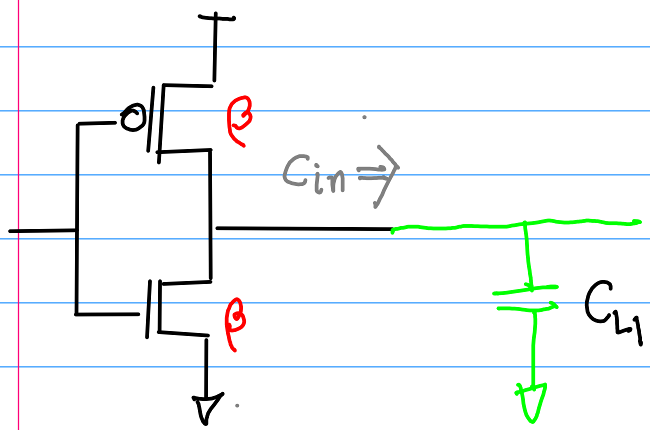
$$C_{in} = C_{ox} L (W_n + W_p)$$

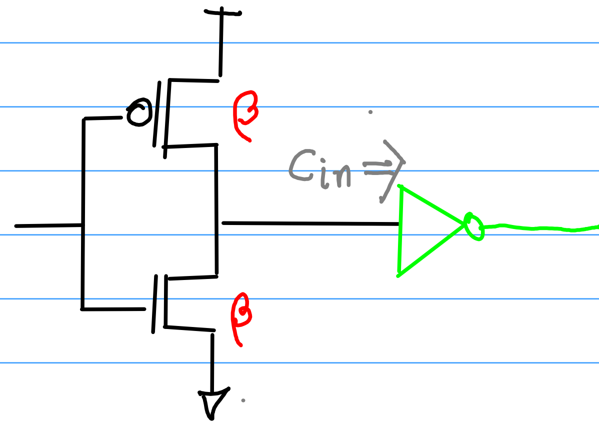
$$= C_{ox} L (W_n + r W_p)$$

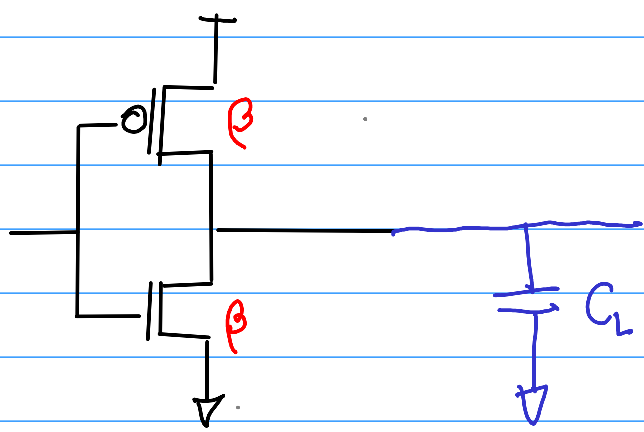
$$= C_{ox} L W_n (1 + r)$$

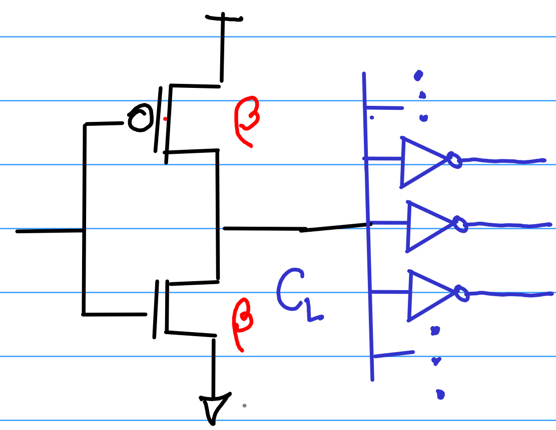
$$= C_{Gn} (1 + r)$$

When $C_L \gg C_{in}$









to minimize t_s

$\alpha \downarrow \Rightarrow R \downarrow \Rightarrow \beta \uparrow \Rightarrow$ bigger size

speed v.s. area <u>tradeoff</u>

$$\boxed{t_s = t_0 + \alpha C_L \qquad t \approx RC \qquad \alpha \propto \frac{1}{\beta(V_{DD}-V_T)} \qquad C_L}$$

to minimize t_s

$\alpha \downarrow \Rightarrow R \downarrow \Rightarrow \beta \uparrow \Rightarrow$ bigger size

speed v.s. area tradeoff

Scaling Factor S

$$\beta' = S\beta$$

$$R' = \frac{R}{S}$$

$$\alpha' = \frac{\alpha}{S}$$

$$t_s = t_0 + \overset{R}{\frac{\alpha}{S}} \overset{C}{C_L}$$

Compensation Factor $\frac{1}{S}$

enables a NOT gate drive larger values of C_L

If $C_L = S\, C_{in}$ (increased by the scaling factor S)

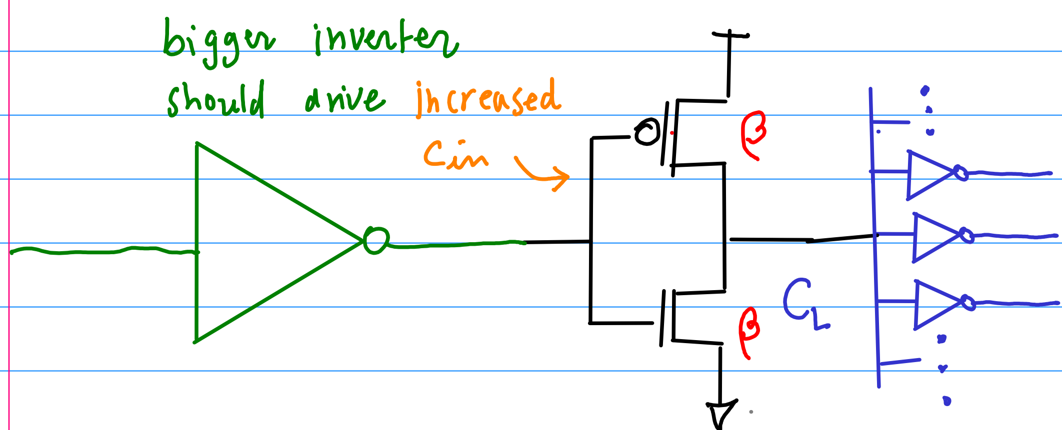
then the switching time is the same

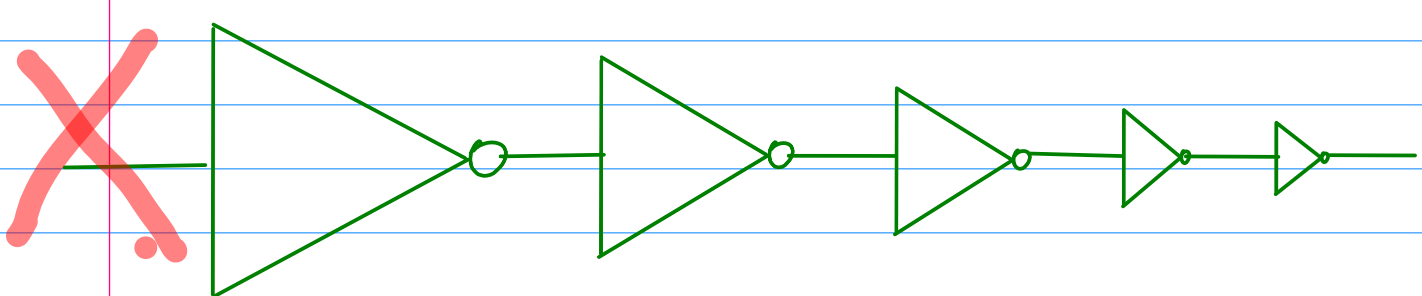
Scaling Factor S

$$\boxed{\begin{aligned} \beta' &= S\,\beta \\ R' &= \frac{R}{S} \\ \alpha' &= \frac{\alpha}{S} \end{aligned}} \Longrightarrow \boxed{\begin{aligned} W_n' &= S\,W_n \\ C_{in}' &= S\,C_{in} \end{aligned}}$$

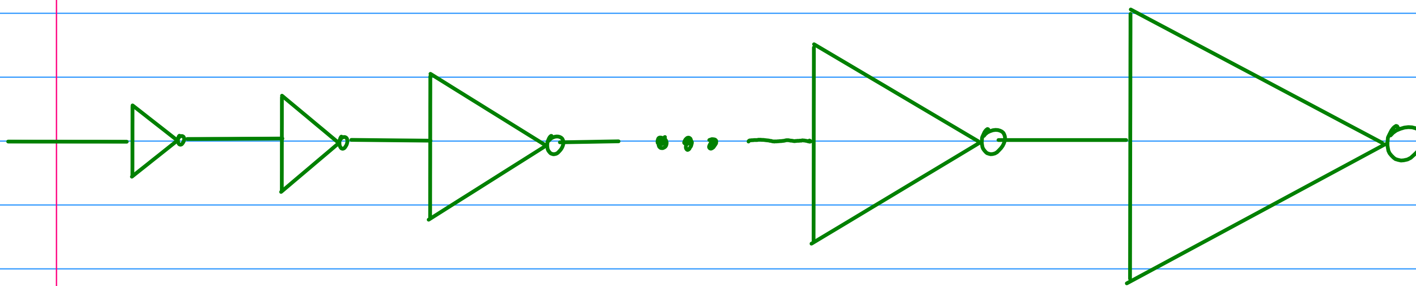
Cause problem to the driver.

$$t_s = t_0 + \overset{R}{\frac{\alpha}{S}}\;\overset{C}{C_L}$$





Delay Minimization in an inverter cascade



$\beta_1 < \beta_2 < \beta_3 < \dots < \beta_{N-1} < \beta_N$

$\beta_2 = S\beta_1$

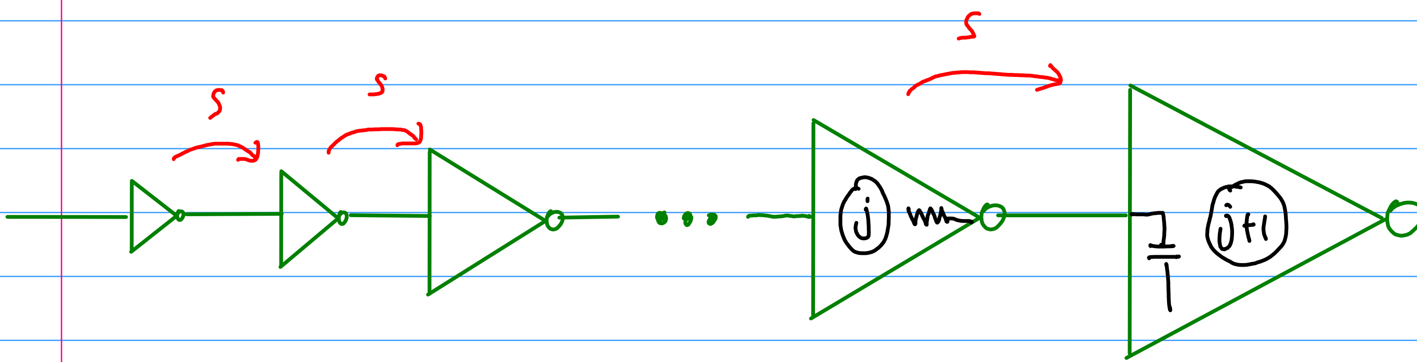
$\beta_3 = S\beta_2 = S^2\beta_1$

$\beta_4 = S\beta_3 = S^3\beta_1$

$\beta_j = S\beta_{j-1} = S^{j-1}\beta_1$

$$\boxed{\beta_j = S^{j-1}\beta_1}$$

$$\boxed{\begin{aligned} C_j &= S^{j-1} C_1 \\ R_j &= \frac{R_1}{S^{j-1}} \end{aligned}}$$



$$\tau_j = R_j C_{j+1}$$

N-stage inverter chain

$$\tau_d = \tau_1 + \tau_2 + \cdots + \tau_N$$

$$= R_1 C_2 + R_2 C_3 + \cdots + R_N C_L \qquad (C_{N+1} = C_L)$$

$$= R_1 S C_1 + \frac{R_1}{S} S^2 C_1 + \frac{R_1}{S^2} S^3 C_1 + \cdots + \frac{R_1}{S^{N-1}} S^N C_1$$

$$= S R_1 C_1 + S R_1 C_1 + S R_1 C_1 + \cdots + S R_1 C_1$$

$$= N S R_1 C_1$$

$$= N S \tau_r$$

equalize the signal delay through each stage

$$C_L = S^N C_1$$

$$\ln(S^N) = \ln\left(\frac{C_L}{C_1}\right) = N \ln(S)$$

$$\boxed{N = \frac{\ln\left(\frac{C_L}{C_1}\right)}{\ln(S)}}$$

$$\boxed{z_d = N S z_r = z_r \ln\left(\frac{C_L}{C_1}\right) \left(\frac{S}{\ln S}\right)}$$

$$\frac{\partial z_d}{\partial S} = \frac{\partial}{\partial S}\left[\frac{S}{\ln(S)}\right] = 0$$

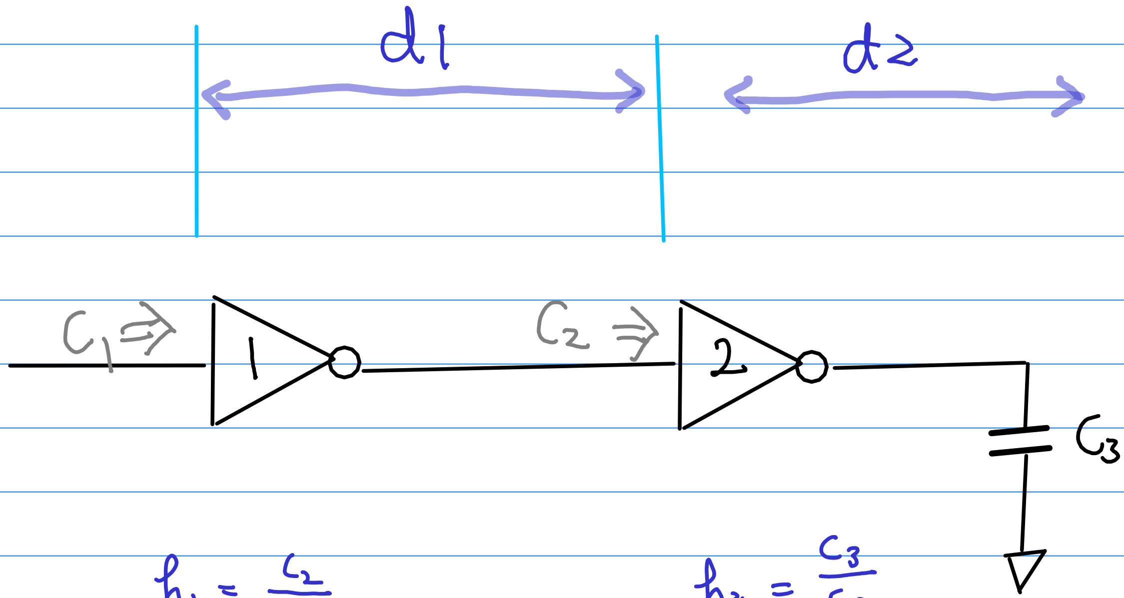
$$\ln(S) = 1 \qquad \left(\frac{\ln(S) - S \cdot \frac{1}{S}}{(\ln S)^2} = 0\right)$$

$$S = e \Rightarrow \ln(S) = 1$$

$$\boxed{N = \ln\left(\frac{C_L}{C_1}\right)}$$

$$\boxed{z_d = e \ln\left(\frac{C_L}{C_1}\right) z_r}$$

* Example



Electrical Effort

$h_1 = \frac{C_2}{C_1}$ $\qquad$ $h_2 = \frac{C_3}{C_2}$

normalized path delay $D = \Sigma$ individual delays

$= d_1 + d_2$

$= (h_1 + p_1) + (h_2 + p_2)$

$= \left(\frac{C_2}{C_1} + p_1\right) + \left(\frac{C_3}{C_2} + p_2\right)$

Path Electrical Effort

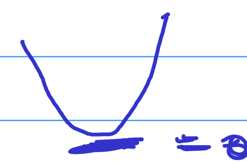
$$H = \frac{C_{last}}{C_{first}} = \frac{C_3}{C_1} = \left(\frac{C_2}{C_1}\right)\cdot\left(\frac{C_3}{C_2}\right) = h_1 h_2$$

$$h_2 = \frac{H}{h_1}$$

Path Delay $D = (h_1 + p_1) + \left(\frac{H}{h_1} + p_2\right)$

Minimize path delay $D(h_1, h_2)$

$$\Rightarrow \frac{\partial D}{\partial h_1} = \frac{\partial}{\partial h_1}\left[(h_1+p_1)+\left(\frac{H}{h_1}+p_2\right)\right] = 0$$



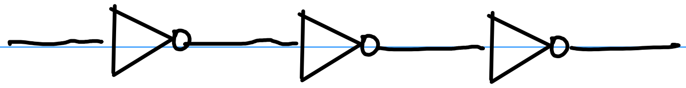
$$= 1 - \frac{H}{h_1^2} = 0$$

$$\frac{1}{h_1^2}\left(h_1^2 - h_1 h_2\right) = \frac{1}{h_1}\left(h_1 - h_2\right) = 0$$

When $\boxed{h_1 = h_2}$, $D(h_1, h_2)$ has a minimum.

minimum delay by equalizing the delay through each stage

$$\boxed{d_1 = d_2}$$



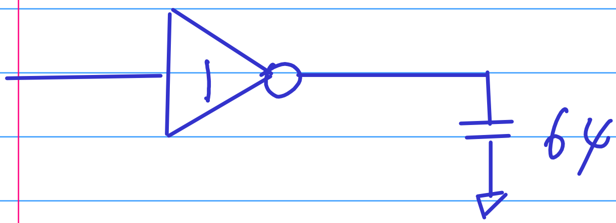
Path Delay $D = (h_1 + p_1) + (h_2 + p_2) + (h_3 + p_3)$

$$\frac{h_1 + h_2 + h_3}{3} \geq \sqrt[3]{h_1 h_2 h_3}$$

$$h_1 + h_2 + h_3 \geq 3 \sqrt[3]{h_1 \cdot h_2 \cdot h_3} = 3 H^{\frac{1}{3}}$$

minimum when $h = h_1 = h_2 = h_3$

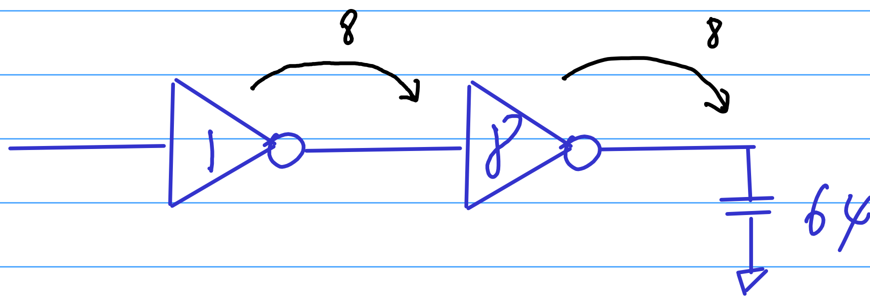
arithmetic average $\geq$ geometric average



$N=1$
$f=64$

$$D = (gh + p) = (1 \cdot 64 + 1) = 65$$

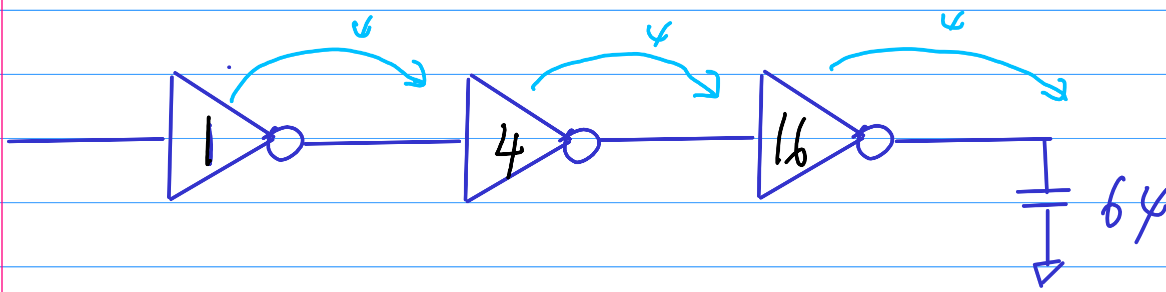
$S=8$



$N=2$
$f=8$

$$D = (1 \cdot 8 + 1) + (1 \cdot 8 + 1) = 18$$

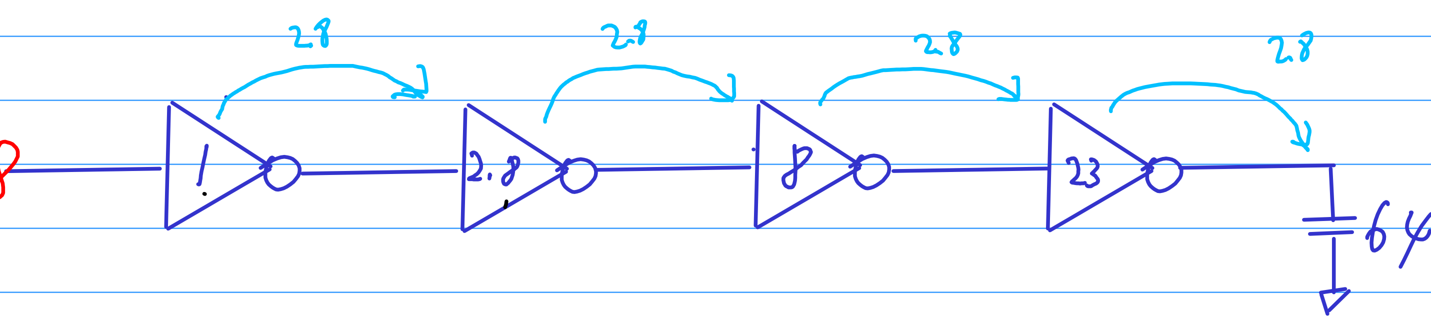
$S=4$



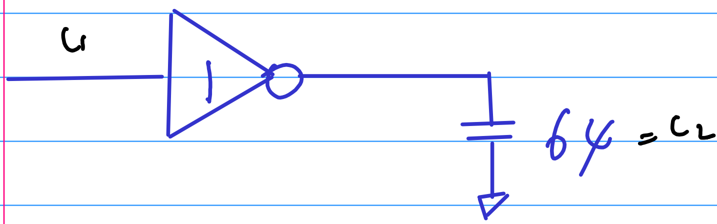
$N=3$
$f=4$

$$D = (1 \cdot 4 + 1) + (1 \cdot 4 + 1) + (1 \cdot 4 + 1) = 15$$

$S=2.8$



$$D = (1 \cdot 2.8 + 1) + (1 \cdot 2.8 + 1) + (1 \cdot 2.8 + 1) + (1 \cdot 2.8 +) = 15.2$$



$$\boxed{N = \ln\left(\frac{C_L}{C_1}\right)} = \ln(64) = 4.15 \Rightarrow N = 4$$

$$\boxed{\tau_d = e \ln\left(\frac{C_L}{C_1}\right) \tau_r} = e \ln(64)\, \tau_r \qquad \tau_r\,?$$

$$S = \left(\frac{C_L}{C_1}\right)^{1/N} = \sqrt[4]{64} = \underline{2.8}$$

Ring Oscillators

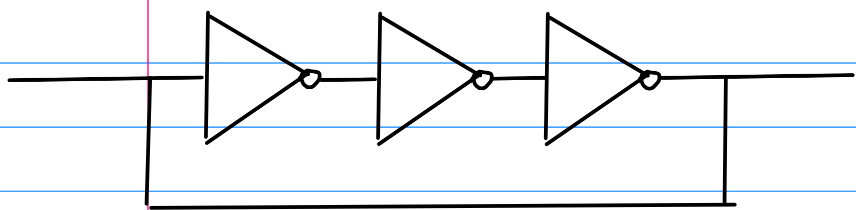
a uniform way of measuring $t_p = \frac{t_{pr} + t_{pf}}{2}$

ring oscillator

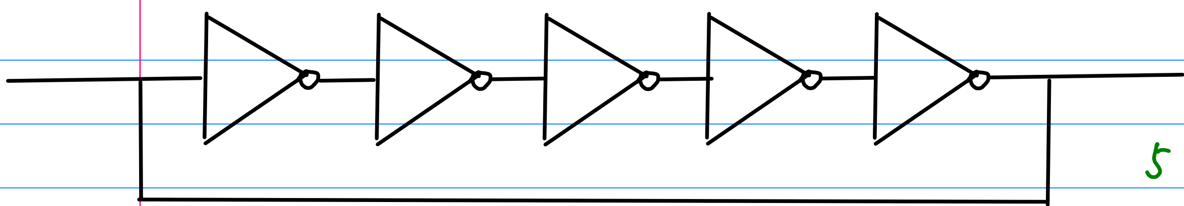
odd number of inverters

connected in circular chain

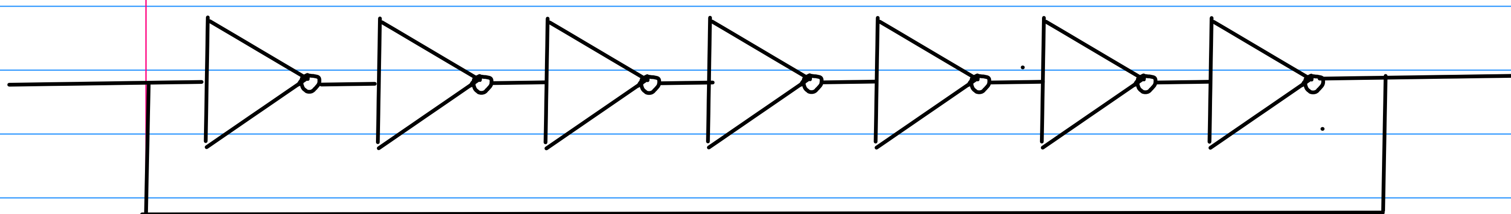
Odd Number of Inverters



3 inverters



5 inverters

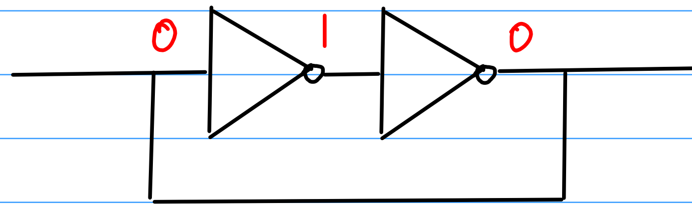


7 inverters

Odd number of inverters

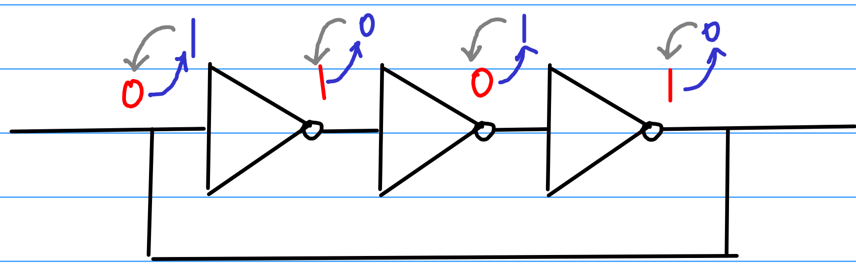
No stable operating points → Oscillating

ring oscillator



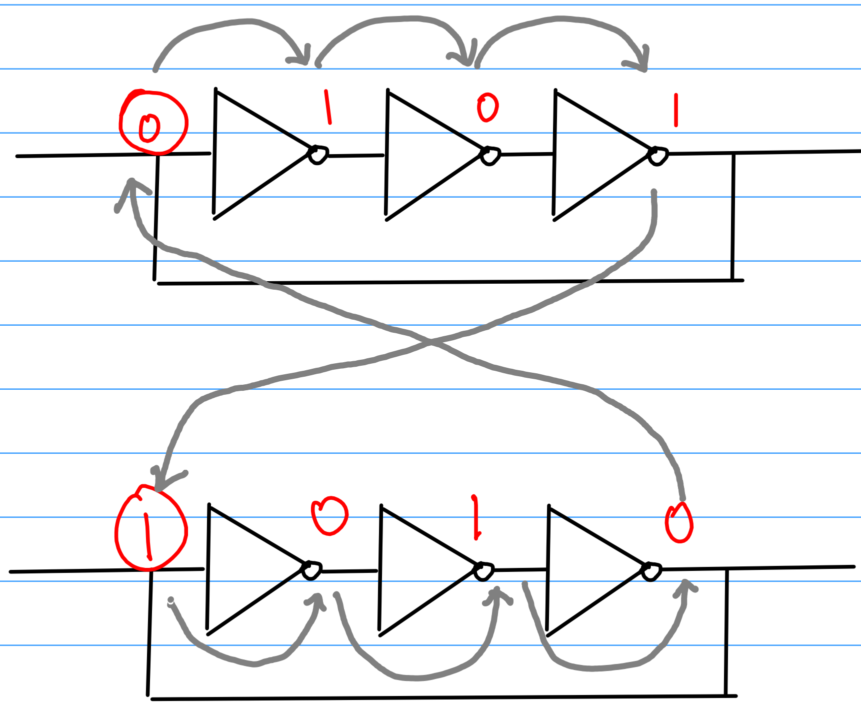
$\boxed{\text{Stable}}$

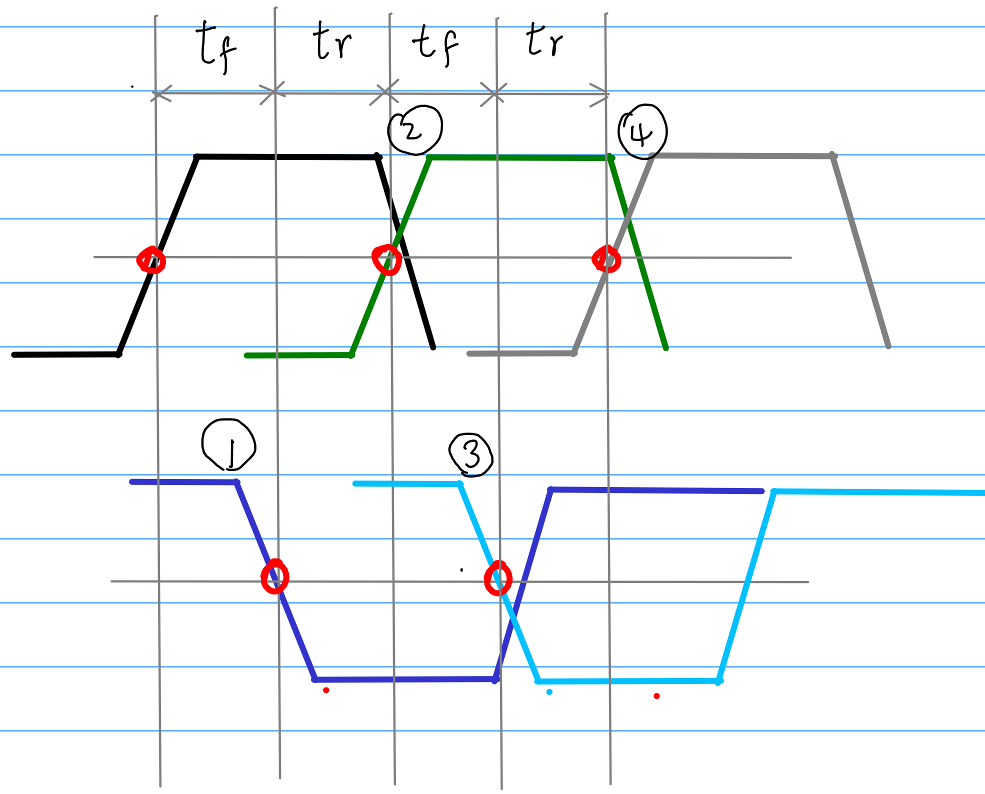
latch



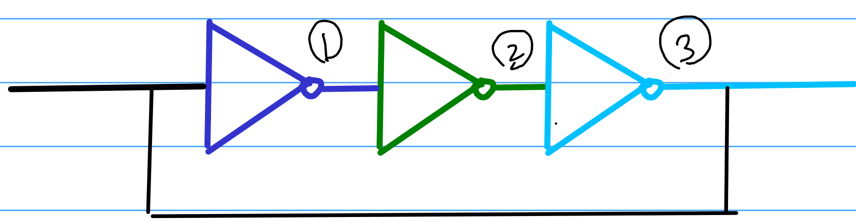
$\boxed{\text{Astable}}$

ring oscillator

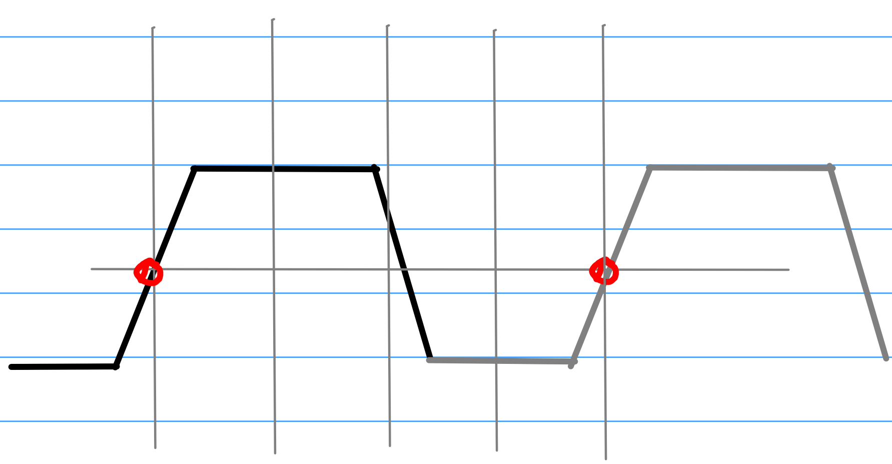


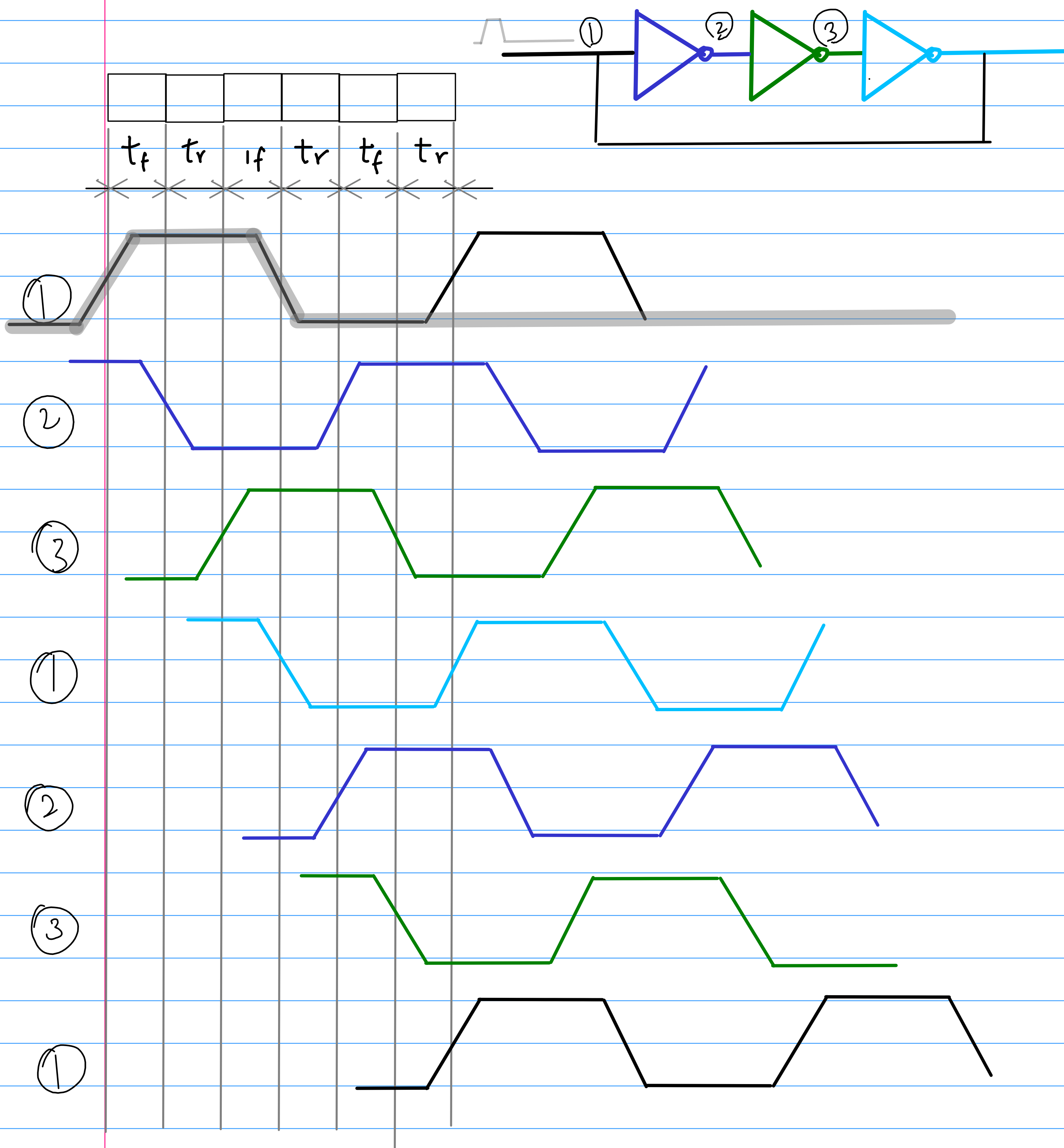


t_f
t_r
t_f
t_r
2
4
1
3

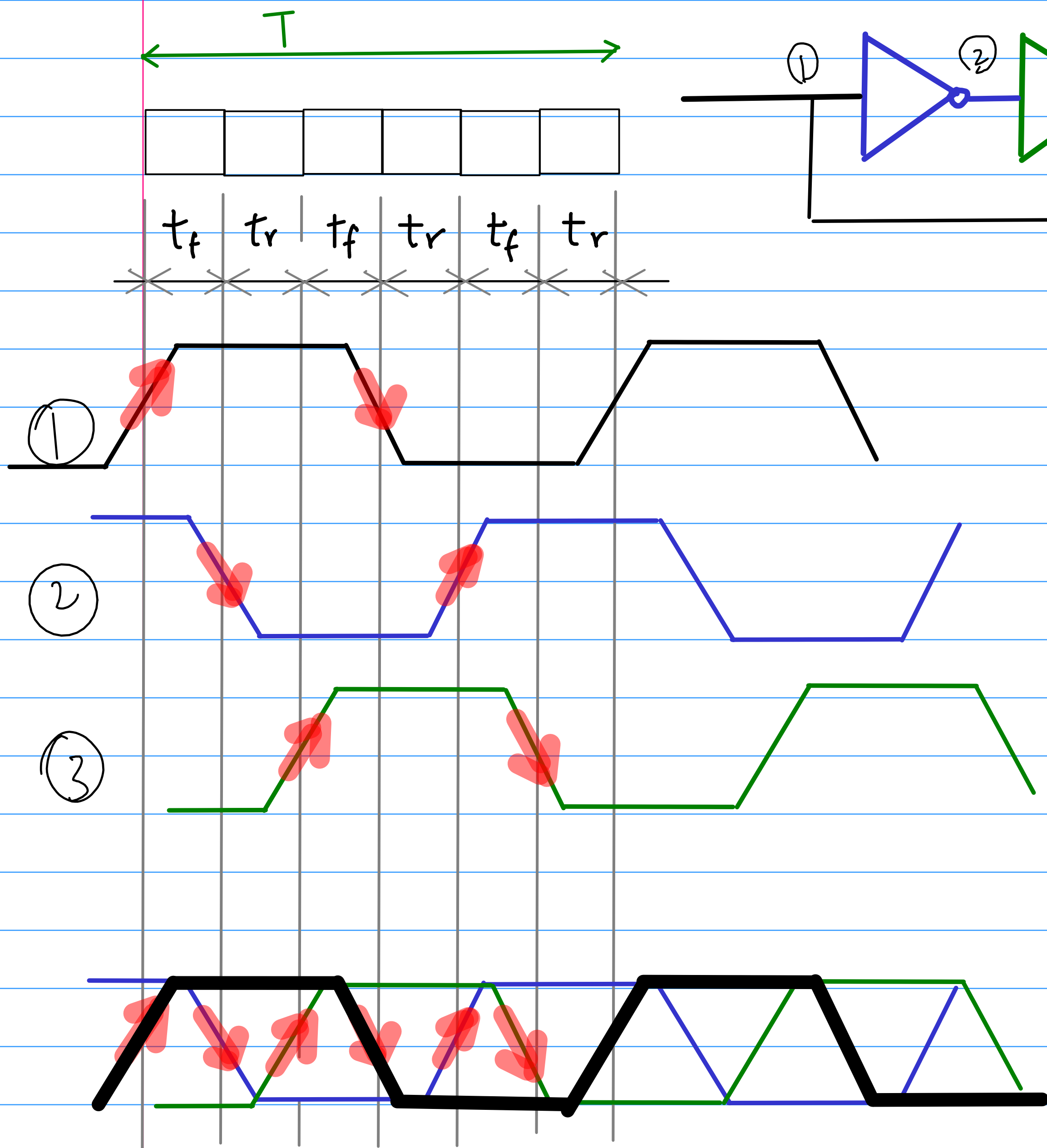


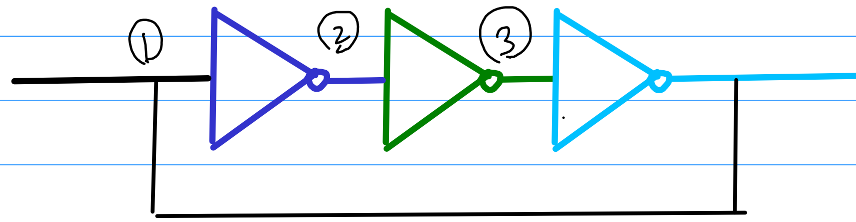
1
2
3

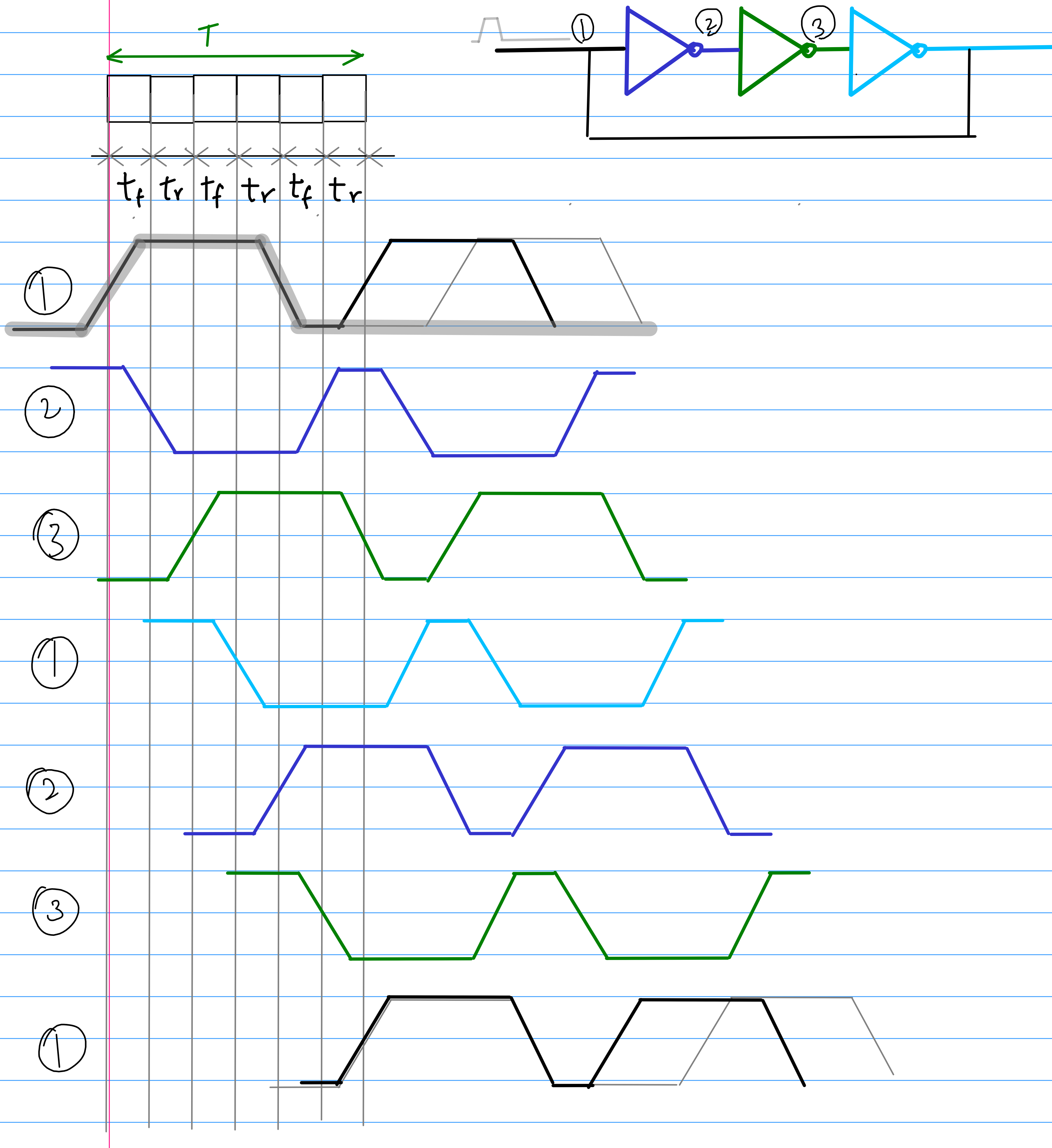


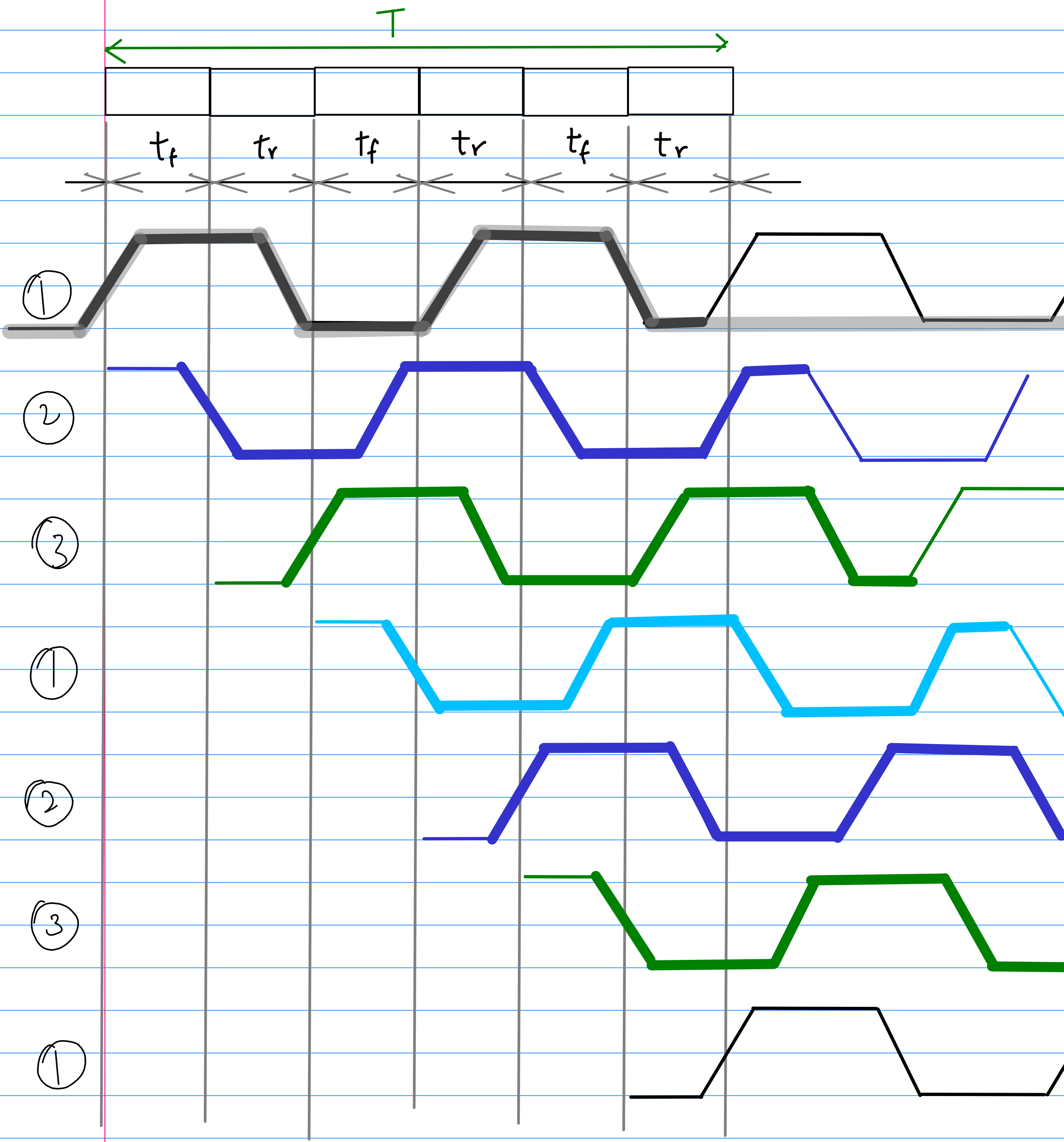


①
②
③
t_f
t_r
t_f
t_r
t_f
t_r
①
②
③
①
②
③
①


T
t_f t_r t_f t_r t_f t_r
1
2
3


1
2
3


T
tf tr tf tr tf tr
1
2
3
1
2
3
1
2
3
1


T
t_f
t_r
t_f
t_r
t_f
t_r
1
2
3
1
2
3
1

$$T = 2 \cdot t_p \cdot N$$

t_p: propagation delay
N: # of inverters in chain

$$T \gg t_f + t_r$$

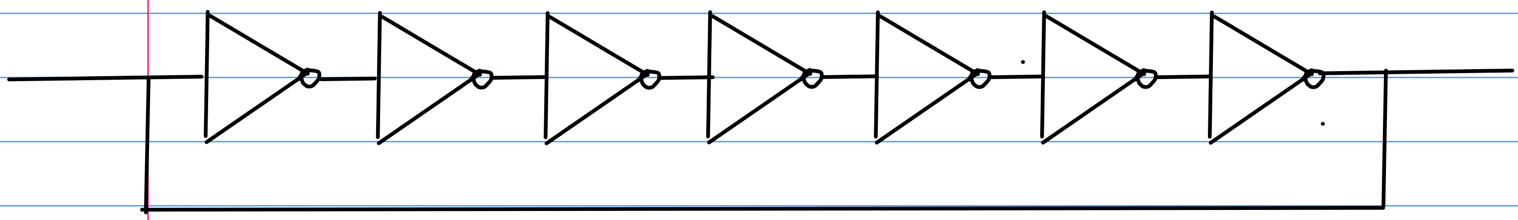
- used to measure the average propagation delay of a typical inverter with minimum capacitive loading

$$t_p = \frac{T}{2 \cdot N}$$

Characterise a particular design/fabrication process

- used as a simple on chip clock

N inverters (odd number)



$$g = \frac{C_{in}}{C_{ref}} = \frac{C_{ref}}{C_{ref}} = 1$$

$$h = \frac{C_{out}}{C_{in}} = \frac{C_{ref}}{C_{ref}} = 1$$

$$p = \left(\frac{C_{p,ref}}{C_{ref}}\right) = \left(\frac{\text{internal diffusion cap}}{\text{gate cap of ref inv}}\right) = \frac{3}{3} = 1$$

$$d = gh + p = 2 \qquad d_{abs} = 2\tau$$

$$freq = \frac{1}{2N\, d_{abs}} = \frac{1}{4N\tau}$$