

Path Delay

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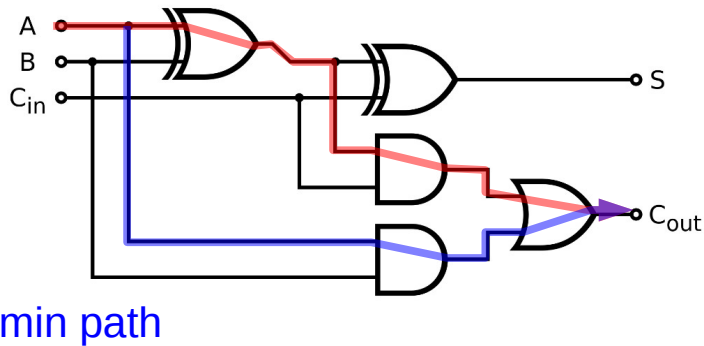
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Gate Delay

Fan out
Path Delay
Max-Path
Min-Path
Clock
Setup & Hold Time
Metastability
Synchronizer

Max Path / Min Path

Max path



Max delay

min delay

min path

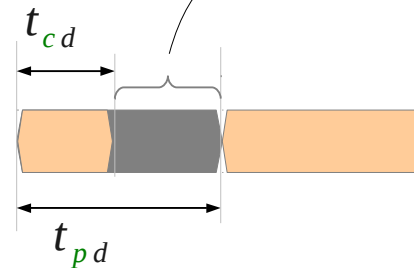
$$t_{cd} \leq t_{delay} \leq t_{pd}$$

min delay

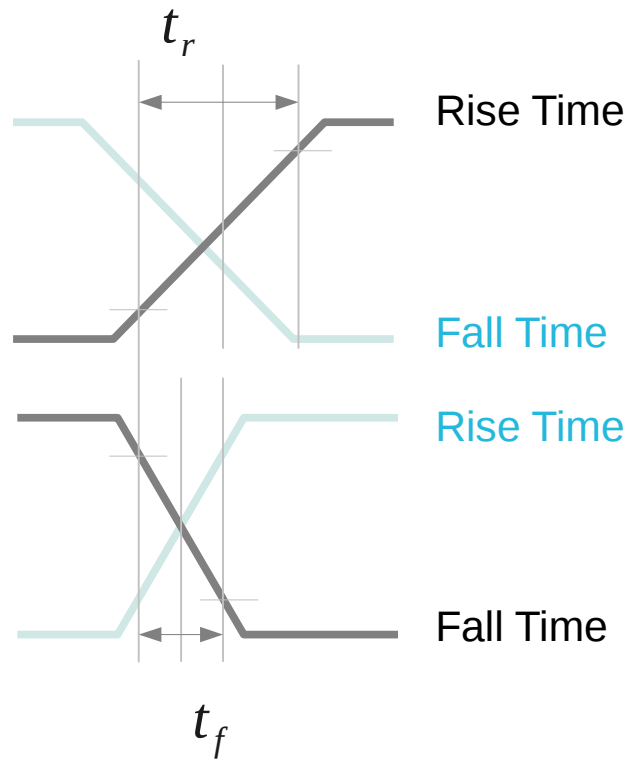
Max delay



the output is changing

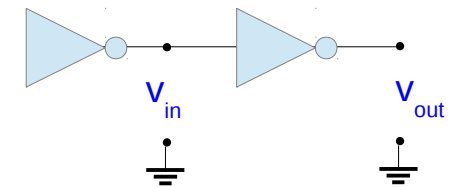
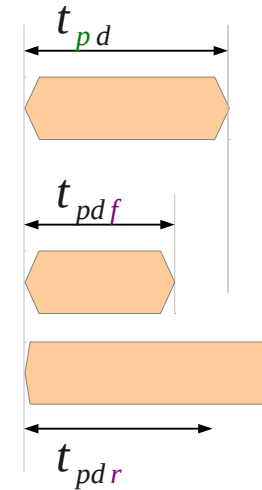


Rise / Fall Times



Max delay

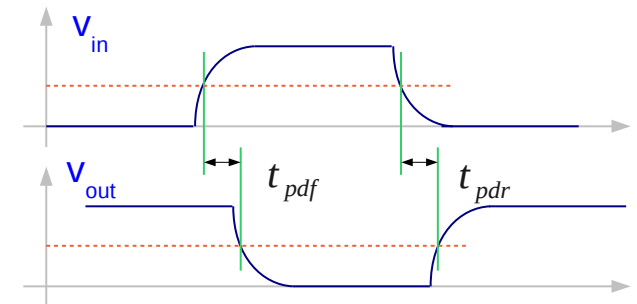
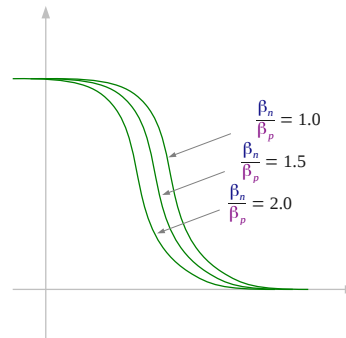
min delay



$$\frac{t_f}{t_r} = \frac{2.2\tau_n}{2.2\tau_p}$$

$$\frac{\beta_n}{\beta_p} > 1 \quad \frac{R_n}{R_p} < 1$$

$$\frac{\tau_n}{\tau_p} = \frac{R_n C_{out}}{R_p C_{out}} = \frac{R_n}{R_p} < 1$$

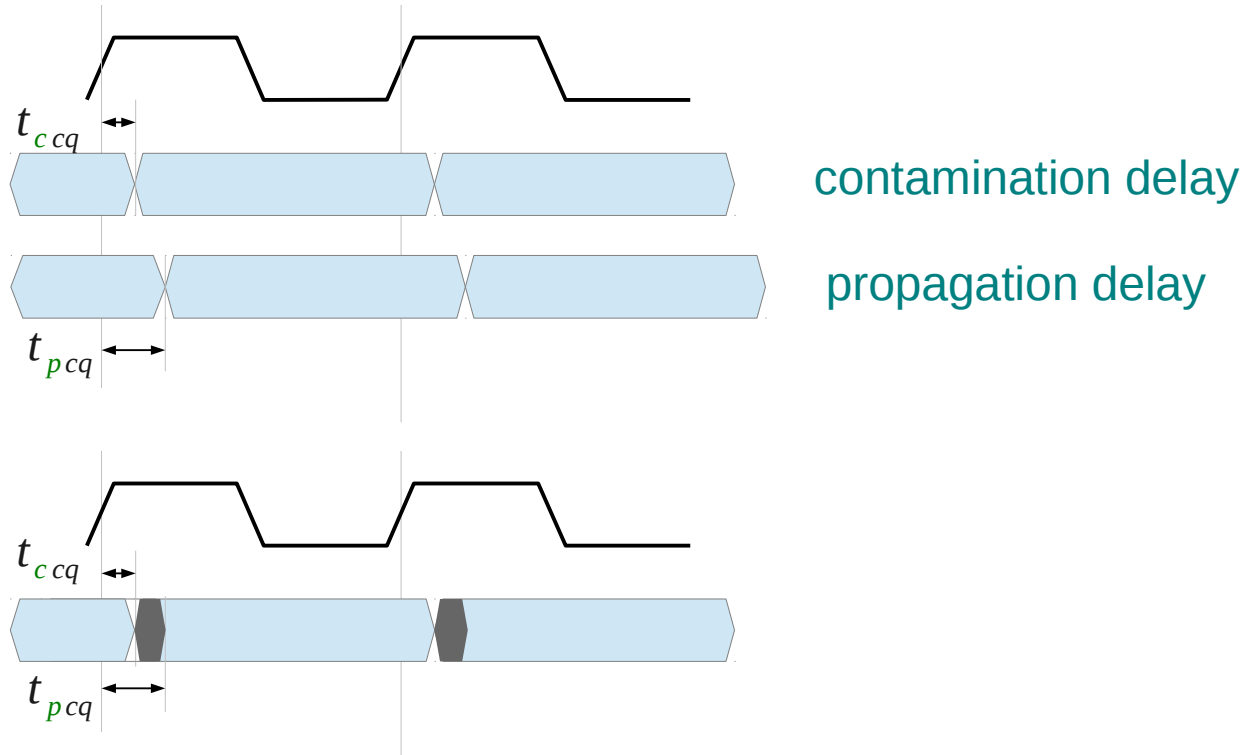


PVT Variation

{ Process
Voltage
Temperature

High temperature **Max delay**
Low temperature **min delay**

FF Output Delay



contamination delay

propagation delay

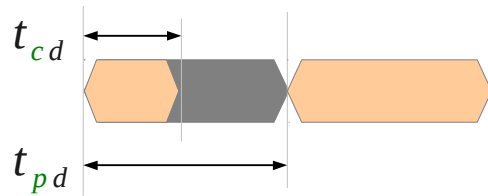
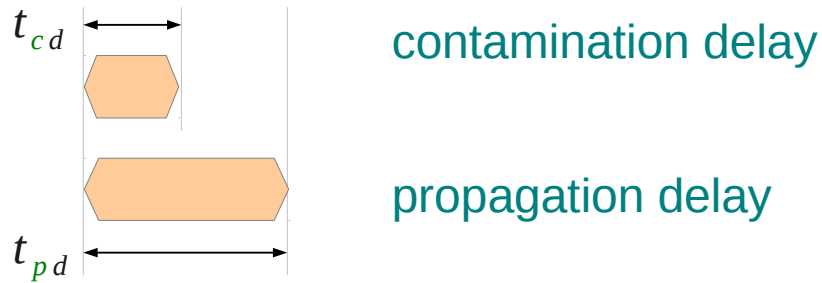
flipflop clock-to-q

$$t_{ccq} \leq t_{delay} \leq t_{pcq}$$

min delay

Max delay

Path Delay



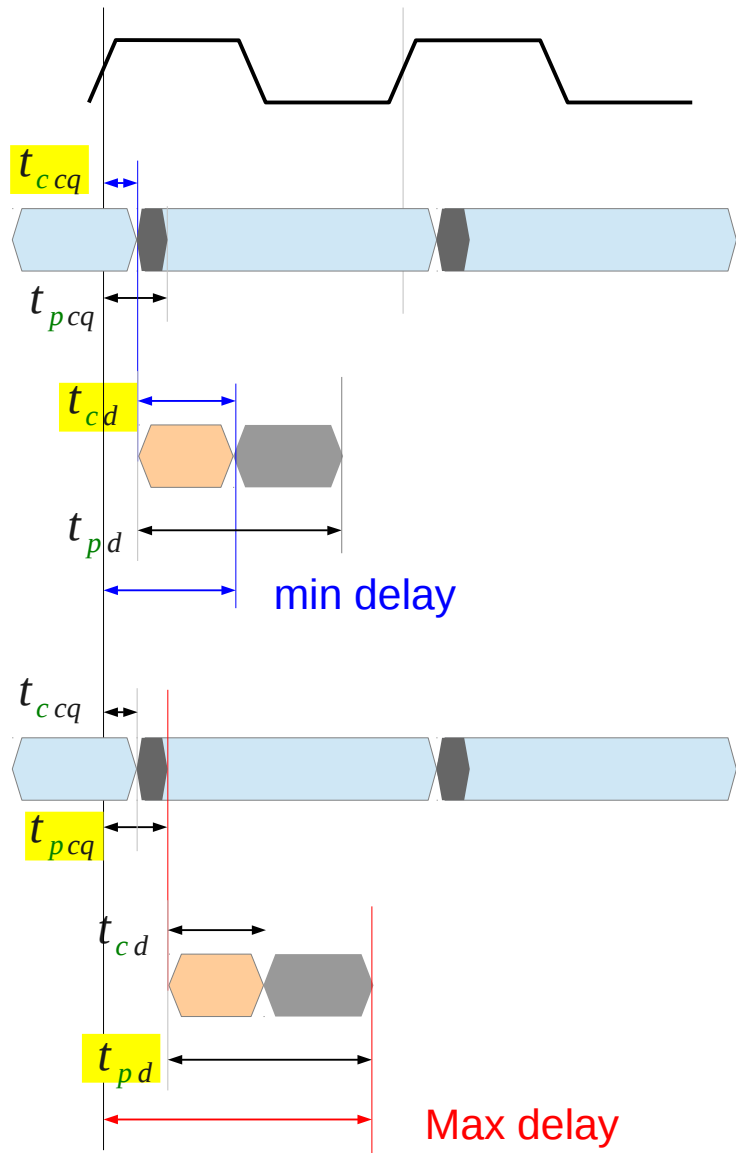
combinational logic delay

$$t_{cd} \leq t_{delay} \leq t_{pd}$$

min delay

Max delay

Reg-to-Reg Delay (1)



$$t_{ccq} \leq t_{FF} \leq t_{pcq}$$

min delay

Max delay

$$t_{cd} \leq t_{comb} \leq t_{pd}$$

min delay

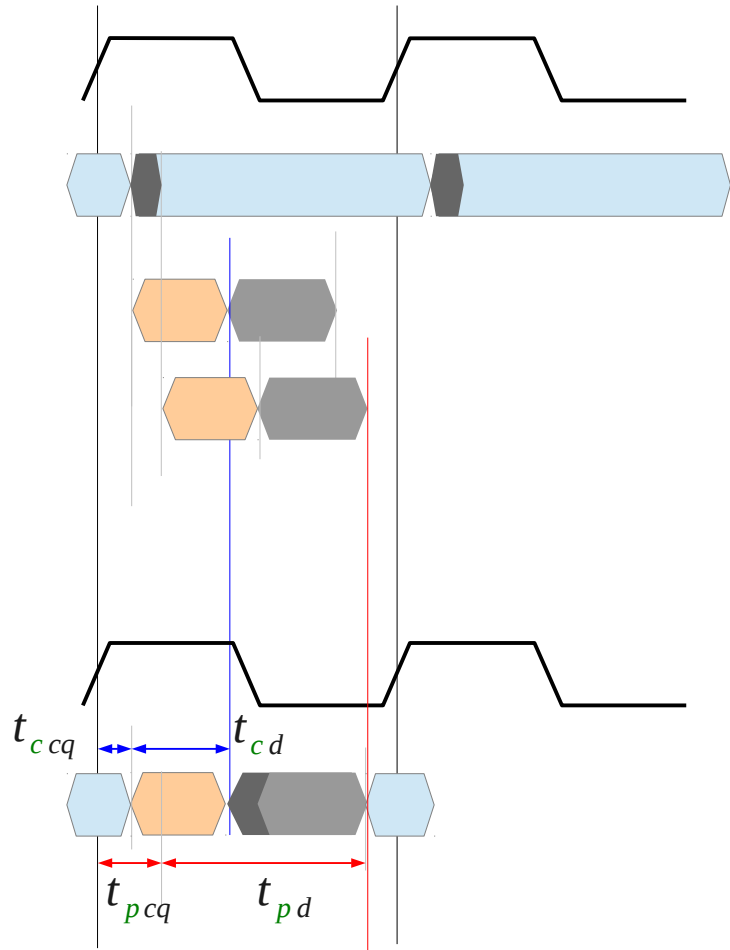
Max delay

$$t_{ccq} + t_{cd} \leq t_{delay} \leq t_{pcq} + t_{pd}$$

min delay

Max delay

Reg-to-Reg Delay (2)



$$t_{ccq} \leq t_{FF} \leq t_{pcq}$$

min delay

Max delay

$$t_{cd} \leq t_{comb} \leq t_{pd}$$

min delay

Max delay

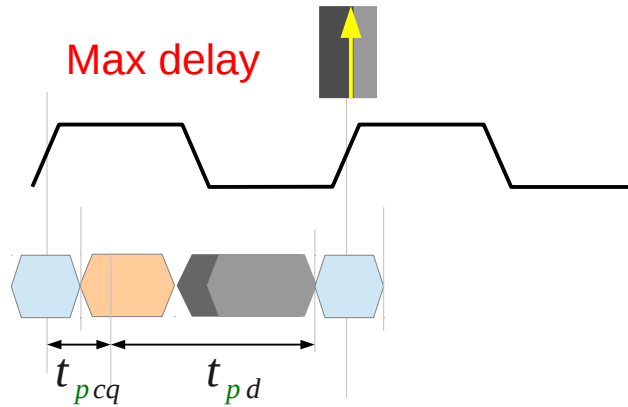
$$t_{ccq} + t_{cd} \leq t_{delay} \leq t_{pcq} + t_{pd}$$

min delay

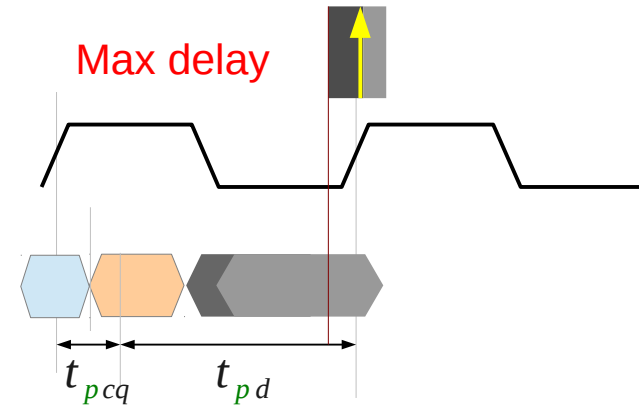
Max delay

Setup Time / Hold Time

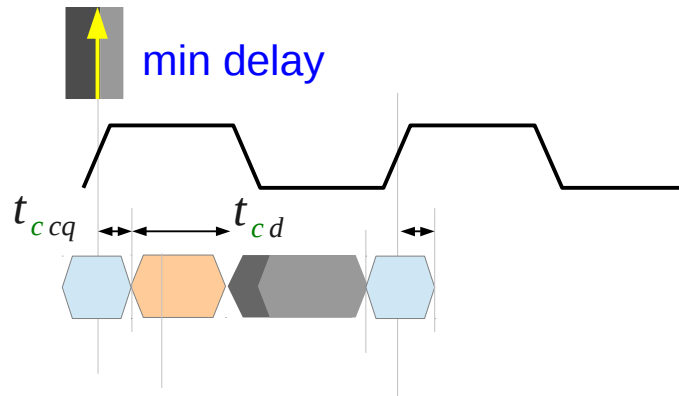
Setup Time OK



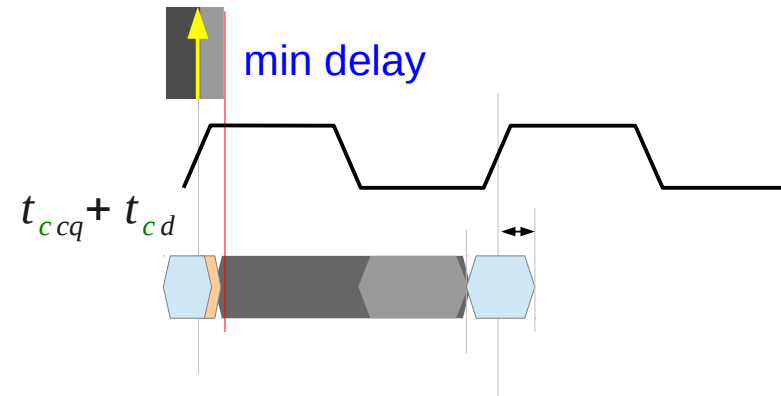
Setup Time Violation



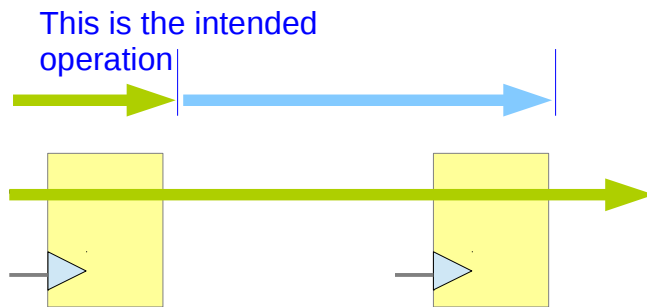
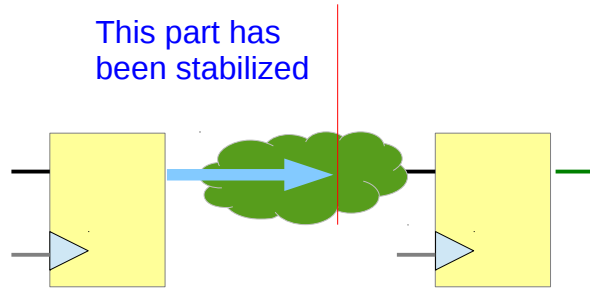
Hold Time OK



Hold Time Violation

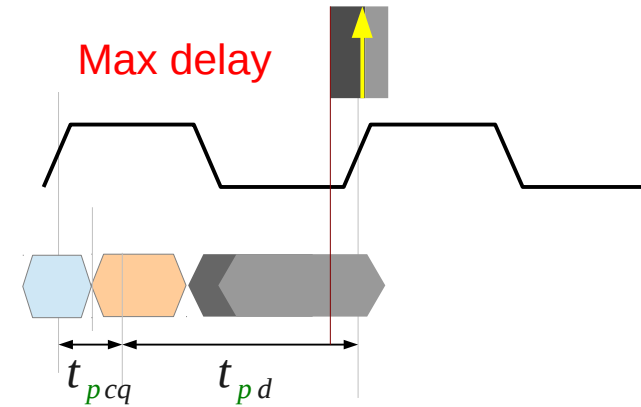


Setup Time / Hold Time

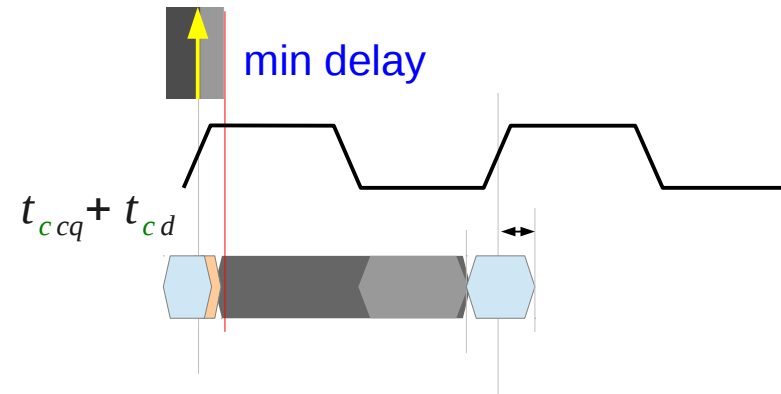


Since the delay is too small signal passes through the 2nd FF

Setup Time Violation



Hold Time Violation



References

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- [2] <http://www.allaboutcircuits.com/>
- [3] W. Wolf, "Modern VLSI Design : Systems on Silicon"
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