Logic Circuit Design
NOR-1

20170217

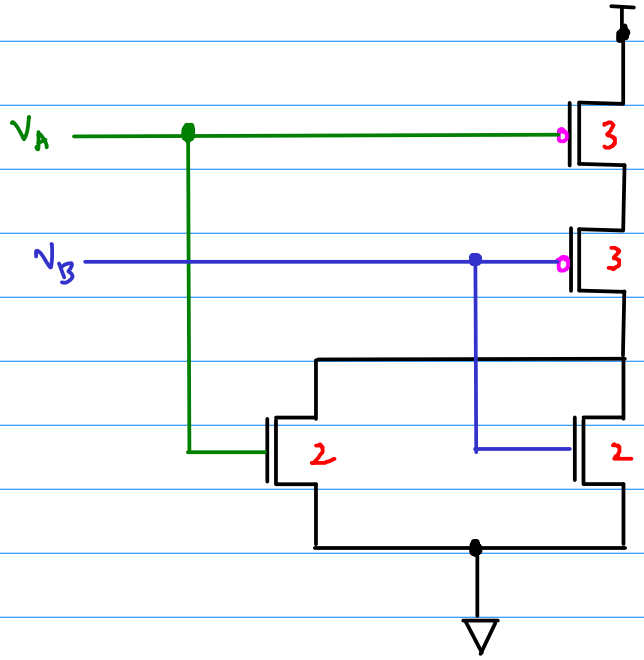
References

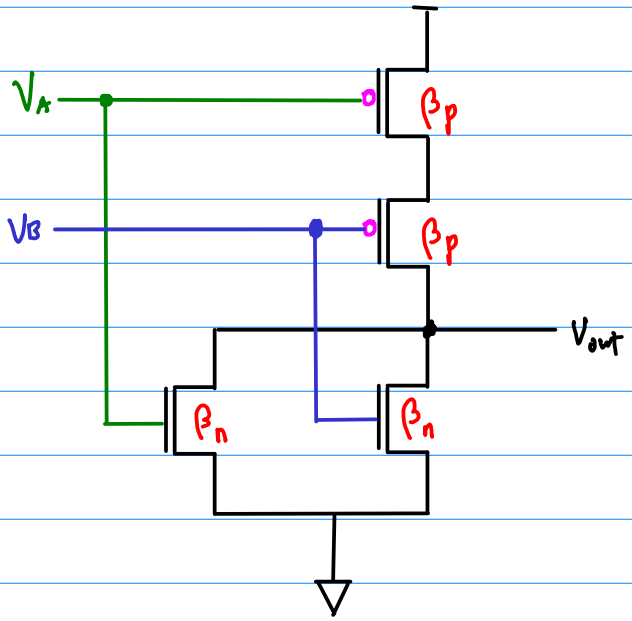
Some Figures from the following sites

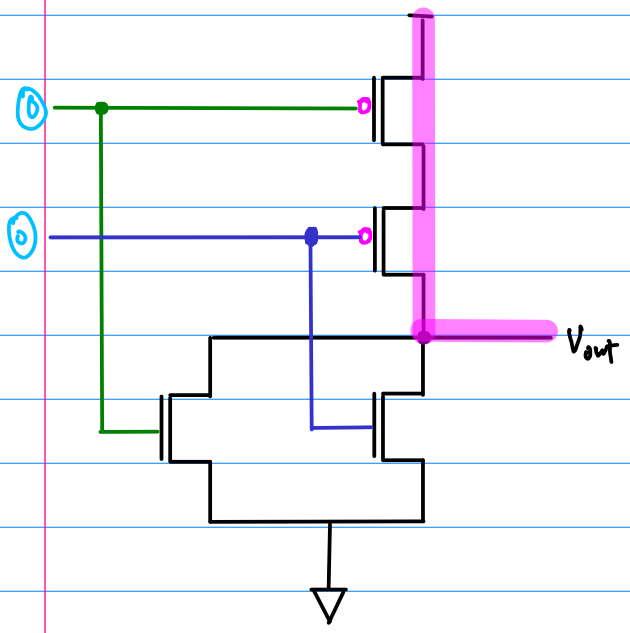
[1] http://pages.hmc.edu/harris/cmosvlsi/4e/index.html
Weste & Harris Book Site

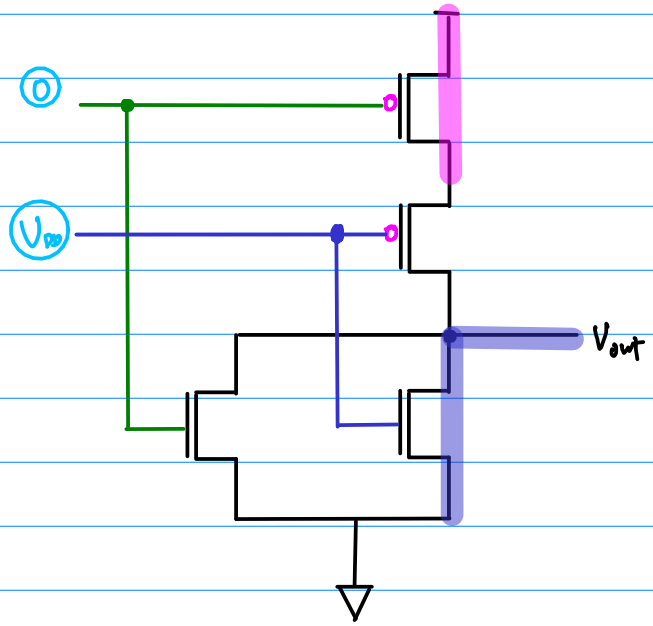
[2] Introduction to VLSI Circuits and Systems, Uyemura

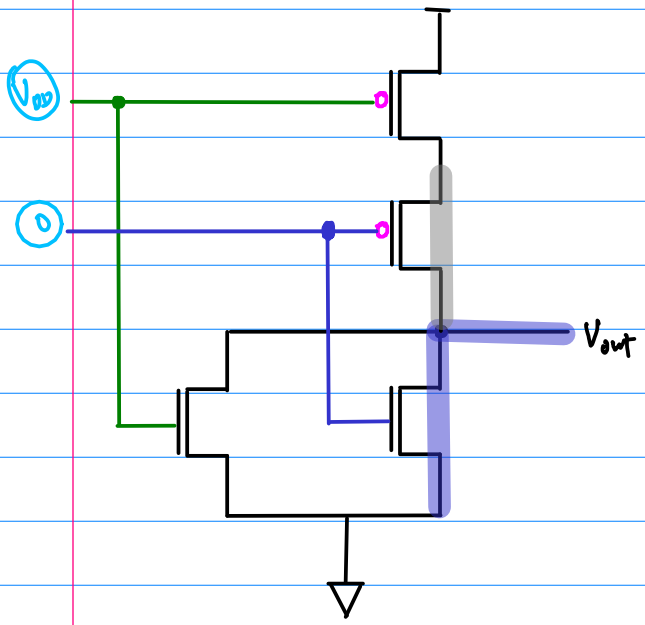
[2] en.wikipedia.org

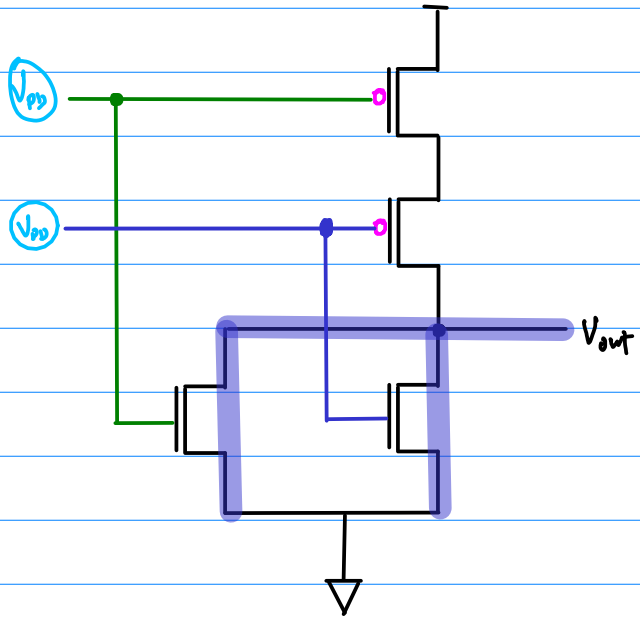

V_A
V_B
3
3
2
2

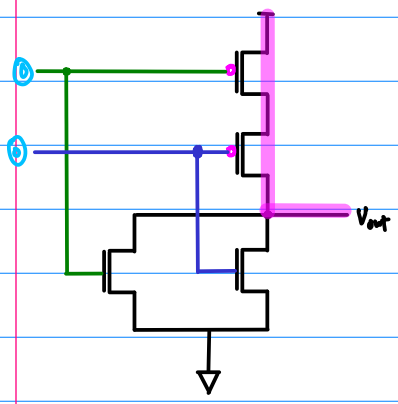

V_A
V_B
β_p
β_p
V_{out}
β_n
β_n

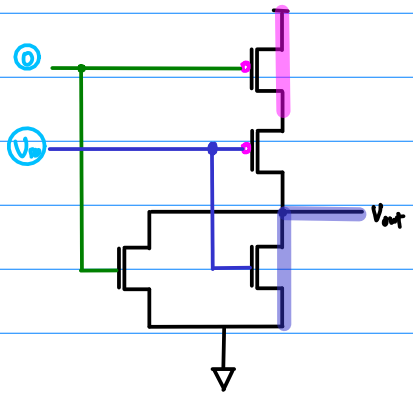

0
0
V_{out}

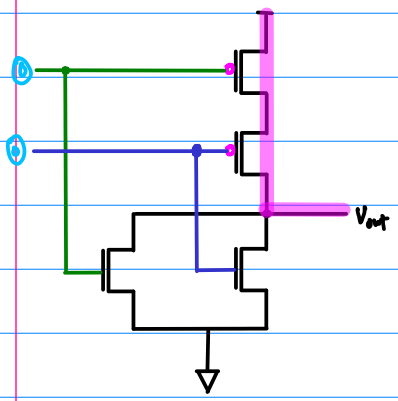

0
V_{DD}
V_{out}

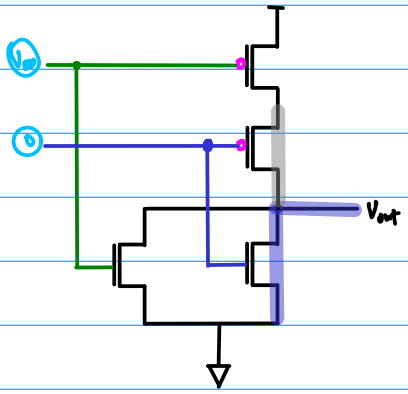

V_{DD}
0
V_{out}

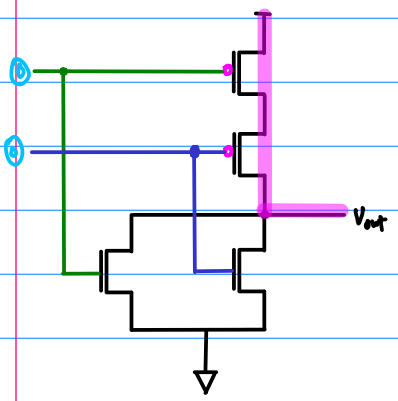

V_{DD}
V_{DD}
V_{out}

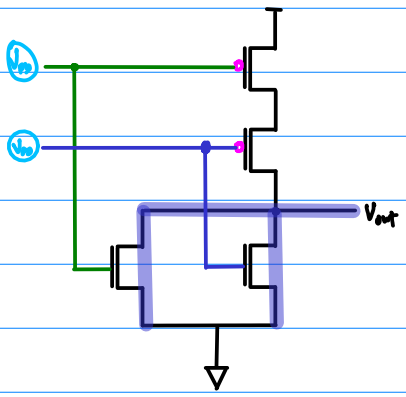

0
0
Vout


0
Vin
Vout

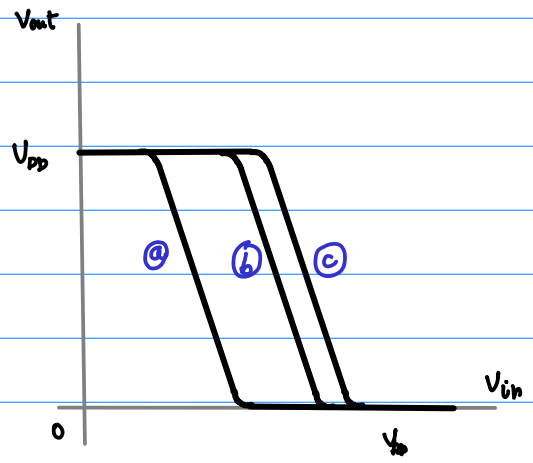

0
0
Vout

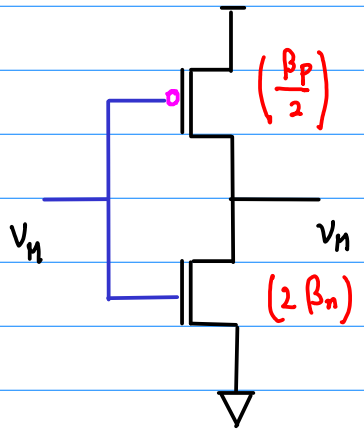

Vin
0
Vout

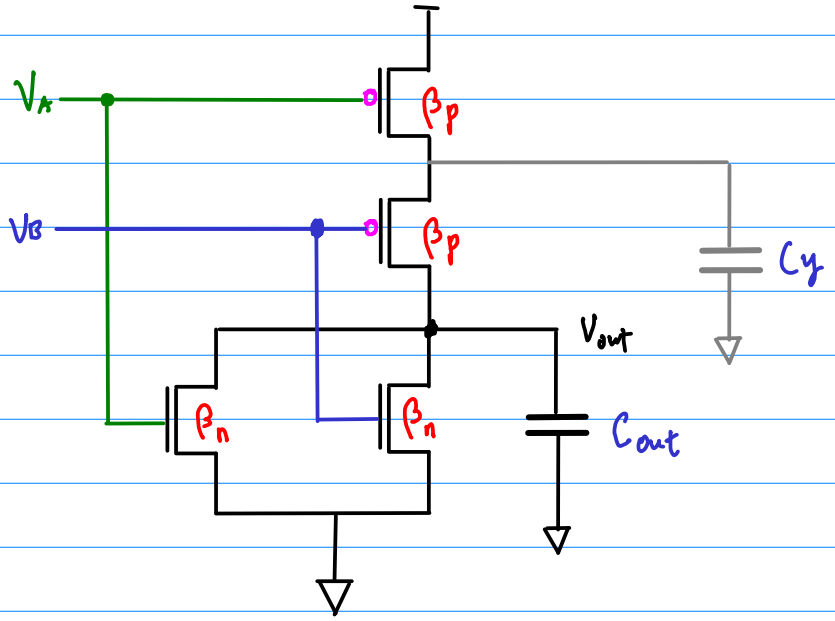

0
0
Vout

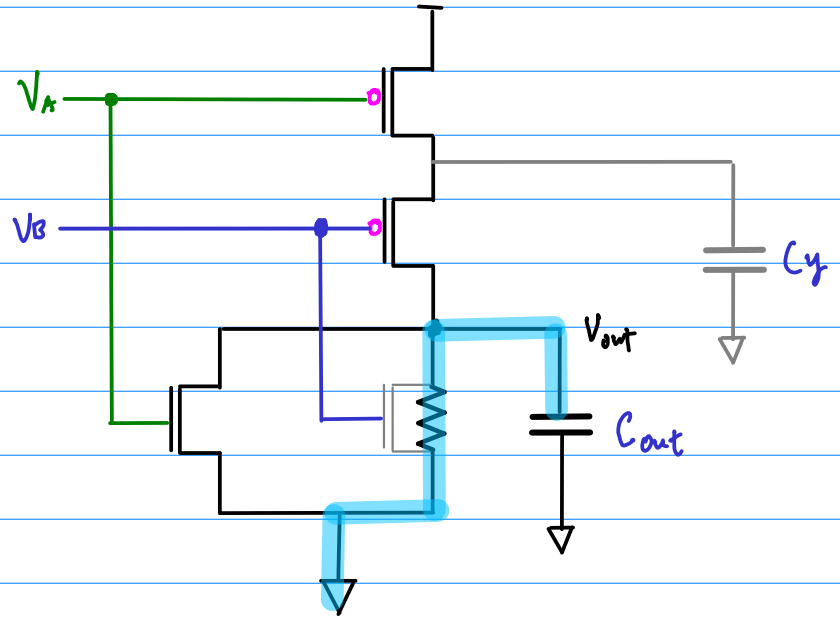

Vin
Vin
Vout

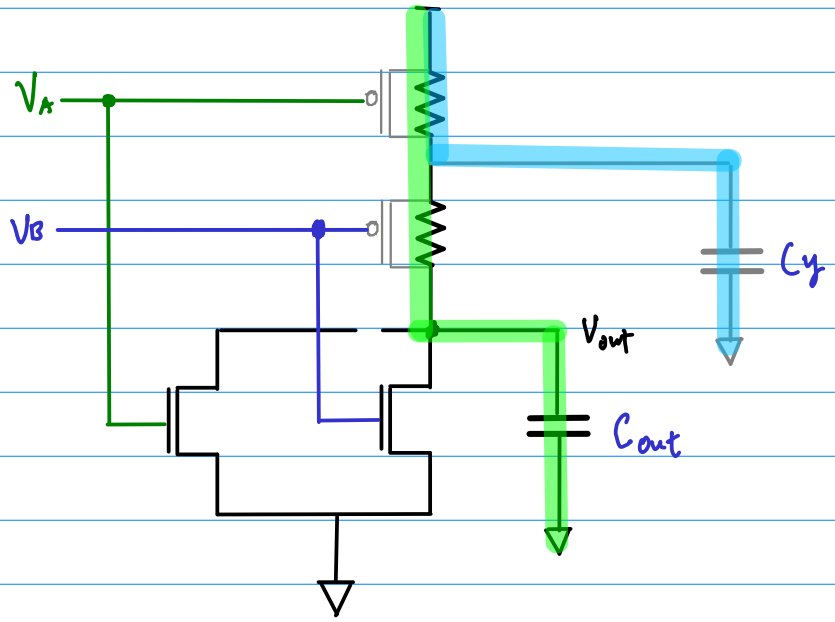
	V_A	V_B	V_{out}
	0	0	V_{DD}
ⓒ	0	V_{DD}	0
ⓑ	V_{DD}	0	0
ⓐ	V_{DD}	V_{DD}	0




$\left(\frac{\beta_p}{2}\right)$
V_M
V_M
$(2\beta_n)$


V_A
V_B
β_p
β_p
C_y
V_{out}
β_n
β_n
C_{out}


V_A
V_B
C_y
V_{out}
C_{out}


V_A
V_B
C_y
V_{out}
C_{out}