

CMOS Sequential Circuits

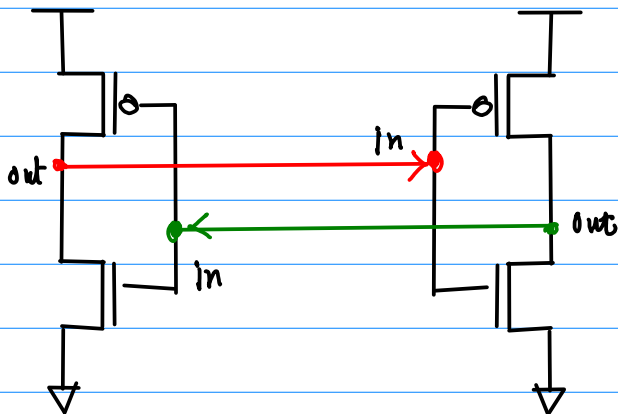
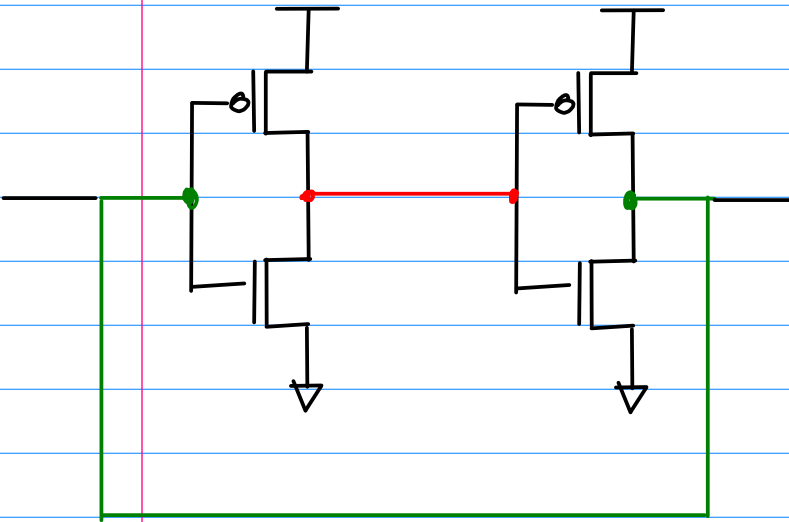
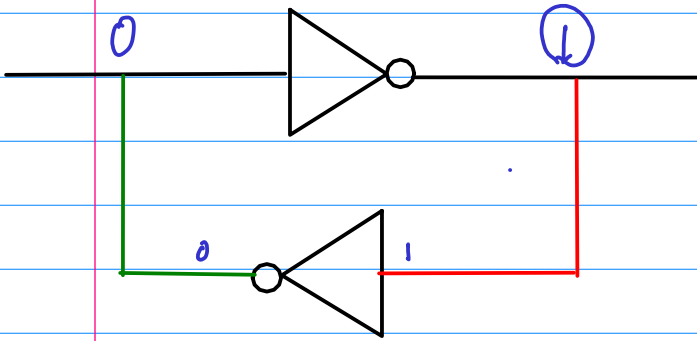
Seq-2 (H.2)

20151215

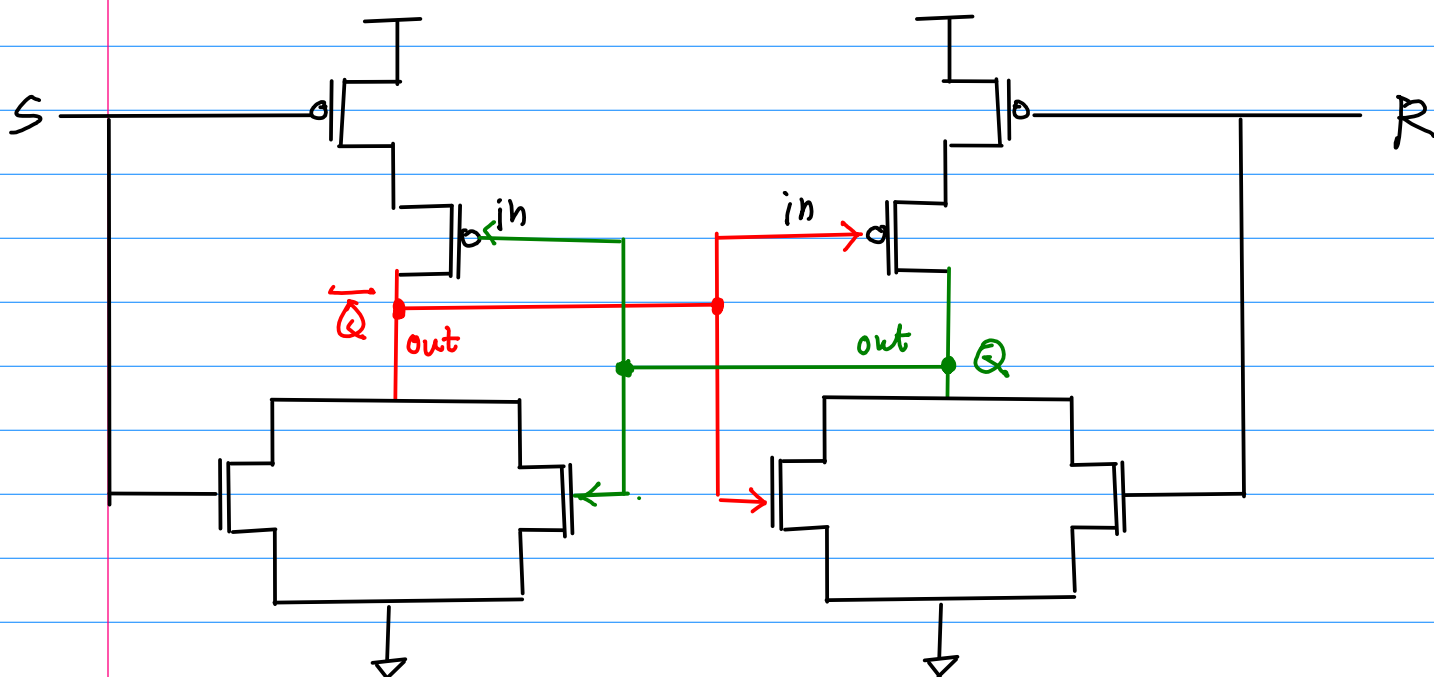
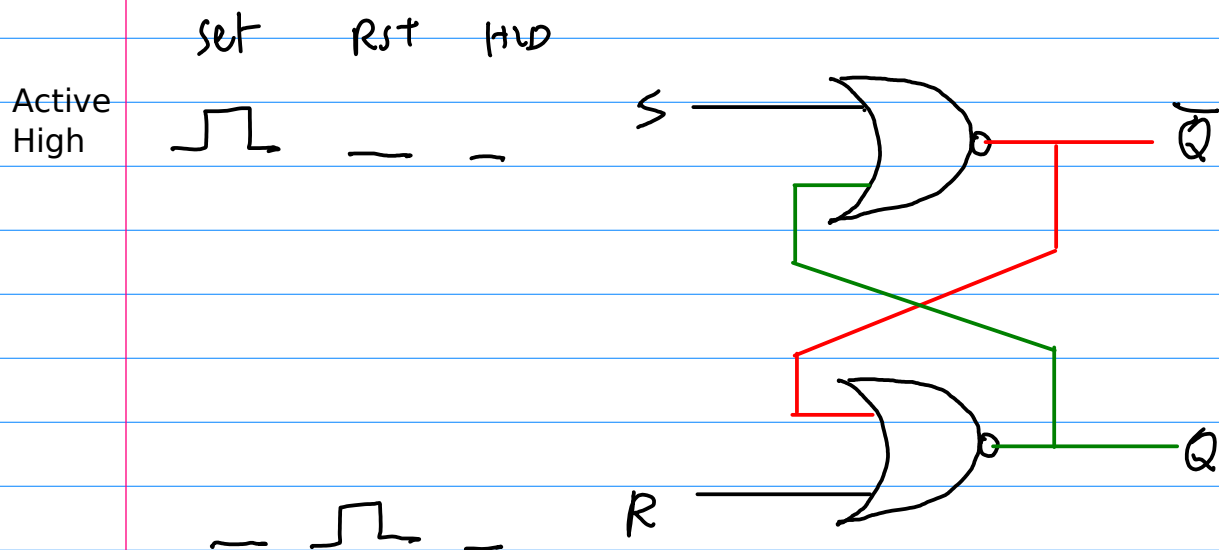
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Bistable Latch

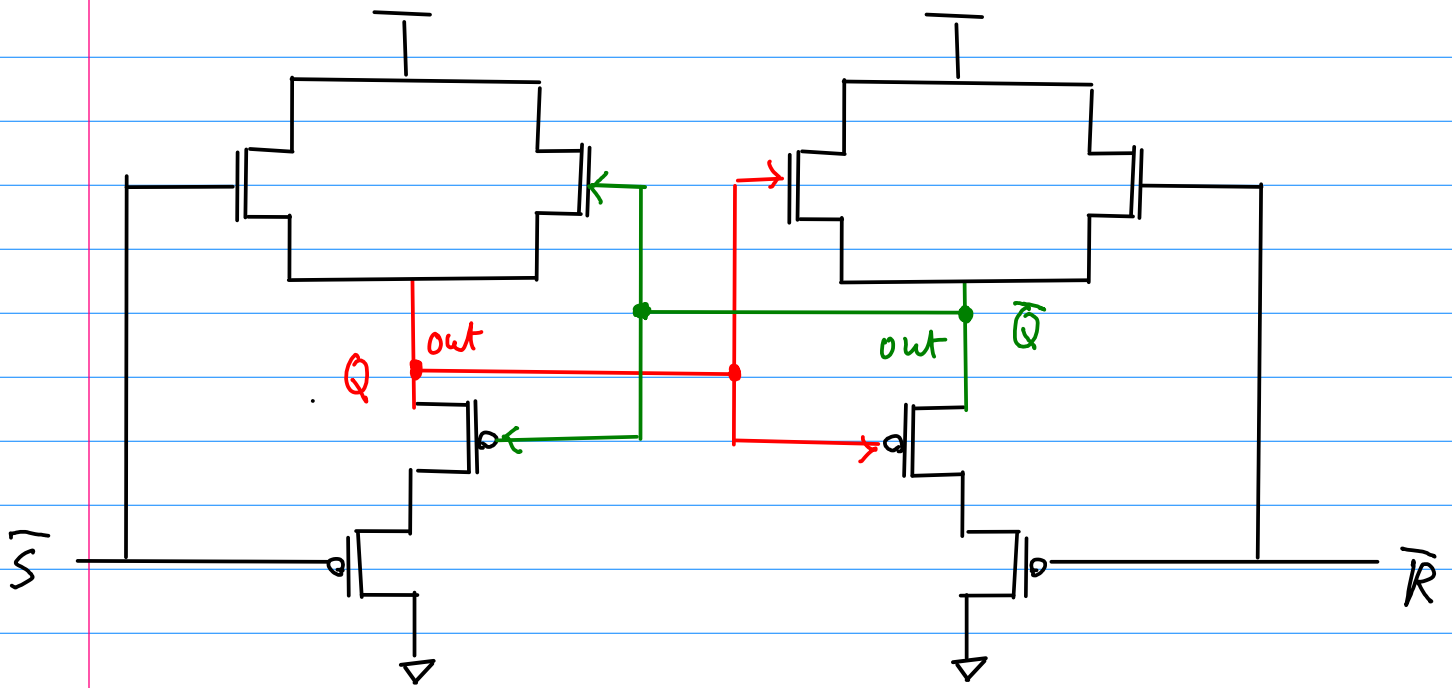
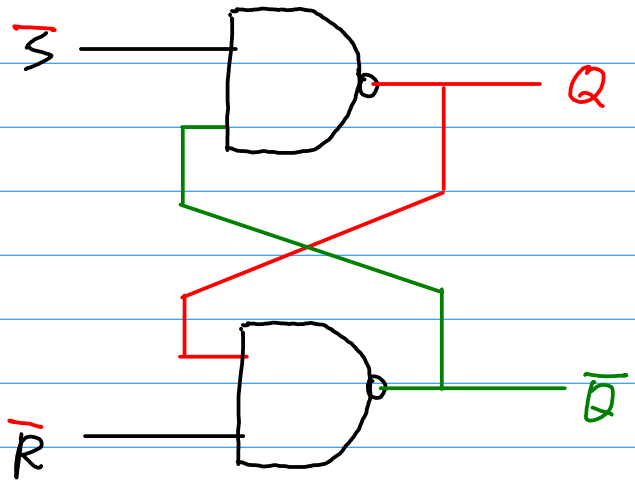
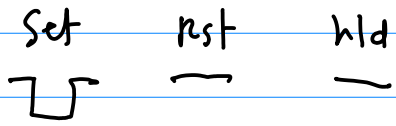


NOR-based RS Latch

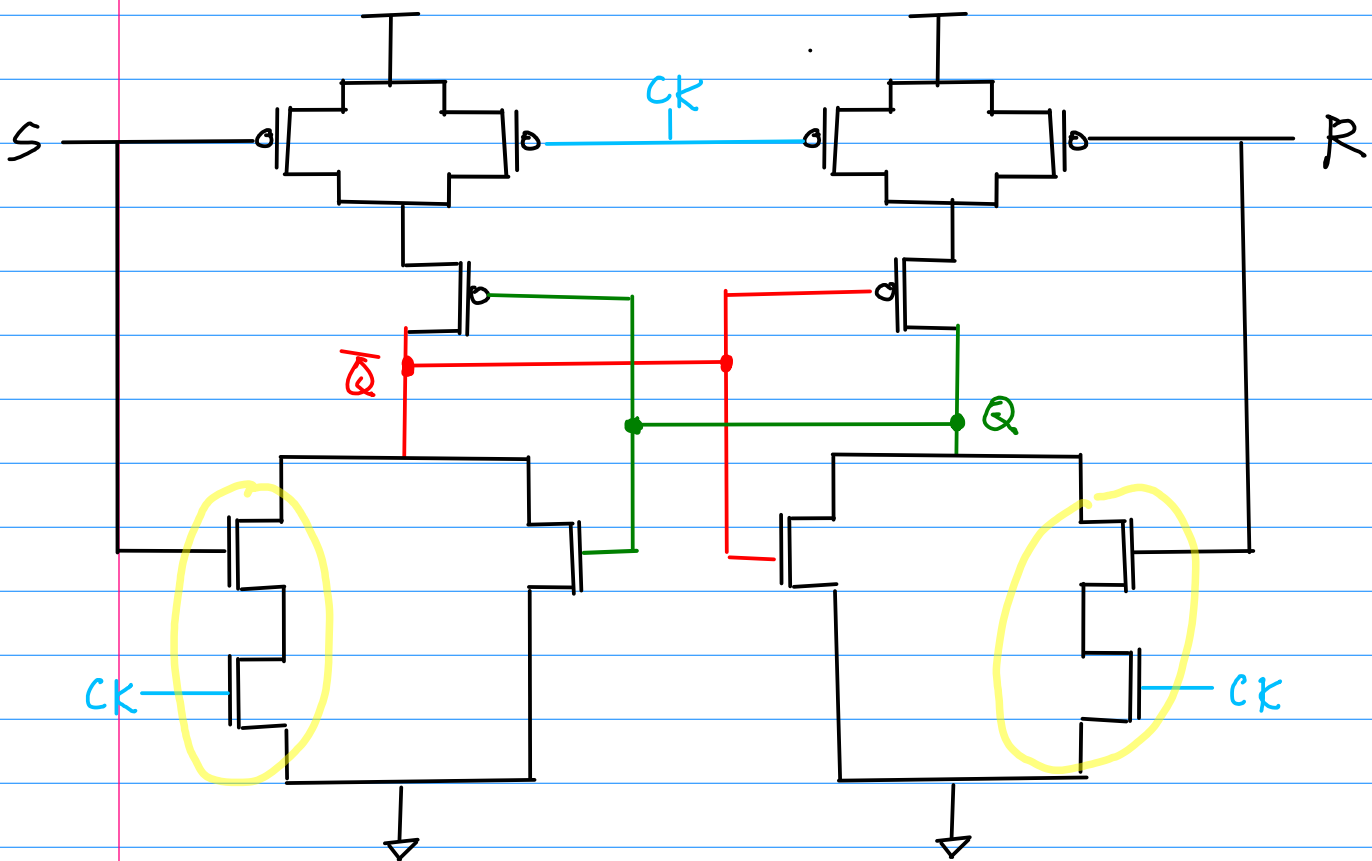
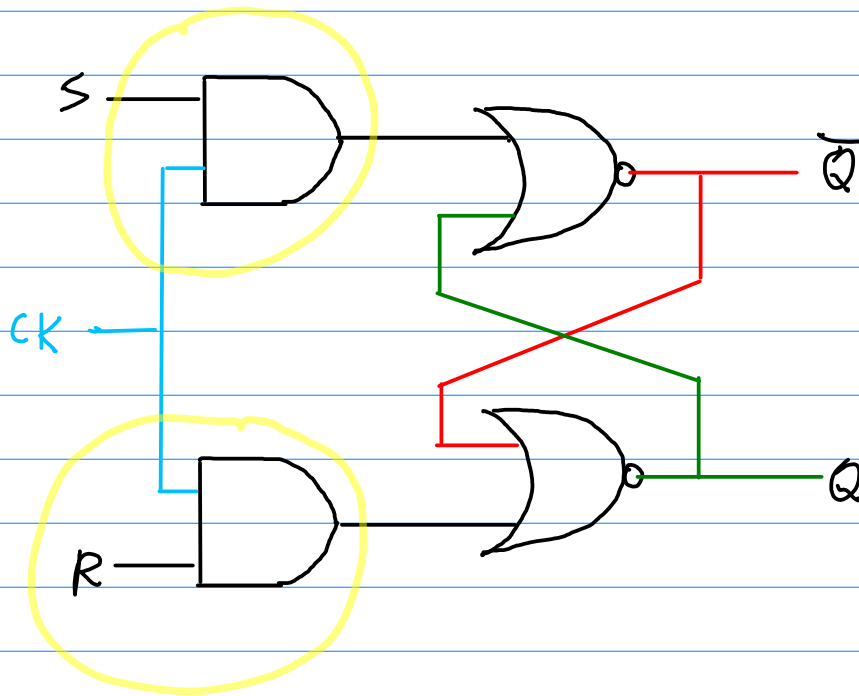


NAND-based RS Latch

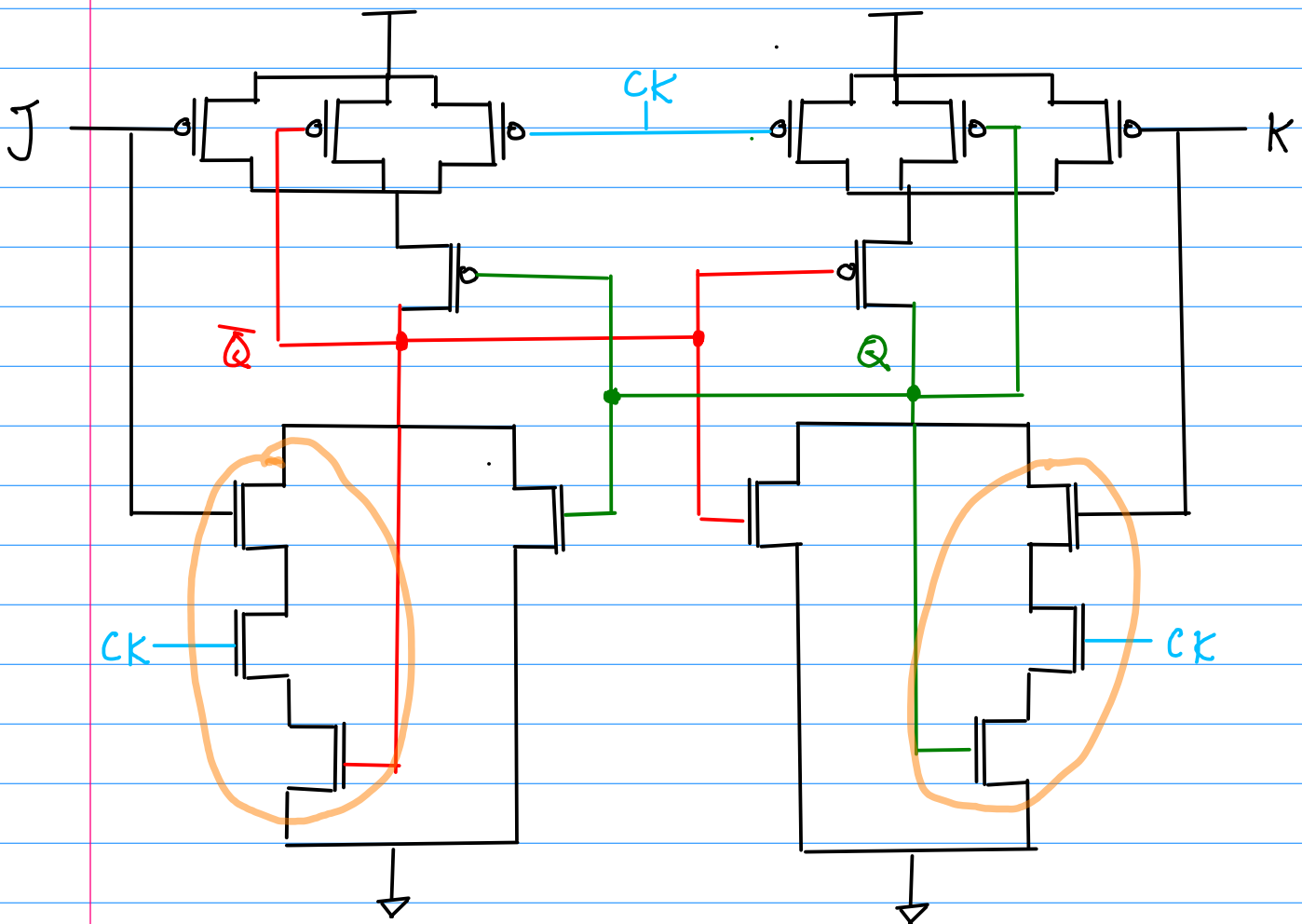
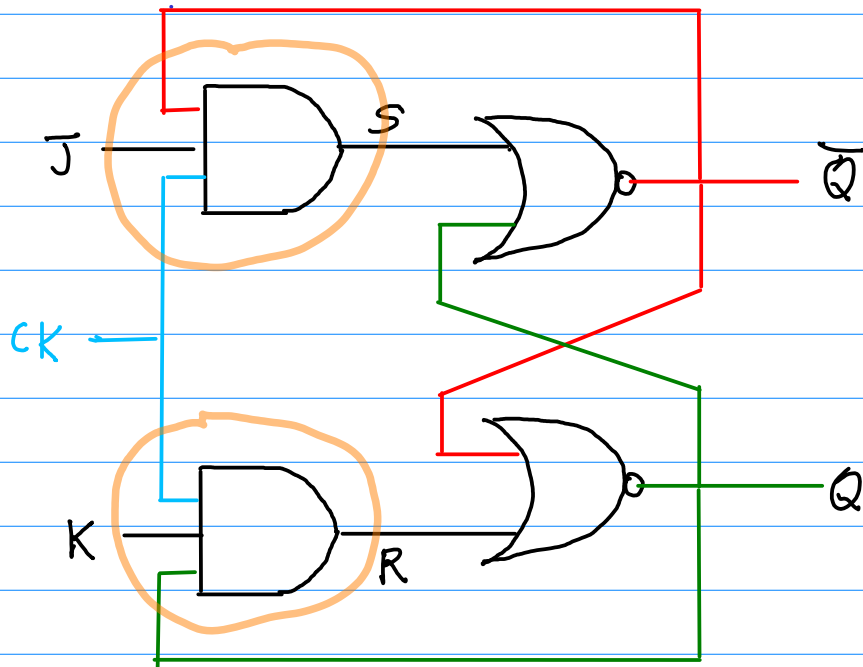
Active Low



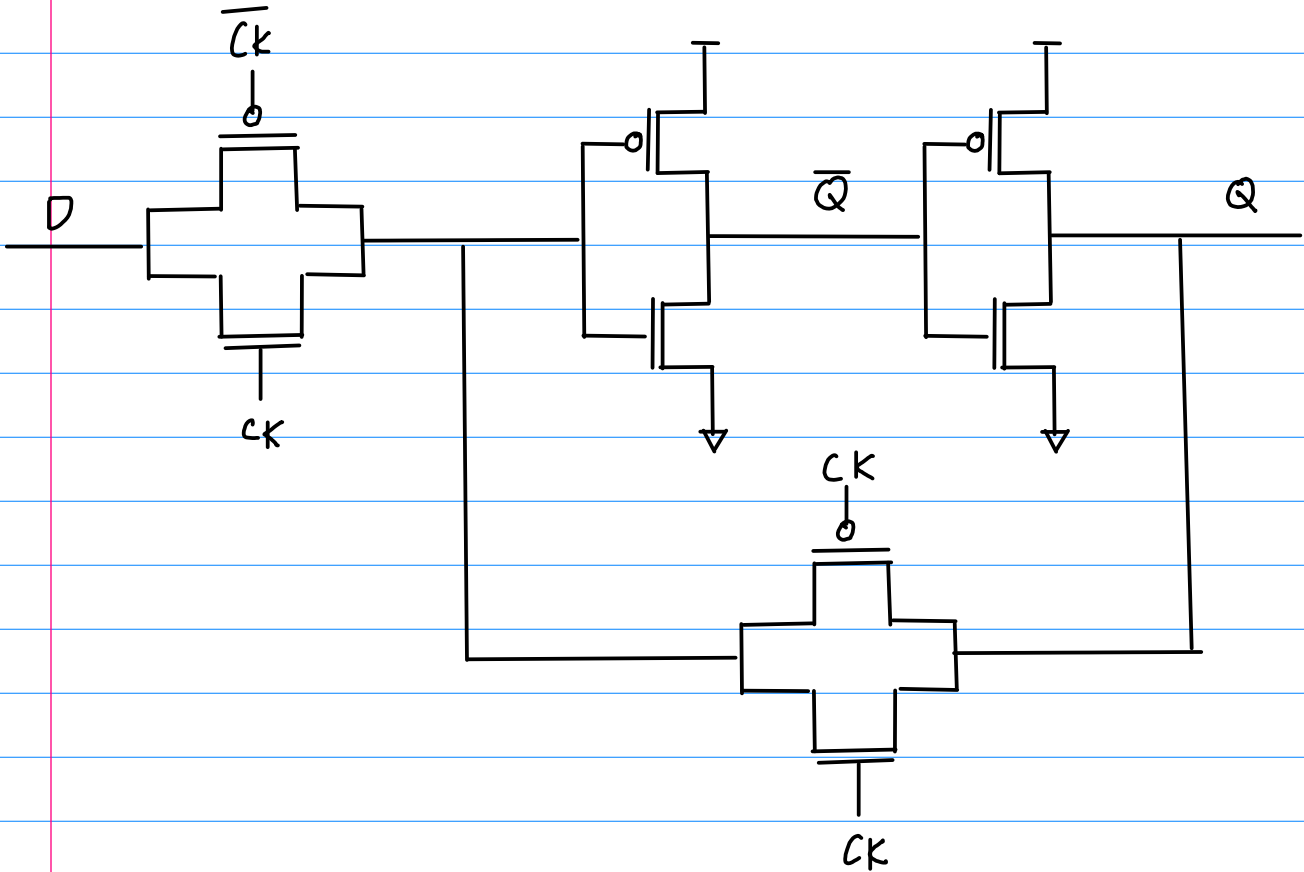
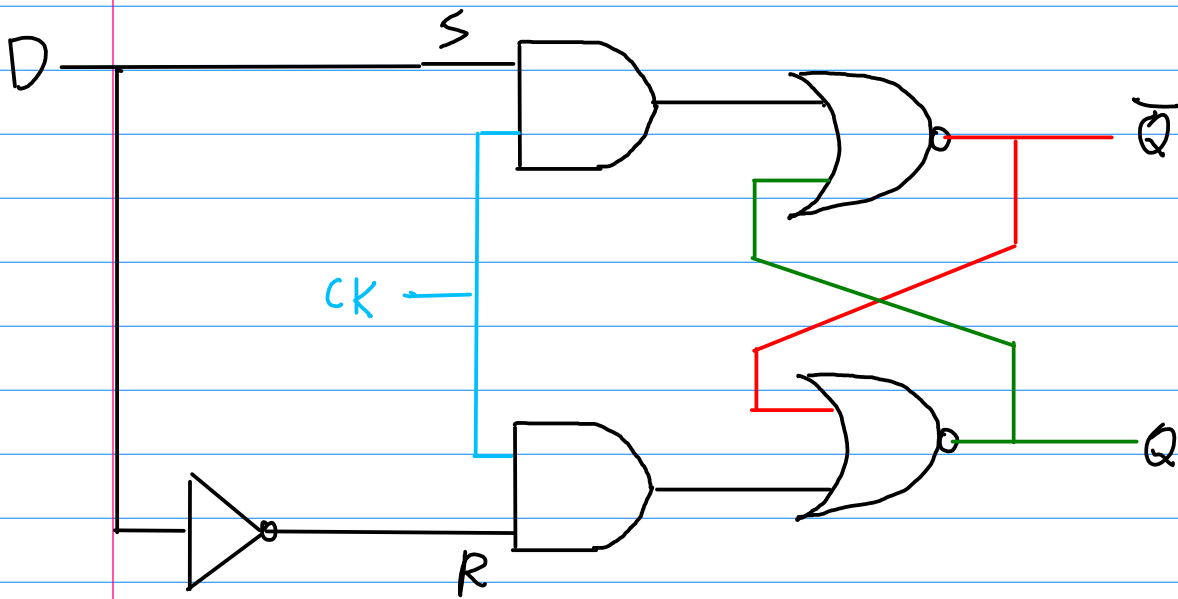
Clocked NOR-based RS Latch

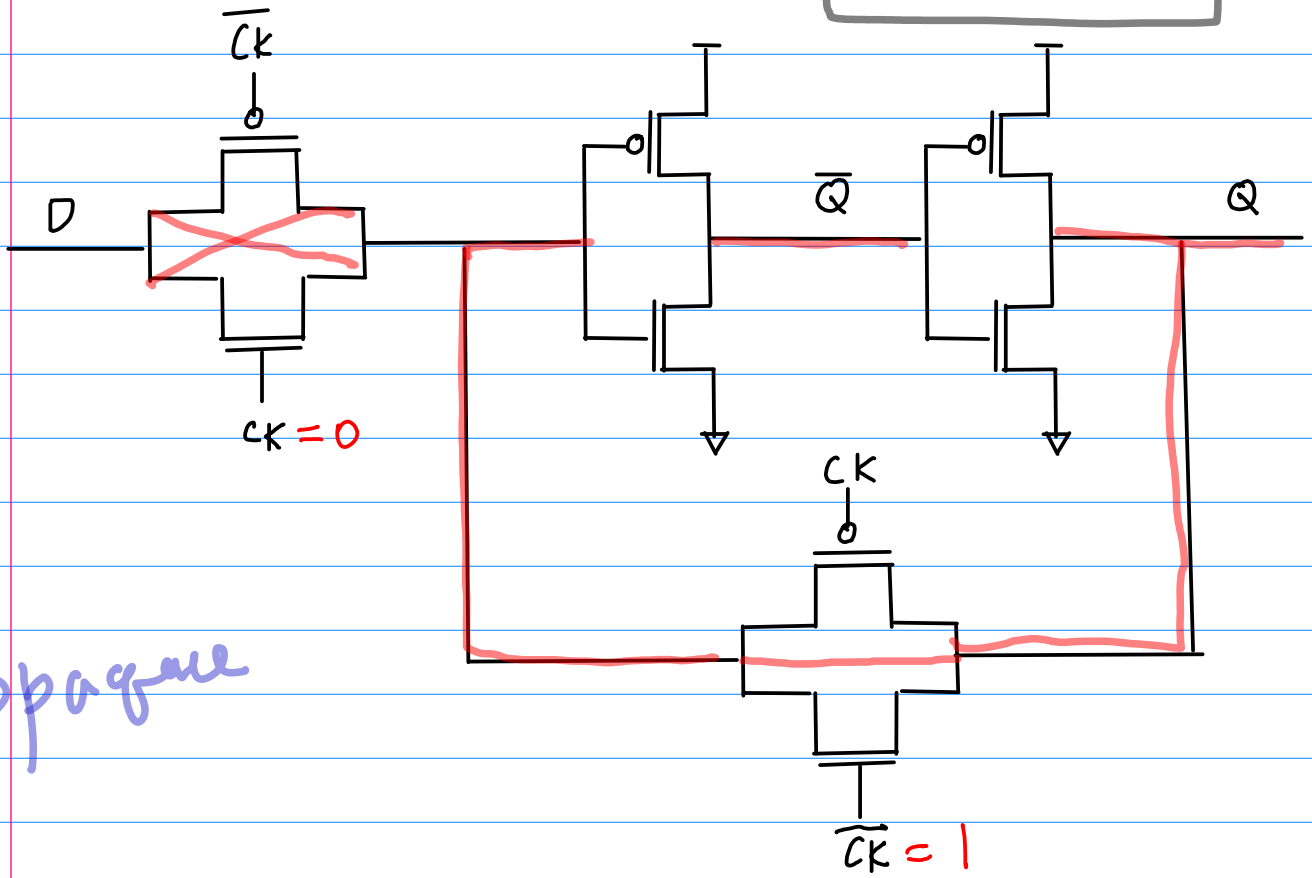
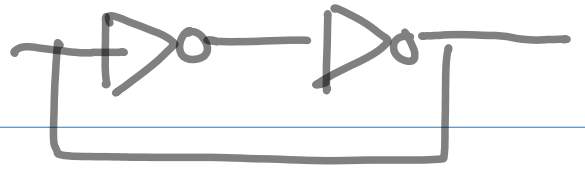


NOR-based Clocked JK Latch

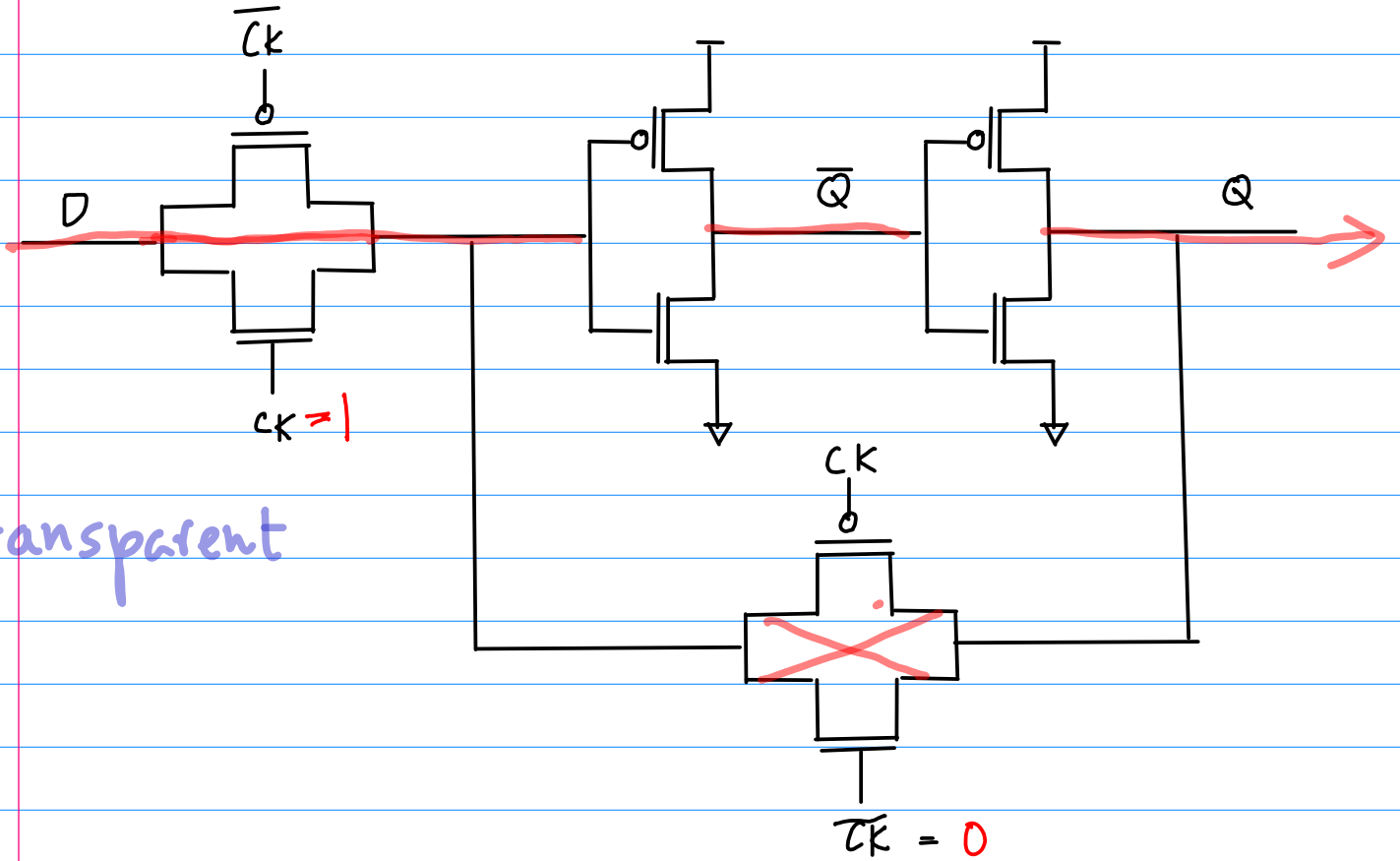


NOR-based D Latch



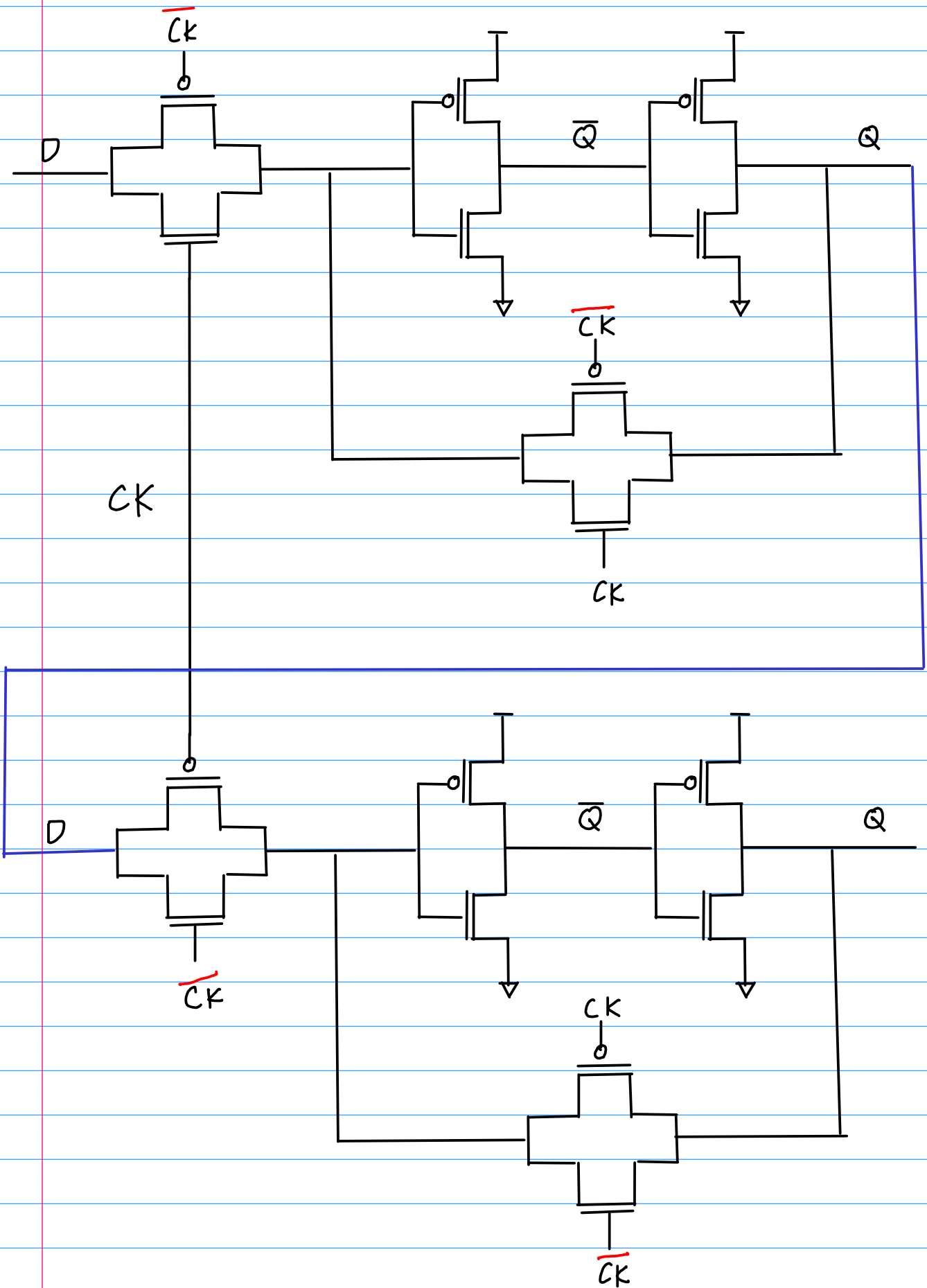


opaque



transparent

Master Slave D FlipFlop



Clocked CMOS (C²MOS) D Latch

