CMOS Delay-7 (H.8)
Delay Model

20170208

.

Copyright (c) 2015 - 2016 Young W. Lim.
Permission is granted to copy, distribute and/or modify this document under the terms of the GNU Free Documentation License, Version 1.2 or any later version published by the Free Software Foundation; with no Invariant Sections, no Front-Cover Texts, and no Back-Cover Texts. A copy of the license is included in the section entitled "GNU Free Documentation License".

References

Some Figures from the following sites

[1] http://pages.hmc.edu/harris/cmosvlsi/4e/index.html
Weste & Harris Book Site

[2] en.wikipedia.org

β : Device Transconductance Parameter
k : Process Transconductance Parameter
μ : Electron / Hole Mobility

pMOS $\quad \beta_p = k'_p \left(\frac{W}{L}\right)_p \qquad k'_p = \mu_p C_{ox} \qquad C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

nMOS $\quad \beta_n = k'_n \left(\frac{W}{L}\right)_n \qquad k'_n = \mu_n C_{ox} \qquad C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$

pMOS $\quad \beta_p = \mu_p \frac{\varepsilon_{ox}}{t_{ox}} \left(\frac{W}{L}\right)_p$

nMOS $\quad \beta_n = \mu_n \frac{\varepsilon_{ox}}{t_{ox}} \left(\frac{W}{L}\right)_n$

Saturation Current

$$I_{dp} = \frac{\beta_p}{2} \left(V_{GSn} - |V_{Tp}|\right)^2 \qquad V_{Tp} < 0$$

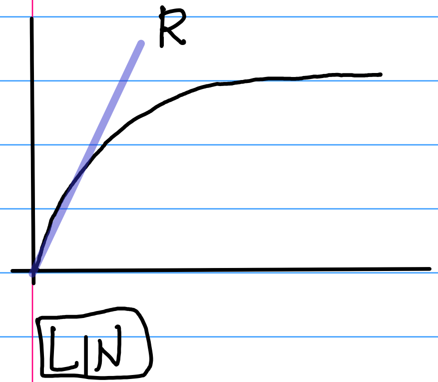
$$I_{dn} = \frac{\beta_n}{2} \left(V_{GSn} - V_{Tn}\right)^2 \qquad V_{Tn} > 0$$

$$\frac{\beta_n}{\beta_p} \simeq \frac{k_n' \left(\frac{W}{L}\right)_n}{k_p' \left(\frac{W}{L}\right)_p}$$

$$\frac{k_n'}{k_p'} = 2 \sim 3$$

$$\frac{k_n'}{k_p'} = \frac{\mu_n}{\mu_p} = r$$

$$\frac{\beta_n}{\beta_p} = \frac{k'_n \left(\frac{W}{L}\right)_n}{k'_p \left(\frac{W}{L}\right)_p}$$



$$R_n = \frac{1}{\beta_n (V_{DD} - V_{Tn})}$$

$$R_p = \frac{1}{\beta_n (V_{DD} - V_{Tn})}$$

fall time t_f $\qquad \tau_n = R_n C_{out}$

rise time t_r $\qquad \tau_p = R_p C_{out}$

$$C_{out} = C_{para} + C_L$$

MODEL

fall time	$t_f = 2.2\,\tau_n = \ln 9\,\tau_n$	$0.9\,V_{DD} \rightarrow 0.1\,V_{DD}$
rise time	$t_r = 2.2\,\tau_p = \ln 9\,\tau_p$	$0.1\,V_{DD} \rightarrow 0.9\,V_{DD}$
propagation delay time	$t_p = \frac{1}{2}(t_{pf} + t_{pr})$ $= 0.35(t_{pf} + t_{pr})$	$0.5\,V_{DD} \rightarrow 0.5\,V_{DD}$
propagation fall time	$t_{pf} = 0.7\,\tau_n = \ln 2\,\tau_n$	$V_{DD} \rightarrow 0.5\,V_{DD}$
propagation rise time	$t_{pr} = 0.7\,\tau_p = \ln 2\,\tau_p$	$0 \rightarrow 0.5\,V_{DD}$

$$\tau_n = R_n(C_{para} + C_L)$$

$$\tau_p = R_p(C_{para} + C_L)$$

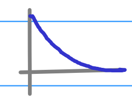
$$C_{out} = C_{para} + C_L$$

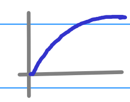
$$\left(\frac{W}{L}\right)_p = r\left(\frac{W}{L}\right)_n$$

$$r = \frac{\mu_n}{\mu_p} = \frac{k'_n}{k'_p} > 1$$

$$R_n = R_p = R = \frac{1}{\beta(V_{DD} - V_T)}$$

$$\begin{cases} V_{out}(t) = V_{DD}\left(1 - e^{-t/\tau}\right) \\ V_{out}(t) = V_{DD}\, e^{-t/\tau} \end{cases}$$





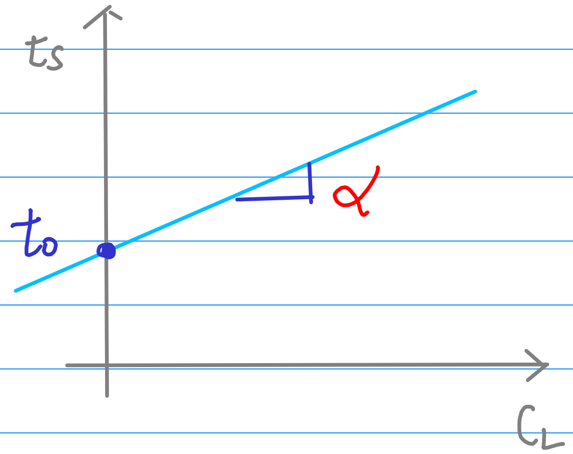
$$\tau = R\,C_{out} = R\,(C_{par} + C_L)$$

Generic Switching Delay

$$t_s = t_0 + \alpha C_L \quad \Rightarrow \quad t_s = t_r = t_f$$

Generic Switching Delay

$$t_s = t_0 + \alpha C_L$$



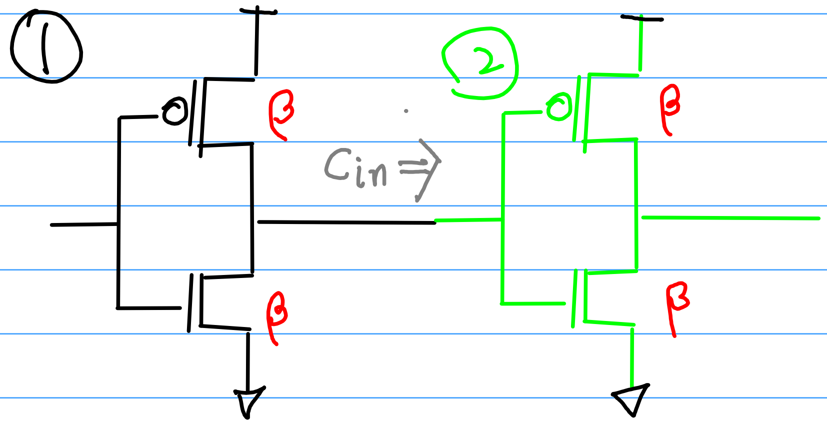
t_0 : zero delay

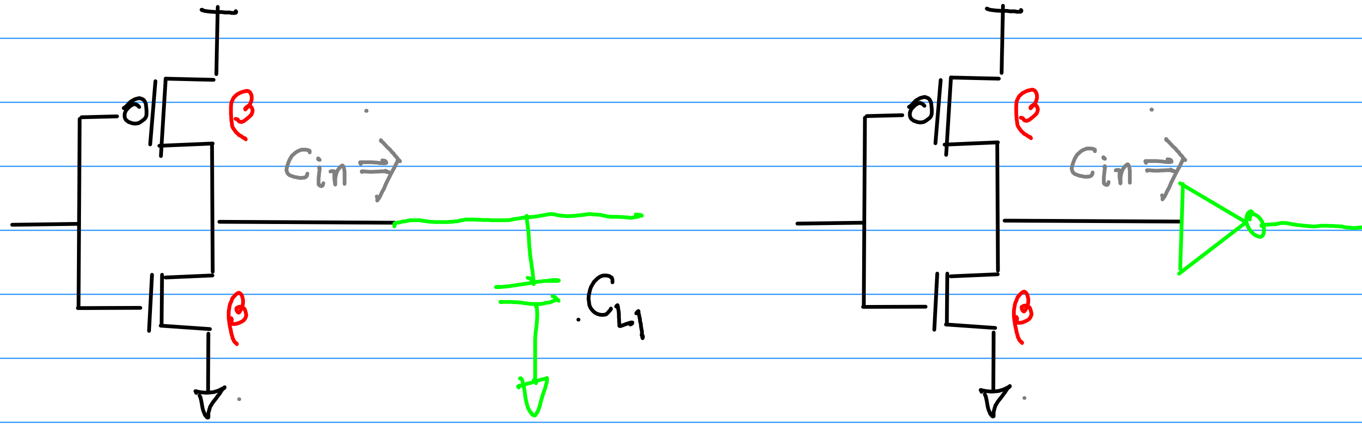
α : slope

$$t \approx RC$$

$$\alpha \propto \frac{1}{\beta (V_{DD} - V_T)}$$

C_L





reference case $C_{in} = C_{L1}$

Generic Switching Delay of (1)

$$t_{s1} = t_0 + \alpha C_{L1}$$
$$= t_0 + \alpha C_{in}$$

$$C_{in} = C_{Gn} + C_{Gp}$$

$$= C_{ox}(A_{Gn} + A_{Gp})$$ A: gate area

the channel length L assumed

$$C_{in} = C_{ox} L (W_n + W_p)$$

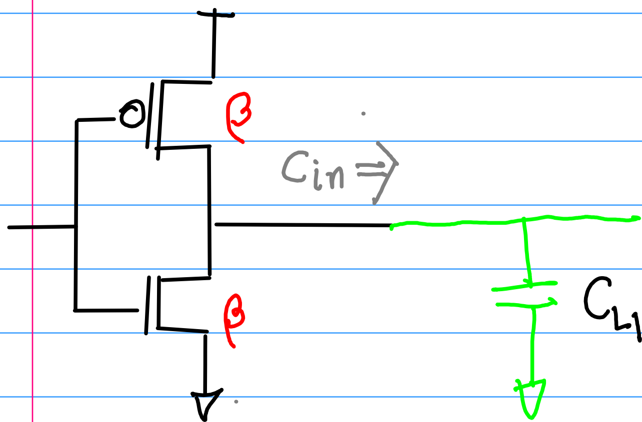
$$= C_{ox} L (W_n + r W_p)$$

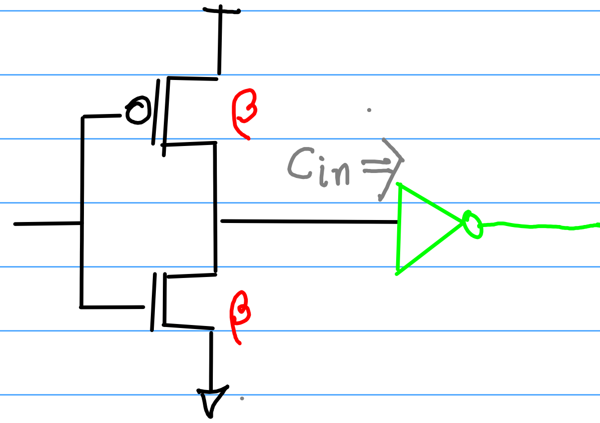
$$= C_{ox} L W_n \cdot (1 + r)$$

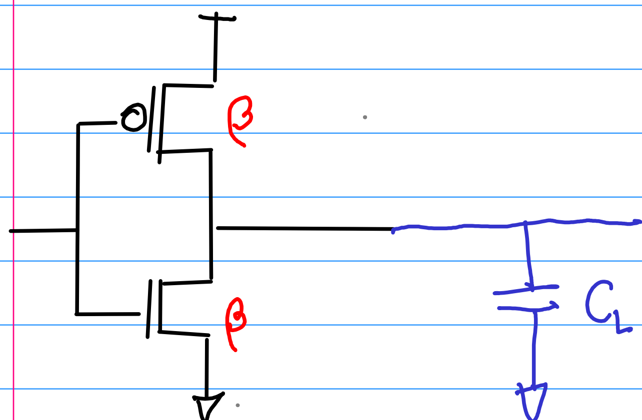
$$= C_{Gn}(1+r)$$

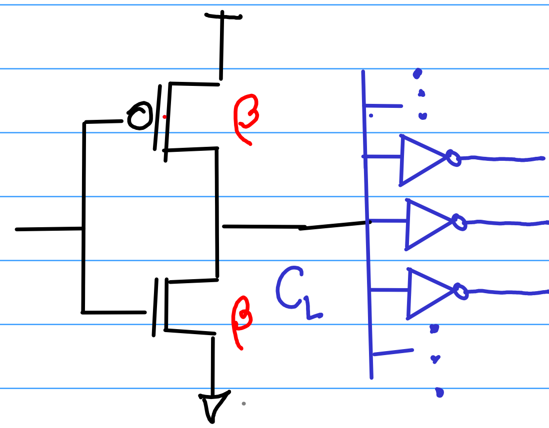
MODEL

When $C_L \gg C_{in}$









to minimize t_s

$\alpha \downarrow \Rightarrow R \downarrow \Rightarrow \beta \uparrow \Rightarrow$ bigger size

speed v.s. area tradeoff

$$t_s = t_0 + \alpha C_L \qquad t \approx RC$$

$$\alpha \propto \frac{1}{\beta (V_{DD} - V_T)} \qquad C_L$$

to minimize t_s

$\alpha \downarrow \Rightarrow R \downarrow \Rightarrow \beta \uparrow \Rightarrow$ bigger size

speed v.s. area tradeoff

Scaling Factor S

$$\beta' = S\beta$$

$$R' = \frac{R}{S}$$

$$\alpha' = \frac{\alpha}{S}$$

$$t_s = t_0 + \underbrace{\frac{\alpha}{S}}_{R}\underbrace{C_L}_{C}$$

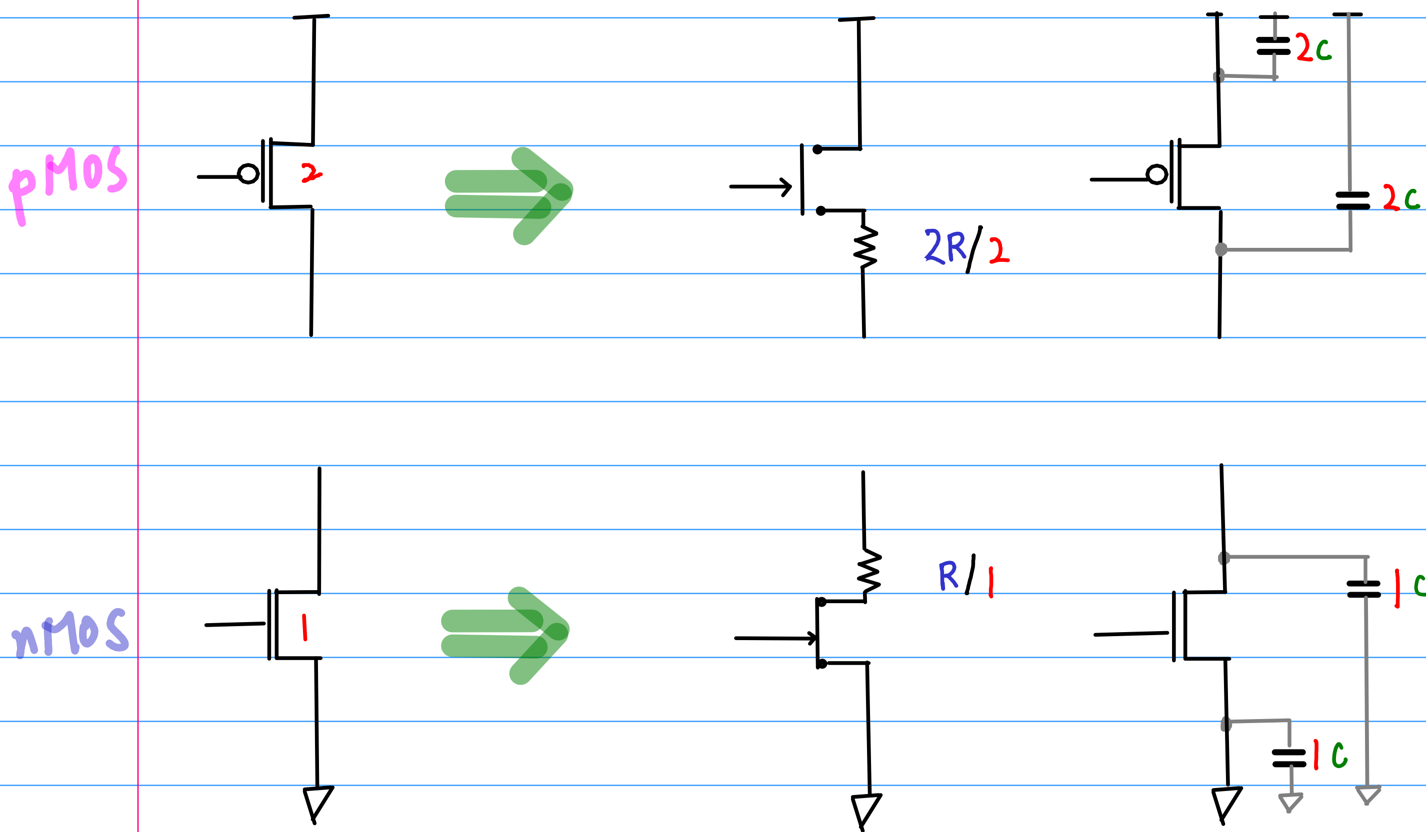
Compensation Factor $\frac{1}{S}$

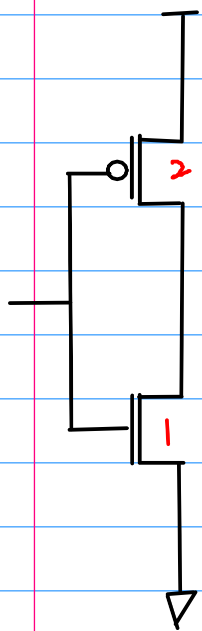
enables a NOT gate drive larger values of C_L

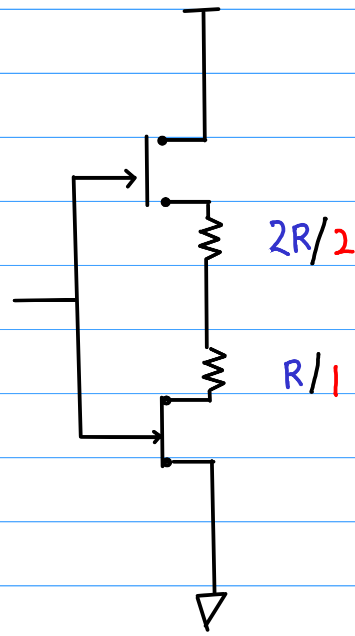
If $C_L = S\,C_{in}$ (increased by the scaling factor S)

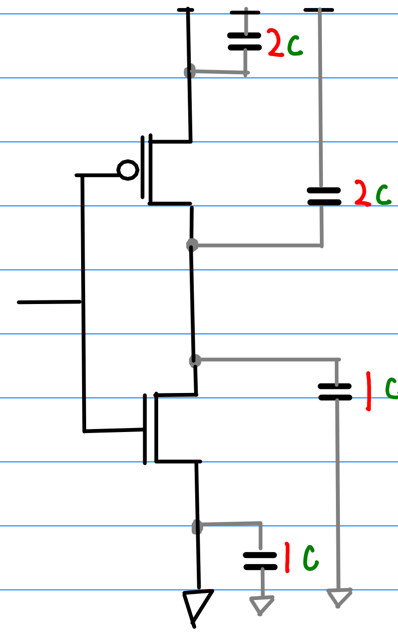
then the switching time is the same

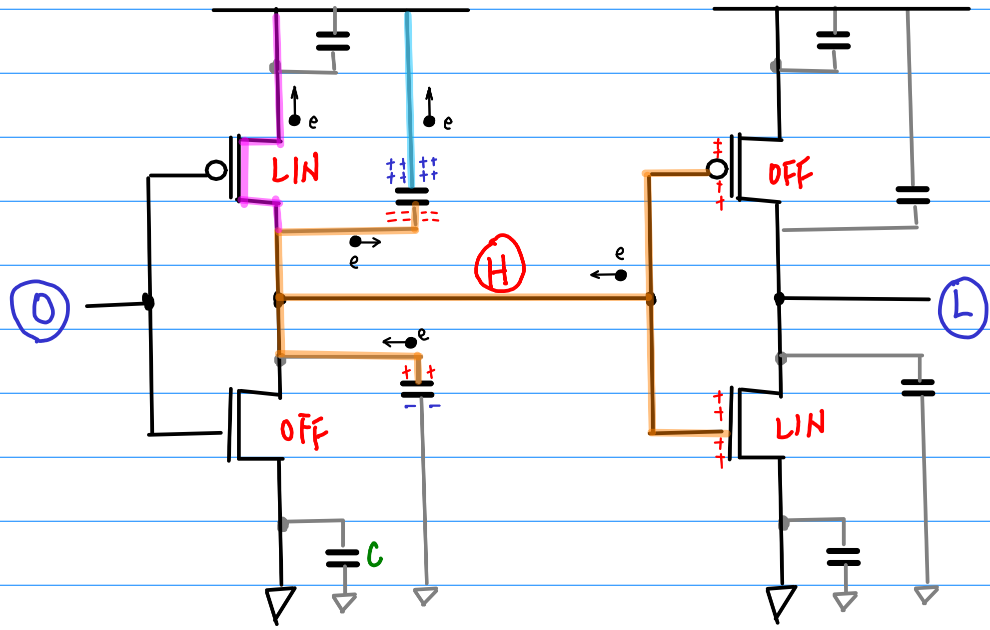
RC Delay Model

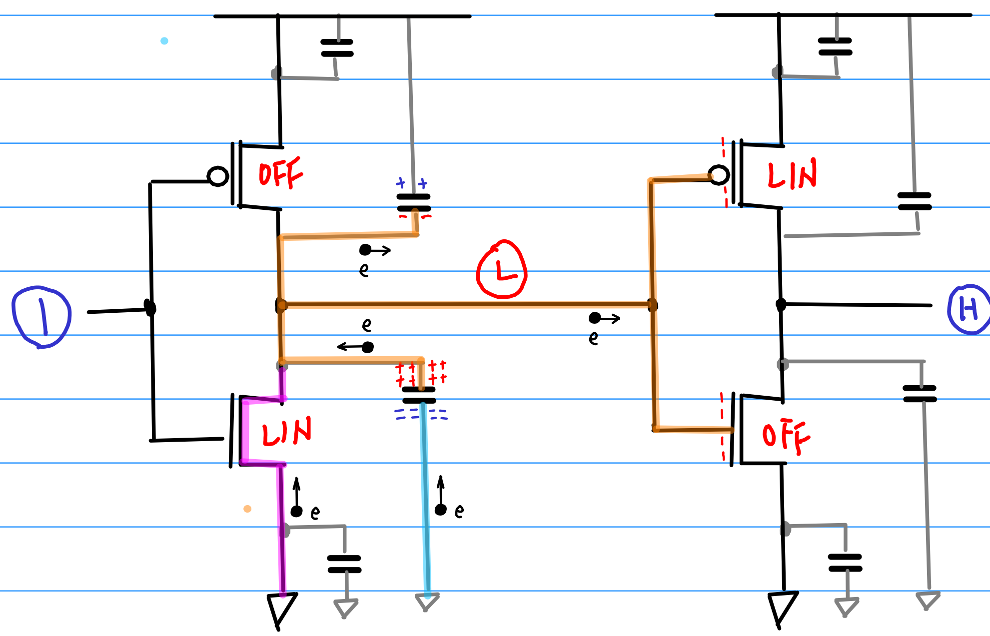


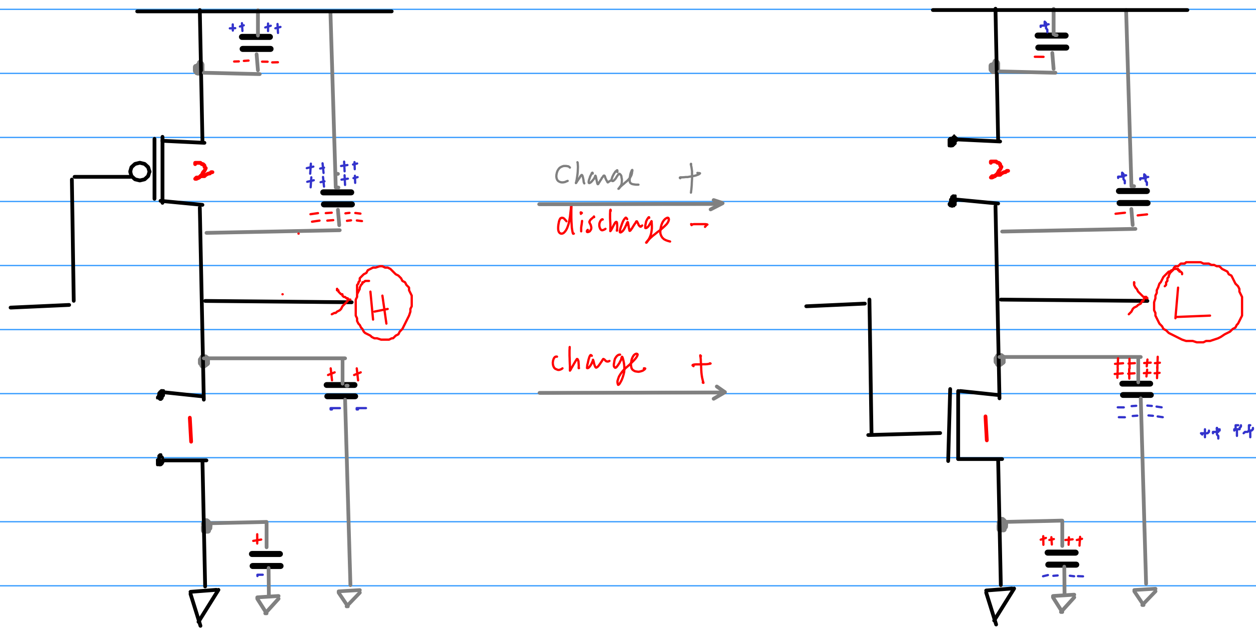

2
1

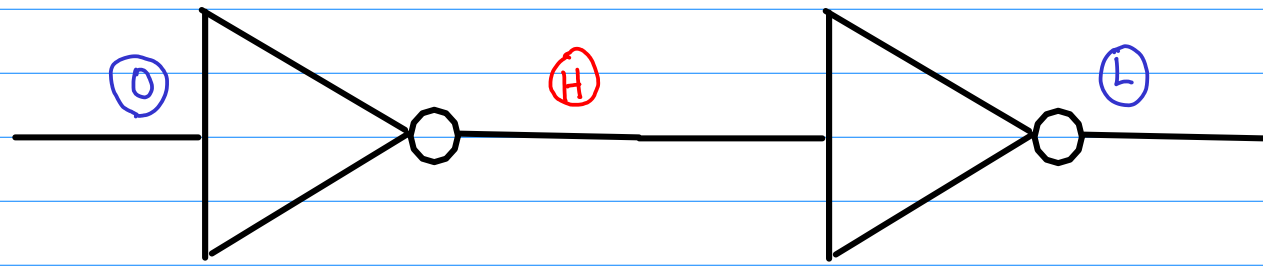

2R/2
R/1

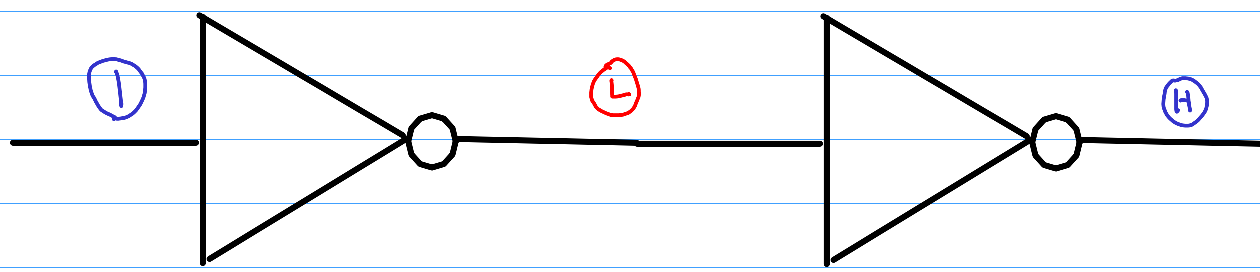

2c
2c
1c
1c

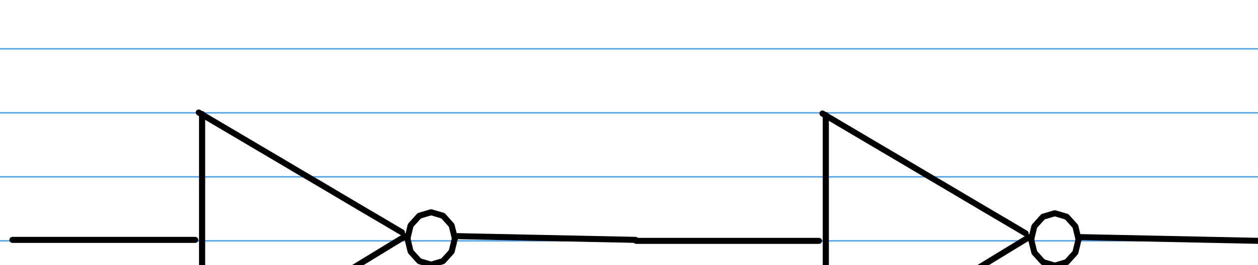

LIN
OFF
OFF
LIN
0
H
L
e
C

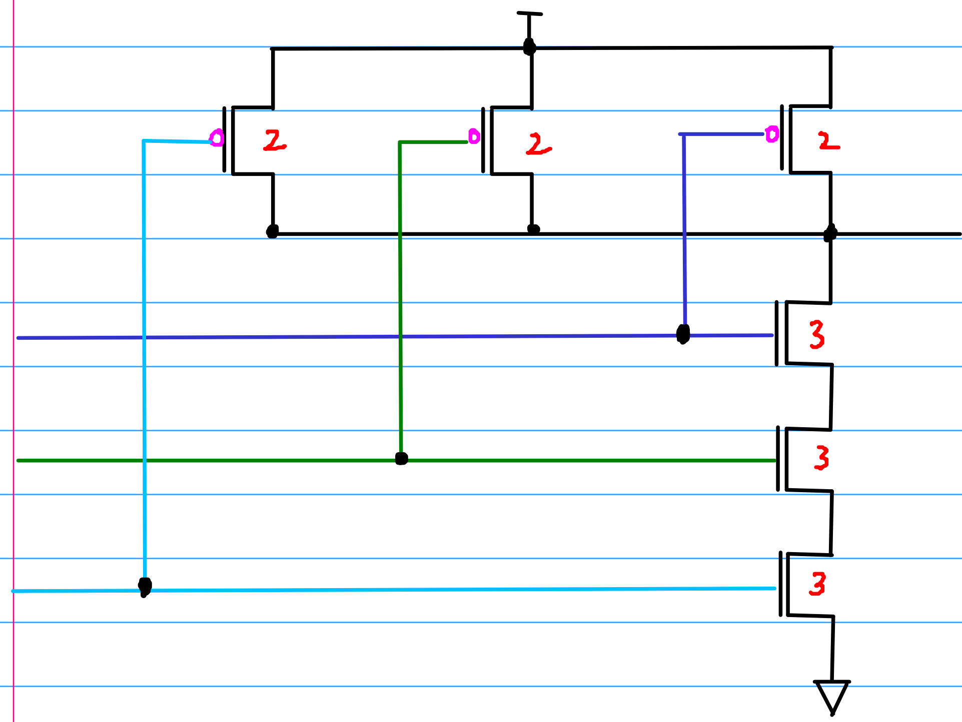

OFF
LIN
LIN
OFF
1
L
H
e

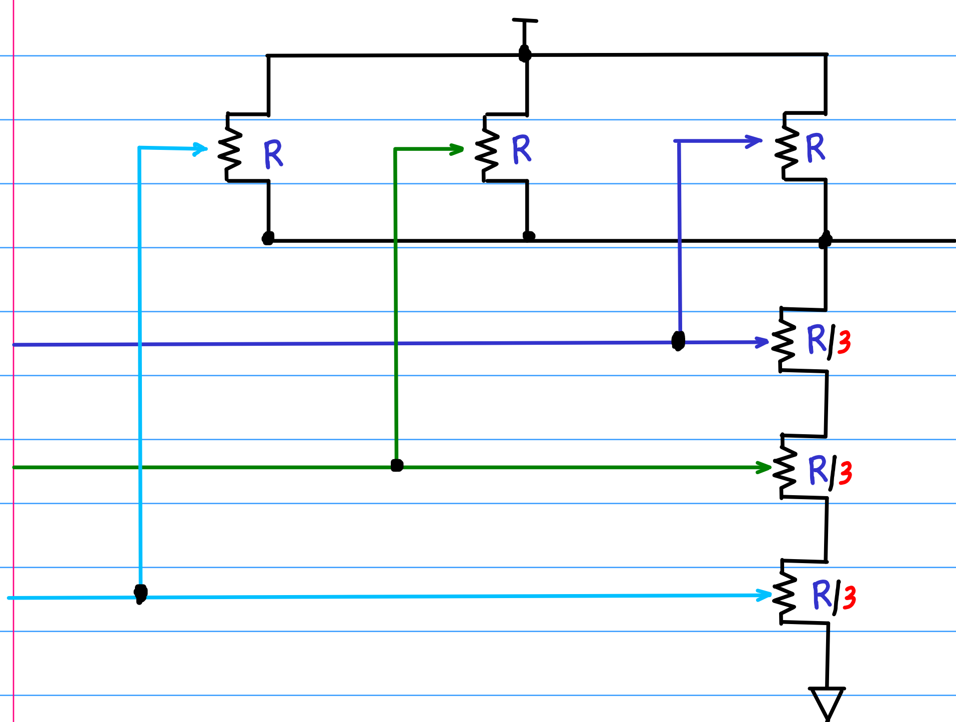

2
H
Charge +
discharge −
charge +
1
2
L
1

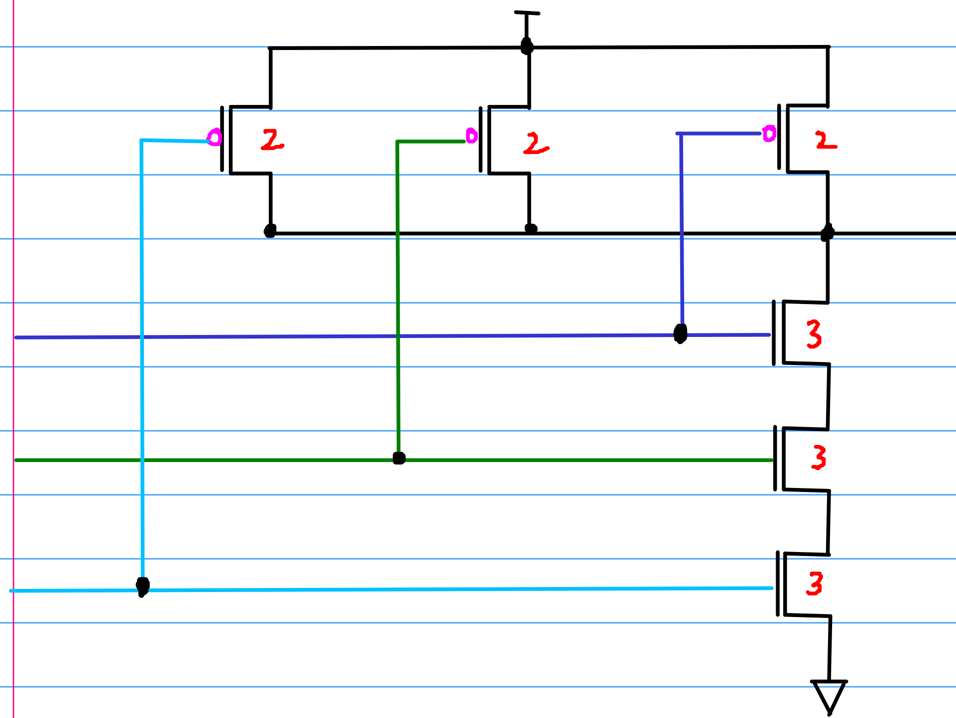

0
H
L

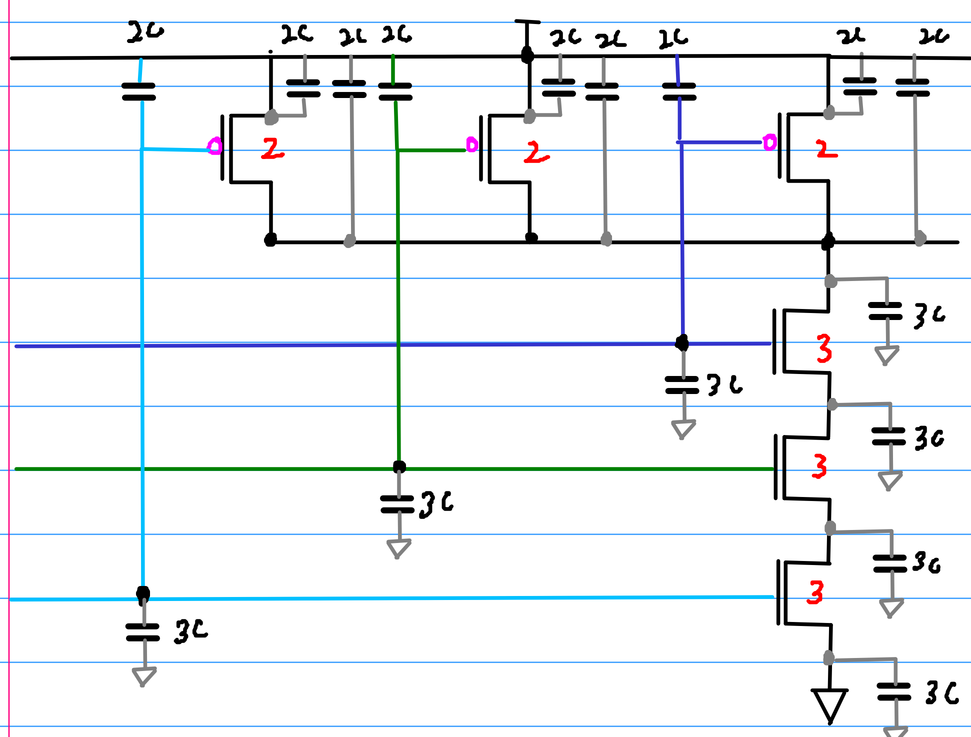

1
L
H

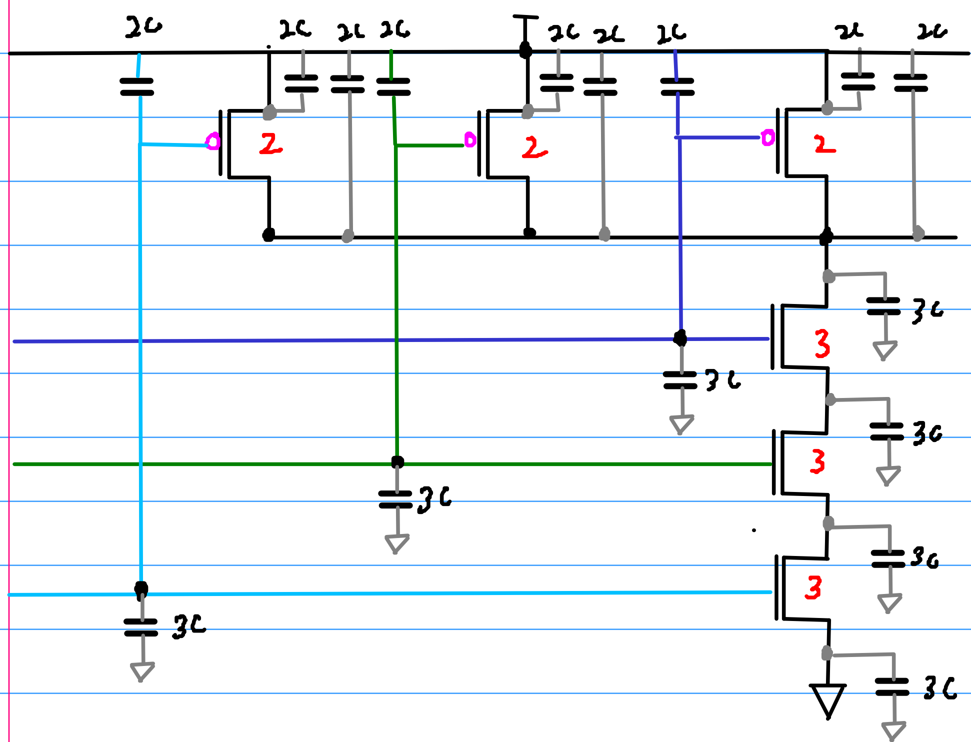


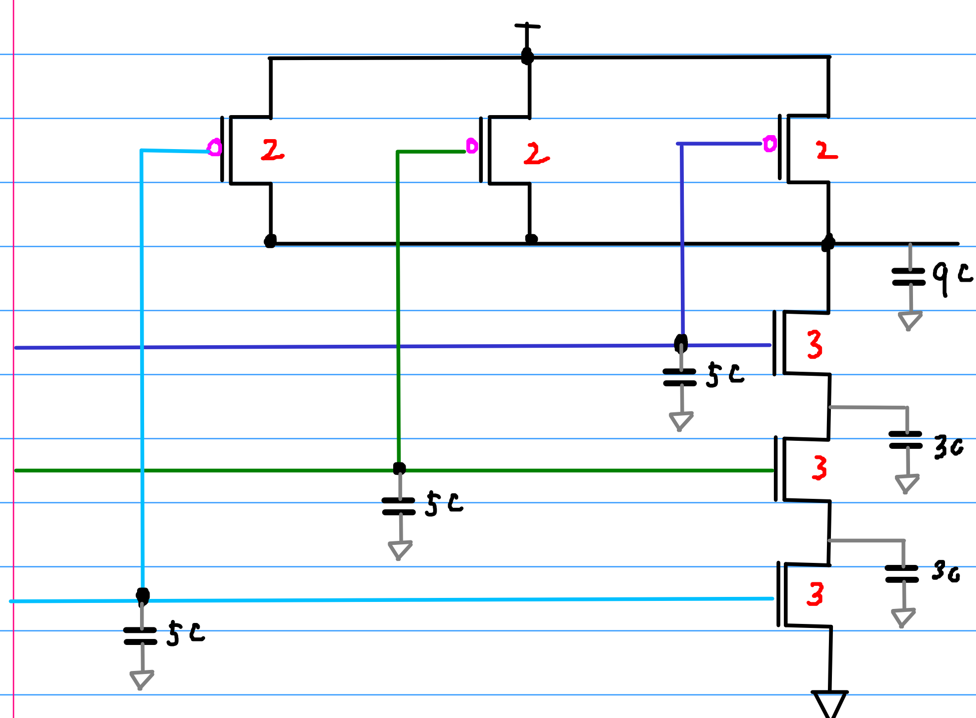

2
2
2
3
3
3


R
R
R
R/3
R/3
R/3

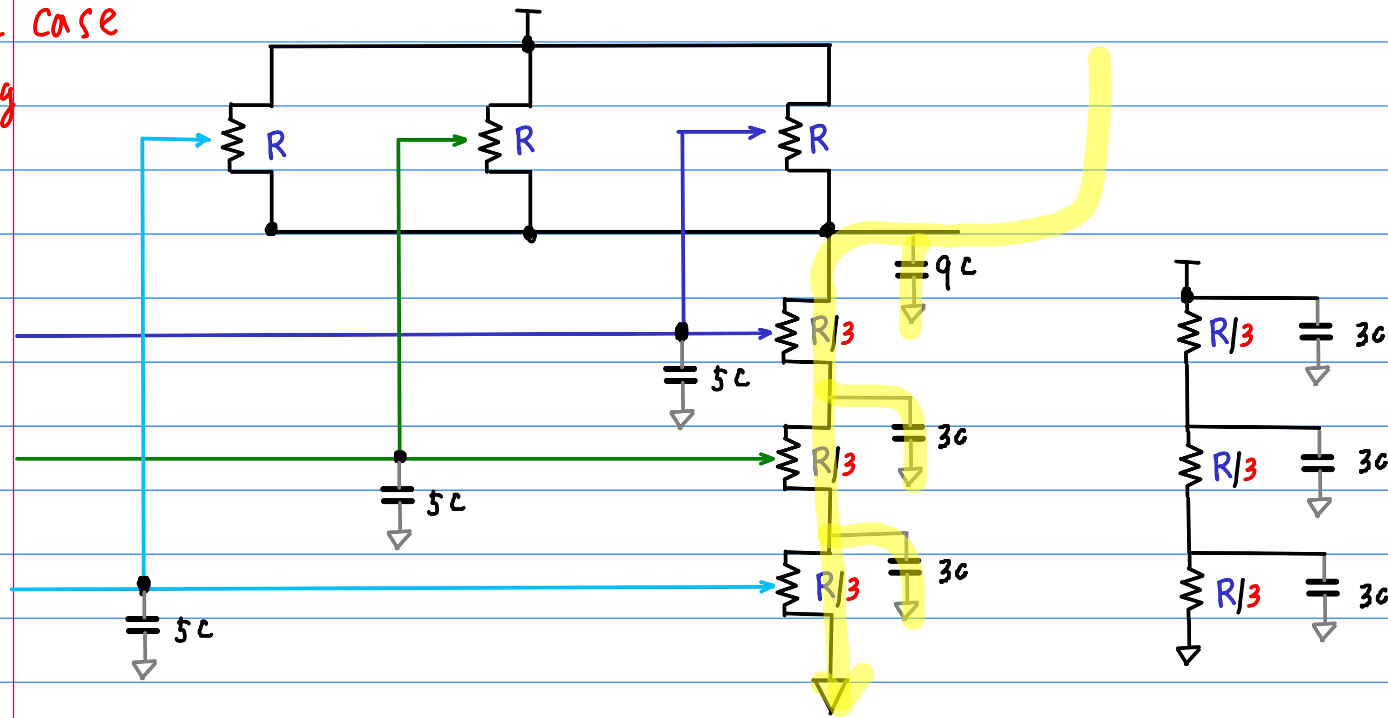

2
2
2
3
3
3


2C
2C
2C
2C
2C
2C
2C
2C
2C
2
2
2
3C
3
3C
3C
3
3C
3C
3
3C
3C

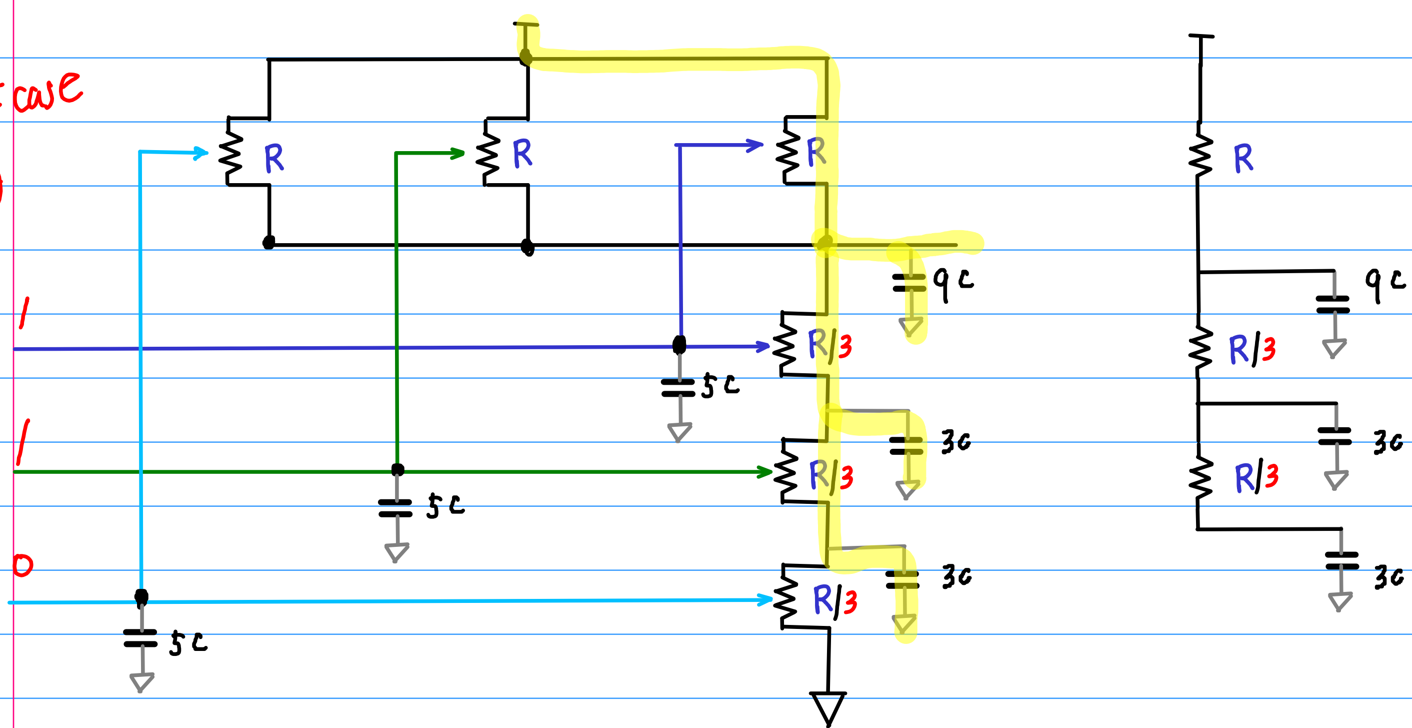

2c
2c
2c
2c
2c
2c
2c
2c
2c
2
2
2
3c
3
3c
3c
3
3c
3c
3
3c
3c


2
2
2
9c
3
5c
3
3c
5c
3
3c
5c

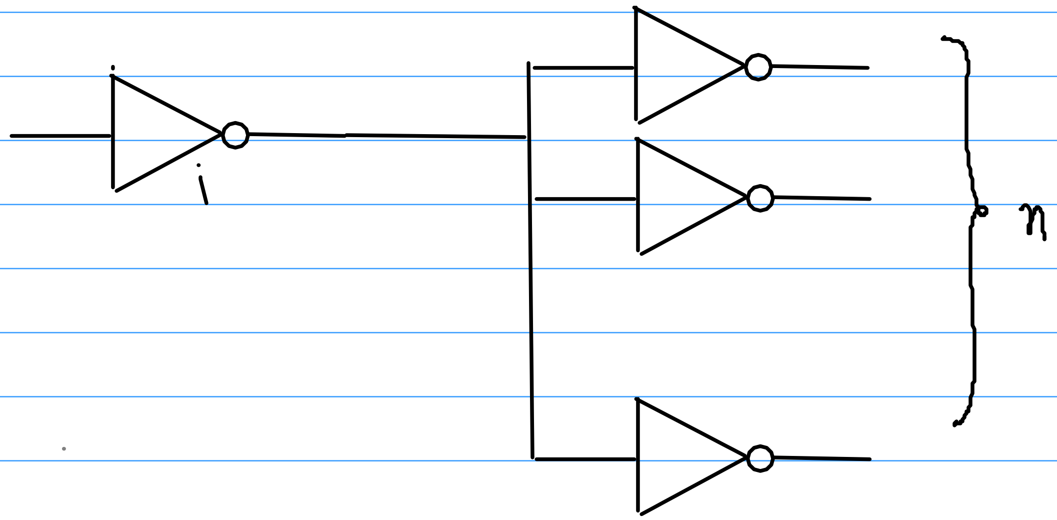
Worst case falling



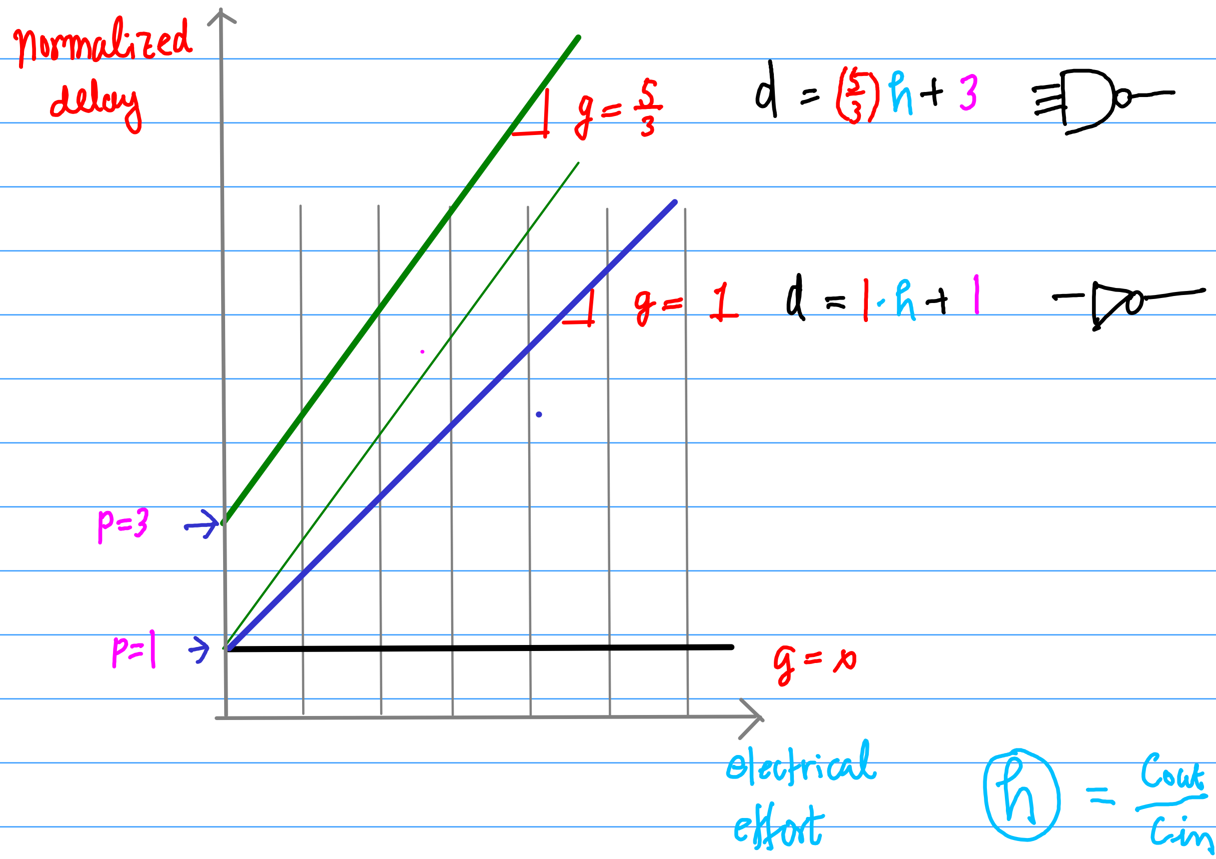
worst case rising

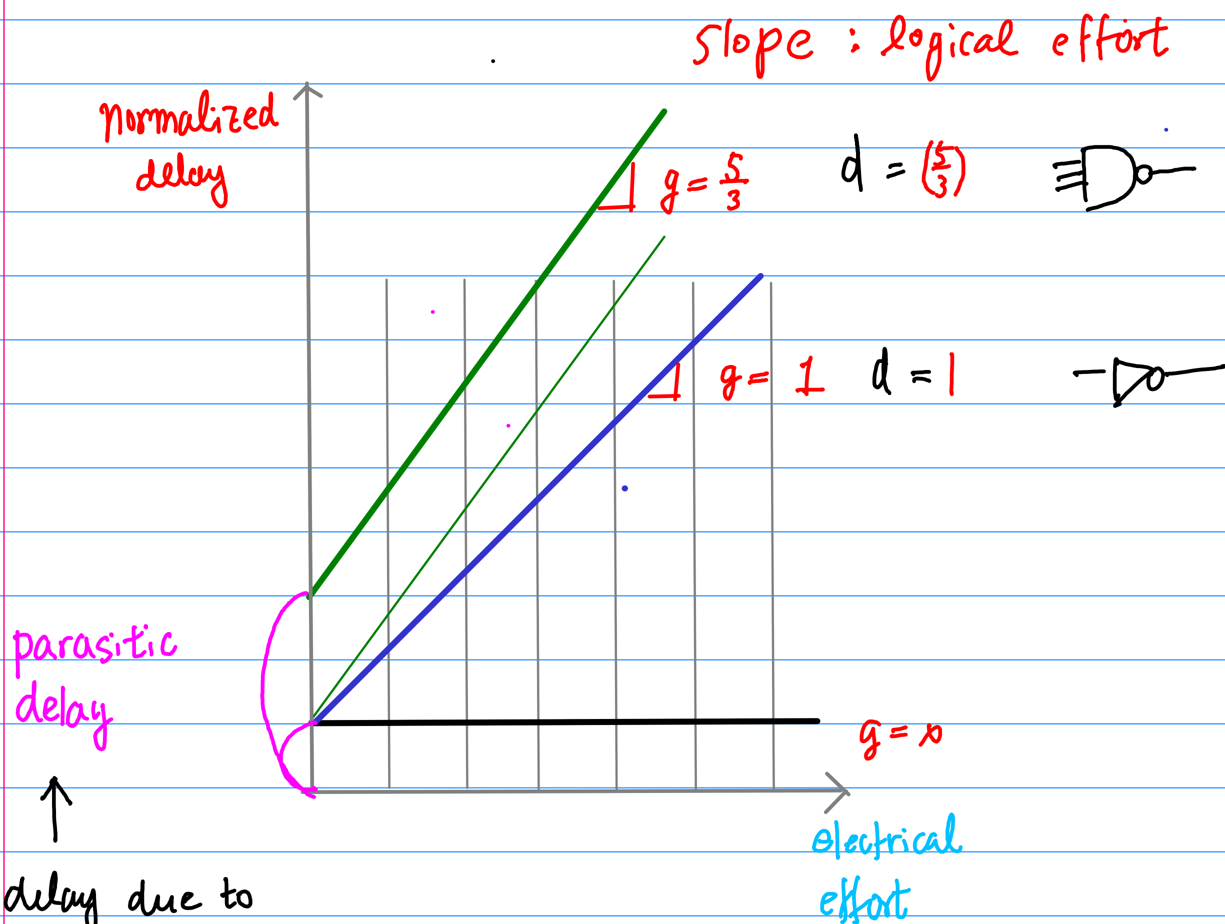


0



Linear Delay Model





↑

delay due to
only internal cap
without external load cap

$$d = g \cdot h + p$$

(k) (c) (c)

FET RC Model

$$R_n = \frac{V_{DS_n}}{I_{D_n}}$$

$$I_{dn} \cong \beta_n (V_{GS_n} - V_{T_n}) V_{DS_n}$$

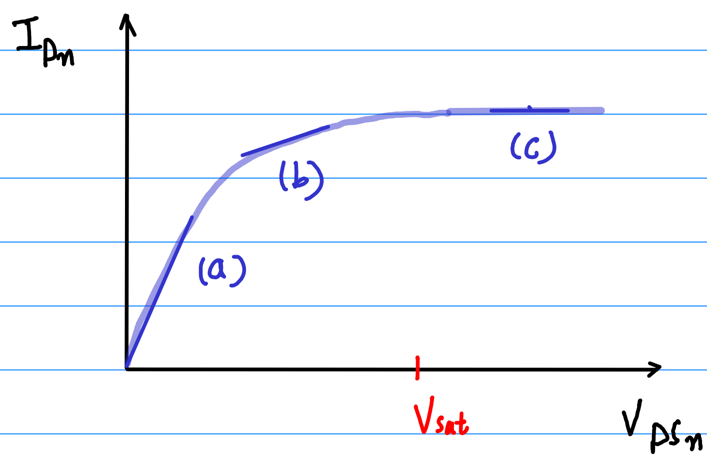
non-saturated

$$R_n \cong \frac{1}{\beta_n (V_{GS_n} - V_{T_n})}$$ (a) small V_{DS_n} $V_{DS_n}^2 \approx 0$

$$R_n = \frac{2}{\beta_n [2(V_{GS_n} - V_{T_n}) - V_{DS_n}]}$$ (b) $V_{DS} \neq 0$

saturated

$$R_n = \frac{2V_{DS_n}}{\beta_n (V_{GS_n} - V_{T_n})^2}$$ (c)



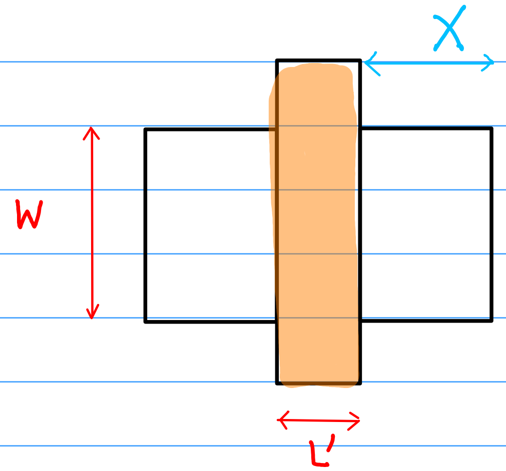
$$R_n \propto \frac{1}{\beta_n} \qquad \beta_n = k_n' \left(\frac{W}{L}\right)_n$$

$$R_n = \frac{\eta}{\beta_n (V_{DD} - V_{Tn})} \qquad \eta = 1 \sim 6$$

↑ largest possible V_{GSn}

$$\boxed{R_n = \frac{1}{\beta_n (V_{DD} - V_{Tn})}} \ \Omega \qquad \eta = 1$$

MOS Capacitance



$C_G = C_{ox} A_G \qquad A_G = W L'$

$= C_{ox} W L'$

$C_{GS} = \frac{1}{2} C_G$

$C_{GD} = \frac{1}{2} C_G$.

Junction Capacitance

A_{pn}: area of p-n junction
V_R: the reverse bias voltage

$C_0 = C_j A_{pn}$ C_0: zero-bias capacitance ($V_R = 0$)

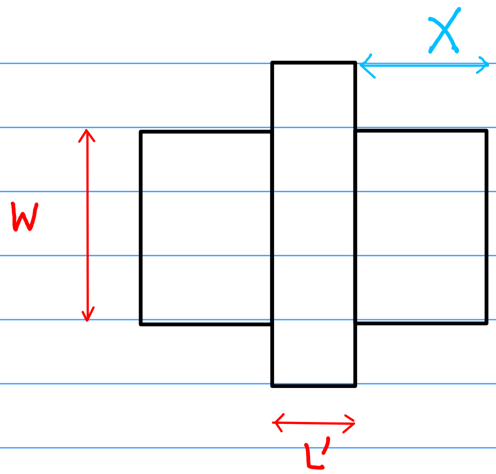
$$C = \frac{C_0}{\left(1 + \frac{V_R}{\phi_0}\right)^{m_j}}$$

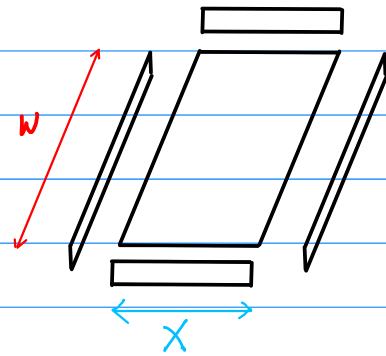
m_j: grading coefficient
ϕ_0: built-in potential
m_j, ϕ_0 ← doping characteristics

$$\phi_0 = \left(\frac{kT}{q}\right) \ln\left[\frac{N_d N_a}{n_i^2}\right]$$

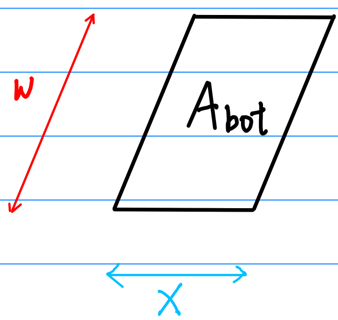
for an abrupt (step) junction

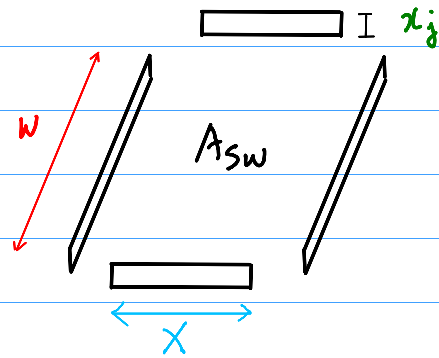
for a linearly graded function





bottom | **sidewall**





side wall

$$A_{bot} = X W$$

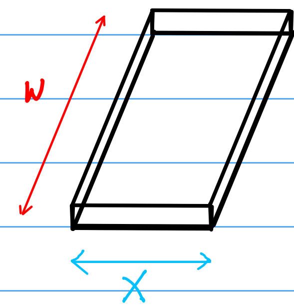
$$A_{sw} = 2(W \cdot x_j) + 2(X \cdot x_j)$$
$$= x_j P_{sw} = x_j (2W + 2X)$$

$C_{bot} = c_j A_{bot}$
$C_{sw} = c_j A_{sw}$
$= c_j x_j P_{sw}$
$= c_{jsw} P_{sw}$

$$A_{bot} = XW$$
$$A_{sw} = 2(W \cdot x_j) + 2(X \cdot x_j)$$
$$P_{sw} = (2W + 2X)$$
$$c_{jsw} = c_j x_j$$

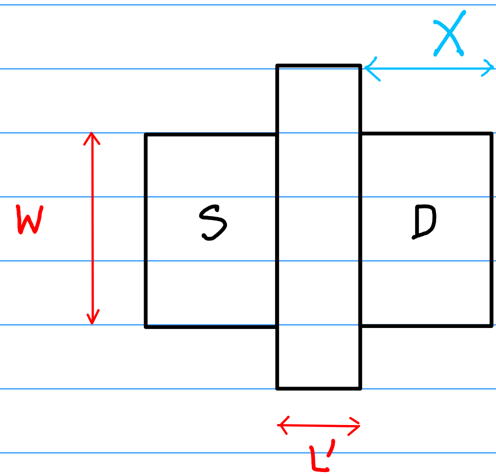
for overlap $X \leftarrow X + L_o$

The total zero-bias capacitance of n^+ region



$$C_n = C_{bot} + C_{sw}$$
$$= C_j A_{bot} + C_{jsw} P_{sw}$$

$$C_n \Rightarrow C_{SB} \ \& \ C_{DB}$$



$$C_S = C_{GS} + C_{SB}$$
$$C_D = C_{GD} + C_{DB}$$

non-linear version

$$C_n = \frac{C_j A_{bot}}{\left(1 + \frac{V}{\phi_0}\right)^{m_j}} + \frac{C_{jsw} P_{sw}}{\left(1 + \frac{V}{\phi_{osw}}\right)^{m_{jsw}}}$$

V : reverse voltage

m_j : grading coefficients
ϕ_o : buit-in potential
) bottom

m_{jsw} : grading coefficients
ϕ_{osw} : buit-in potential
) sidewalls

$$C_S = C_{GS} + C_{SB}$$

$$C_D = C_{GD} + C_{DB}$$

pFET Characteristics

$$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

$$I_{Dp} = \frac{\beta_p}{2}\left(V_{SGp} - |V_{Tp}|\right)^2$$

$$\beta_p = k'_p \left(\frac{W}{L}\right)_p$$

$$k'_p = \mu_p C_{ox}$$

$$r = \frac{\mu_n}{\mu_p} = 2 \sim 3$$

$$\beta_n = k'_n \left(\frac{W}{L}\right)_n$$

$$\beta_p = k'_p \left(\frac{W}{L}\right)_p$$

$$V_{sat} = V_{SGp} - |V_{Tp}|$$

$$I_{Dp} = \frac{\beta_p}{2}\left[2\left(V_{SGp} - |V_{Tp}|\right)V_{SDp} - V_{SDp}^2\right]$$

$$I_{Dp} = \frac{\beta_p}{2}\left[V_{SGp} - |V_{Tp}|\right]^2$$

$$R_p = \frac{1}{\beta_p\left(V_{DD} - |V_{Tp}|\right)}$$

$$R_p \propto \frac{1}{\beta_p} = \frac{1}{k'_p \left(\frac{W}{L}\right)_p}$$

$$C_{Gp} = C_{ox}(WL)_p$$

$$C_{GS} = \frac{1}{2} C_{GP} \approx C_{GP}$$

$$C_P = C_j A_{bot} + C_{jsw} P$$

Fall Time Calculation

$$i = -C_{out}\frac{dV_{out}}{dt} = \frac{V_{out}}{R_n}$$

$$V_{out}(t) = V_{DD}\, e^{-t/\tau_n}$$

$$\tau_n = R_n C_{out}$$

$$t = \tau_n \ln\left(\frac{V_{DD}}{V_{out}}\right)$$

$$t_f = t_y - t_x = \tau_n \ln\left(\frac{V_{DD}}{0.1 V_{DD}}\right) - \tau_n \ln\left(\frac{V_{DD}}{0.9 V_{DD}}\right)$$

$$= \tau_n \ln(9)$$

$$t_{HL} = t_f \cong 2.2\tau_n$$

Rise Time Calculation

$$i = -C_{out}\frac{dV_{out}}{dt} = \frac{V_{DD} - V_{out}}{R_p}$$

$$V_{out}(t) = V_{DD}\left[1 - e^{-t/\tau_p}\right]$$

$$\tau_p = R_p C_{out}$$

$$t = \tau_p \ln\left(\frac{V_{DD}}{V_{out}}\right)$$

$$t_f = t_v - t_u = \tau_p \ln\left(\frac{V_{DD}}{0.1 V_{DD}}\right) - \tau_n \ln\left(\frac{V_{DD}}{0.9 V_{DD}}\right)$$

$$= \tau_p \ln(9)$$

$$t_{LH} = t_r \cong 2.2\tau_p$$

Propagation Delay

$$t_p = \frac{(t_{pf} + t_{pr})}{2}$$

$$t_{pf} = \ln(2) \cdot \tau_n$$
$$t_{pr} = \ln(2) \cdot \tau_p$$

$$t_p \cong 0.35(\tau_n + \tau_p)$$

$$C_{out} = C_{FET} + C_L$$

$$t_r = 2.2\, R_p\, (C_{FET} + C_L)$$
$$t_f = 2.2\, R_n\, (C_{FET} + C_L)$$

$$t_r = t_{ro} + \alpha_p C_L$$
$$t_f = t_{ro} + \alpha_n C_L$$

$C_L = 0 \rightarrow$ $$t_r = t_{ro} \cong 2.2\, R_p\, C_{FET}$$
$C_L = 0$ $$t_f = t_{ro} \cong 2.2\, R_n\, C_{FET}$$

$$\alpha_p = 2.2 R_p = \frac{2.2}{\beta_p (V_{DD} - |V_{Tp}|)}$$
$$\alpha_n = 2.2 R_n = \frac{2.2}{\beta_n (V_{DD} - |V_{Tn}|)}$$

$$\beta_p = k'_p \left(\frac{W}{L}\right)_p$$

$$\beta_n = k'_n \left(\frac{W}{L}\right)_n$$