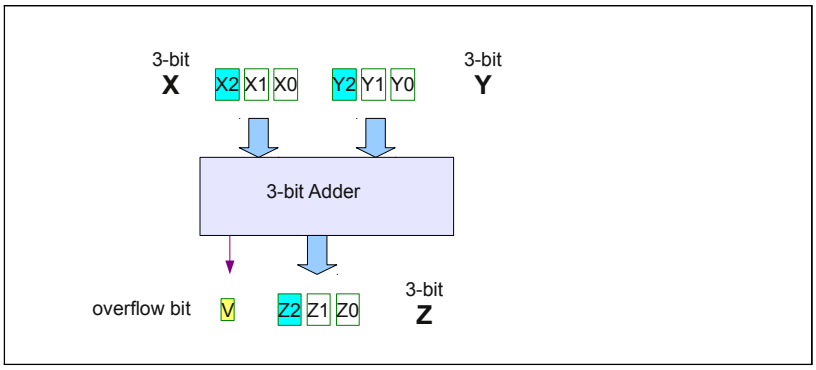
HW Overflow Detection Circuit Design

Consider a 3-bit binary signed number adder.



Read the following materials.
http://www.cs.umd.edu/class/sum2003/cmsc311/Notes/Comb/overflow.html
www.cs.utexas.edu/users/chris/cs310/f2005/notes/**d3.pdf**

Text (4.5 Binary Adder-Subtractor)

(1) Using the Full Adder in Fig 4.9, draw a 3-bit adder.

(2) Overflow Detection Circuit

Overflow can be detected by considering the sign bits of two input numbers and the result.

(pos number) + (pos number) → (neg number)
(neg number) + (neg number) → (pos number)

(a) Find the Boolean function V which gives 1 when an overflow condition occurs.
(b) What are the input variables to the function V?
X0, X1, X2, Y0, Y1, Y2, Z0, Z1, Z2
(c) Make a truth table for the function V.
(d) Try to minimize the function using K-map if possible.

(3) Draw the whole schematic for the 3-bit adder. (using the circuits in fig 4.7 and 4.9)

(4) Simulate 010 + 001, 011 + 010 on the schematic of (3), by marking the outputs of all the gates. (You can use the copied paper)

(5) Explain the overflow detection scheme in Fig 4.13